CHIPIX65

Web-site: http://chipix65.to.infn.it

CALL Project CSN5 approved in October 2013 - total funding: 730ke in three years

Development of an innovative **CHIP** for a **PIX**el detector, using a CMOS **65**nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. A unique opportunity for an efficient propagation across INFN of CMOS 65nm technology and constitutes the greatest collaboration on a microelectronics project ever made across INFN

Principal Investigator : Natale Demaria - INFN/Torino

Funding members of RD53 Collaboration

Institutes:

Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa, Torino

People (44 of which 50% ASIC designers; 12.4 FTE)**:** (Torino: 9 people; 3.4 FTE)

N.Demaria, G.Dellacasa, G.Mazza, A.Rivetti, M.D.Da Rocha Rolo, E.Monteil, L.Pacher, F.Ciciriello, F.Corsi, C.Marzocca, G.De Robertis, F.Loddo, C.Tamma, M.Bagatin, D.Bisello, S.Gerardin, S.Mattiazzo, L.Ding, P.Giubilato, A.Paccagnella, F.De Canio, L.Gaioni, M.Manghisoni, V.Re, G.Traversi, E.Riceputi, L.Ratti, C.Vacchi, R.Beccherle, G.Magazzu, M.Minuti, F.Morsani, F.Palla, V.Liberali , S.Shojaii , A.Stabile , G.M.Bilei , M.Menichelli , S.Marconi, D.Passeri , P.Placidi, S.D'Amico, C.Veri,

Work Packages:

Radiation Hardness – A.Paccagnella (Padova)
Digital Electronics – R.Beccherle (Pisa)
Analog Electronics - A.Rivetti (Torino)
Chip Integration - V.Re (Pavia/Bergamo), V.Liberali (Milano)

International Collaborations/ supports:

RD53, CMS, ATLAS : all wrote support letters

Papers / talks / thesis

- 18 talks at International conferences
- 3 degree theses, 1 PhD thesis
- 17 papers on international journals

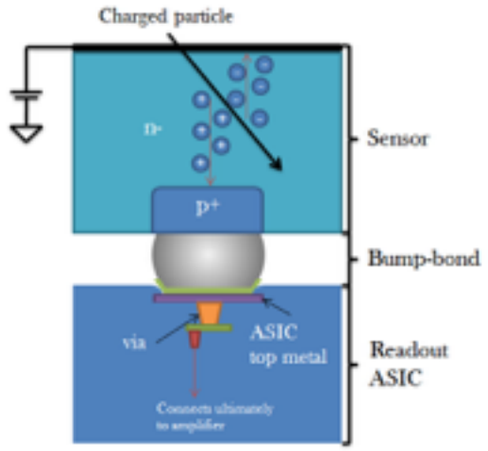
Pixel Detector at HL_LHC

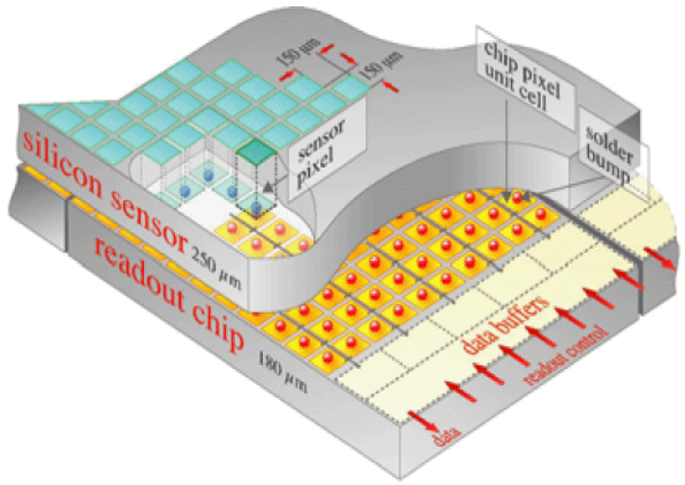
Requirements from HL_LHC experiments

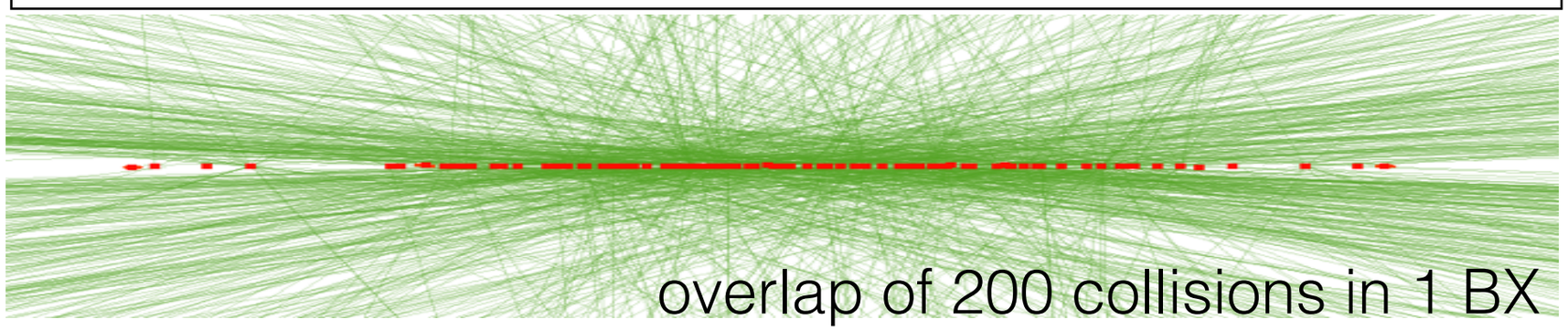
Small pixels: 50x50um^2
Large chips: 2cm x 2cm (~1 billion transistors)
Pixel Hit rates: up to 3 GHz/cm^2 (200 P.U.)
Radiation: 1Grad, 10^{16} n/cm^2 (unprecedented)

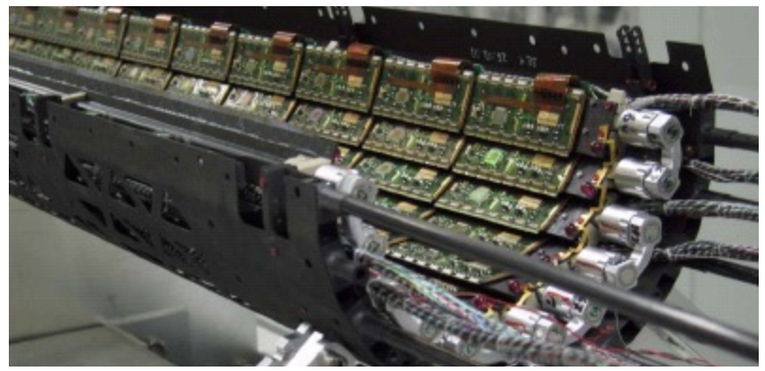
Trigger: up to 1MHz with 12.8us latency
(~100x buffering and readout)
Low power - Low mass systems

Data readout : up to 4-5 Gbs/s
TRIGGER Latency up to 12.8us (x3) ==> deeper storage buffer



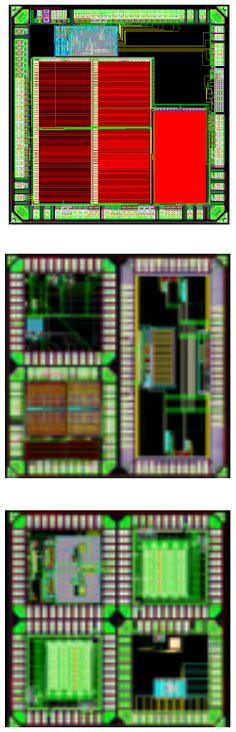




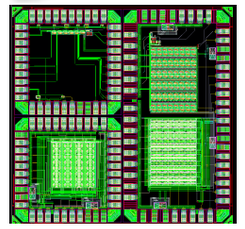
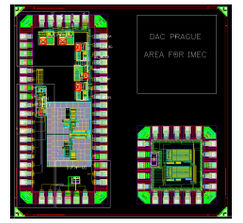


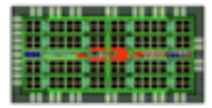
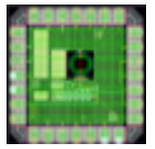
CHIPIX65 deliverables

Radiation characterisation
- x-ray machine at LNL / Pd-INFN)
  - Total Ionising Dose (TID)
  - 1 GRad in ~ 2 weeks
- Low-p at CN accelerator LNL
  - TID and Total Displacement damage
- TANDEM / SIRAD
  - Single Event Effects - with Heavy Ion
- Studies on n-MOS, p-MOS
- Irradiation of IP-block, Noise measurements vs Irradiation



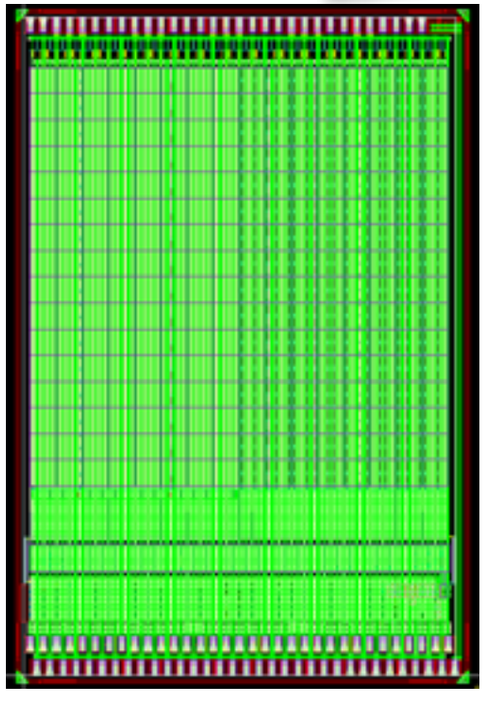
- Band Gap : **Pavia**
- DAC :**Bari**
- SLVDS driver : **Pavia, Pisa**
- SLVDS receiver : **Pavia,Pisa**
- PLL : Torino, (Padova)
- SER : **Pisa**
- DES : **Pisa**
- Monitoring ADC : **Bari**
- SRAM EOC : **Milano**
- Dual Digital Cell : Milano
- DC-DC : Lecce

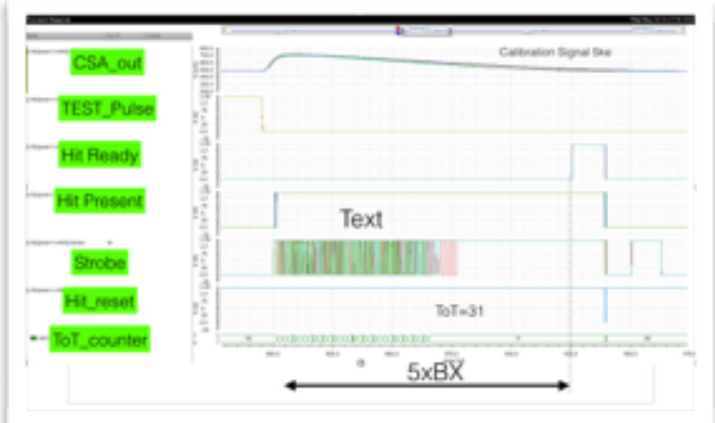



- Analog-VFE synch : **Torino**
- Analog-VFE synch : **Pavia/Bg**

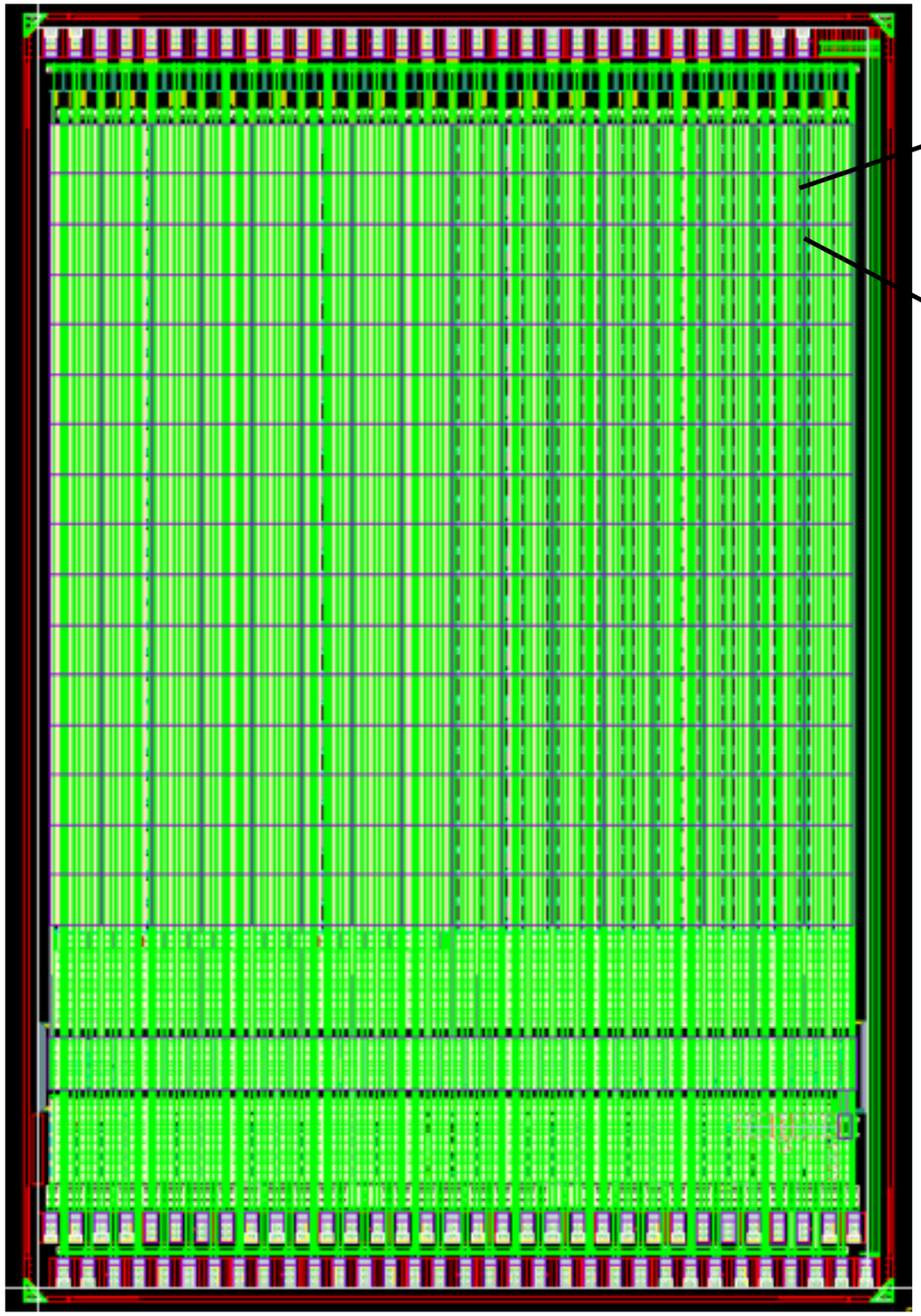
Digital Electronics:
- Simulation Framework (Perugia)
  - System-Verilog-UVM (VEPIX53)
- Digital Architecture Studies (To/Pg)
- Input protocols definition
  - fast/efficient/continuos (while readout)
  - SEE robust

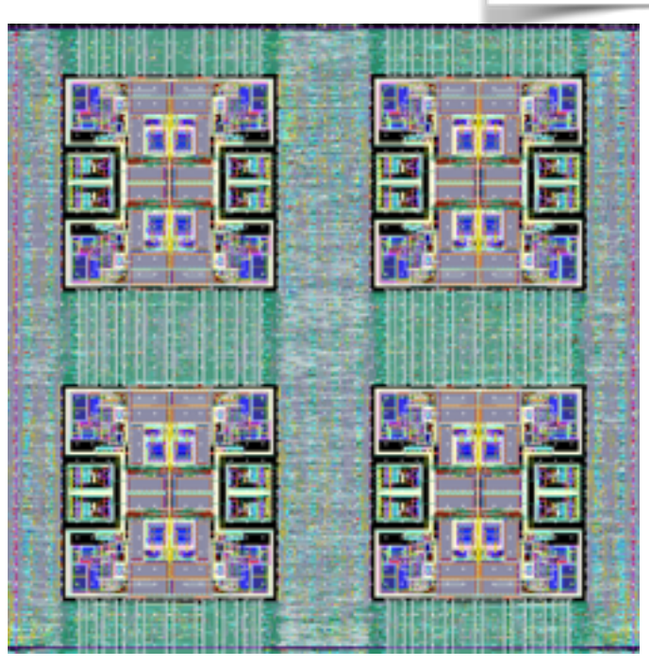


CHIPIX65 demonstrator



CHIPIX65 demonstrator





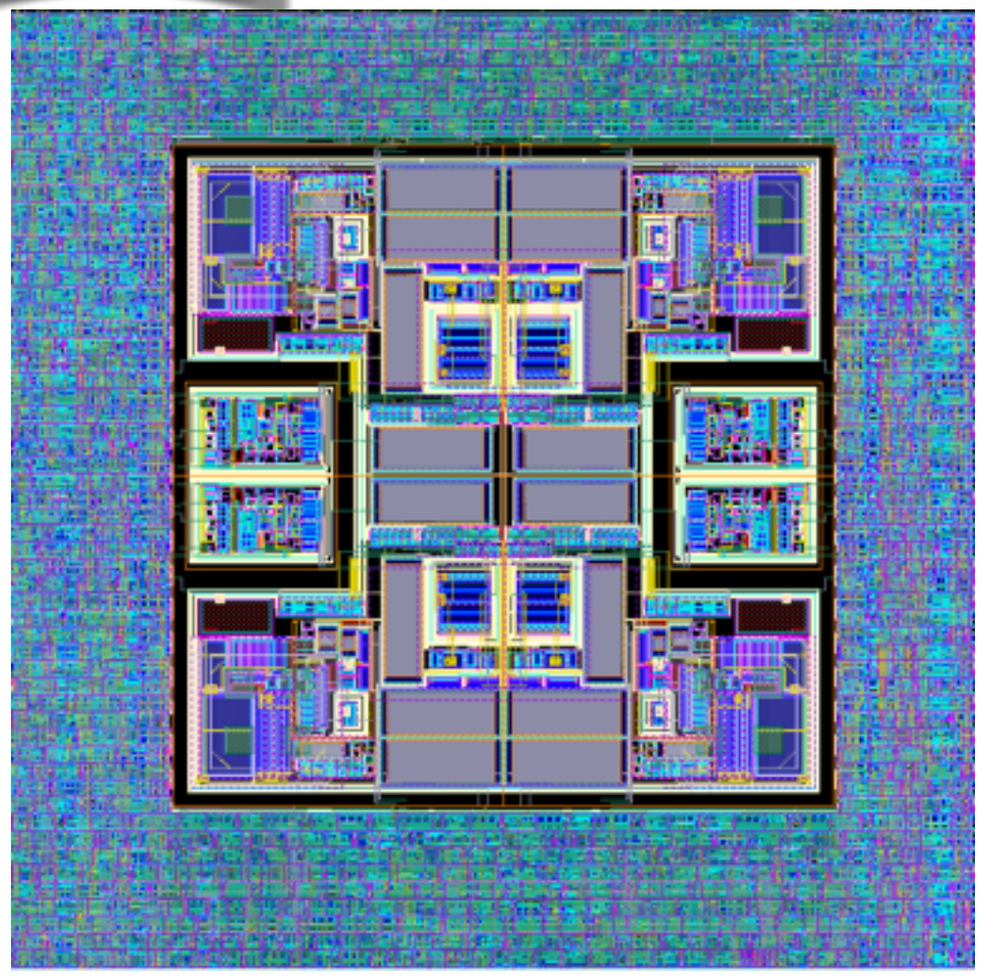
64x64 pixel matrix - 50x50 um²
Organised into (4x4) Pixel Region

HL_HLC flux rates: 3 GHz/cm²
Trigger latency : 12,5 us
In-time threshold : 1200 e-
Noise ~100e- @50fF input capacitance

Dimensions: 3,463 mm x 5,148 mm
~3M of digital standard cells

L.Pacher, A.Paterno, G.DellaCasa
G.Mazza, M.Rolo

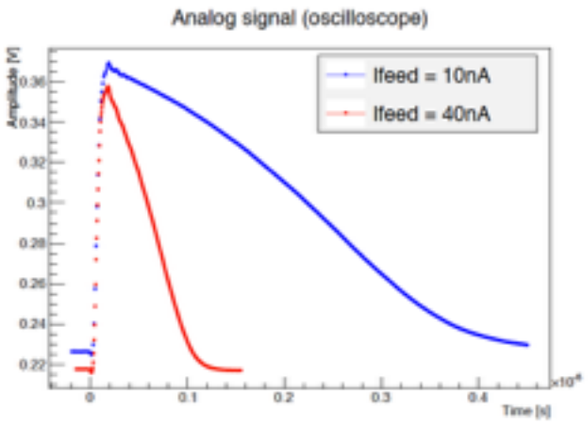
Analog Island

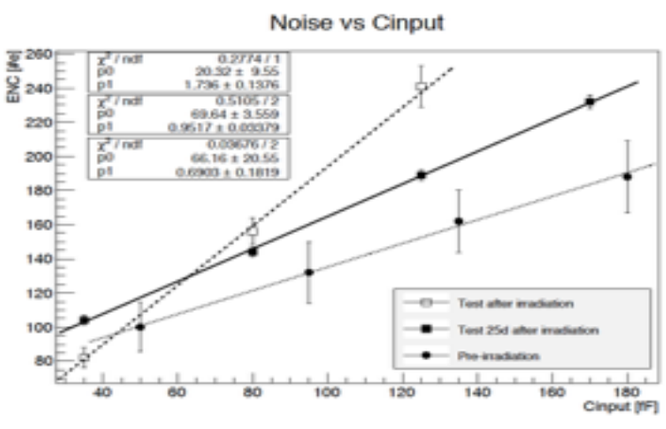


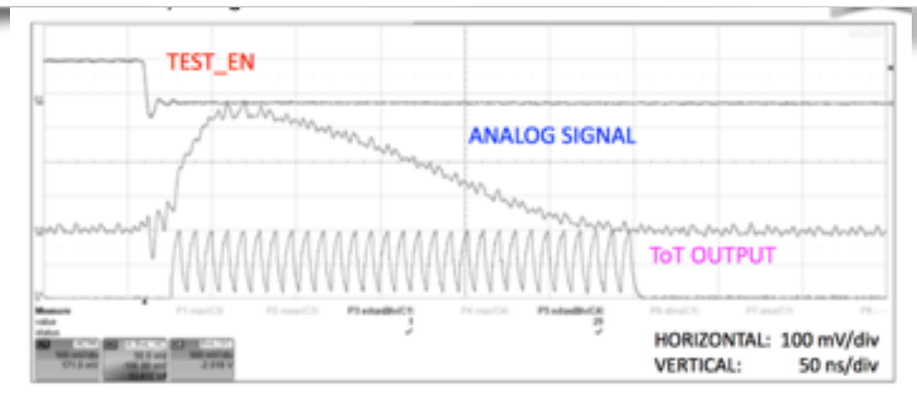
- (2x2) analog Island surrounded by digital logic

Torino ANALOG Very Front End performance SUMMARY

- Compact: < 35um x 35 um
- Low power: 5.5 uW
- Low noise: ENC=90e @C_{det}= 50 fF
- Threshold dispersion : 70e-
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 10 ke with 5-bit digitisation (ToT) in 120ns
- NO Threshold-Trimming:
  - autozeroing made by hardware





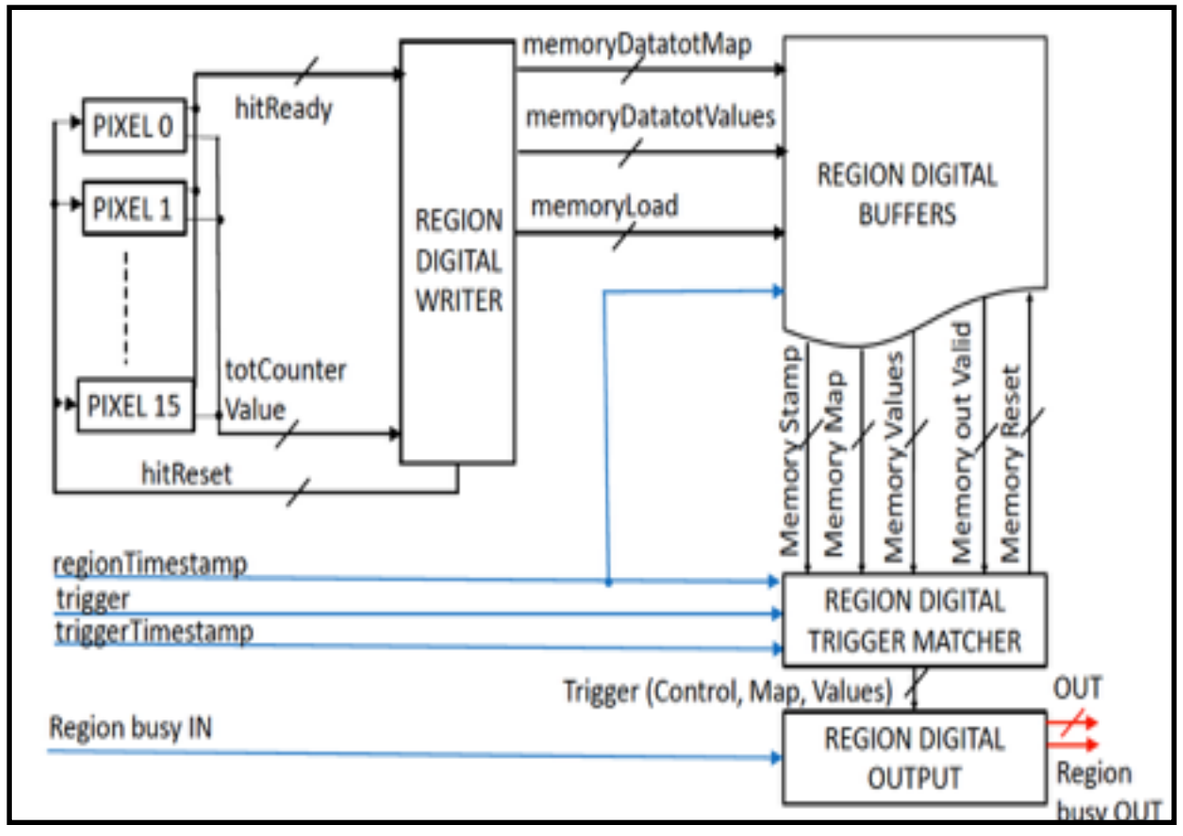


E.Monteil, L.Pacher, LD, AR, MR

test: F.Rotondo; bonding: B.Pini / F.Dumitrache

Region Digital Architecture

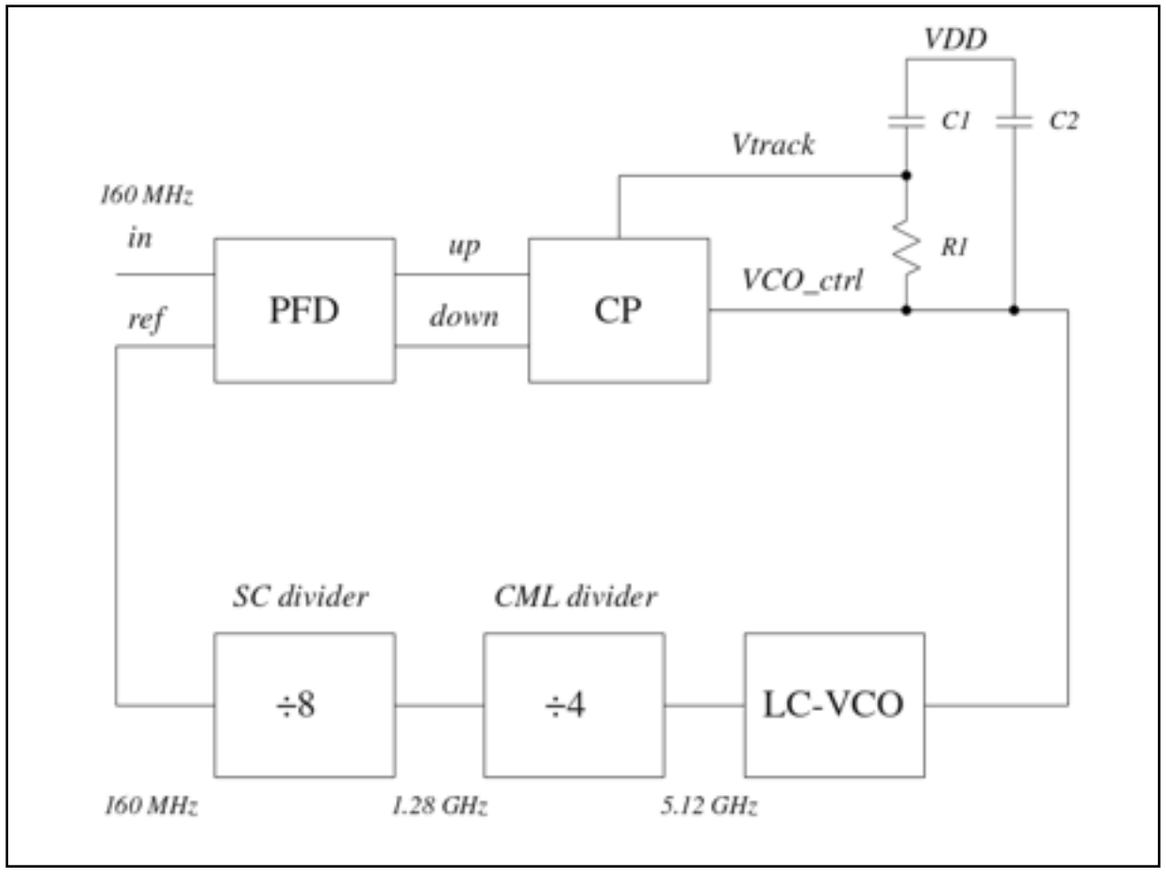
- Inefficiencies (digital) @3GHz/cm^2 ; 12.8 us trigger latency:
  - particle loss < 0.2%
  - single pixel loss = 0; 5-bit ToT ~0,4%
  - aliasing prob (ghosts) < 0,03%
- Inefficiency (analog)
  - depends on dead time : 0.7% (Fast mode, Low dead-time)
- Digital Region functioning modes:
  - TriggerLess / Triggered / Debug
  - BinaryOnly / 5-bit-Tot
  - High / Low deadtime (for Slow or Fast digitisation modes)

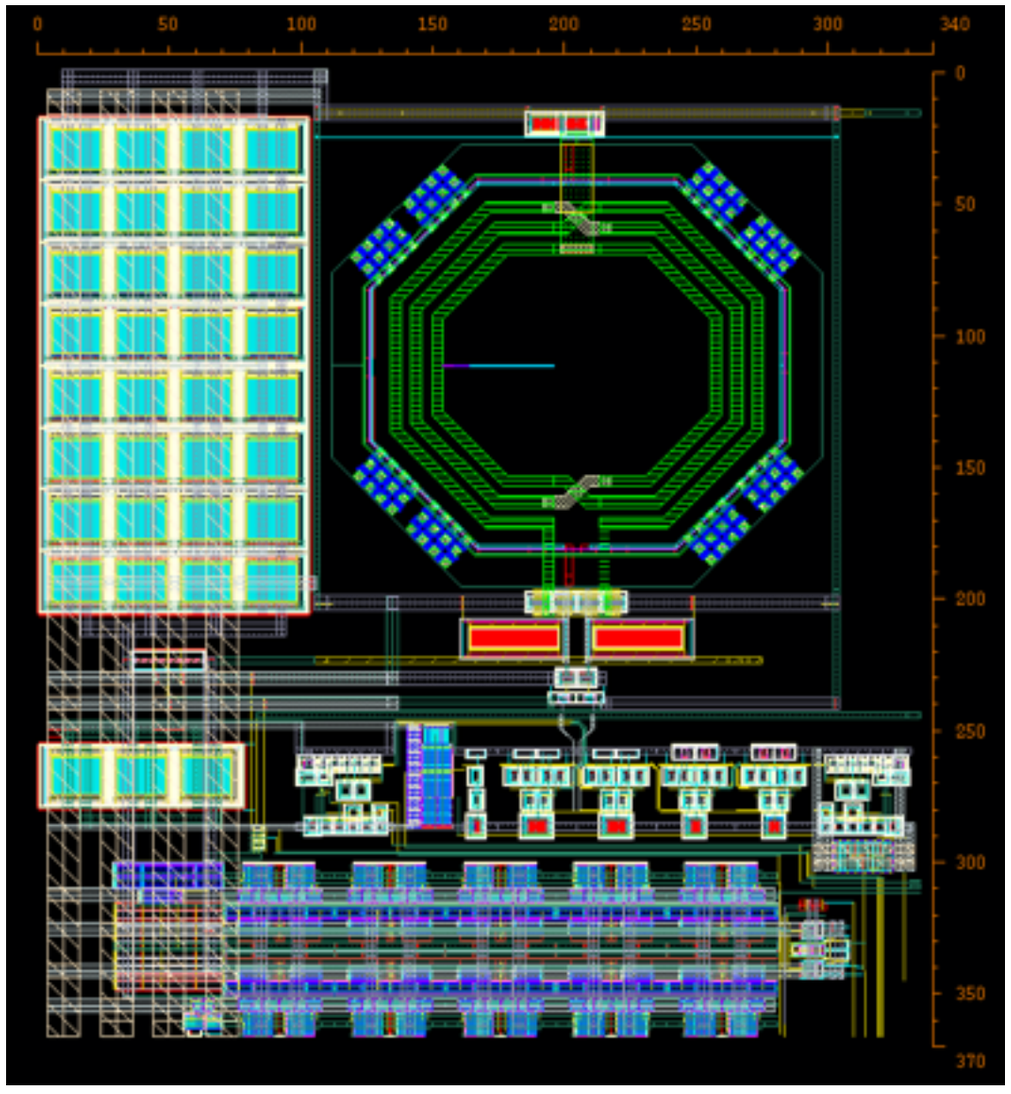


A.Paterno', G.Della Casa, L.Pacher

	Pixel Matrix	Analog VFE	Analog / Digital Isolation	IP-Block	Pixel Region & Arch	Bias-Distrib	Powering	Digital CORE
FE65P2	64x64 pixels	AFE_LBNL	Analog in deep n-well Digital in deep n-well PAD in deep n-weel	few and not RD53A	(2x2) Distributed Latency Buffer	Single stage mirroring	standard	(4x64)
CHIPIX65 demonstrator	64x64 pixels	AFE_TO AFE_PV	Analog in deep n-well	**RD53A IP-blocks**: DAC, ADC, SER, sLVS-TX, sLVS-RX, Bandgap, CERN I/O Pads	(4x4) central Latency Buffer	Double stage mirroring	standard	(4x4)
RD53A	400x192 pixels	AFE_LBNL AFE_TO AFE_PV AFE_FNAL -- tbc : review	Analog in deep n-well Digital in deep n-well PAD in substrate tbc	**RD53A IP-blocks**: DAC, ADC, SER, sLVS-TX, sLVS-RX, Bandgap, CERN I/O Pads, PLL , ShuntLDO, T-sens, Rad-sens	tbd	Double stage mirroring	standard / Serial-Poweering	(8x8) / (4x16)

cp-PLL





LC-based oscillator
Oscillator frequency : **5.12 GHz**
Main output frequency : **1.28 GHz** (fIN × 8)C

Secondary output frequency : 2.56 GHz (fIN × 16)
Technology : CMOS 65 nm
Status : submitted to foundry

PFD: Phase Frequency Detector
CP charge pump

G.Mazza

Activities 2017

- Test CHIPIX65 demonstrator
  - bump bonding con sensori 3D e planari (50x50 e 25x100 um^2)
- Design of RD53A (~2cm^2)
  - Torino Analog VFE
  - Pixel Region architecture
  - Other digital
- Test of RD53A (Q3/Q4 2017)
- On-going activities
  - Analog VFE
  - IP-block

CdS 2016

DOMANDA DI UTILIZZO DEI SERVIZI DI BASE

Data della richiesta: 27-06-2016

Lab. Tecnologico	Lab. Elettronica	Centro di Calcolo
	✓	

nuova richiesta	
richiesta di continuazione	✓

Esperimento: CHIPIX65

Responsabile locale: Natale Demaria

Responsabile dell'attivita':

Descrizione dettagliata dell'attivita' richiesta

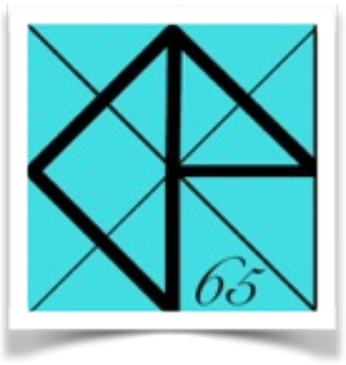
Principali impegni di CHIPIX65/TO: (1) test dimostratore CHIPIX sottomesso nel 2016 senza e con sensori a pixel (15mm2); (2) test RD53A; (3) disegno IP-blocks e VFE-analogici ; (4) sviluppo blocchi digitali per futuro dimostratore CHIPIX65 ed in vista di RD53B . Alcuni dettagli in piu' :
1-2.a) Test-pcb: disegno per adattamento ad uso in test-beam; supporto per il test
1-2.b) Test-DAQ: ulteriore supporto per software su FPGA per il test
1-2.c) Wire-bonding : micro-saldatura dei chip alle pcb
3) Micro-ana : supporto disegno di elettronica analogica di front-end e IP-block (PLL e altri eventuali)

PLANNING													MILESTONES	
Subattivita'	G	F	M	A	M	G	L	A	S	O	N	D	Data-mese	Descrizione
test-pcb		✓				✓	✓			✓				Vedi sopra
test-DAQ		✓				✓								
Micro-ana			✓		✓	✓			✓					
Digitale					✓				✓	✓	✓			
Wire-bonding			✓				✓							

Tecnici e tecnologi attualmente assegnati all'attivita'					Richieste di supporto tecnico per		
INFN		ALTRI ENTI				l'anno:	
Nome	mesi/U	Ente	Nome	mesi/U	Tipologia	N.	mesi/U
Manuel Rolo	20%				Tecnici mecc. /elettr/CdC	2	5m
Gianni Mazza	20%				Disegnatori meccanici		
Angelo Rivetti	15%				Microsaldatori	1	2m
Giulio Della Casa	3m				Tecnologi progett. mecc.		
Richard Wheadon	20%				Tecnologi elettronici/CdC	1	20%
Dumitrache + Ro	4m				Tecnologi microelettronica	2	40%

Note:

La sottomissione di RD53A e' prevista per Aprile 2017: potrebbe essere soggetta a ritardi di qualche mese, ma sara' comunque entro l'estate 2017



BackUp Slides

CdS 2015

DOMANDA DI UTILIZZO DEI SERVIZI DI BASE

Data della richiesta:	Lab. Tecnologico	Lab. Elettronica	Centro di Calcolo	nuova richiesta	richiesta di continuazione
22-06-2015		✓			✓

Esperimento: CHIPIX65 (progetto CALL CSN5)

Responsabile locale: Natale Demaria

Responsabile dell'attivita':

Descrizione dettagliata dell'attivita' richiesta

Principali impegni di CHIPIX65/TO: (1) test del CHIP DIMOSTRATORE INFN (circa 16mm2) disegnato nel 2015; (2) DISEGNO per il prototipo di RD53 (RD53A, circa 2cm2). Le richieste dettagliate sono:
1.a) Test-pcb : disegno elettronica ancillare per adattamento DIMOSTRATORE INFN a setup di test, supporto su test
1.b) Test-DAQ: adattamento chip al set-up di test general purpose (con FPGA) con scrittura firmware per FPGA
1.c) Bonding di chip sottomessi
2.a) Micro-ana: Supporto DISEGNO elettronica analogica di front-end per PROTOTIPO RD53A
2.b) Micro-dig : Supporto DISEGNO elettronica digitale per PROTOTIPO RD53A
2.c) IP : DISEGNO IP-block in 65nm (PLL, other)

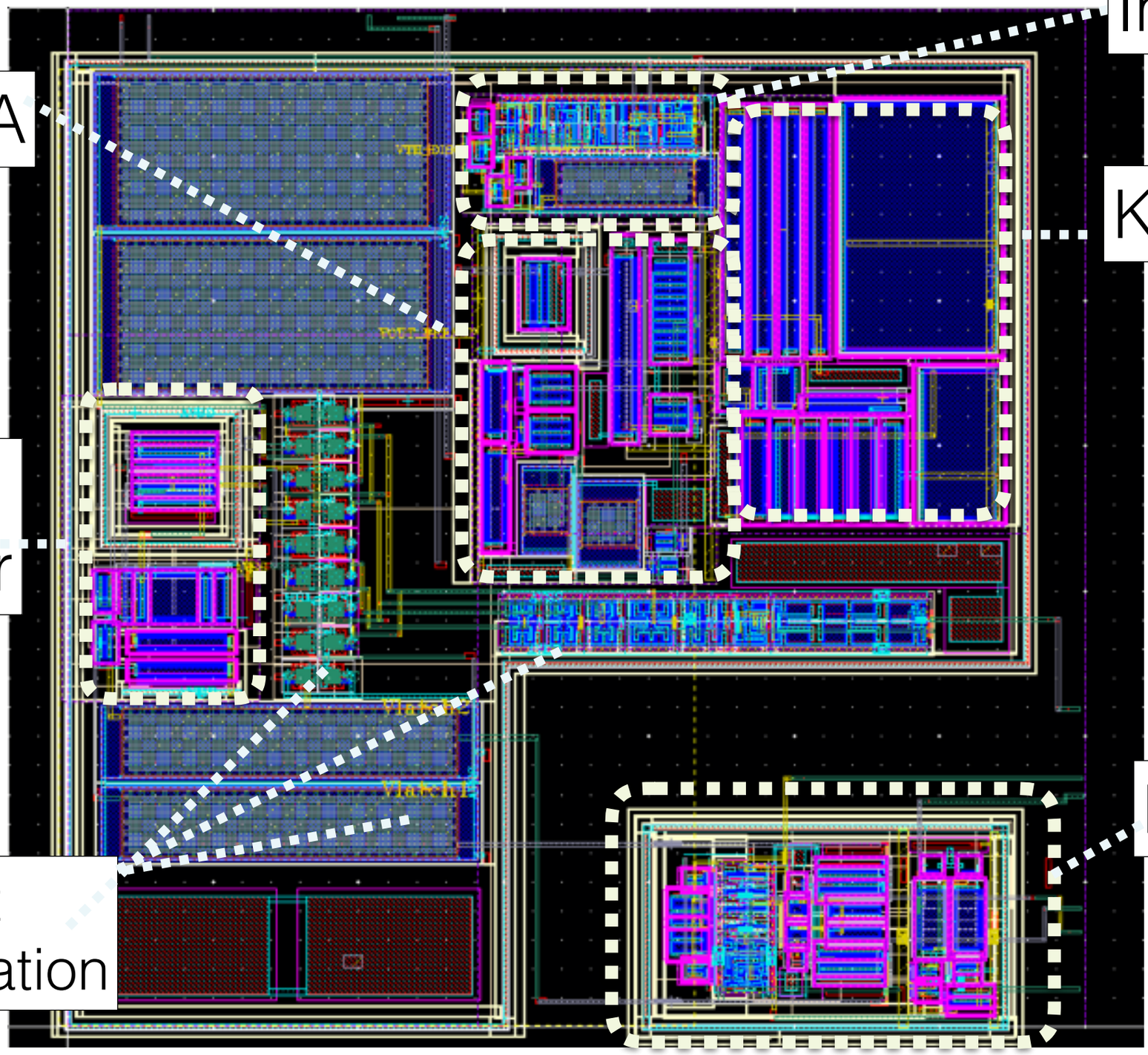
PLANNING													MILESTONES	
Subattivita'	G	F	M	A	M	G	L	A	S	O	N	D	Data-mese	Descrizione
test-pcb		✓	✓	✓	✓									vedi sopra
test-DAQ				✓	✓	✓								
bonding			✓			✓			✓					vedi sopra
micro-ana			✓	✓	✓	✓				✓	✓			
micro-digi		✓	✓	✓	✓	✓			✓	✓				
IP		✓	✓	✓					✓					

Tecnici e tecnologi attualmente assegnati all'attivita'					Richieste di supporto tecnico per		
INFN		ALTRI ENTI				l'anno:	2016
Nome	mesi/U	Ente	Nome	mesi/U	Tipologia	N.	mesi/U
Giovanni Mazza	30%				Tecnici mecc. /elettr/CdC	2	5m
Angelo Rivetti	15%				Disegnatori meccanici		
Giulio Della Casa	3m				Microsaldatori	1	2m
Richard Wheadon	20%	(rich.x204			Tecnologi progett. mecc.		
Flori Dumitrache	2m				Tecnologi elettronici/CdC	1	20%
F. Rotondo	2m				Tecnologi microelettronica	2	45%

Note:

La sottomissione del chip RD53A e' prevista in Q3-Q4/2016, ma puo' facilmente slittare a Q1-2017 (questo non varia la richiesta di progettazione di micro-elettronica)

Synch VFE



AREA: 35um x 35um to fit with other designs, but could be made smaller

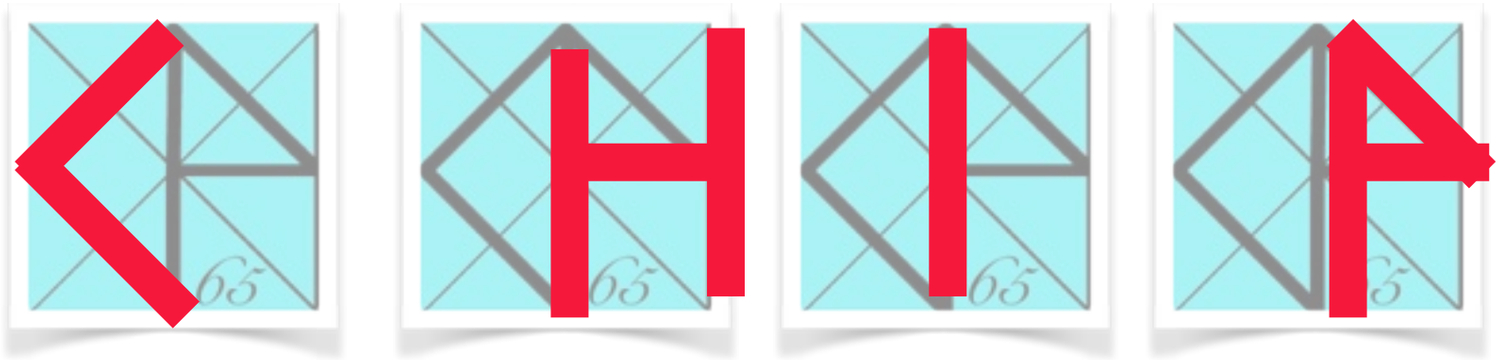
AFE and Latch in different deep n-well

I/O interface

Name	Direction	Description
CLK_BX±	input	40 MHz BX clock
RSTN±	input	global asynchronous reset (active low)
TRIGGER±	input	trigger
CLK_SER±	input	$\geq$ 320 MHz serializer clock
SDO±	output	output serial data stream
TESTP±	input	charge-injection control signal
SCAN_MODE	input	global scan test-mode enable (CMOS)
SCLK±	input	13.33 MHz SPI configuration clock
SSN_or_SCAN_EN±	input	multiplexed SPI slave-select/shift-enable
MOSI_or_SCAN_IN±	input	multiplexed SPI input configuration data/scan-in
MISO_or_SCAN_OUT±	output	multiplexed SPI output configuration data/scan-out / Fast Or
VREF	inout	monitored bandgap reference voltage
IDAC	inout	monitored multiplexed global DACs reference current
VADC	inout	monitored ADC input voltage
VTH_ADC	inout	monitored ADC reference voltage
VTH_BYPASS	inout	bypass point in case ADC extra-noise filtering is required

- dedicated **test pads** for monitoring purposes
- **320 Mb/s readout bandwidth** enough to comply with nominal HL-LHC hit rates re-scaled on a small 64×64 pixel array

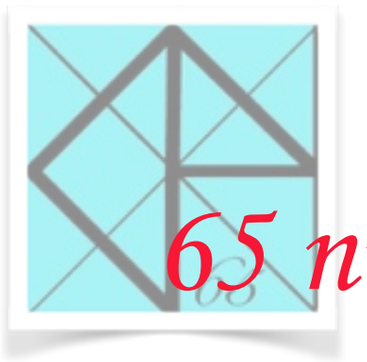
An innovative



for a

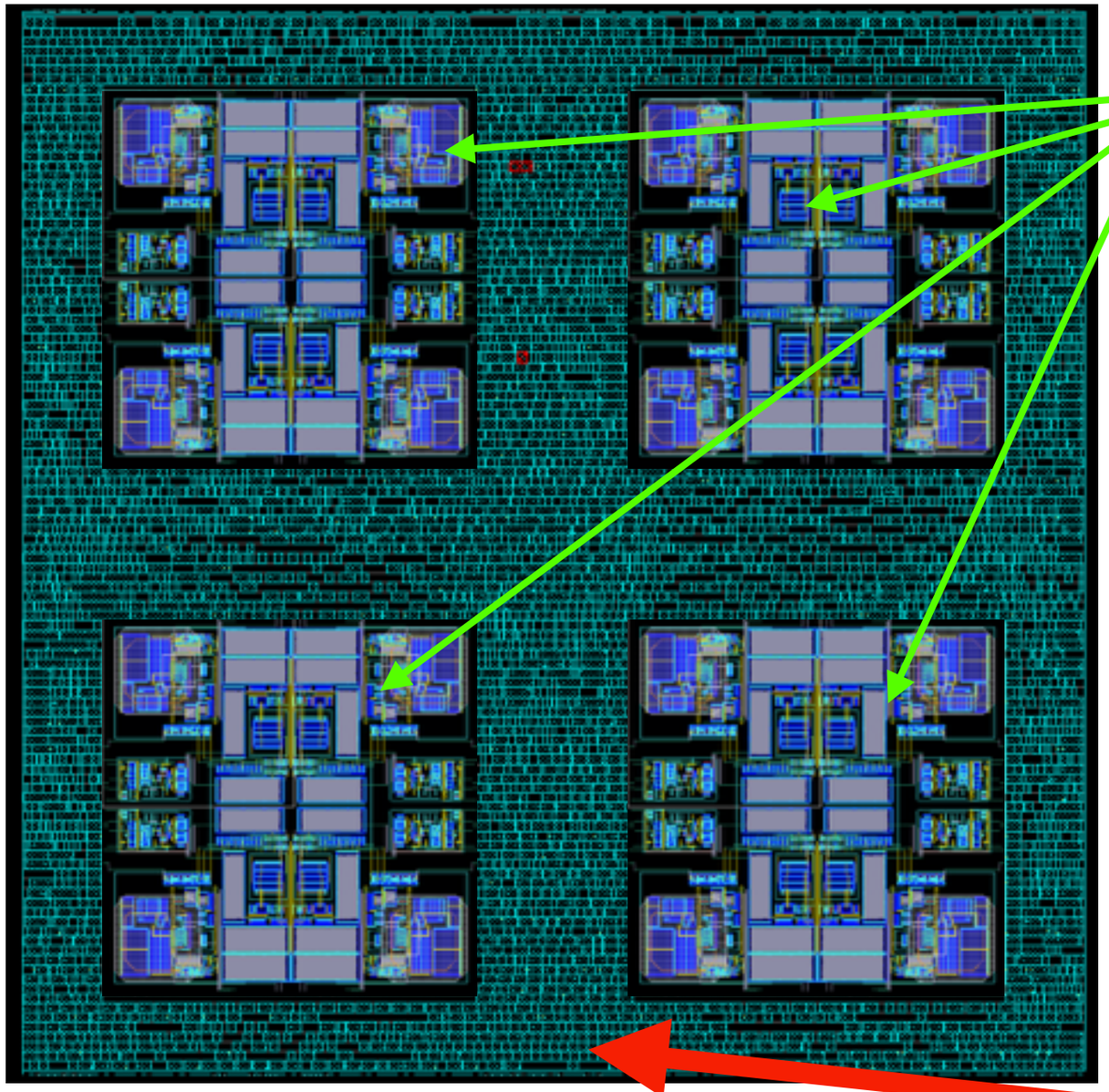
EL detector

using a CMOS



65 nm technology

Pixel Region (4x4)

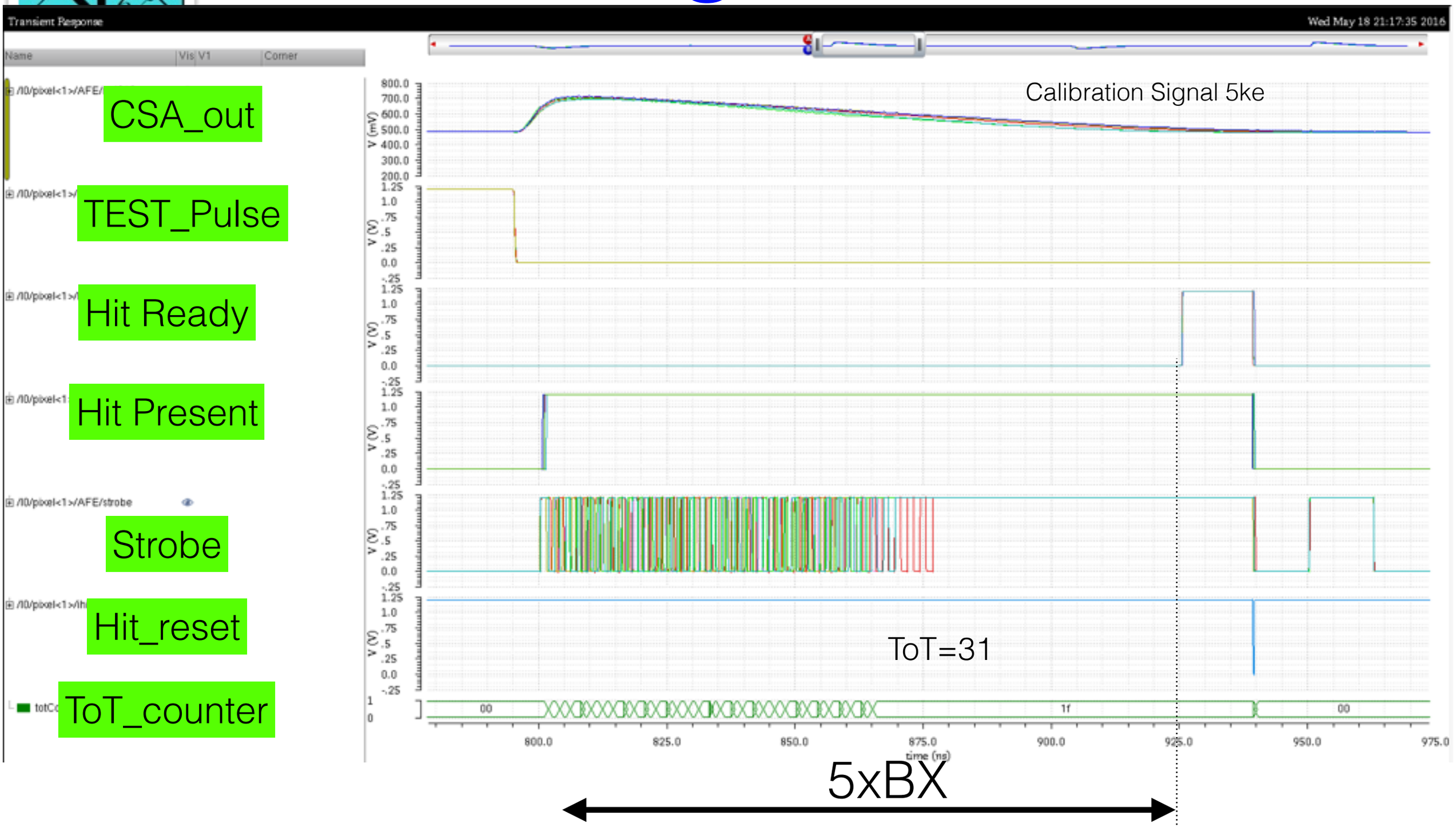


- (2x2) **analog inlands** in deep n-wells
- routing in lower metal
- shielding of bias-lines
- top three metals for power grid
- Digital P&R at 67% despite using **5-bit ToT** information. Some space remain still available

- Total power ~ 92 uW ==> 5.7 uW/pix (but with 5bit -ToT)

Sea of Digital standard cells

Hit Logic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TEST_Pulse
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Hit Present
Strobe
Hit_reset
ToT_counter
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