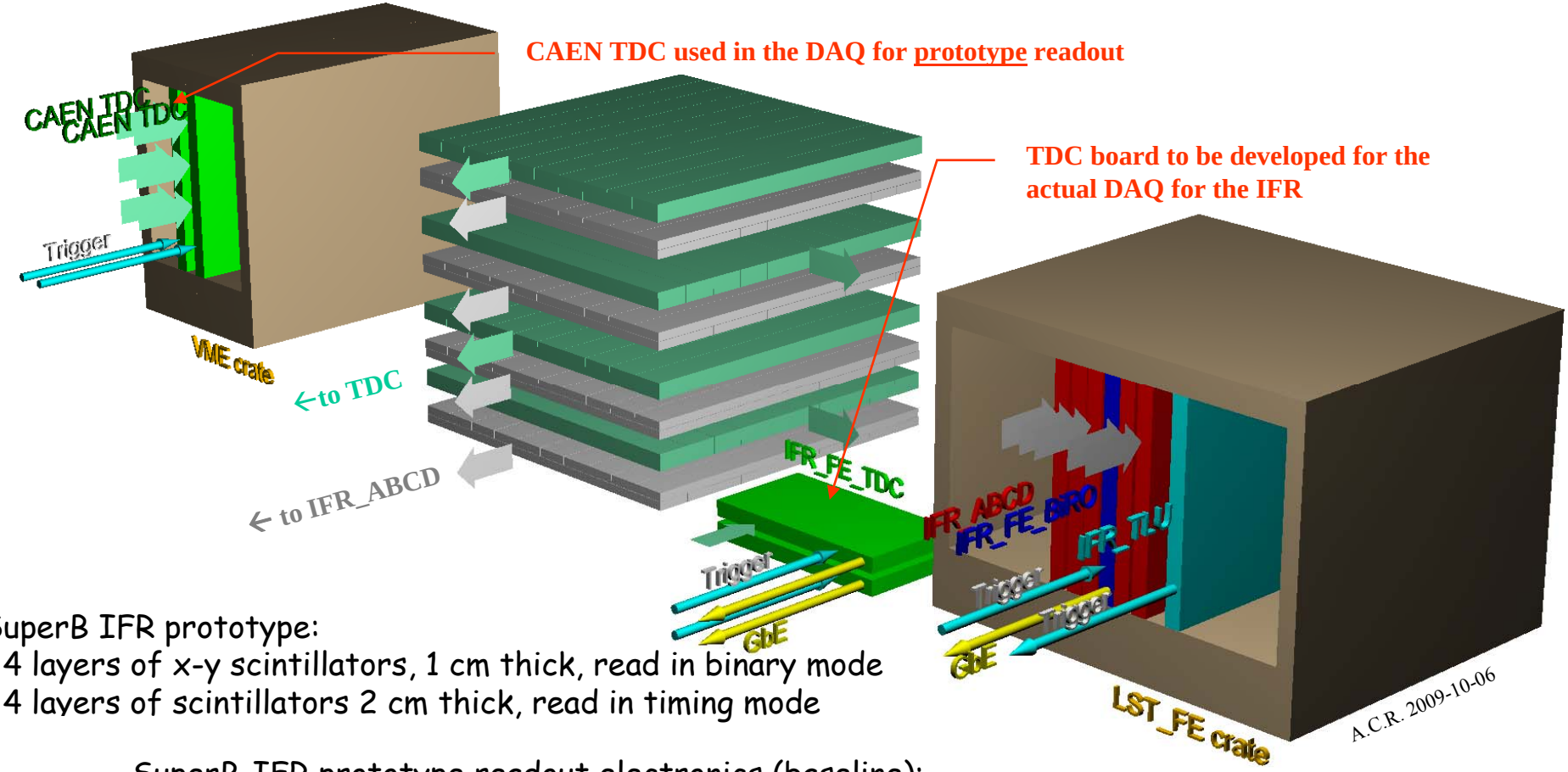
SuperB IFR: outline of the IFR DAQ electronics

Summary

- prototype detector and electronics for a proof of principle
- status of IFR prototype development
- updated IFR detector data bandwidth and event size estimates

outline of the IFR DAQ electronics: prototype detector and electronics for a proof of principle

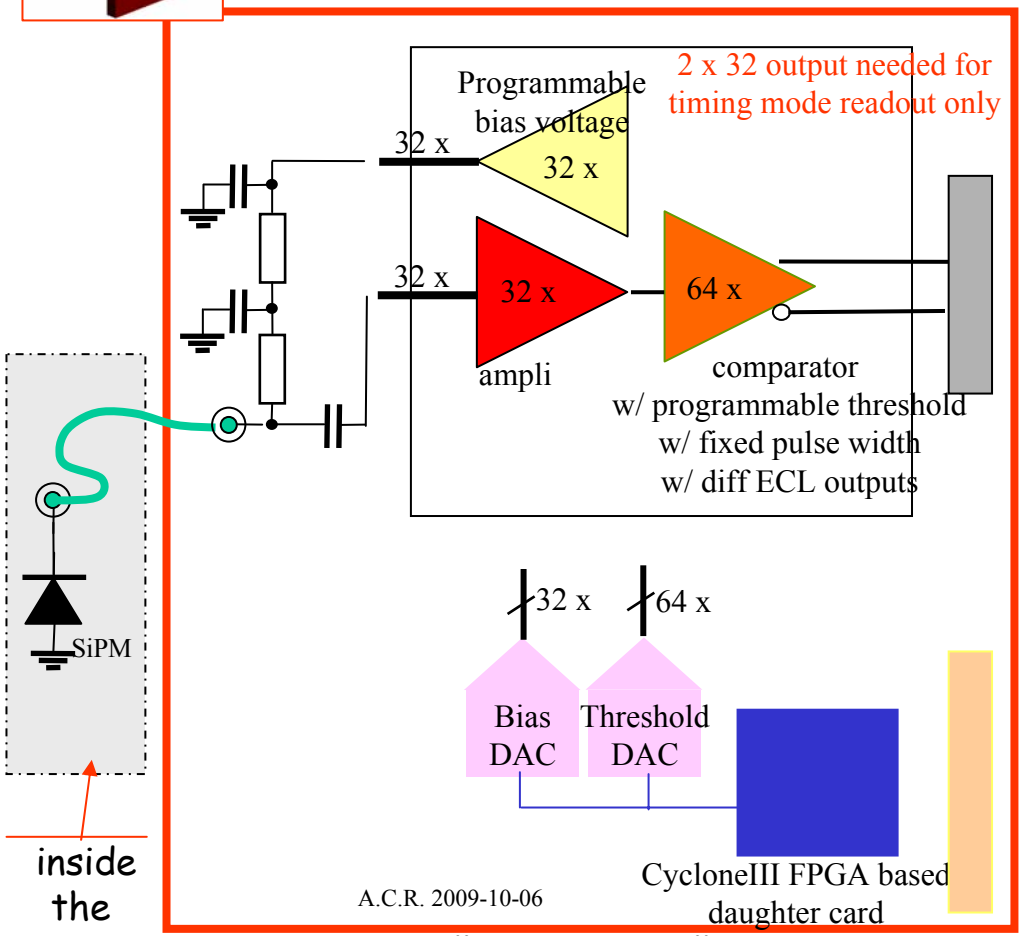


SuperB IFR prototype:
- 4 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode

SuperB-IFR prototype readout electronics (baseline):
- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, (new!) Data processing: it samples and stores the comparators outputs, pending the trigger request
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

outline of the IFR DAQ electronics: prototype detector and electronics for a proof of principle

dimensions: VME 6U x 220mm



Outline of the **"IFR_ABCD"** card

(Amplifier, Bias, Comparator,DataProcessing)

IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by R. Malaguti, INFN-Ferrara

"IFR_ABCD" card features:

- ampli: two stage w/discrete components: BGA2748(0.42$ea) + BGA2716(0.33$ea)
- discri: ADCMP562BRQ (PECL out, dual, 2.7$ea) or ADCMP563BRQ (ECL out, dual, 2.7$ea)

For the readout in timing mode of the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

- DAC: LTC2625CGN#PBF (I^2C, 12bit, octal, 11.63$ea)
- FPGA: ALTERA EP3C40Q240C8 (80$ ea), Cyclone III family, 40KGates
- signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD (3€ea for the PCB-mount+ 6.5€ea for the cable mount)

Total **"IFR_ABCD"** needed for prototype readout : **8**

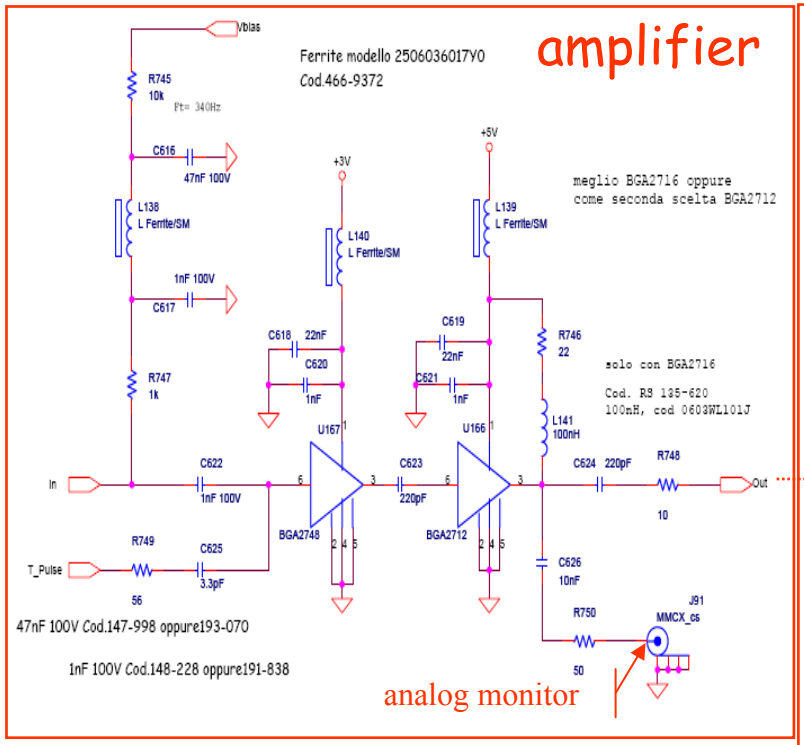
In the board for the final DAQ the Cyclone III will be replaced by a simpler ALTERA MAX-II CPLD (flash-based)

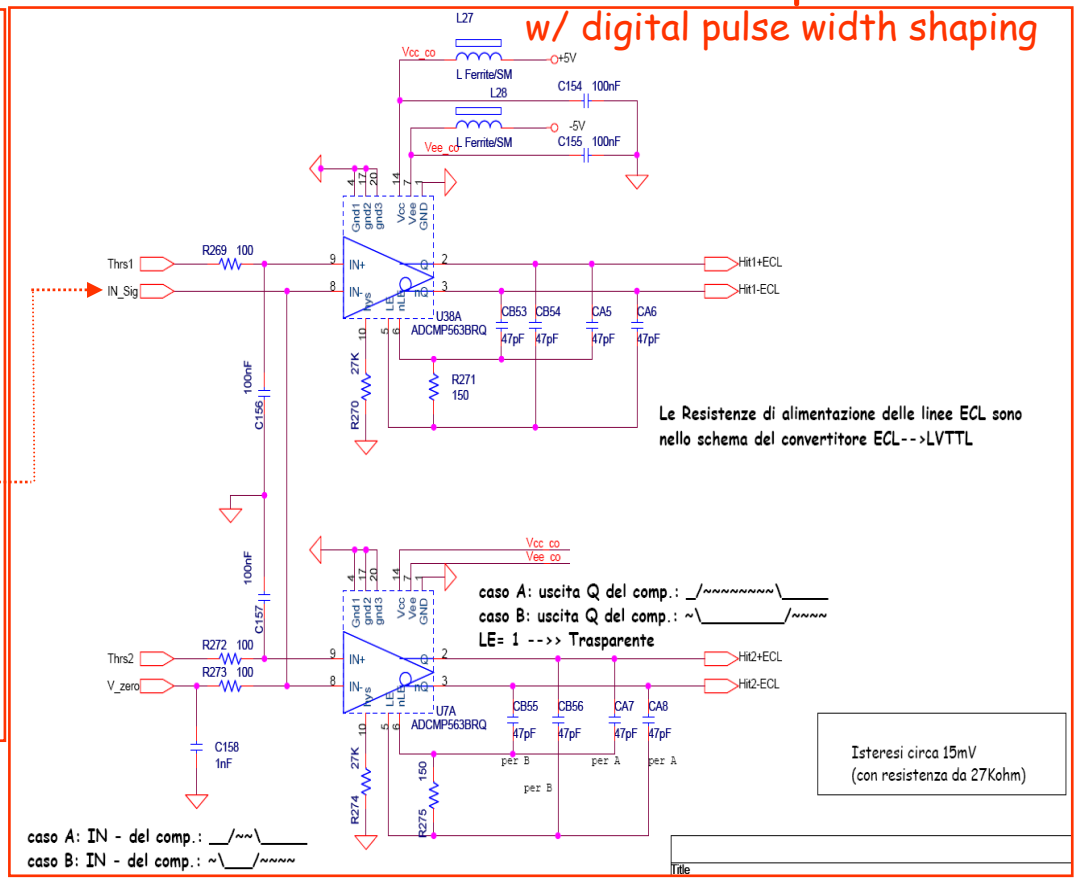
"IFR_ABCD" card schematic: amplifier stage based on the MMIC amplifiers BGA2748/BGA2716

amplifier

Dual comparator

w/ digital pulse width shaping

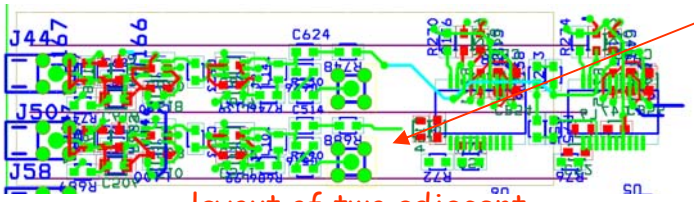




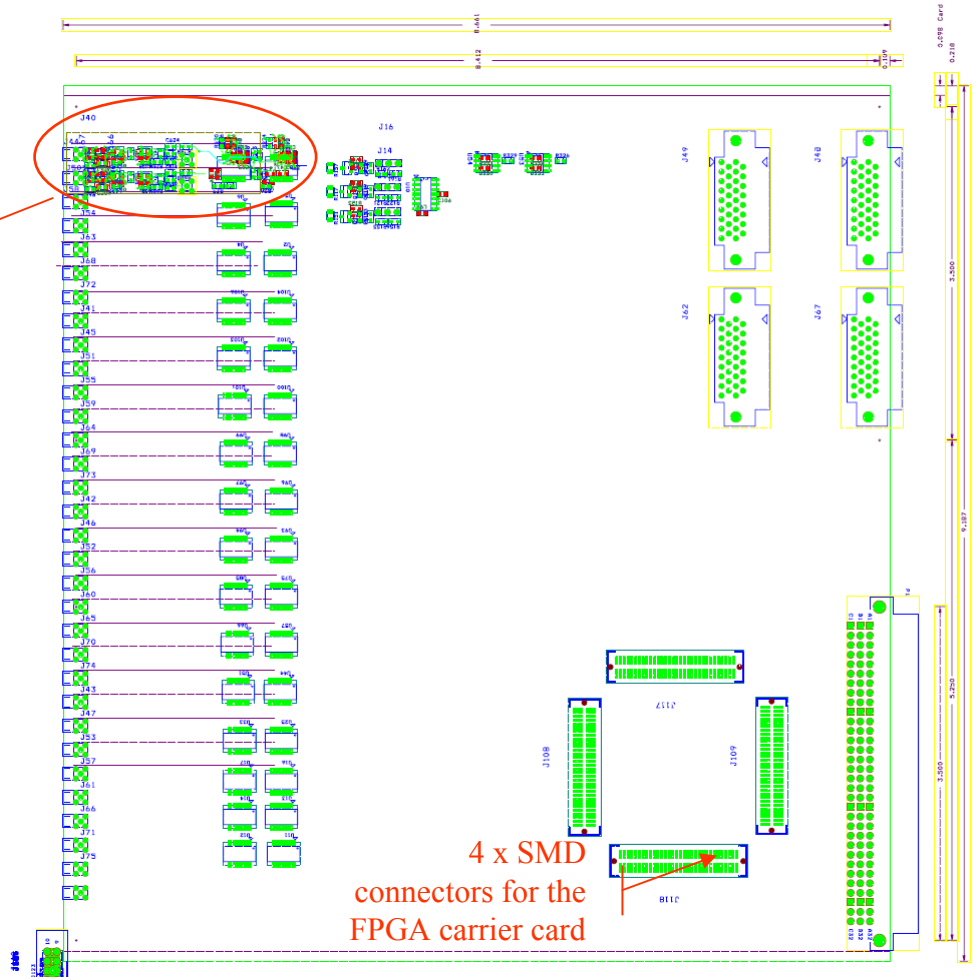
IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by R. Malaguti, INFN-Ferrara

Outline of readout electronics for the SuperB IFR prototype

"IFR_ABCD" card preliminary placement studies

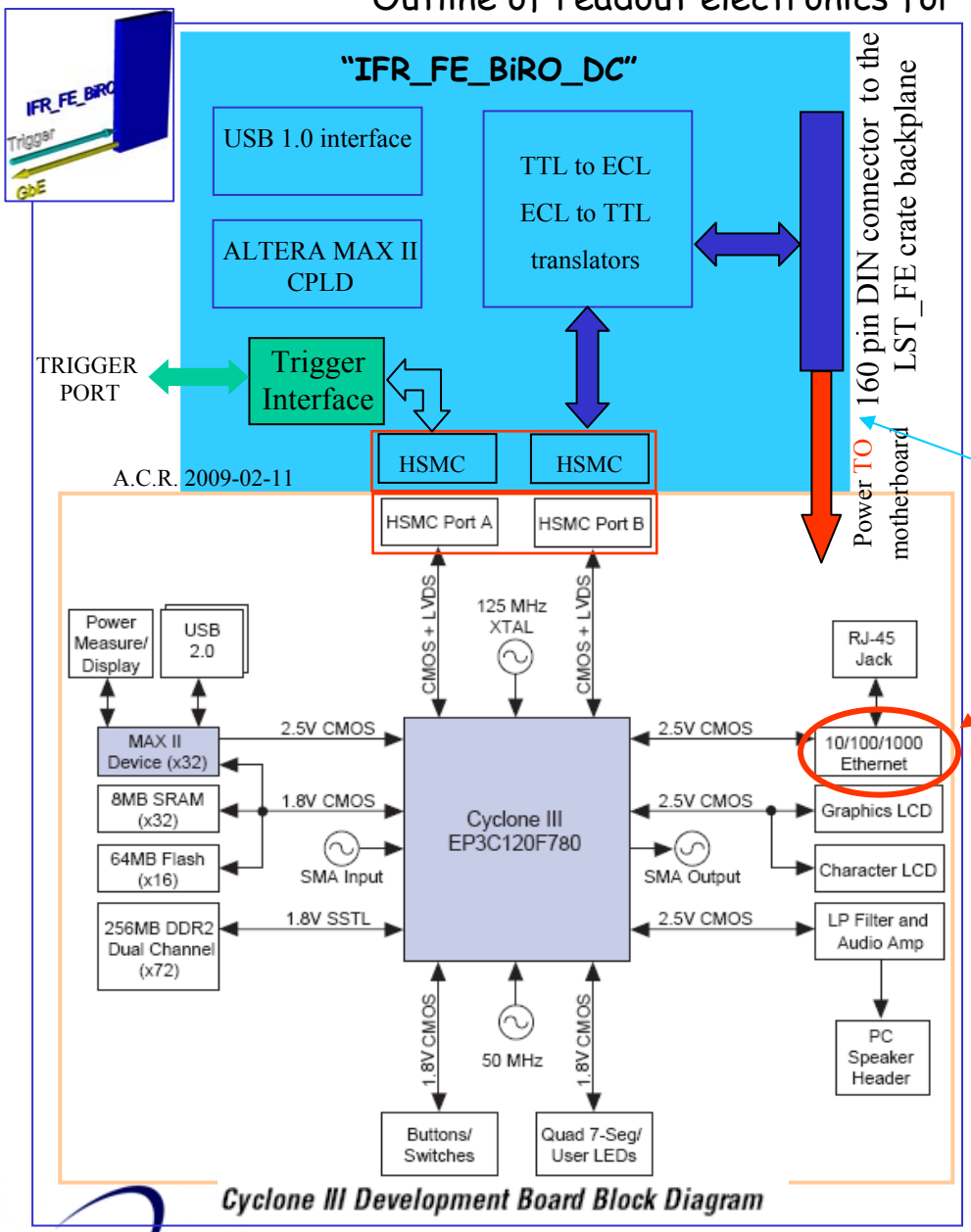


layout of two adjacent amplifier-discriminator-bias channels



IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by R. Malaguti, INFN-Ferrara

Outline of readout electronics for the SuperB IFR prototype



Outline of the "IFR_FE_BiRO" card

"IFR_FE_BiRO" card features:

• motherboard: it is based on an ALTERA development board for the Cyclone III FPGA (**DK-DEV-3C120N, cost 1000 €**). The Cyclone III FPGA has enough on board memory resources to buffer the data collected from the LST_FE boards. Data requested by a trigger is sent over the GbE link featured by the development board.

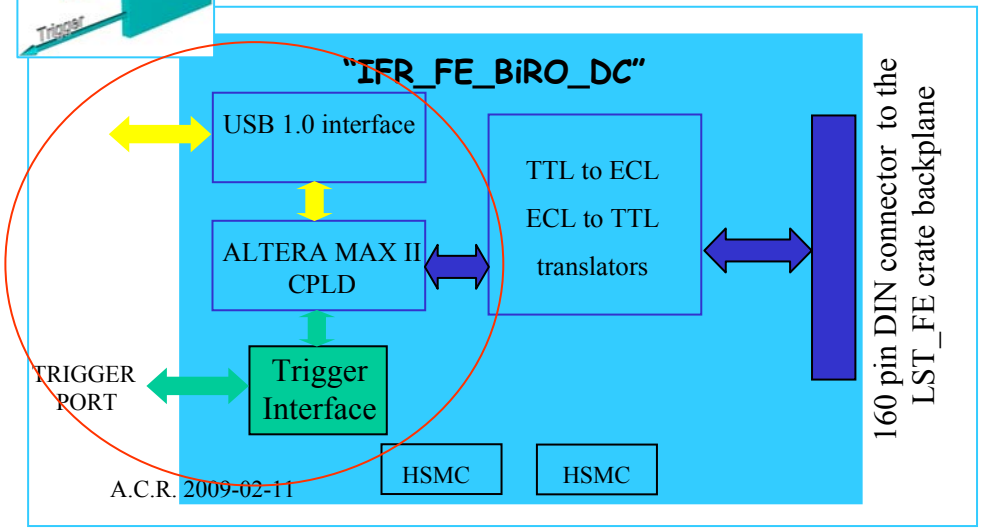
• daughter card (**"IFR_FE_BiRO_DC"**): it provides mostly level translators and connections to:

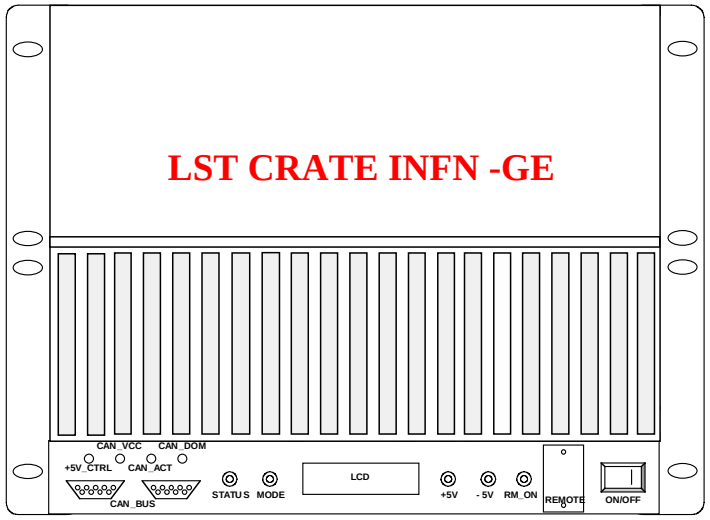
- the LST_FE crate backplane
- the Trigger Logic Unit
- the motherboard through the HSMC connectors (SAMTEC ASP-122952-01)

The final "IFR_FE_BiRO" will be single – decked and the receivers for the differential inputs signals would be integrated on the PCB. It will feature 128 inputs (driven by the "IFR_ABC" boards)

Outline of readout electronics for the SuperB IFR prototype

Outline of the "IFR_TLU" card





Layout of the BaBar LST crate

"IFR_TLU" card features:

- **it is simply the "IFR_FE_BiRO_DC"** (plugged in a specific location of the LST_FE backplane) in which the section based on the ALTERA MAX-II CPLD is activated.

  The CPLD performs programmable (via USB 1.0 ?) combinatorial functions on the "Fast-OR" signals coming from the "LST_FE" cards to generate the trigger requests to the DAQ.

the "IFR_TLU" provides level translators and connections to:

- the LST_FE crate backplane
- the Trigger Logic Unit I/o port (which includes an Open Collector "Busy" Line driven by the FE cards)
- additional inputs for external trigger sources

outline of the IFR DAQ electronics: prototype detector and electronics for a proof of principle

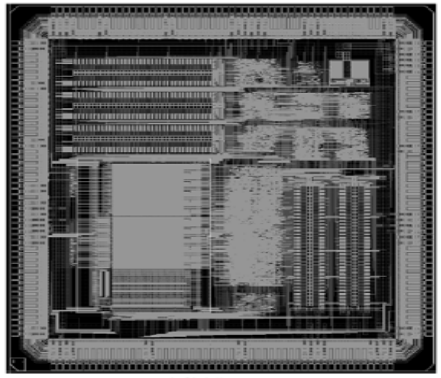
Multihit TDC candidates:

HPTDC

High Performance Time to Digital Converter

Version 2.2, March 2004

for HPTDC version 1.3



J. Christiansen
CERN/EP - MIC
Email: jorgen.christiansen@cern.ch

- **reference clock frequency: 40MHz**
- **"trigger matching" function:**

A unique feature of the trigger matching in the HPTDC is its capability to assign hit measurements to multiple triggers. This becomes important in applications with large drift times and closely spaced triggers. Hits are only removed from the L1 buffers if they are older (not within matching window) than the latest processed trigger or have been found "rejectable" by a special reject function.

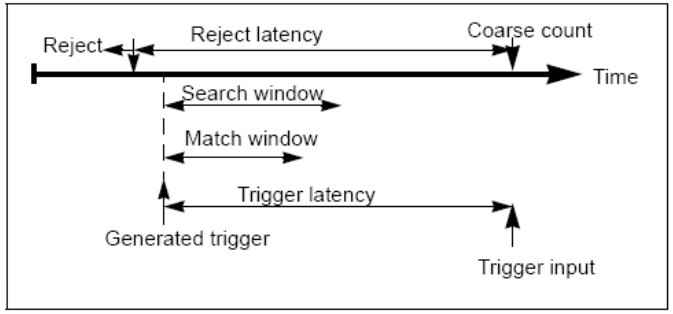


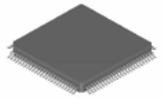
Fig. 8 Trigger, trigger latency and trigger window related to hits on channels

acam ness electronic

TDC-GPX

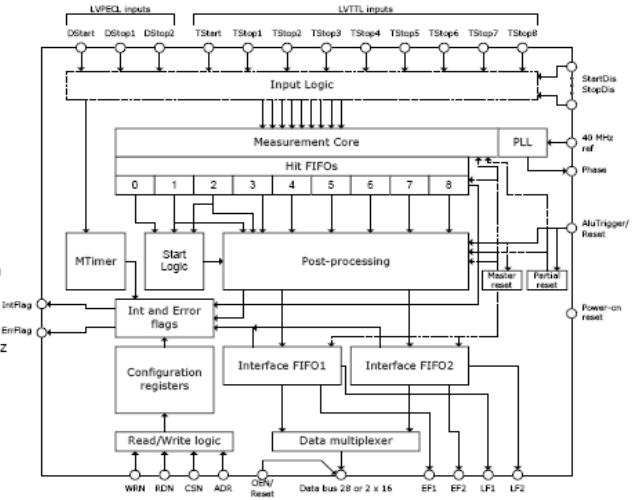
1. Introduction

1.1 System overview



I-Mode

- 8 channels with typ. 81 ps resolution
- 9 LVTTL inputs, optional 3 LVPECL inputs
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability – 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range 9.8 µs, endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip



- **reference clock frequency: 40MHz**
- **no "trigger matching" function**

On-chip trigger matching could be exploited with great advantage when the L1 trigger is at fixed latency w.r.t. the event, as proposed by D.Breton (LAL), U.Marconi (INFN) in: "Proposal for the Electronics Trigger and DAQ architecture of SuperB".

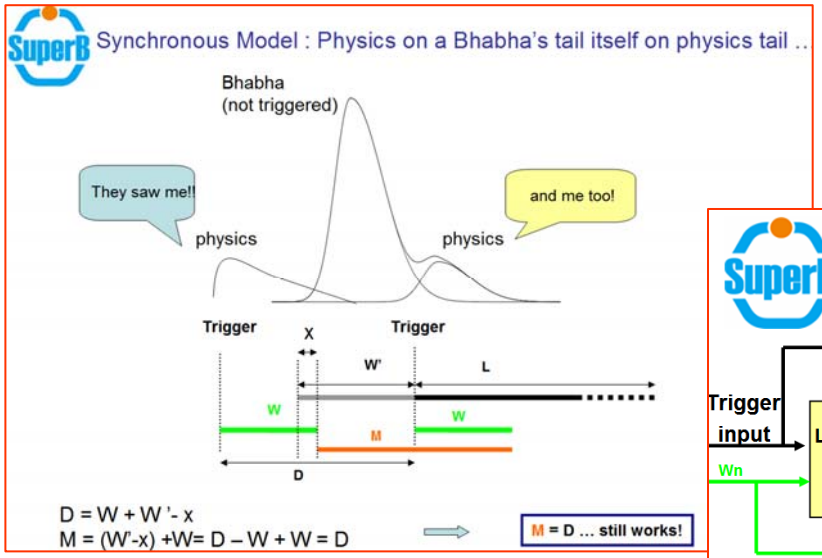
But…→

outline of the IFR DAQ electronics: prototype detector and electronics for a proof of principle

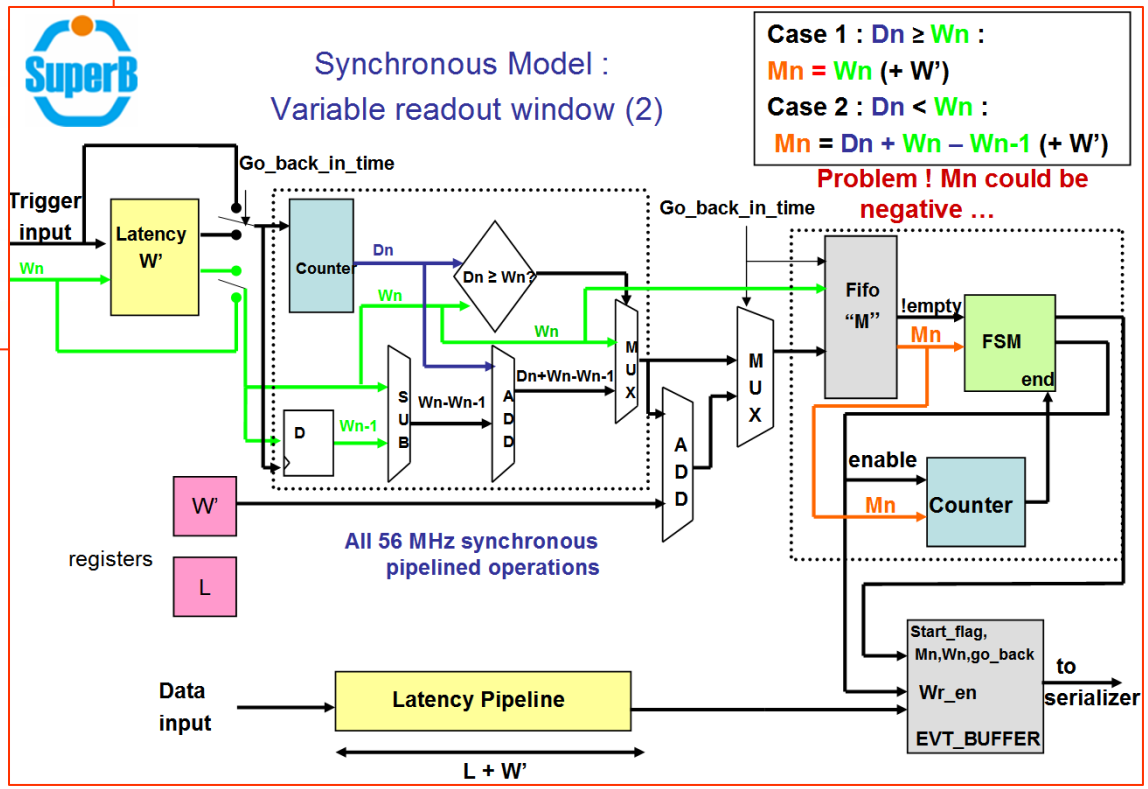
Multihit TDC candidates:

… continuing:

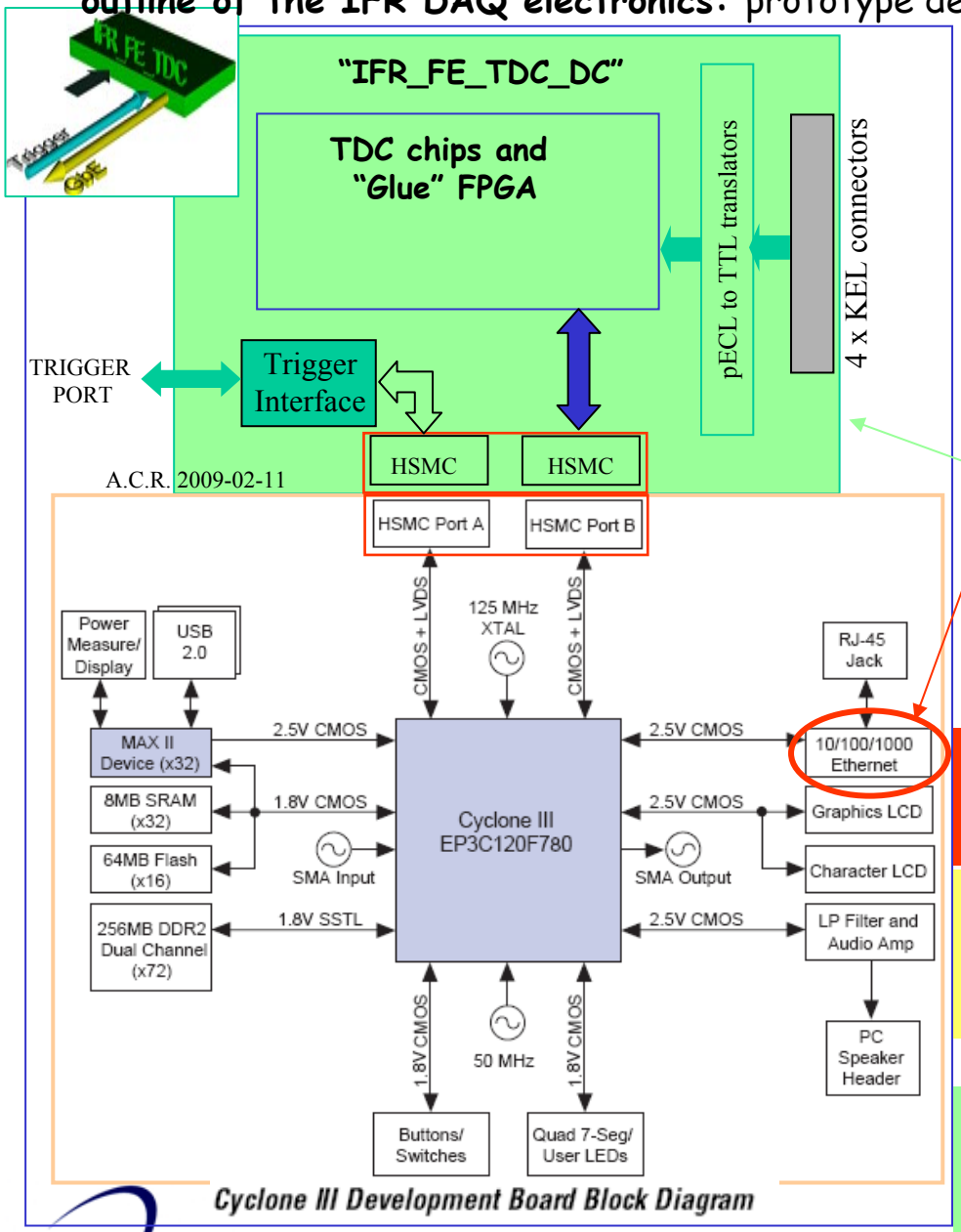
the L1 trigger handling outlined in **« Modelisation of SuperB Front-End Electronics » (Christophe Beigbeder, Dominique Breton, Jihane Maalmi)** cannot be performed by the HP-TDCs on chip trigger matching function → ALL DATA MUST BE TRANSFERRED FROM THE TDC TO AN OFF-CHIP DATA STORAGE MANAGED BY AN FPGA WHICH COULD IMPLEMENT THE MODELS SUGGESTED IN THE PAPER:



➔ THE HP-TDC LOOSES ITS ADVANTAGE OVER ACAM's TDC-GPX, commercially available and of simpler utilization



outline of the IFR DAQ electronics: prototype detector and electronics for a proof of principle



Outline of the "IFR_FE_TDC" card

"IFR_FE_TDC" card features (prototype version):

• motherboard: it is based on the ALTERA **DK-DEV-3C120N** development board.The Cyclone III FPGA continuously collects data from the **"IFR_FE_TDC_DC"** daughter card and stores it in a circular buffer pending a trigger request. Data requested by a trigger is sent over the on-board GbE link.

• daughter card (**"IFR_FE_TDC_DC"**): it features 8 x ACAM TDC-GPX chips to handle at least 64 channels per board. An on-board "glue" FPGA configures the TDC chips and reads them out periodically to pass ALL recorded events to the motherboard. The daughter card also forwards the trigger signal to the motherboard.

Unfortunately it does not seem possible to build a prototype "IFR_FE_TDC" in time for reading out the IFR prototype.

It is assumed that the TDC could be located far enough from the IFR iron to be in a low radiation environment → SEU mitigation resources provided by the CycloneIII FPGA should suffice

The final "IFR_FE_TDC" will be single – decked and will (likely) feature 64 inputs (driven by the "IFR_ABC" boards)

Current status:

- **IFR_ABCD:**
  - the schematic of the motherboard is complete and it has been sent out for layout.
  - the design of the schematic for the daughter card carrying the on-board FPGA has started
  - active components have been ordered.

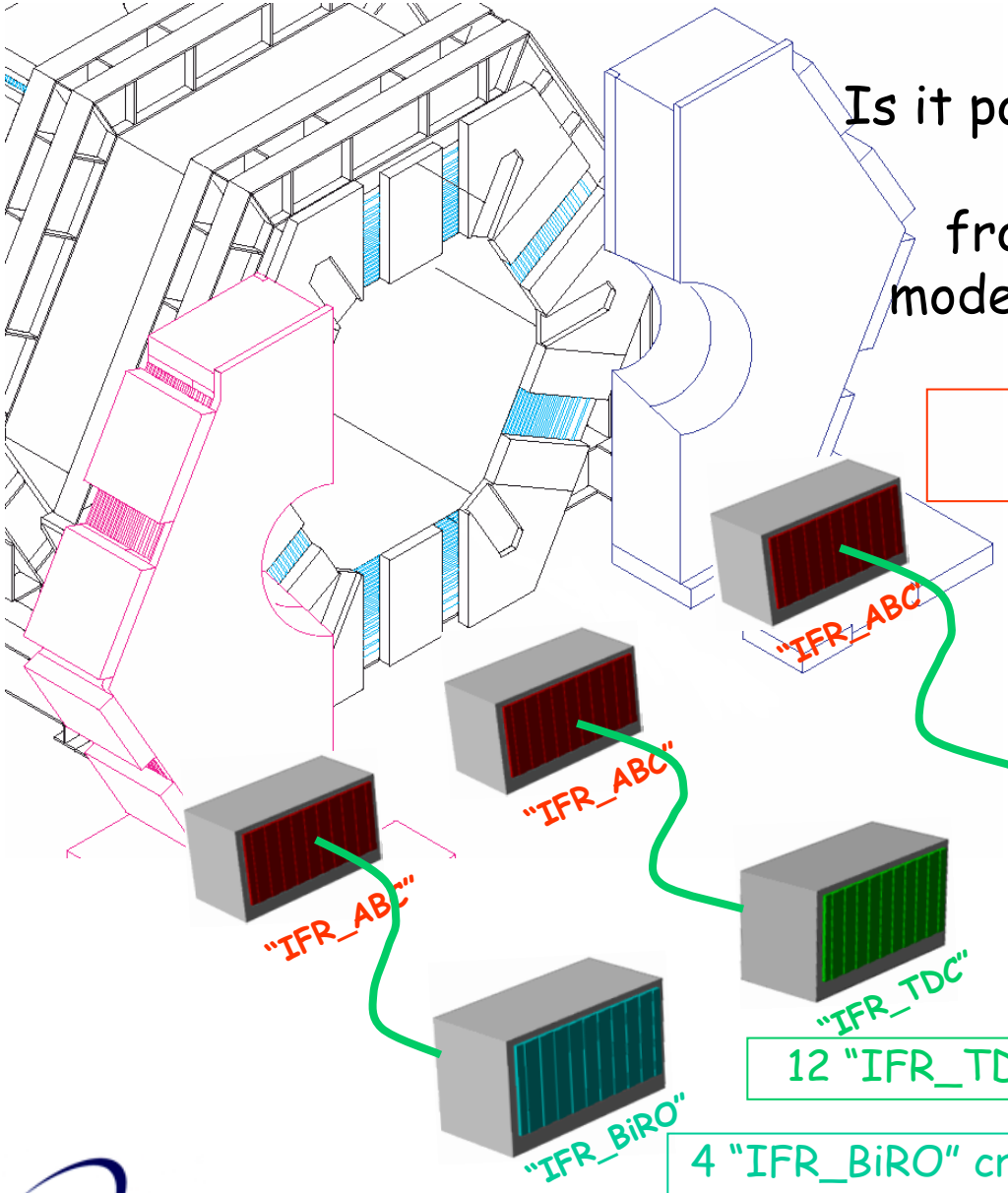
- **IFR_Fe_BIRO, IFR_TLU:**
  - the motherboard consists of a Cyclone III development kit; a simple reference design based has been implemented to test I/O operation of the board through the GbEthernet interface.
  - HSMC adapters have been purchased to breadboard the interface card; schematic design will start after breadbord test.

- **modules for timing mode readout:**
  - the TDC, the crate and a stand-alone software for TDC readout exist; **this software must be adapted to a larger DAQ framework.**

- LST_FE crate:
  - a fully equipped "LST_FE" crate, provided by INFN_Genova, is in Ferrara

- **IFR_DAQ:**
  - Code is being written to simulate the generation of events by the IFR_FE_BiRO and the TDC and test data collection and histogramming

outline of the IFR DAQ electronics: original layout of DAQ electronics



Is it possible to locate the digitizers far enough from the iron yoke to be in a moderately hostile environment ?

12 "IFR_ABC" crates for BARREL
8 "IFR_ABC" crates for ENDCAPS

12 "IFR_TDC" crates for BARREL readout

4 "IFR_BiRO" crates for ENDCAPS readout

What is a moderately hostile environment ?

From:

Compact data acquisition and power supply system designed for hostile environment condition concerning radiation and magnetic field

L. Colombini, M. Lippi, A. Mati, G. Passuello, S. Petrucci*, M. Pieracci, G. Selmi, C. Tintori

CAEN S.p.A., Via Vetraia 11, Viareggio, Italy
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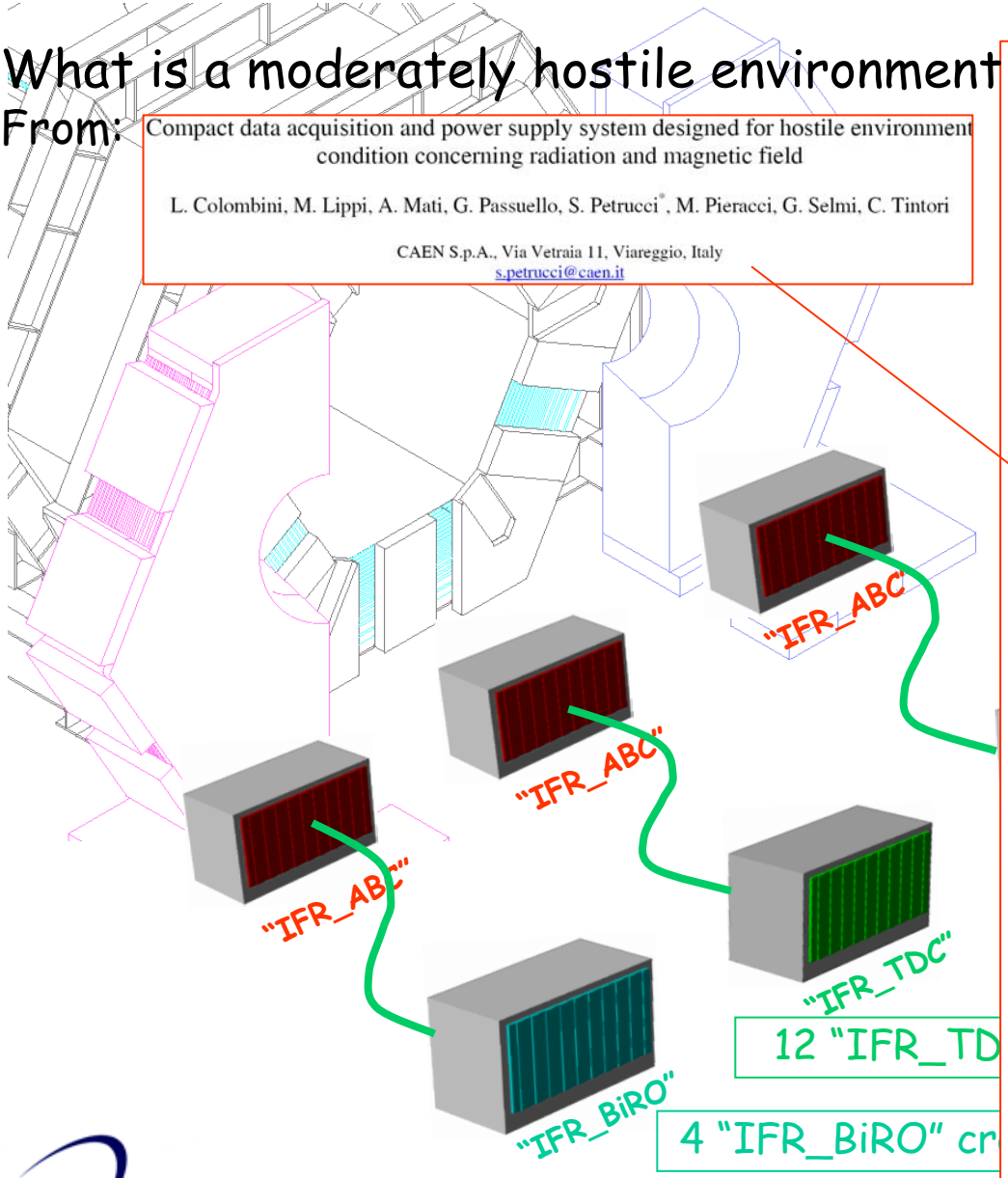


A. *Radiation Tolerance*

The crate will operate in a moderate hostile environment for what concerns total levels of radiation (Table 1) [8]. If damages for total integrated dose are likely to be negligible, protections for latchups are needed, as well as an adequate SEU protection/detection.

Table 1: The expected doses and hadron fluences for 10 years

Total dose	1.2 Gy
Neutron fluence (>20 MeV):	2.1 10^9 cm^{-2}
Max Charged hadron/neutron (>20MeV) fluence rate	89 Hz/cm^2

The SEL protection is achieved by dividing each board in sections with separate power supply. Each section is independently monitored and "protected" by a current-limiting device (MAX893L), while an Atmel µC handles the section ON/OFF status: if SEL faults are signalled by the relevant indicators, the Atmel µC detects them and switches off the sections with SEL faults in order to correct the SEL condition and to avoid permanent damages.

The SEU protection/detection architecture is based on radiation tests carried on the key components of the ALICE TOF readout modules [9]. Such tests reported an esteem of the SEU rates and helped to select the proposed components. The implemented solution was then the following: Flash based FPGA Actel ProAsic Plus (APA 750), which are substantially immune to SEU in the configuration bits, are used for vital sections, while other sections use RAM based ALTERA FPGA (reprogrammed after a CRC error). The SRAM implements a CRC check in order to identify NOT valid data. No SEE effect was observed in the Flash and in the Atmel µC (ATMEGA). The HPTDC look-up tables will be periodically monitored via CRC and require reload from Flash memory.

outline of the IFR DAQ electronics: data bandwidth estimates

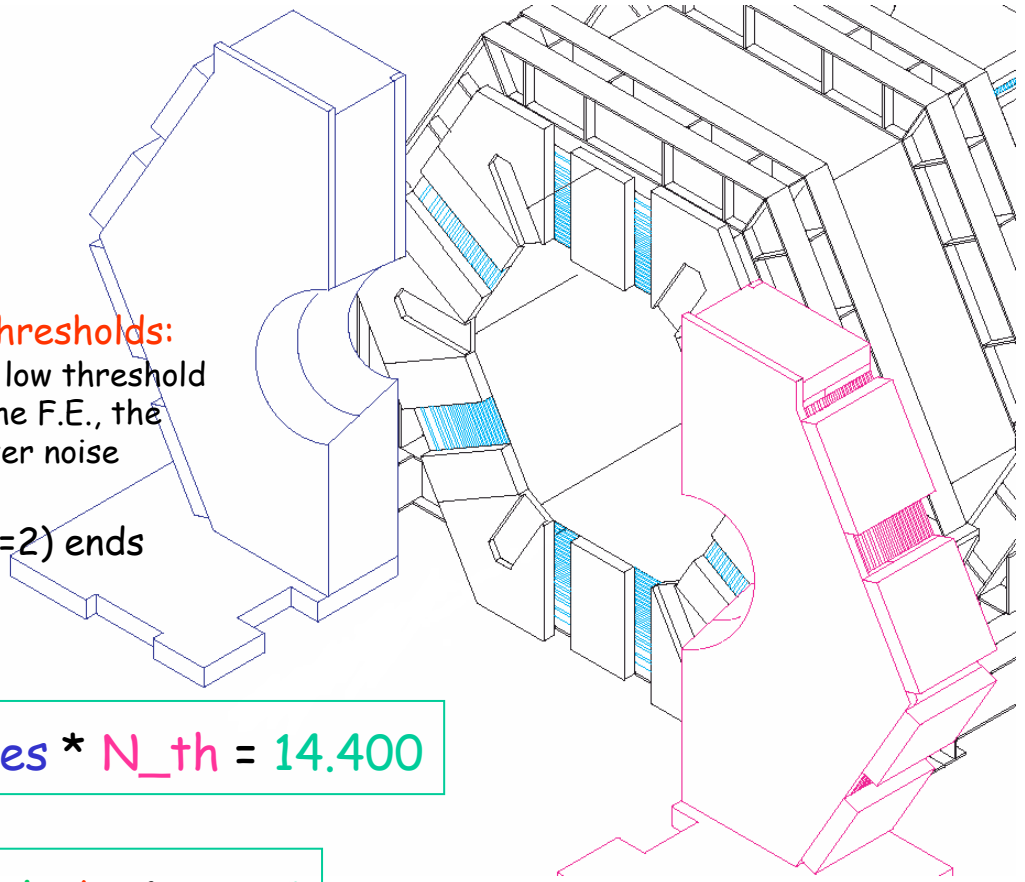
SuperB-IFR numerology:

• Barrel: N_Barrel = 3600 scintillator bars
(quoting G. Cibinetto)

Assuming:

• readout in TIMING mode with N_th (=2) thresholds:
both the high threshold (2.5 p.e. for instance) and the low threshold (1.5 p.e. for instance) crossing times are acquired by the F.E., the second threshold crossing validating the first for better noise rejection.

• each scintillator is readout from N_sides (=2) ends
-> total number of TDC channels: N_TDC_ch



W.Sands., Princeton Univ., 2003

$$N\_TDC\_ch = (N\_Barrel) * N\_sides * N\_th = 14.400$$

$$N\_TDC\_board = N\_TDC\_ch / 64 = 225$$

Hopefully the tests on the prototype will show that it will be possible to keep:
N_th = 1
but in the meantime it is better to brace for the worst!

!!! Multihit TDC ASICs currently available assume a reference clock of 40MHz meanwhile the latest document edited by D.Breton and U. Marconi assumes a 56.25MHz clock: it might be an issue !!!

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, in the hottest region, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK:**

(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold

- @ 25°C, 34.4V: ≈ 360kHz
- @ 5°C, 33.8V: ≈ 128kHz

@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, one comparator with a low threshold (0.5pe? 1.5pe? Only prototype test will tell) → it's TDC input will see the highest rate.

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≤ 1MHz per TDC input !!!

it is compatible with the TDC-GPX maximum sustained input rate

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

if we do L1 trigger matching on board

--- BARREL

- **assuming a 150ns trigger window**
- **assuming that trigger matching is performed at the front end cards**
- assuming a "hit rate per scintillating element" of 1MHz per channel in the barrel (500Khz of "physics" + 500KHz of dark count rate because of the low threshold needed to improve timing precision)
- assuming that an event from an "IFR_TDC" board is built like outlined below:
  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - Channel ID + hit timing information RELATIVE to beginning of frame : 4 Byte per Hit
  - Trailer = L1_Trigger_Data + WordCount + error code: 12 Byte
- assuming that on each TDC half of the channels has a 1MHz input rate and half has a 500KHz input rate →

The TDC event size and data rates can be estimated as follows:

<"IFR_TDC" event size> = 12 + [(0.15us * 1MHz) hit * 32 + (0.15us * 0.5MHz) hit * 32] * 4 + 12 ≈ 12 + 8 * 4 + 12 ≈ **0.06kB**

and thus the "**trigger matched**" data rate produced by each "IFR_TDC" is:

<"IFR_TDC" data rate> = 150KHz * 0.06kB ≈ **9MB/s**

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

if we do L1 trigger matching on board

BARREL summary

- **Number of "IFR_TDC"s = 225**

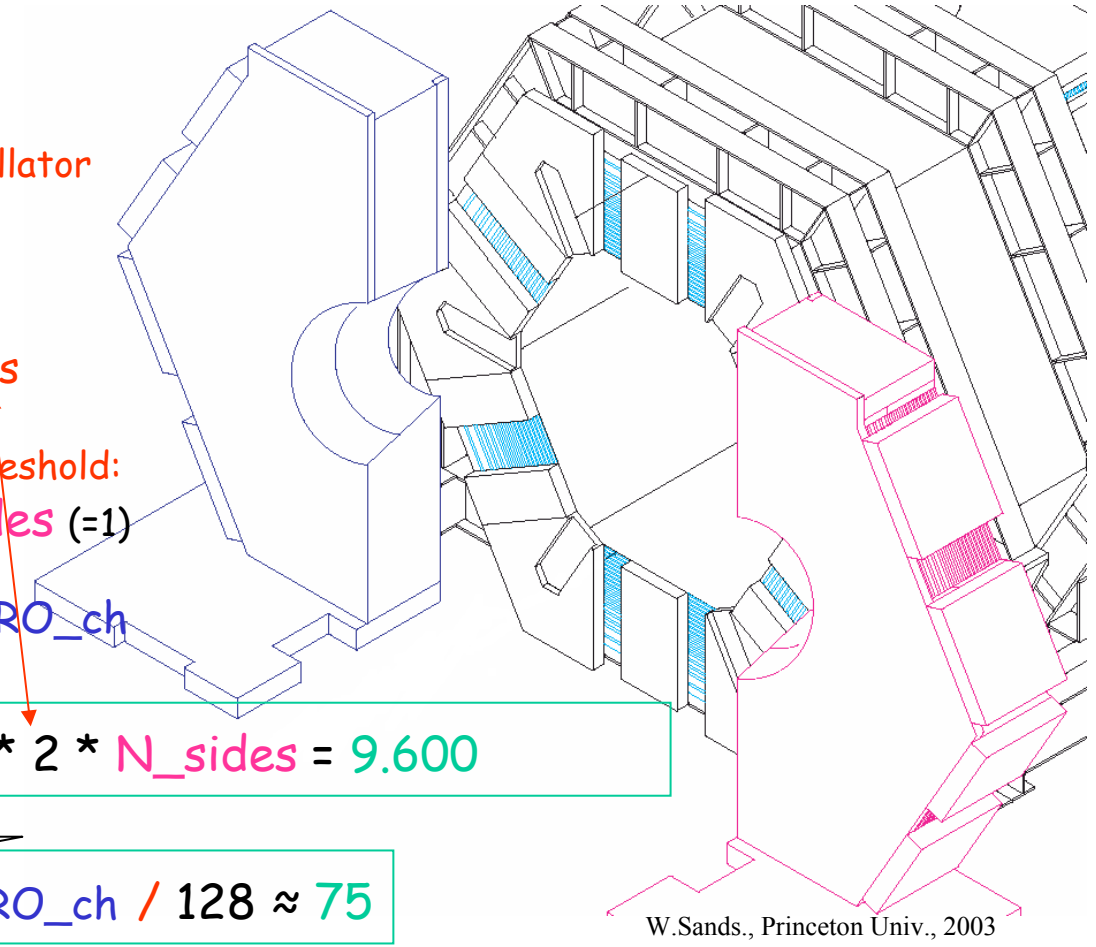
- Numbers per "IFR_TDC" board:
  <"IFR_TDC" event size> = 0.06kB
  <"IFR_TDC" data rate> = 9MB/s
- Average event size for the whole Barrel read in timing mode:
  <Event size Barrel> = 0.06kB * 225 ≈ 13.5kB
- Total data rate produced by the Barrel:
  <Event data rate Barrel> = 9MB/s * 225 ≈ 2,025MB/s
- Tentative calculation of the number of links required (assuming the "concentration" of 10 "IFR_TDC" output links into 1 link at 2Gbps):
  Number_of_data_links_barrel = 225 / 10 ≈ 24
  (i.e. 2 links per digitizer crate)

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

SuperB-IFR numerology:

• EndCaps: N_EndCap = 2400 + 2400 scintillator bars
(quoting G. Cibinetto)

Assuming:
• the number of (thin) scintillators doubles (for X-Y readout; it's a coarse estimate)
• readout in BINARY mode with single threshold:
• each scintillator is readout from N_sides (=1) ends
-> total number of BiRO channels: N_BiRO_ch



W.Sands., Princeton Univ., 2003

$$N\_BiRO\_ch = (N\_EndCap) * 2 * N\_sides = 9.600$$

$$N\_BiRO\_Board = N\_BiRO\_ch / 128 \approx 75$$

For bars read out in "binary" mode N_sides has settled to: 1

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, in the hottest region, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK:**

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@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, just one comparator with a 2.5pe threshold

→ The dark count rate @ 2.5pe threshold is just a fraction of the physics rate

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≈ 600kHz per BiRO input

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

if we do L1 trigger matching on board

- **assuming a 150ns trigger window**
- **assuming that trigger matching is performed at the front end cards**
- assuming a "hit rate per scintillating element" of 600kHz per channel in the endcaps (500Khz of "physics" + 100KHz of dark count rate because in the endcap we can set a higher threshold w.r.t the barrel)
- assuming that an event from an "IFR_BiRO" board is built like outlined below:
  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - 8 samples within the trigger window for all 128 inputs → 8 * (128/8) = 128 Byte
  - Trailer = L1_Trigger_Data + WordCount + error code: 12 Byte

The "IFR_BiRO" event size and data rates can be estimated as follows:

<"IFR_BiRO" event size> = 12 + 128 + 12 ≈ **0.152kB**

and thus the "**trigger matched**" data rate produced by each "IFR_BiRO" is:

<"IFR_BiRO" data rate> = 150KHz * 0.152kB ≈ **22.8MB/s**

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

if we do L1 trigger matching on board

ENDCAP summary

- **Number of "IFR_BiRO"s = 75**

- Numbers per "IFR_BiRO" board:
  <"IFR_BiRO" event size> = 0.152kB
  <"IFR_BiRO" data rate> = 22.8MB/s
- Average event size for the whole Endcap read in binary mode:
  <Event size Endcap> = 0.152kB * 75 ≈ 11.4kB
- Total data rate produced by the Endcap:
  <Event data rate Endcap> = 22.8MB/s * 75 ≈ 1,710MB/s
- Tentative calculation of the number of links required (assuming the "concentration" of 5 "IFR_BiRO" output links into 1 link at 2Gbps):
  Number_of_data_links_endcap = 75 / 5 ≈ 16
  (i.e. 4 links per digitizer crate)