EMC front-end Electronics

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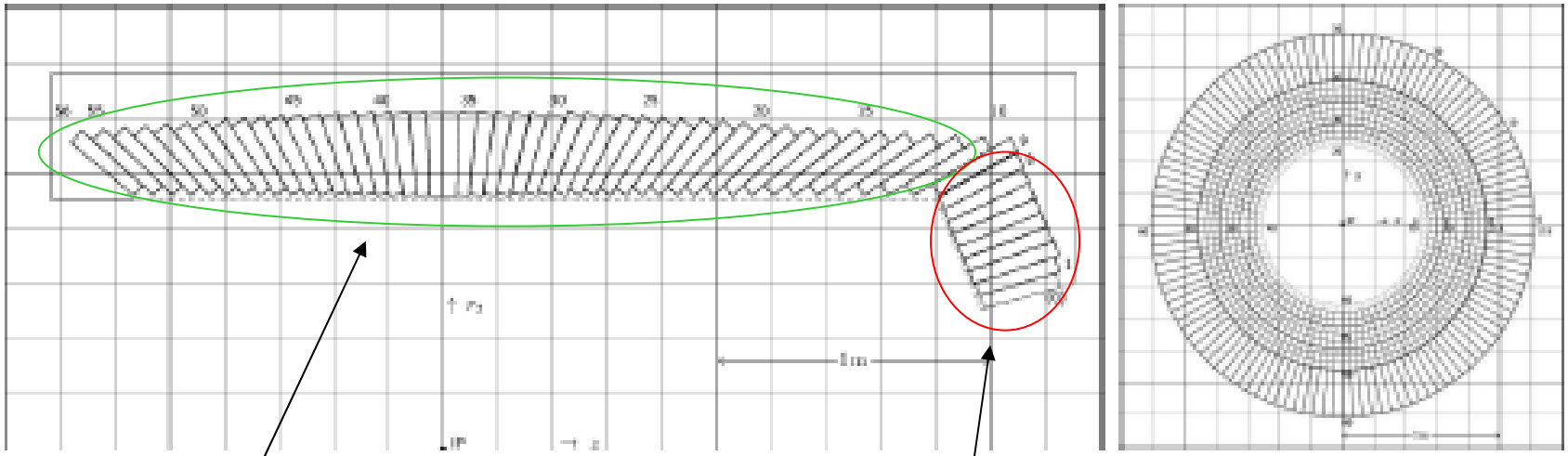
SuperB EMC structure



SuperB EMC Barrel

=

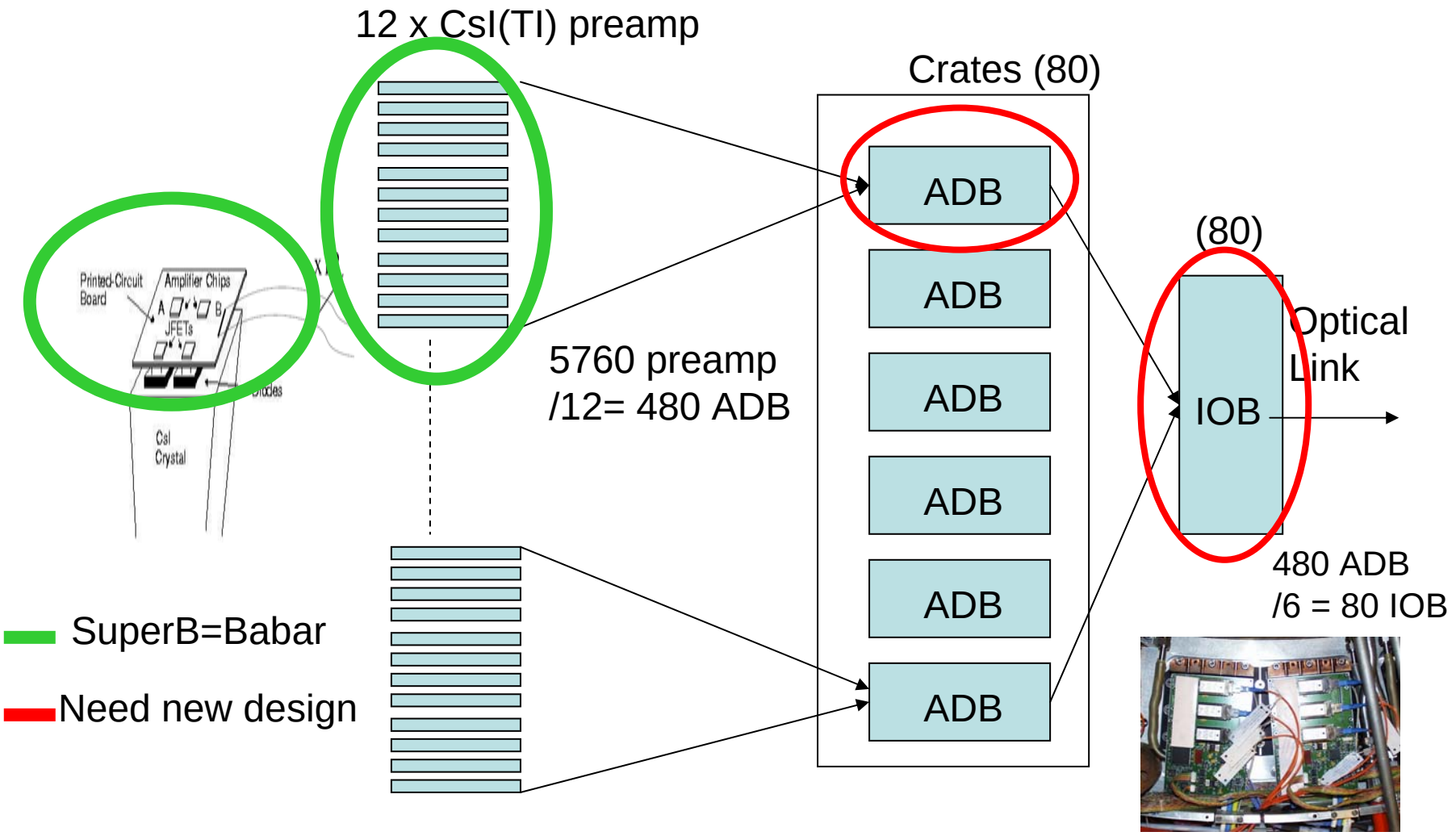
BaBar EMC Barrel

5760 CsI(Tl) Crystals

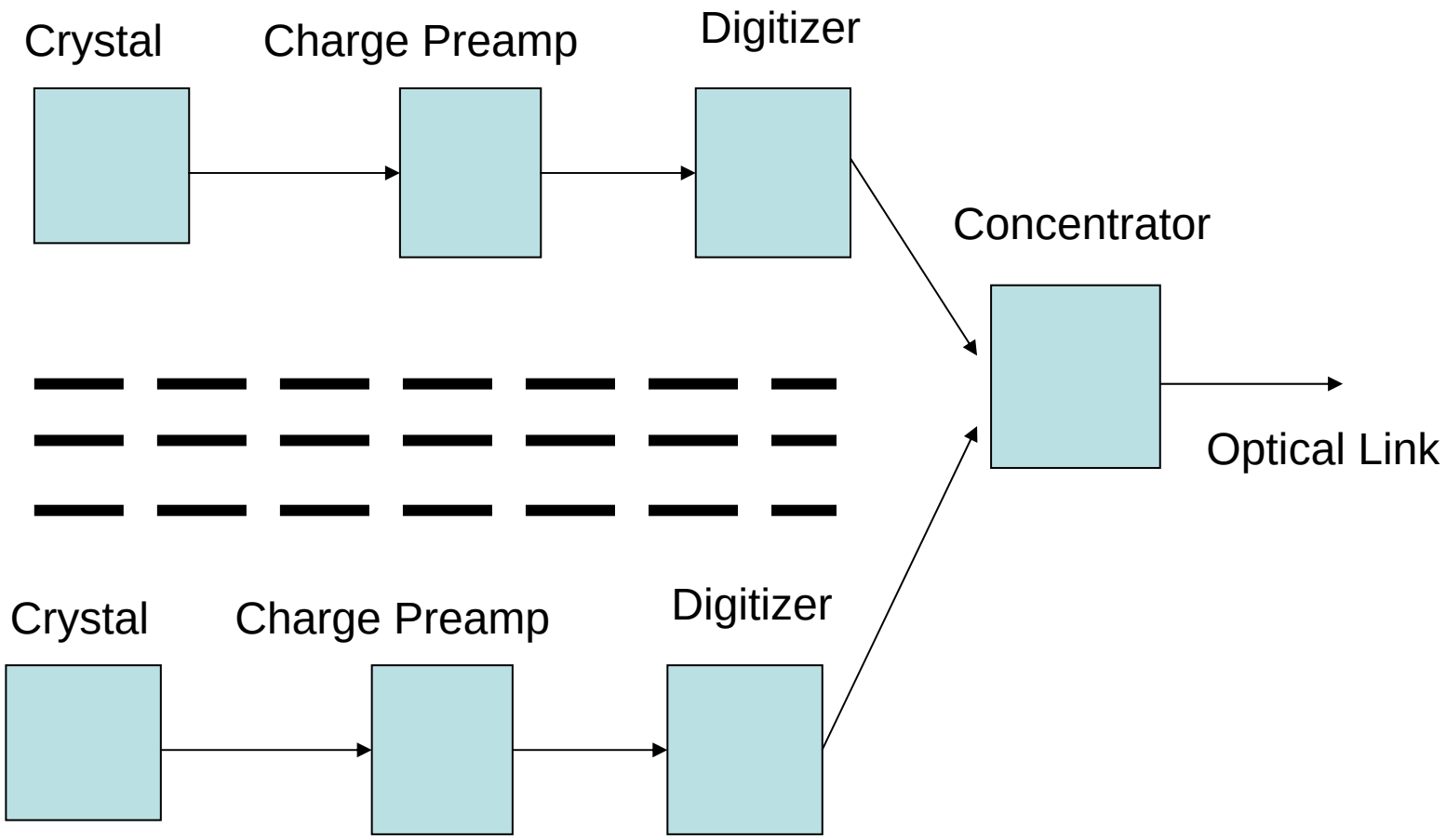
BaBar Crystals
are radiation damaged.
Need replacement

SuperB EMC Forward
= 3600 Lyso Crystals

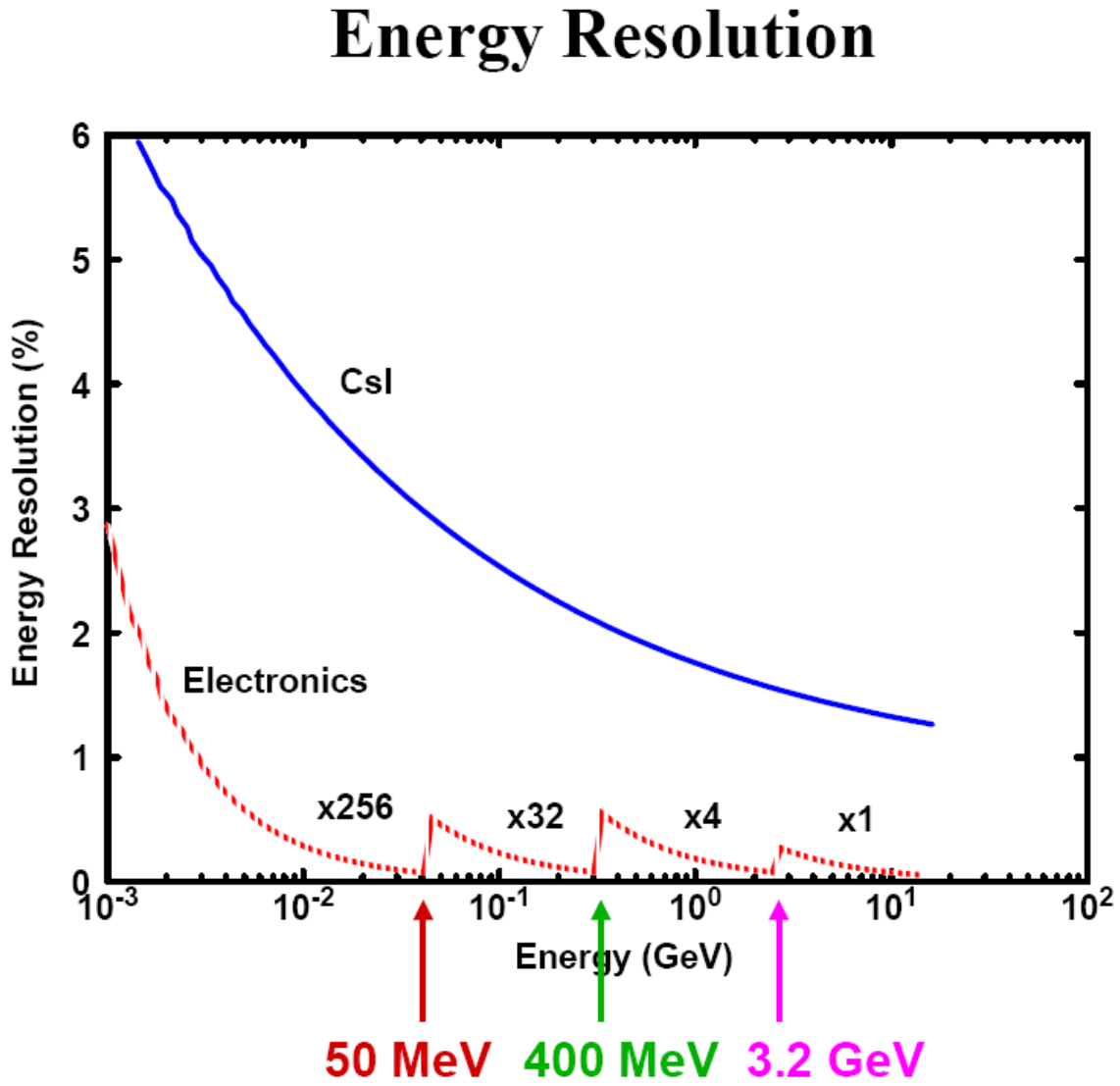
The EMC Front End Electronics



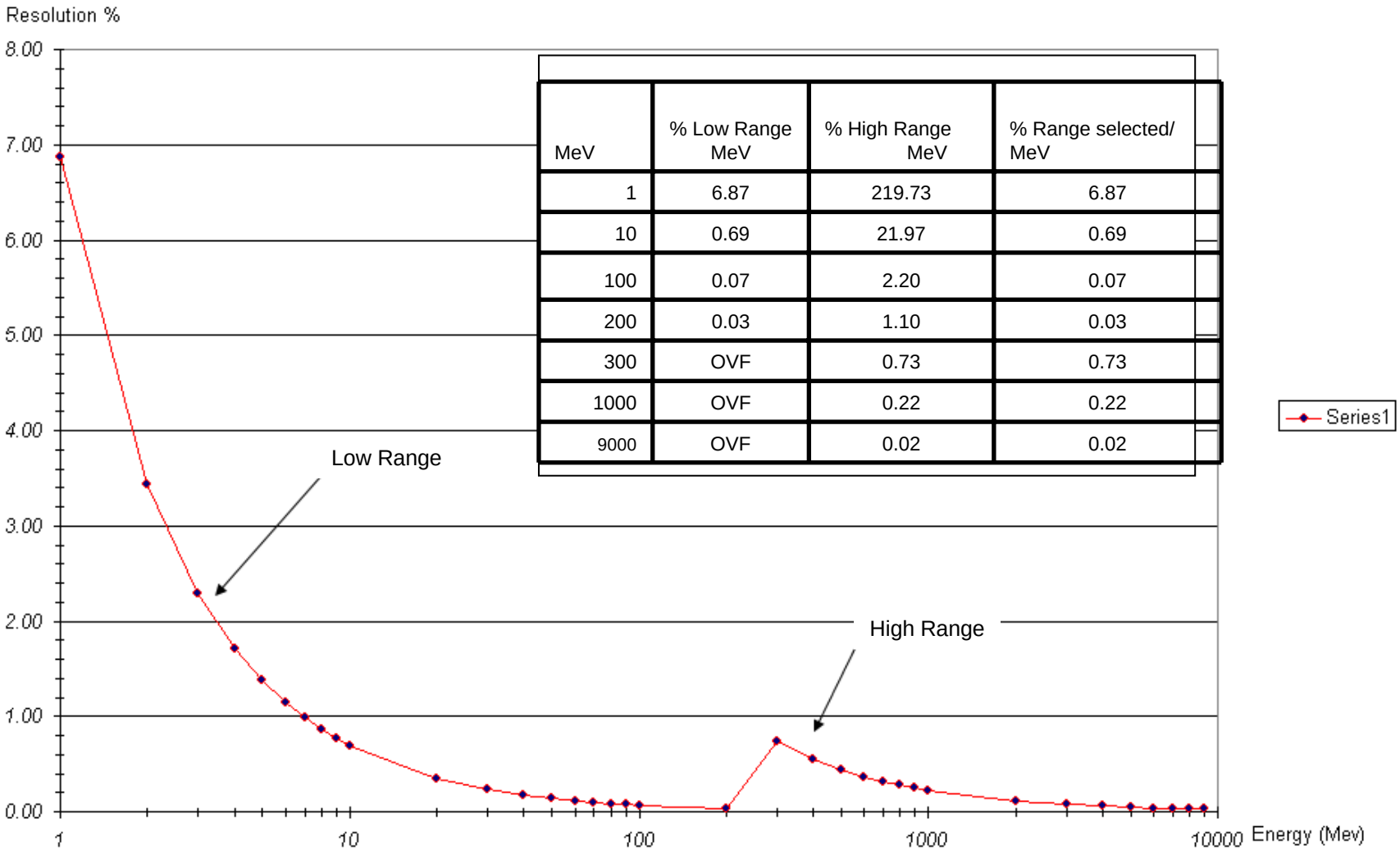
Push architecture



Old ADB Energy resolution

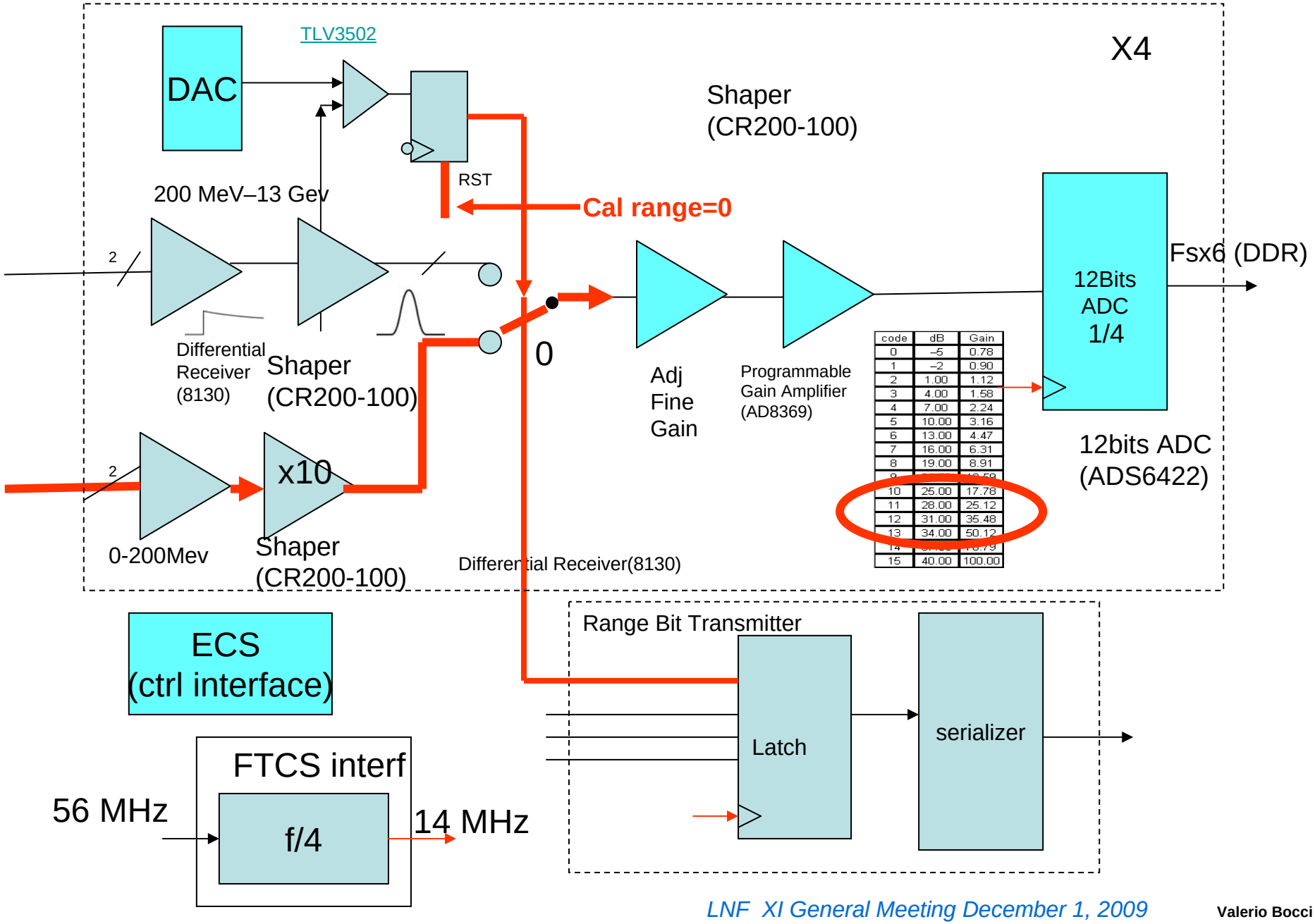


Energy Resolution new ADB

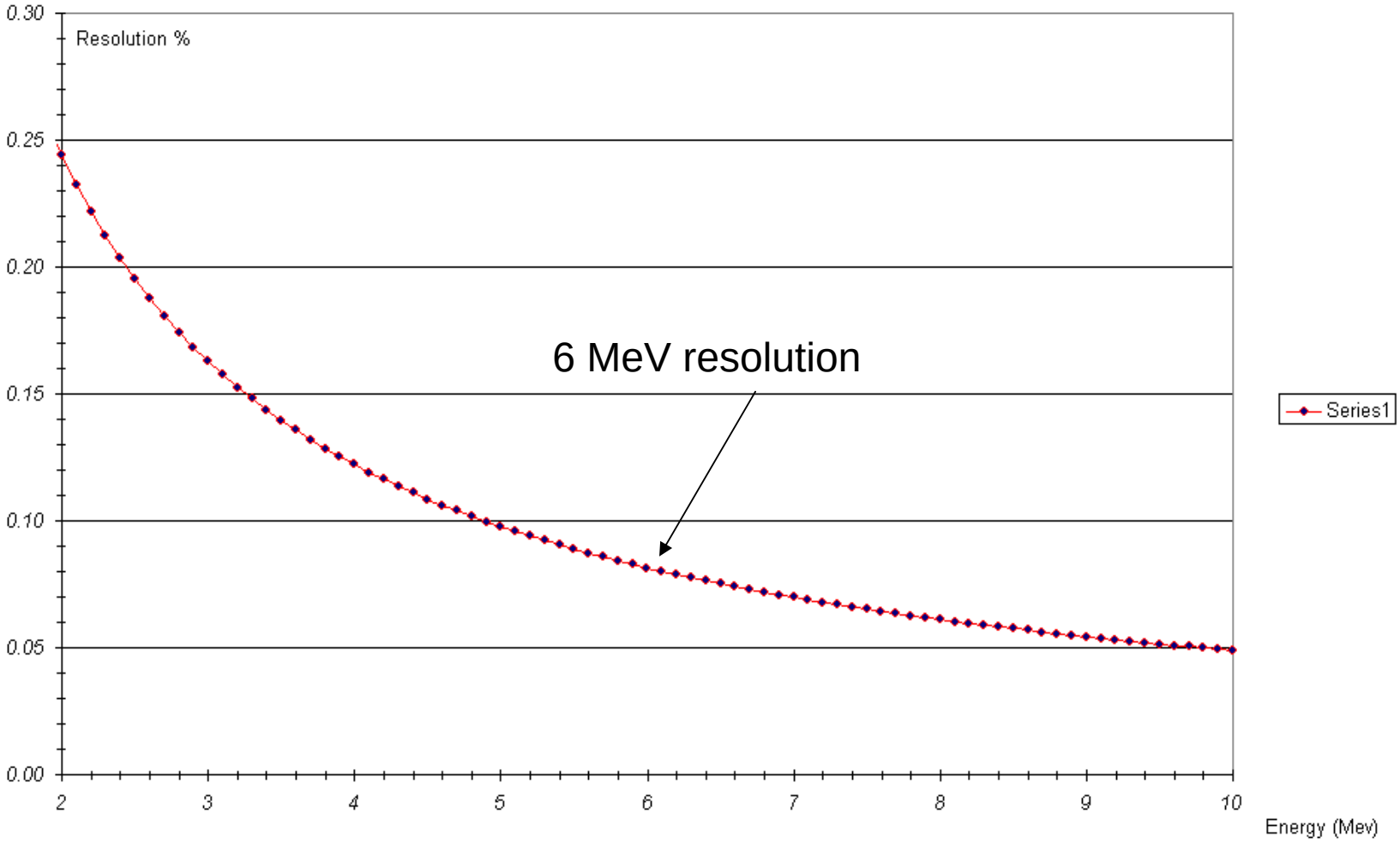


MeV	% Low Range MeV	% High Range MeV	% Range selected/ MeV
1	6.87	219.73	6.87
10	0.69	21.97	0.69
100	0.07	2.20	0.07
200	0.03	1.10	0.03
300	OVF	0.73	0.73
1000	OVF	0.22	0.22
9000	OVF	0.02	0.02

Calibration settings



Resolution in case of Calibration Settings

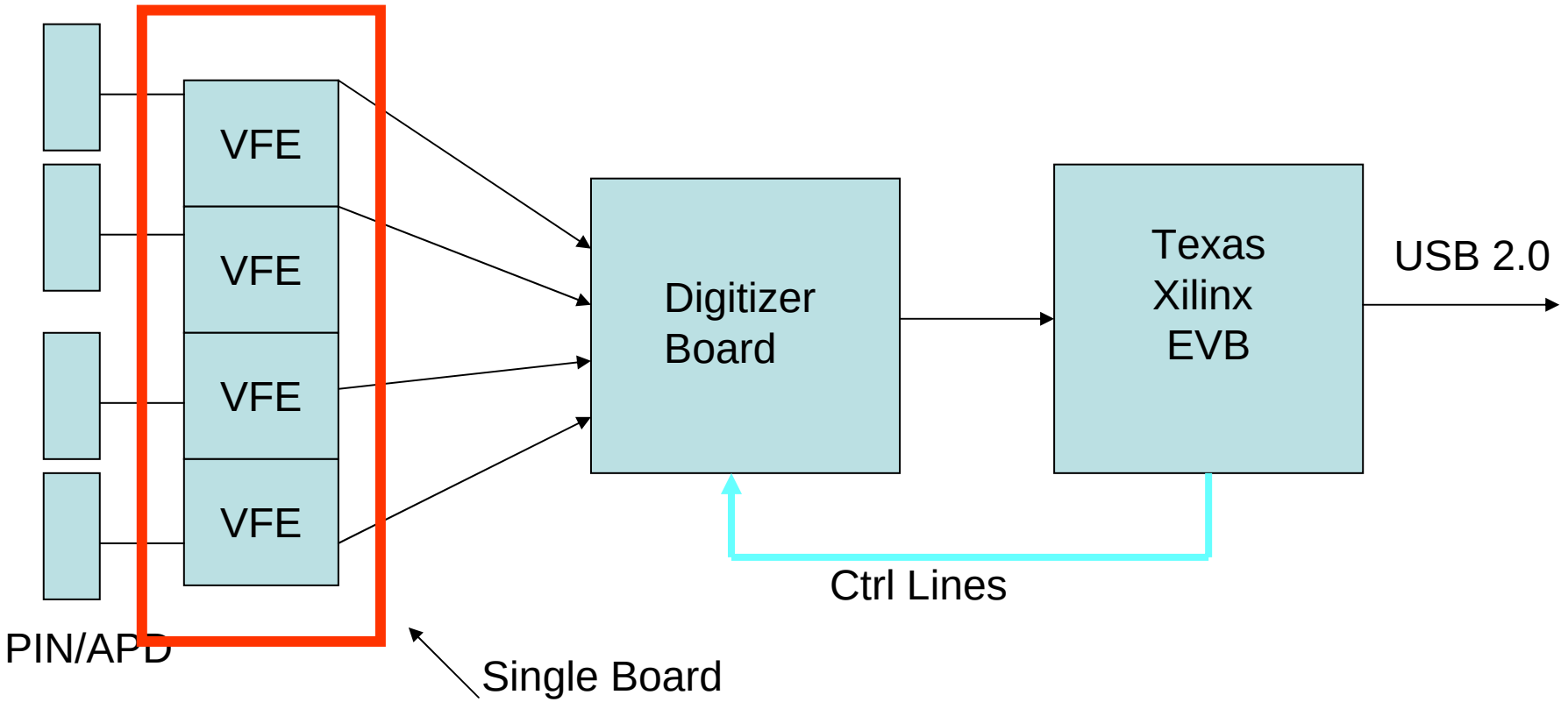


Prototypes boards goal

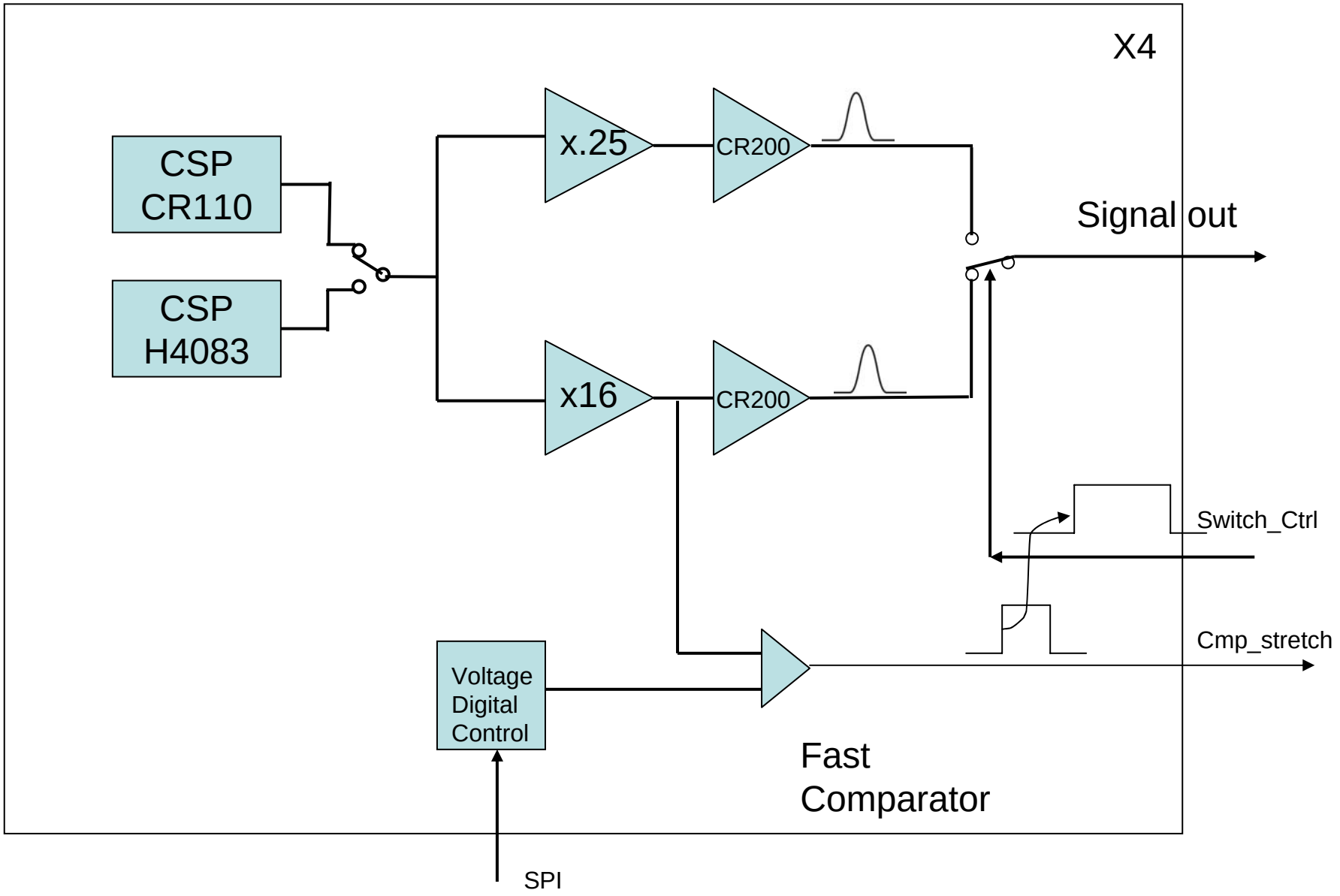
- Test components and architectures
- Create a simple system to play whith different parameters

Prototypes boards

- One single VFE Front End interface four 4 channel
- Digitizer Board
- FPGA data aggregator and PC readout for testing purpose

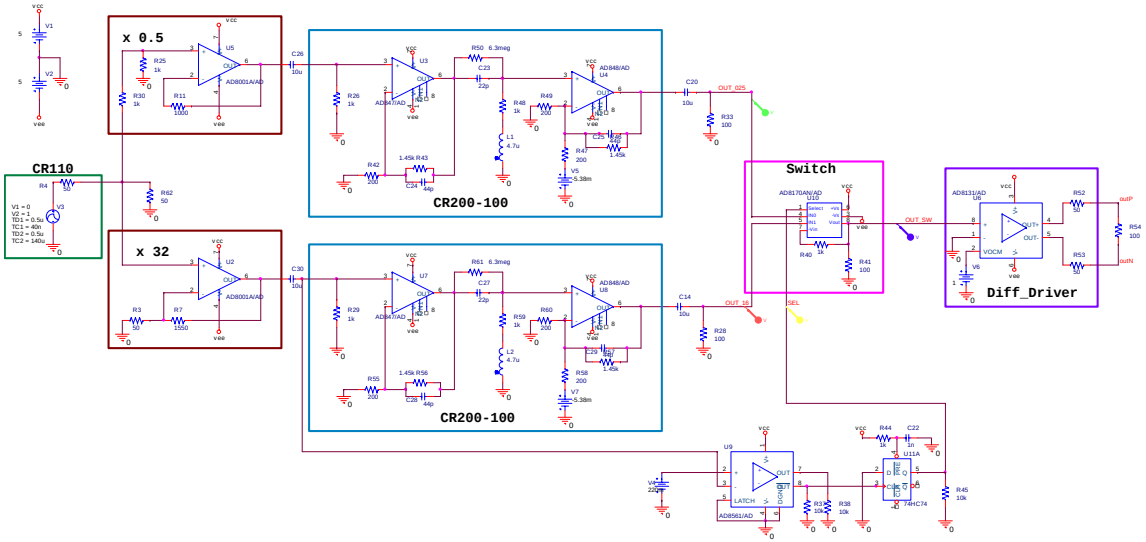


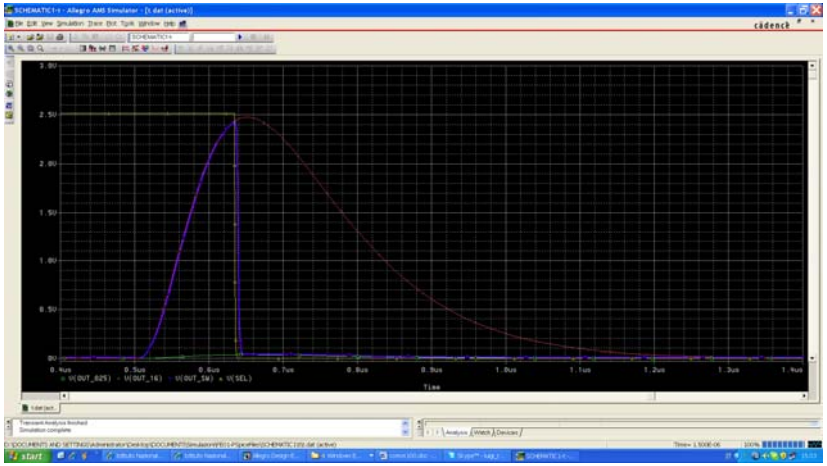
Very Front End Board



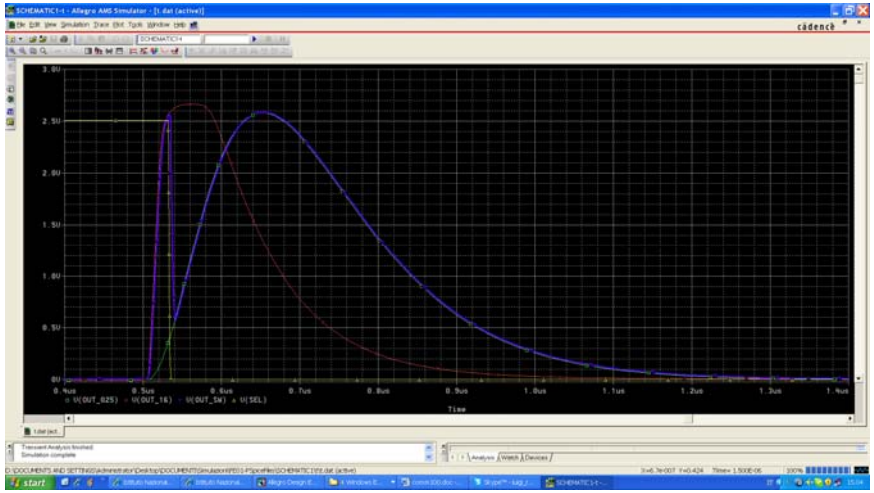
Pspice Simulation

(from Luigi Recchia)





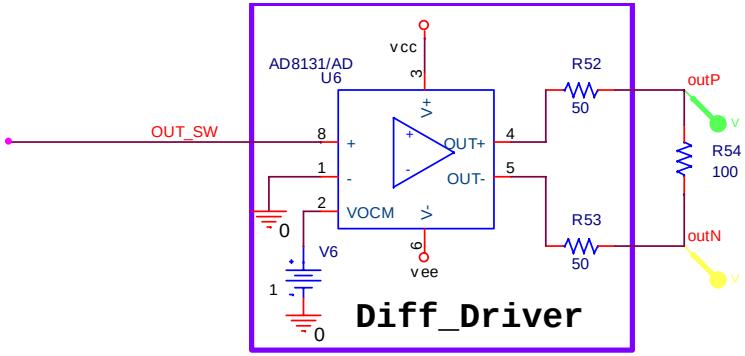
Vin=15mV, Vth=260mV

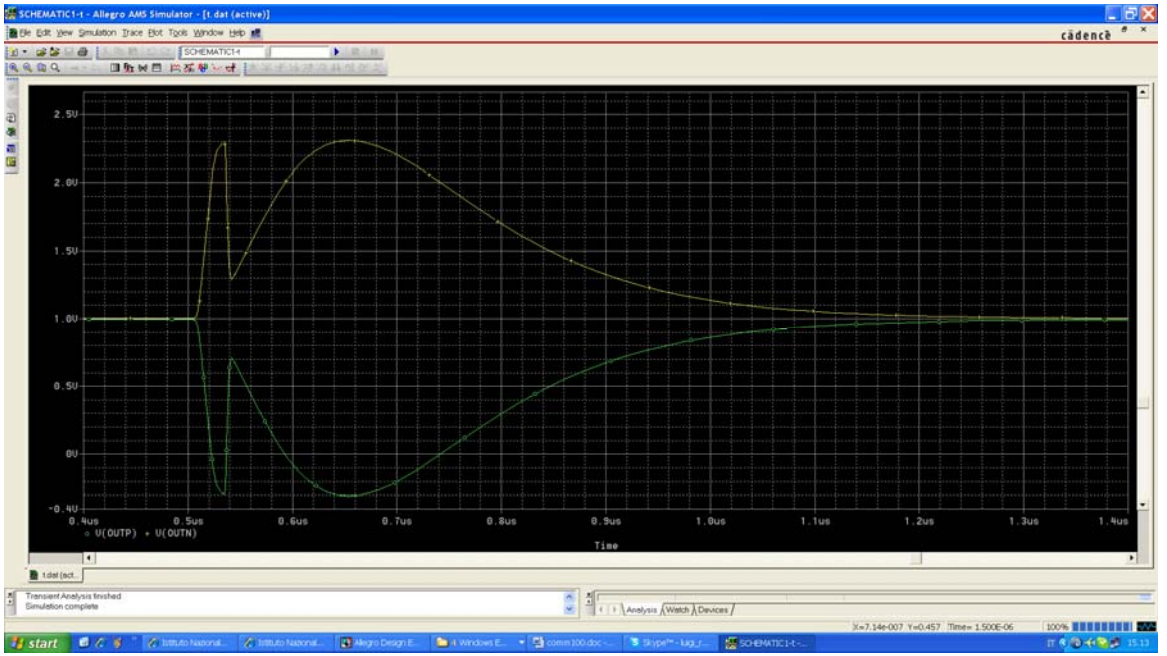


Vin=1V, Vth=260mV

Pspice Simulation

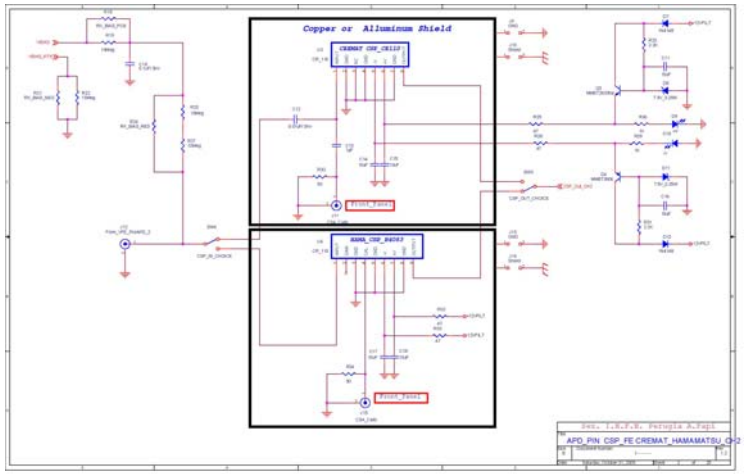
(from Luigi Recchia)

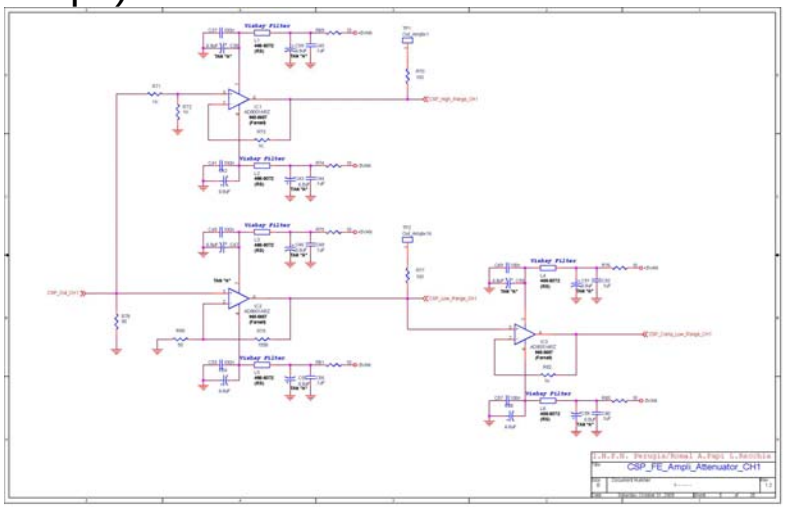


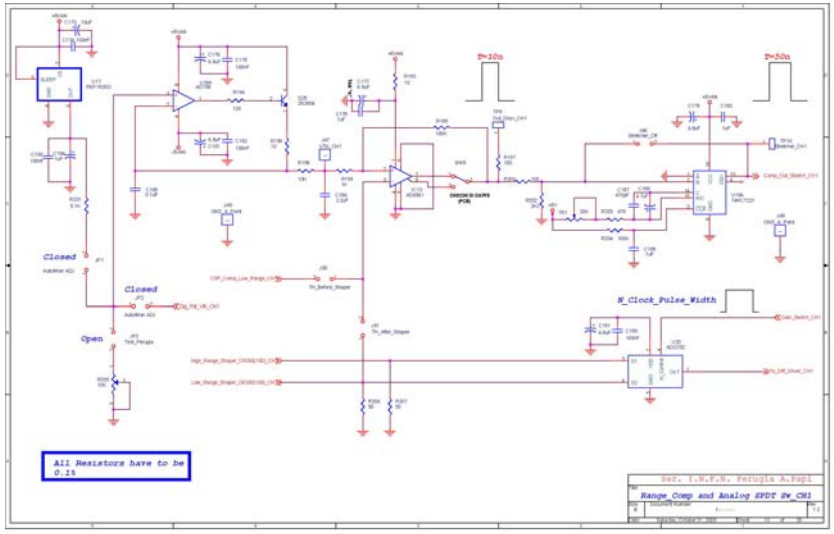


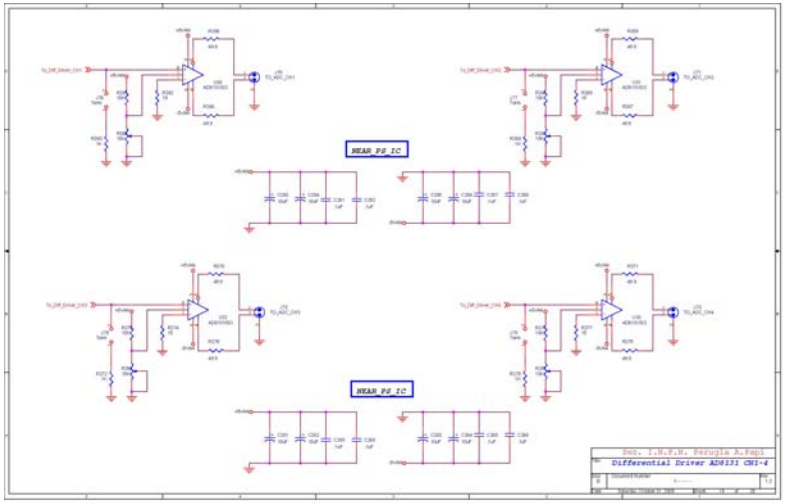
VFE Schematics

(from Andrea Papi)







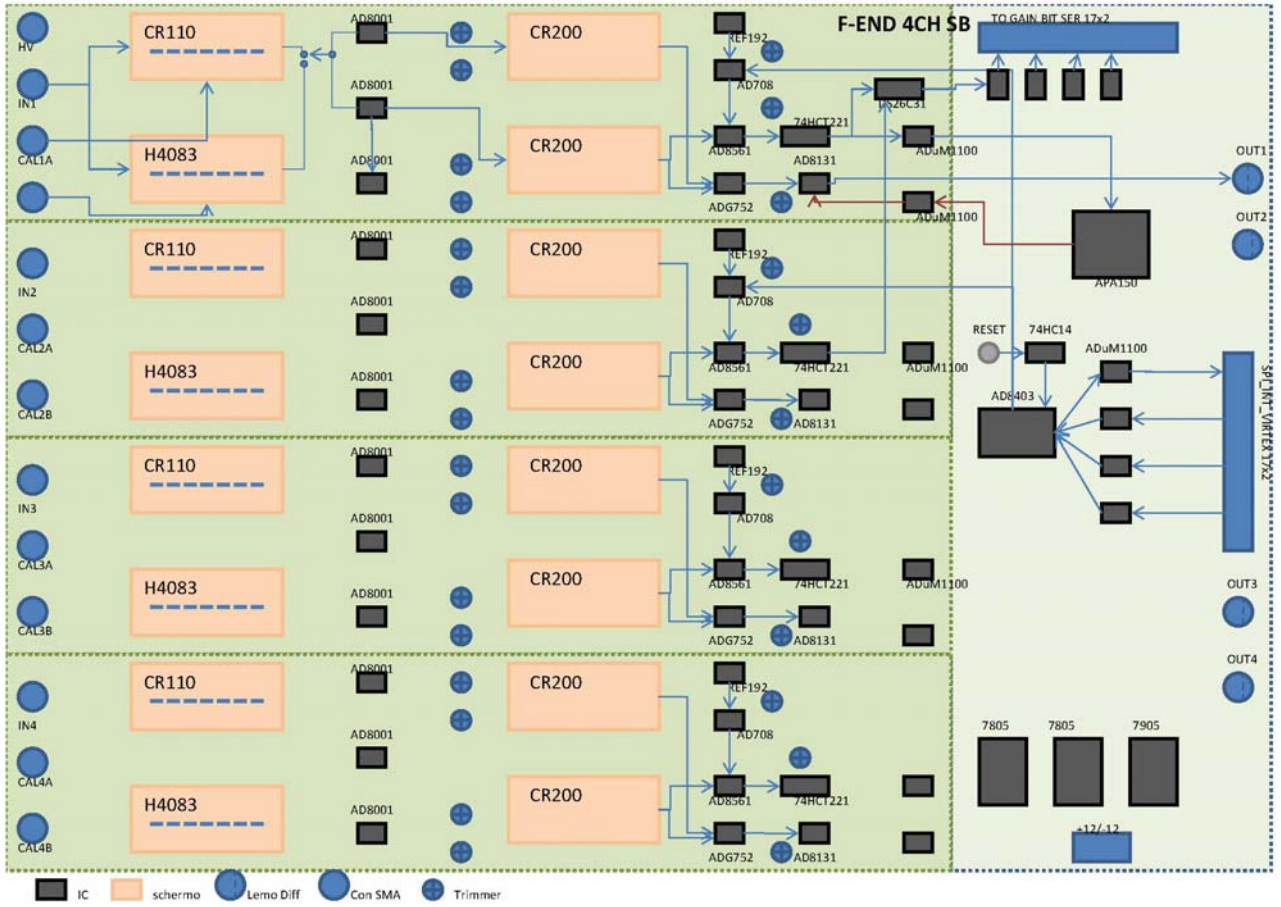


VFE status

- Simulation to prove the principle and different circuits are done.
- The real schematics are ready
- PCB footprint to the Allegro PCB.
- We need to integrate ECAL mechanics informations to finalize board layout.

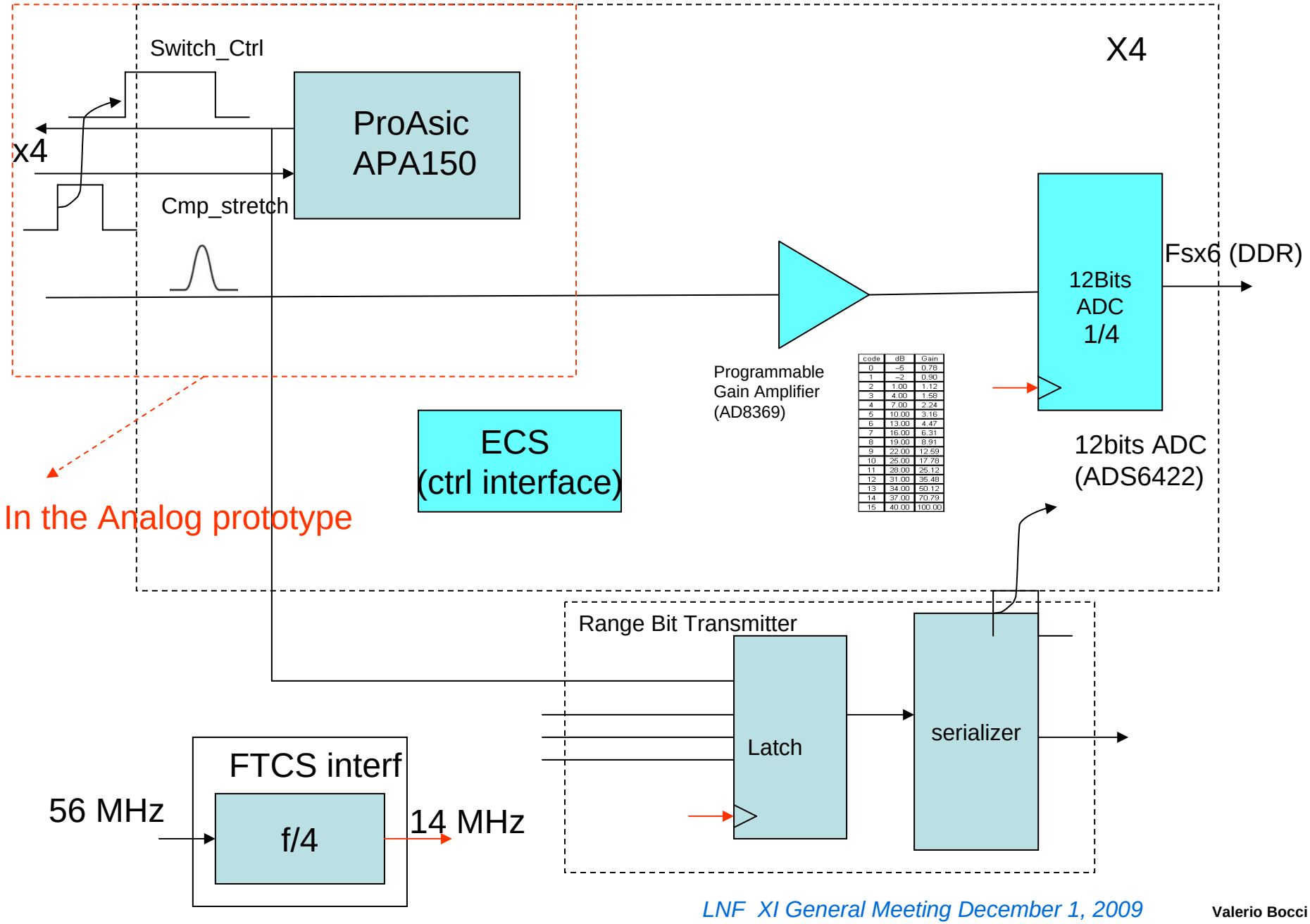
Analog FE Prototype board

(from Luigi Recchia)



180x260mm.

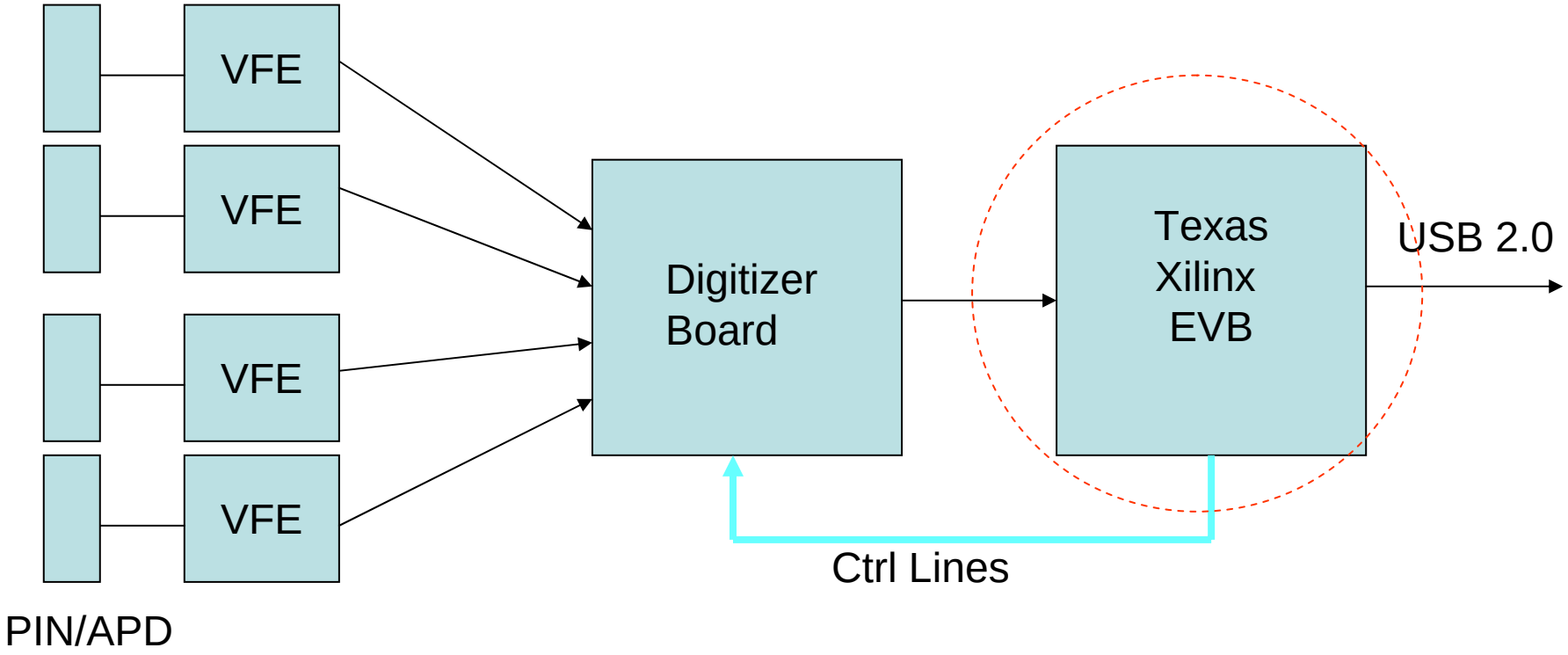
Digitizer Board Prototype



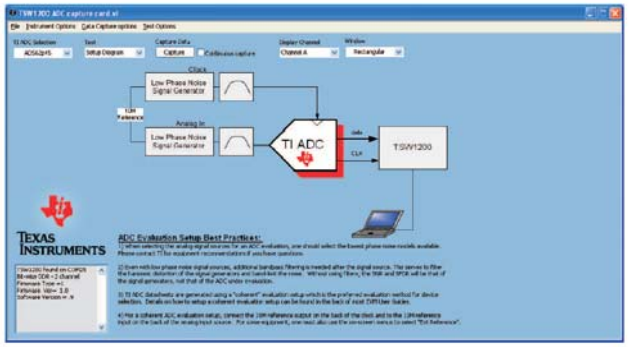
code	dB	Gain
0	-5	0.78
1	-2	0.90
2	1.00	1.12
3	4.00	1.58
4	7.00	2.24
5	10.00	3.16
6	13.00	4.47
7	16.00	6.31
8	19.00	8.91
9	22.00	12.59
10	25.00	17.78
11	28.00	25.12
12	31.00	35.48
13	34.00	50.12
14	37.00	70.79
15	40.00	100.00

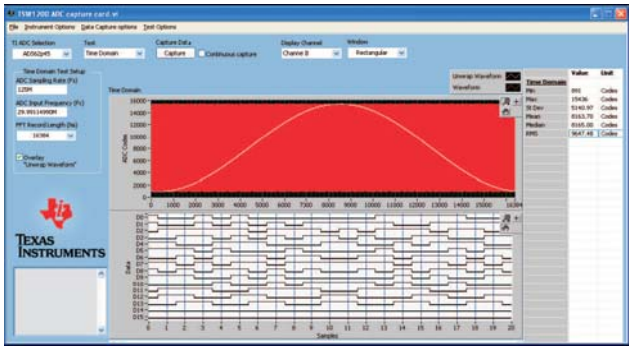
Prototypes boards

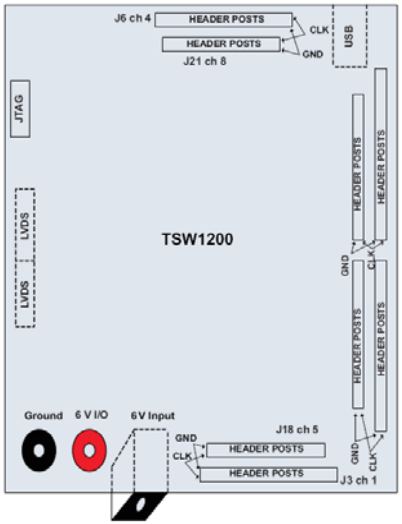
- VFE Front End interface
- Digitizer Board
- FPGA data aggregator and PC readout for testing purpose

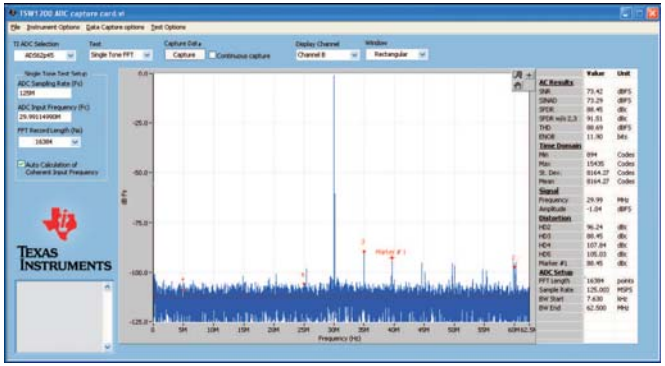


TSW1200EVM: High-Speed LVDS Deserializer and Analysis System

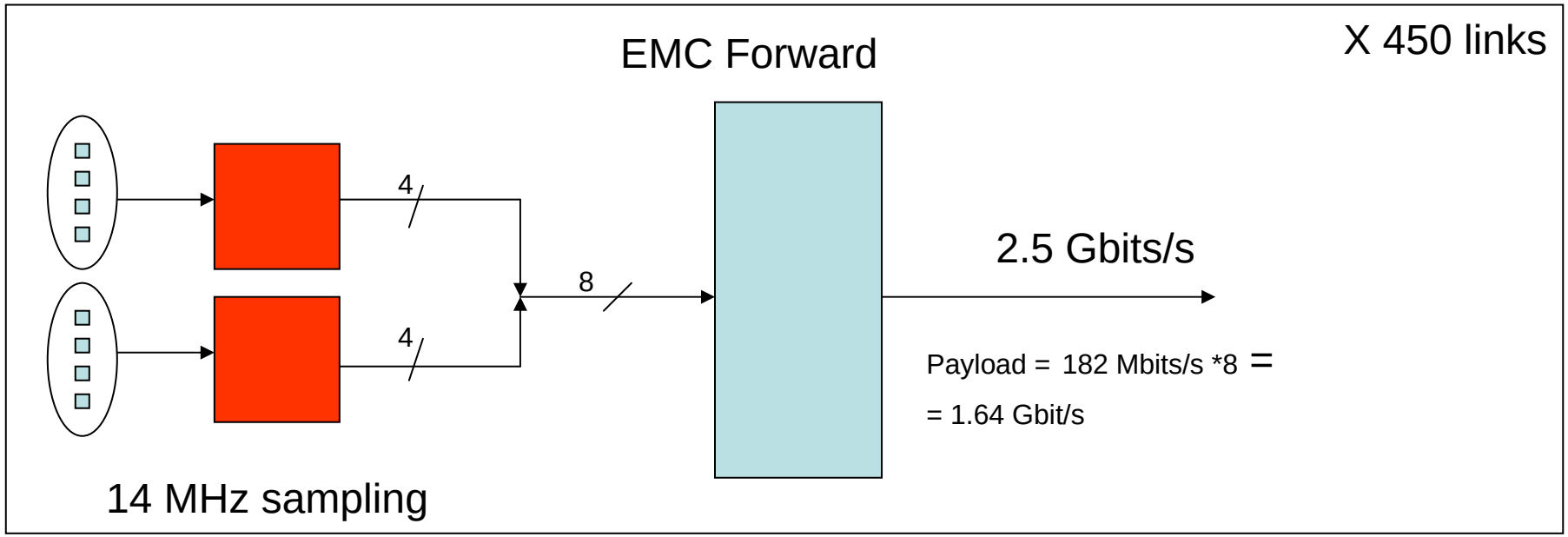








EMC Forward

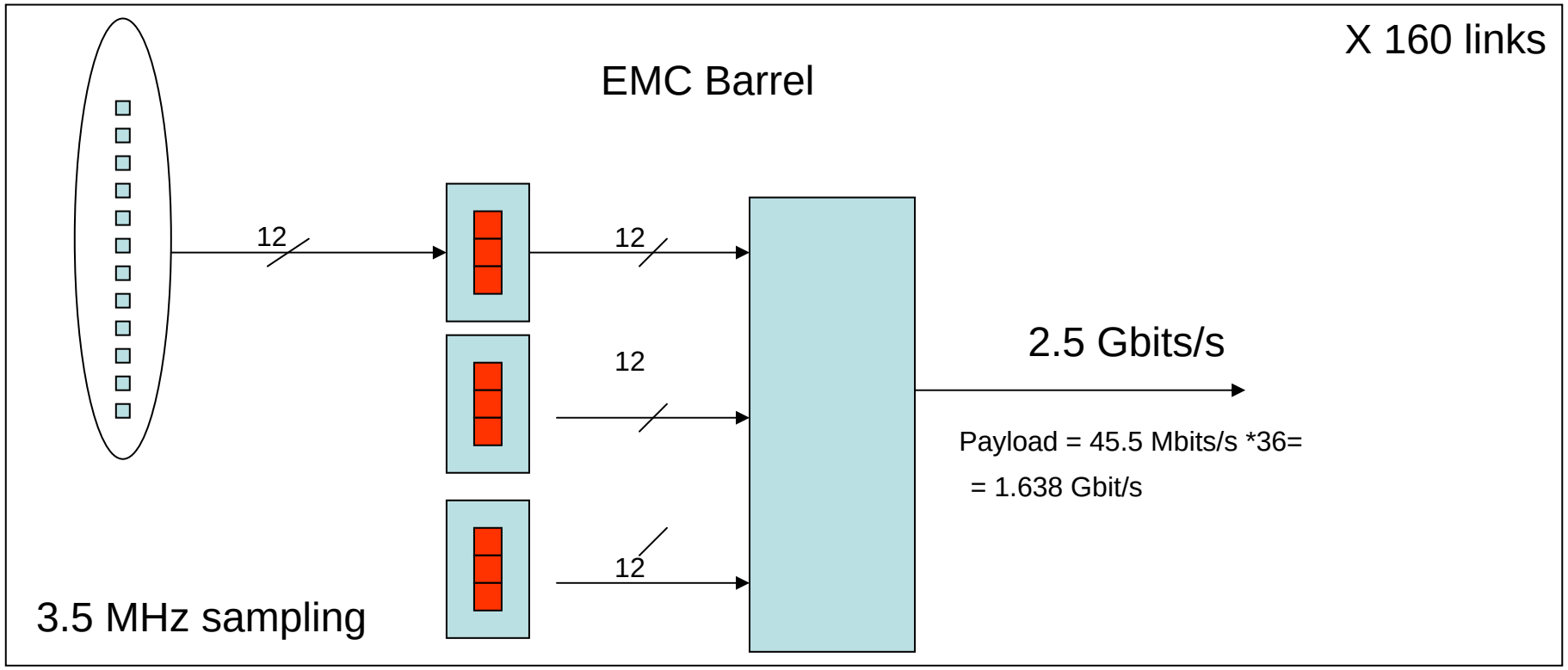

EMC Forward
X 450 links
4
4
8
2.5 Gbits/s
Payload = 182 Mbits/s *8 =
= 1.64 Gbit/s
14 MHz sampling

EMC Forward links

EMC Forward

ch/link	8	
divider	4	
Freq	14	MHz
ADC bits	13	12+1 range
Mbits/s/ch	182	Mbits/s
Gbits/s/link	1.456	
nr links	450	
DATA	900	Gbits/s

EMC Barrel


X 160 links
EMC Barrel
12
12
12
12
2.5 Gbits/s
Payload = 45.5 Mbits/s *36=
= 1.638 Gbit/s
3.5 MHz sampling

EMC Barrel links

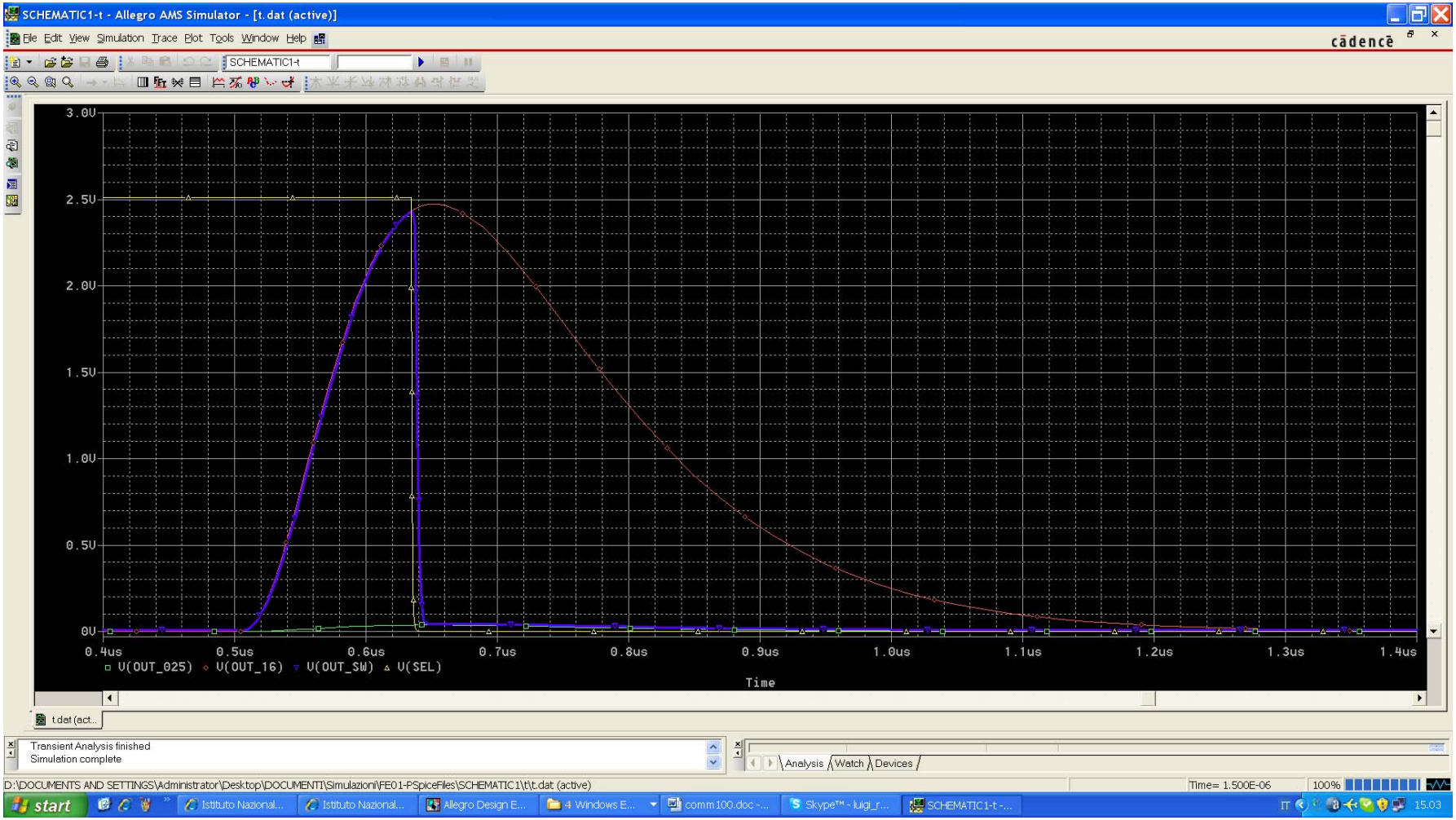
EMC Barrel

ch/link	36	nr
divisore	16	nr
Freq	3.5	MHz
ADC bits	13	12+1 range
Mbits/s/ch	45.5	Mbits/s
Gbits/s/link	1.638	
nr links	160	
DATA	320	Gbits/s

Conclusions

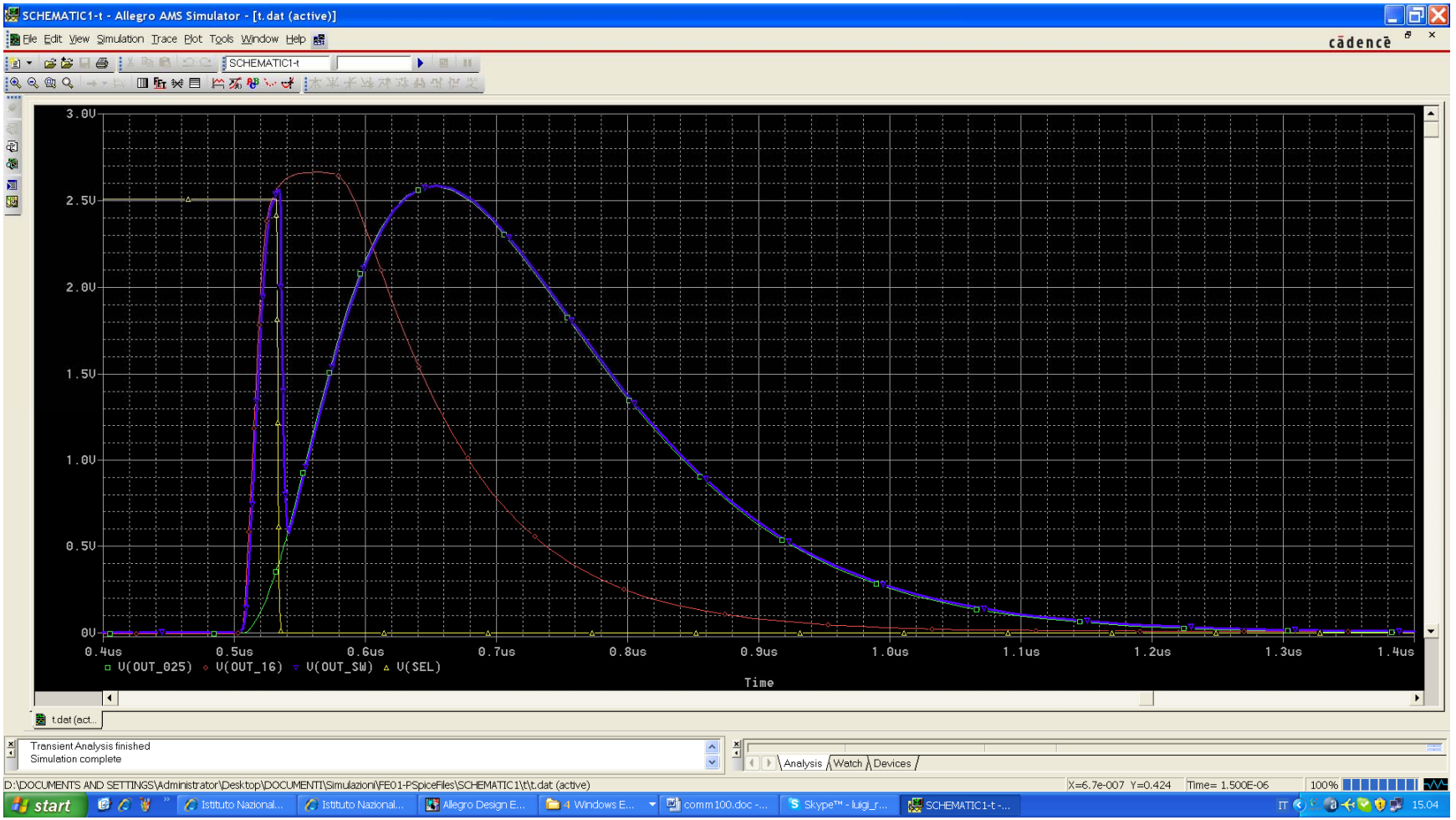
- We try to use in the EMC front end a push architecture.
- All the data are digitized and sended outside the detectors
- We are starting to build Analog prototypes and Digitizer prototipes

Spare 1



Vin=15mV, Vth=260mV

Spare 2



Vin=1V, Vth=260mV