

UK Activities on pixels.

Adrian Bevan¹, Jamie Crooks², Andrew Lintern², Andy Nichols², Marcel Stanitzki², Renato Turchetta², Fergus Wilson².

> ¹Queen Mary, University of London ²STFC, Rutherford Appleton Laboratory







Overview

- TPAC sensor for CALICE
- TPAC sensor for SuperB
 - SuperB INMAPS chip design (derived from the CALICE TPAC chip).
- Support structure
 - Mechanical support, cooling, material budget
- First physics studies
- Summary

Monolithic Active Pixel Sensors (MAPS)

- CMOS
 - down to 180 nm/130 nm feature size
- Charge is collected by diffusion
 - Slow > 100 ns
 - Can be sped up by using other epi material
- Integrated readout
- Thin Epi-layers: 5 µm is standard
- Parasitic charge collection
 - can't use PMOS ...
- Basic MAPS cell → The 3T array



TPAC sensor for CALICE







- Tera Pixel Active Calorimeter (TPAC)
- Extra implant for standard CMOS processing
- Deep P-Well is added beneath pmos transistors in the pixel
- Prevents charge being collected by the electronics
- Allows complex pixel circuits without compromising efficiency



TPAC sensor for CALICE





- Tera Pixel Active Calorimeter.
 - Designed for Calice-UK/SPiDeR (need to re-design for SuperB).
 - 50 µm pixels with analogue pre-amp, comparator, and shaper.
 - Strips of logic and SRAM store location/timestamp of hits in a 1ms bunch with 400 ns resolution (ILC requirements).
 - Binary output









^{55}Fe spectra showing both Ka and K β

X-X correlation plot for two layers (back-to-back)



TPAC-style sensor for SuperB

- Challenge: Layer 0
 - 100 MHz/cm² hit rate.
- Proposed solution.
 - TPAC derived chip
- UK SVT Concept
 - All pixel SVT (a solution for Layer 0 can work for all layers).
 - One sensor for all layers (try to minimize cost and complexity).
 - Material budget... (more later)
 - Analog information (ADC required)



Add a buffer PeakHold /Latch) to the TPAC pixel as a first step of dealing with the rate differences between ILC and SuperB.

The PeakHold keeps data until pixel can be readout/reset. ~12µW static power per pixel.



TPAC sensor for SuperB

- Per pixel ADC
 - Most parallel ADC method
 - Each pixel participates in a ramp-ADC cycle when it has a hit that needs converting
 - Digital ADC result is stored in the pixel until read by a continuously seeking readout chain
- Per column ADC
 - Analog hit magnitude is stored in the pixel until read by a continuously seeking readout chain
 - Several parallel pipelined readout paths are necessary to meet layer0 rates
 - Low-spec pipelined ADC (4Mhz) serves each single column
- Per region ADC
 - As in per-column architecture, but a higher spec ADC serves multiple columns (a "region")
- Per chip ADC
 - A region becomes a full chip
 - Unrealistic for layer0

Advantages	Disadvantages
Advantages • Per-pixel ADC copes best with high hit rate • Digital data from the pixel • Fast transfer • Efficient area storage • Reliable	 Disadvantages Mismatches between pixels may affect quality of ADC result
Advantages •No need to distribute ADC controls, codes, ramp etc over full pixel array •4Mhz pipelined ADC is ok o consider successive approx •Approx 500x fewer ADCs than OPIC style o Lower power o Better matching	 Disadvantages Analog readout is slow, and so must be pipelined to be able to read the rate of hits occurring in layer0 May require column store nodes Added complexity to sparse readout logic Busy pixel No smaller than 50um

Per Column ADC looks like an attractive solution.



Row Addr Hit Data

Token seek	Analog h to colum	nit data tra nn base	ansfers	Token seek					J. Crooks ← Readout channel 1			
	Token seek	Analog ł to colum	nit data tra nn base	ansfers	Token seek				← Readout channel			
	1	Token seek	Analog I to colum	nit data tra nn base	ansfers	Token seek			 ← Readout channel 3 			
			Token seek	Analog ł to colum	nit data tra in base	ansfers	sfers Token seek			← Readout channel 4		
ADC cycle	ADC cycle	ADC cycle	ADC cycle	ADC cycle	ADC cycle	ADC cycle	ADC cycle	ADC cycle	ADC cycle	ADC cycle		
					1	1	1	1				
						2	2	2	2			
							3	3	3	3		
								4	4	4	_	
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- Data rates from Layer 0 are very high
 - Consider an on-chip FIFO with external veto /trigger to reduce data volume
- Data rates from outer layers are much lower
 - Consider a column multiplexer circuit that allows ADCs to be shared while others are powered down in outer layers
 - Could use the same ASIC design with less connections (bonds) for outer layers?







- Alter layout of the chip:
 - 1 module = a 10cm × 2.5 cm × 50µm sensor.



- Radiation hardness should be acceptible~10¹³ n/cm².
 - Planning a test-beam next spring using existing TPACs.
- 10 W power per module.
 - Require active cooling.
 - Ramifications for:
 - Material Budget.
 - Utility hook-up (cooling/power/readout). Frascati Dec 09



SuperB stave

- Stave approach
 - Several modules mounted on super-structure
 - Integrated services
 - Only Connectors at end of stave
- CMS, CDF Run-IIB and ATLAS upgrade are planning to use Staves
- Easy production and assembly
 - Simplified testing
 - Potential to swap a stave







Stave Drawings



Cooling



Some initial studies

- Made first go at Stave structure
- Sandwich
 - Silicon 50 microns
 - Carbon Fiber
 - Silicon Carbide Foam
 - Aluminum Cooling pipes
- Current Material budget
 - 1.1 % per stave
 - Dominated by carbon fiber
- Very conservative design
 - Will be reduced after more FEA studies



Material	Radiation length, D ₀ (mm)	%X ₀
CFRP	240	0.730
Al Alloy	89	0.069
SIC FOAM	1000	0.181
Silicon	94	0.053
Coolant (Water)	360	0114
	TOTAL	1.146%

(Material thickness averaged over section of stave)





Mechanical Layout



The Lamp-Shade geometry can be adapted from this design – need to try barrel vs LS optimization studies to quantify any gains.



Cont'd



Two half-shells to ease mounting on the beam pipe



Front View



The part of the module with electronics on them is at the outermost edge of each layer (indicated by the red dots on L0).



Costs

- Expect a yield of ~60%
 - This is based on previous experience with this foundry.
 - Expect sensor cost of \$0.5M / 330K€.

Total Surface		1	m^2	1
Sensor Size	x	100	mm	100
	x	25	mm	25
sensor/wafer		5		5
Total good sensors needed		400		400
yield		20%		60%
Total number of sensors needed		2,000		667
Total number of wafers		400		134
Cost/wafer		\$ 3,750		3,750
Wafer cost		$1.5M (1M\epsilon)$		$0.5M (0.33M\epsilon)$
Cost/cm^2		\$ 150		\$ 50
NRE (set-up-costs)		\$ 190,000		\$190,000



First physics studies

Use FastSim 1.1 release and PacTwoBodyUser.

Assume several configurations:

- The BABAR geometry with the PEP-II beam conditions.
- The baseline SuperB geometry.
- An all Hybrid Pixel detector (6 layers: 0-5) [Hybrid Pixels].
- A 4-layer Hybrid Pixel detector (4 layers: 0, 1, 4, 5) [Hybrid Pixels-4A].
- The baseline SuperB geometry with an INMAPS Layer 0 assuming a suport structure material budget that matches the Hybrid Pixel baseline [INMAPSL0HYS].
- The baseline SuperB geometry with an INMAPS Layer 0 [INMAPSL0].
- An all Pixel detector INMAPS (6 layers: 0-5) [INMAPS].
- An all Pixel detector INMAPS (4 layers: 0, 1, 4, 5) [INMAPS-4A].
- An all Pixel detector INMAPS (4 layers: 1.6cm, 5cm, 10.2cm, 14.2cm radii) [INMAPS-4B].
- An all Pixel detector INMAPS (6 layers: 0-5) with a low mass L0 support[†] [INMAPS-light].





- Use FastSim V0.1.1, PacTwoBodyUser, and AFit.
 - Simple event selection (Based on BaBar analysis):

$m_{\mathrm{ES}} > 5.26~\mathrm{GeV}/c^2$	Signal Efficiency (no PID):					
$ \Delta E < 0.1 { m GeV}$		•			、 、	

- $|\Delta t| < 20.0$ ps
- $\sigma(\Delta t) < 2.5 \text{ ps}$
- $\cos(\theta_{sphericity}) < 0.8$
- $R_2 < 0.7$
- $Prob(\chi^2) > 0.001$

 1. SuperB (Baseline)
 65.3%

 2. Hybrid Pixels (6-layer)
 62.9%

 3. INMAPS (6-layer)
 62.5%

 4. 4-layer INMAPS-A
 63.7%

 5. 4-layer INMAPS-B
 63.9%

c.f. BaBar efficiency = 53.6% (20% lower) N.B. BaBar's ϵ_{PID} =73.3%.

Signal reconstructed for all samples using TreeFitter with a Geo constraint.



Resolution function is non-trivial for TDCP measurements:

$$\mathcal{P}(x; p_i) = f_{core} G_{core}(x, \sigma(x), \mu_{core}, \sigma_{core}) + f_{tail} G_{tail}(x, \sigma(x), \mu_{tail}, \sigma_{tail}) \\ + (1 - f_{core} - f_{tail}) G_{outlier}(x, \mu_{outlier}, \sigma_{outlier})$$

 Use RMS, FWHM, core Gaussian width as quantifiers of the spread of the resolution distribution for these studies.



SuperB Baseline

RMS	= 1.232 ± 0.007 (ps)
FWHM	= 1.44 (ps)
σ_{core}	= 0.692 ± 0.008 (ps)



First physics studies

 Comparison of baseline performance with other geometry options:





∆t Resolution

Configuration	RMS (ps)	FWHM (ps)	$\sigma_{ m core}$	$f_{ m core}$
BABAR	1.087 ± 0.010	1.33	0.561 ± 0.015	0.721 ± 0.030
SuperB (nominal)	1.232 ± 0.007	1.44	0.692 ± 0.008	0.801 ± 0.008
SuperB (Hybrid Pixels)	1.259 ± 0.001	1.54	0.635 ± 0.024	0.634 ± 0.043
Super B (Hybrid Pixels-4A)	1.249 ± 0.011	1.49	0.537 ± 0.022	0.550 ± 0.037
SuperB (INMAPSL0-HYS)	1.216 ± 0.011	1.39	0.570 ± 0.022	0.620 ± 0.040
SuperB (INMAPSL0)	1.163 ± 0.010	1.40	0.551 ± 0.002	0.627 ± 0.039
SuperB (INMAPS)	1.227 ± 0.011	1.42	0.519 ± 0.036	0.627 ± 0.066
SuperB (INMAPS-4A)	1.212 ± 0.011	1.32	0.505 ± 0.050	0.636 ± 0.090
SuperB (INMAPS-4B)	1.209 ± 0.011	1.29	0.501 ± 0.024	0.626 ± 0.042
SuperB (INMAPS-LIGHT)	1.089 ± 0.010	1.14	0.427 ± 0.027	0.598 ± 0.056

- INMAPS L0 solution gives similar (slightly better) performance to baseline.
- Need to all pixel detector gives comparable performance. What we gain from think Si we loose with support material.
- 4-layer detector again shows interesting result.
- The Pisa Low Mass Support for L0 in a 6-layer pixel detector is as good as BaBar wrt. Δt.
- Promising initial results deserves more study.



- Plan to investigate:
 - 1: sensor operational parameters: (learn what to expect when sensor performance degrades)
 - Effect of sensor efficiency on performance (TPAC has ε>99%, MC has 95%.
 - Effect of hit resolution.
 - Position of L0.
 - 2: Mode dependence: At QM we have people studying: $B^0 \rightarrow \pi^+\pi^ B^0 \rightarrow \pi^0\pi^0$

 Will try and converge on a geometry to include in the next simulation production cycle.



Summary

- TPAC: Evolution of a mature chip design for SuperB.
 - p-well INMAPS design looks very promising.
 - 50µm thick sensors.
 - Analogue information from pixel (column ADC).
 - 10W per 2.5×10cm module (active cooling required).
- All pixel detector concept looks like an interesting alternative design for SuperB.
 - Optimization process of material budget vs. sensitivities has started with $B^0 \to \pi^+\pi^-$
- INMAPS could also be used for Layer0 in the baseline.



Backup

• How much better is the INMAPS-4A resolution c.f. baseline?





Backup

