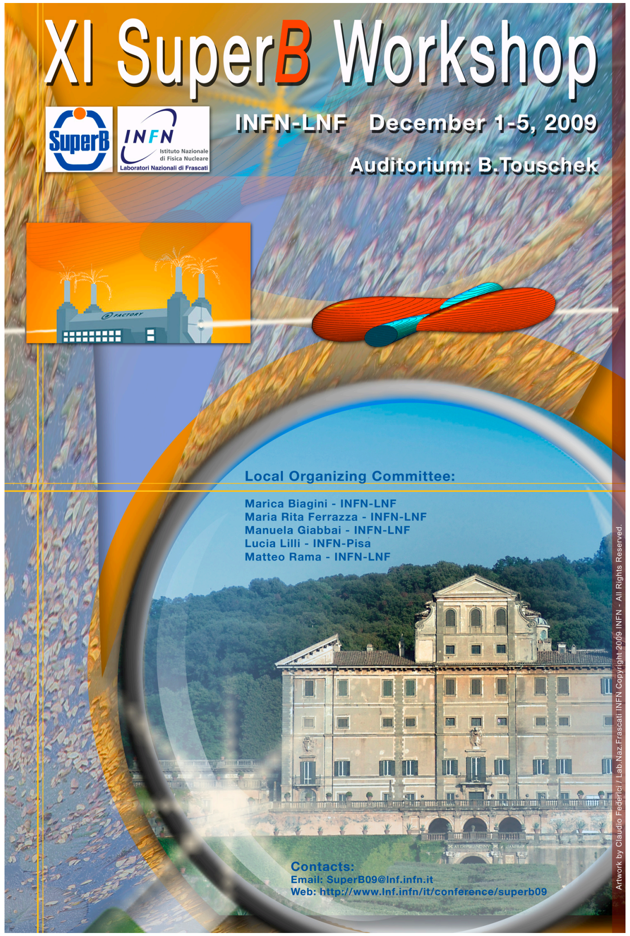
Update on Apsel5T measurements



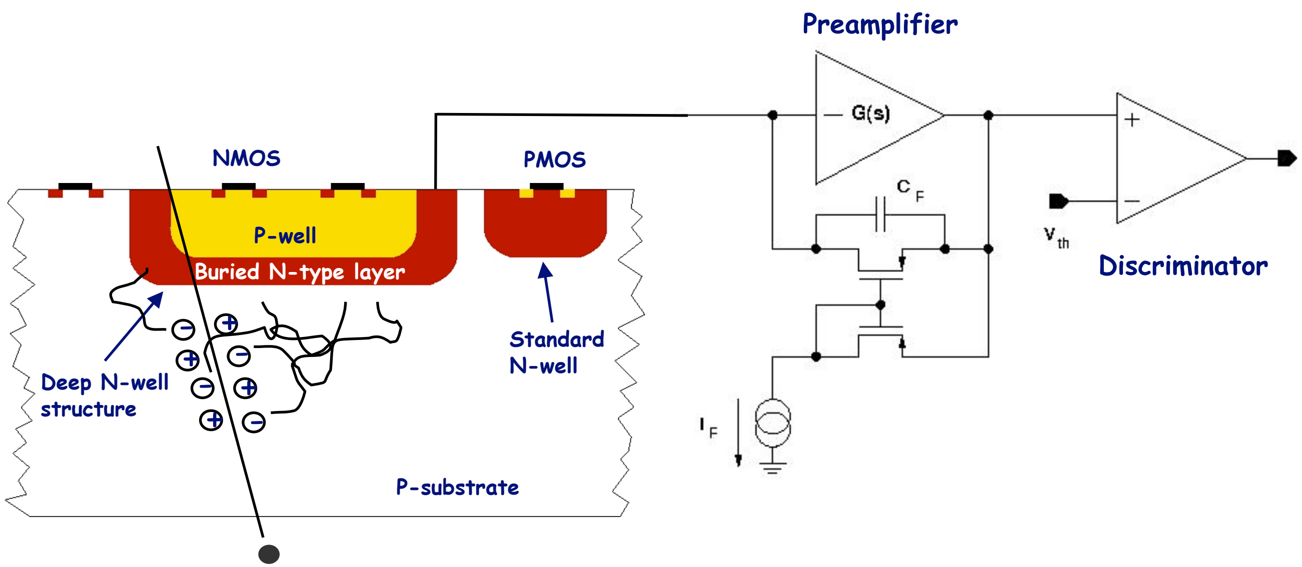
G. Traversi[a], L. Gaioni[b], A. Manazza[b], M. Manghisoni[a], L. Ratti[b], V. Re[a]

[a]Università degli Studi di Bergamo and INFN Pavia

[b]Università degli Studi di Pavia and INFN Pavia

Apsel5T: motivations

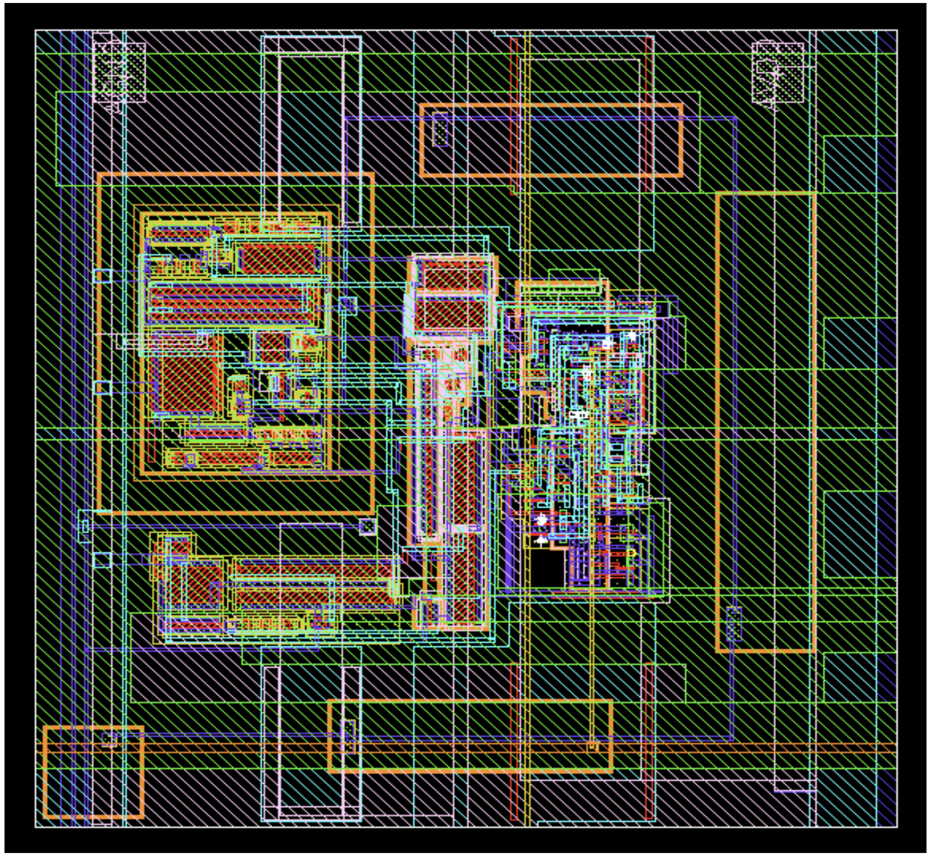
- Classical optimum signal processing chain for capacitive detector can be implemented at pixel level
- A charge preamplifier is used for Q-V conversion → gain decoupled from electrode capacitance
- DNW may house NMOS transistors and using a large detector area, PMOS devices may be included in the front-end design → charge collection efficiency depends on the ratio between the DNW area and the area of all the N-wells (deep and standard)



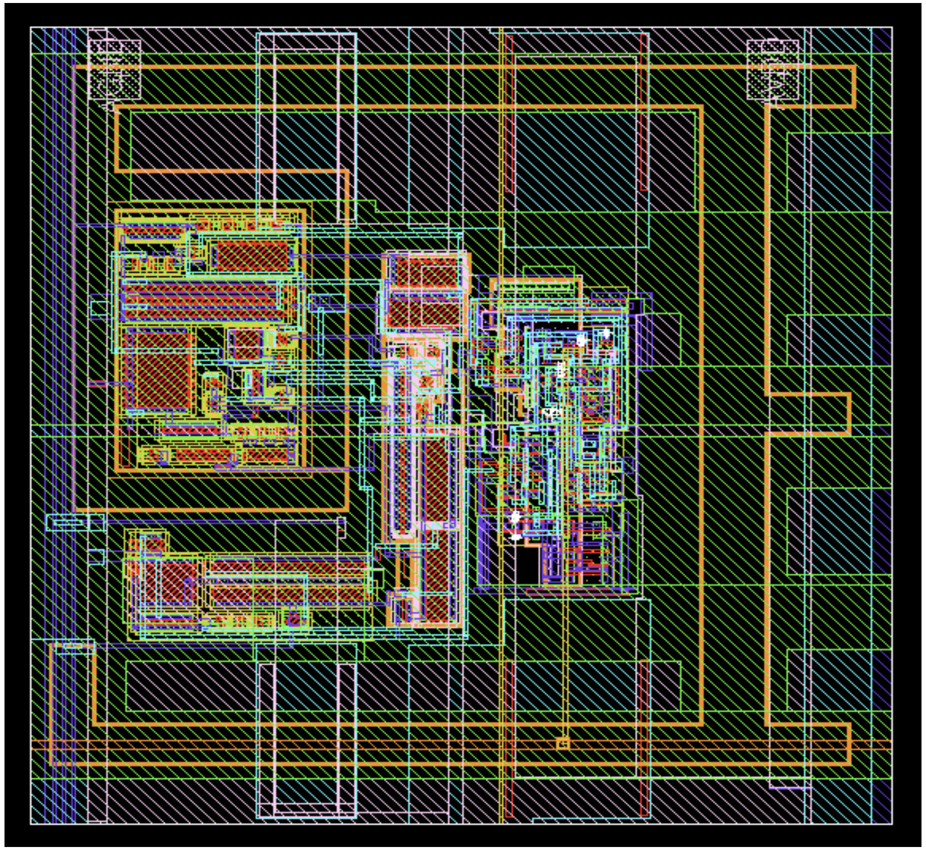
- Scaling Apsel4D to larger matrix size (128x128 or 320x80) dictates to remove the shaper stage to make room for additional macropixel private lines
- Shaper-less front-end makes it possible to reduce the pixel pitch (from 50x50um^2 to 40x40um^2)
- Optimized cell with satellite N-wells surrounding PMOS competitive N-wells in APSEL5T ⇒ Efficiency ~ 99% (from TCAD simulations). Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- Metal shielding between analog and digital voltages improved and made compatible with a large matrix

Pixel layouts

Sensor layout (1): main body + satellites
Sensor area: 410um2
Area NW-PMOS: 70um2
Fill Factor: 0.85
Sensor cap. ≈ 220fF



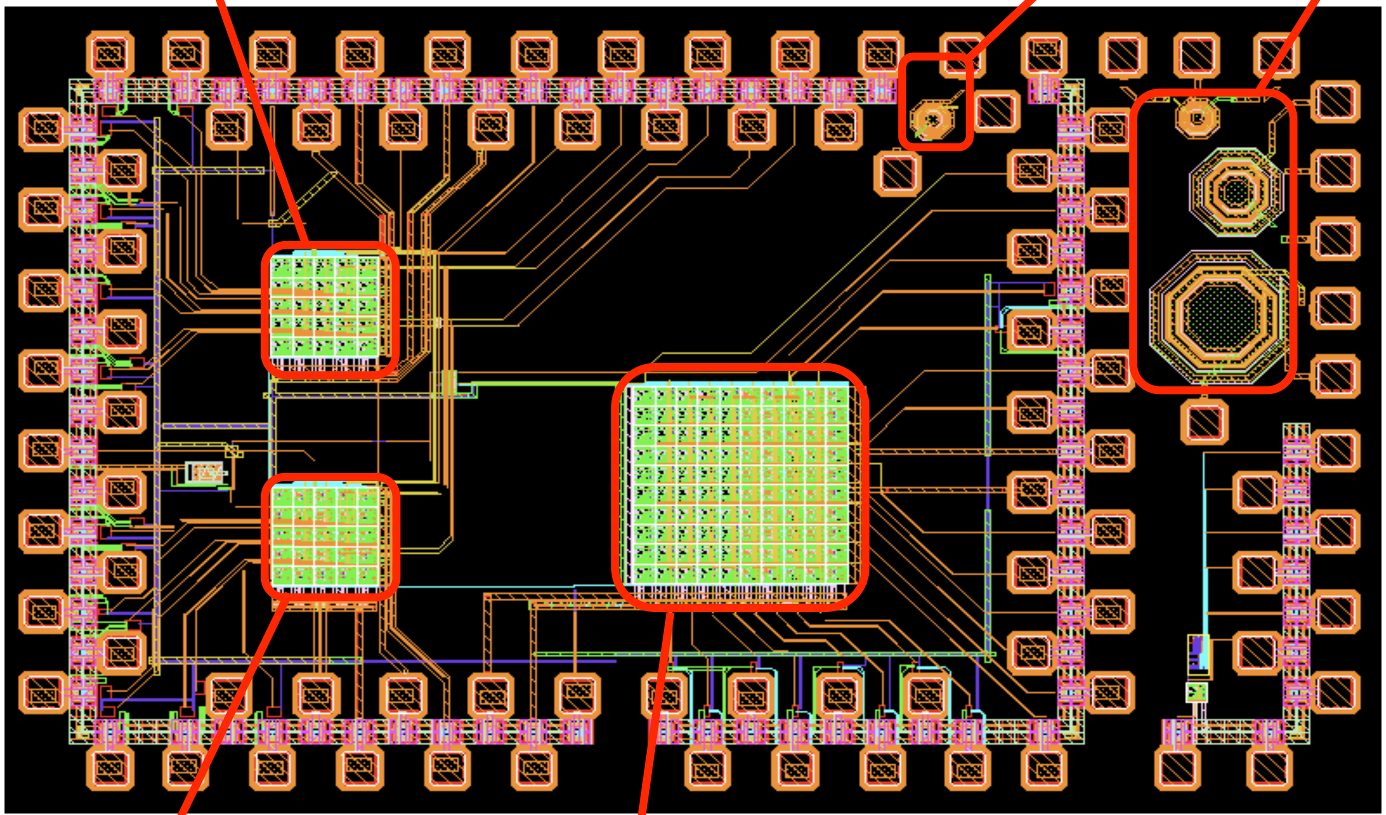
Sensor layout (2): annular shape
Sensors area: 480um^2
Area NW-PMOS: 70um^2
Fill Factor: 0.87
Sensor cap. ≈ 270fF



Apsel5T

M1: 3x3 matrix with all the analog outputs available, injection capacitance for the central pixel, sensor layout (1): main body + satellites

4 NW-P-int. NW-p-sub. diode for radiation hardness tests. 3 different geometries implemented

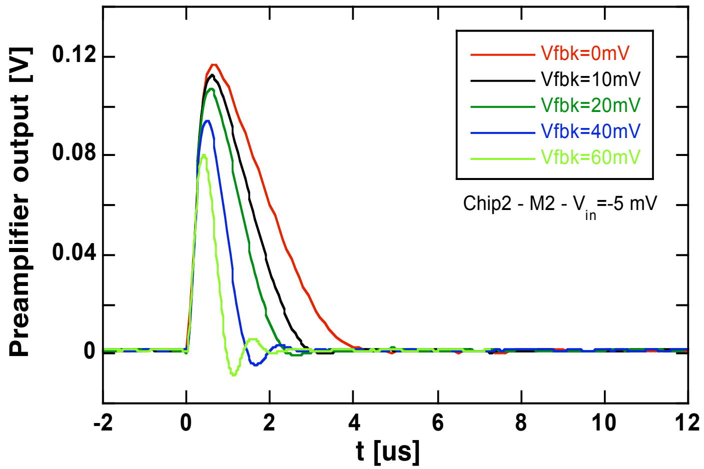


M2: 3x3 matrix with all the analog outputs available, injection capacitance for the central pixel, sensor layout (2): annular shape

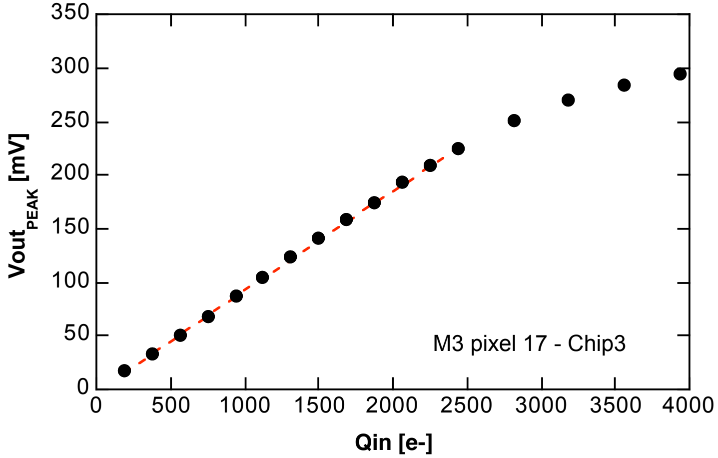
M3: 8x8 matrix with a row-by-row sequential readout. Injection capacitance and analog output available on pixel 17. Sensor layout (1) in the left 8x4 matrix and sensor (2) in the right 8x4 matrix

Apsel5T experimental results

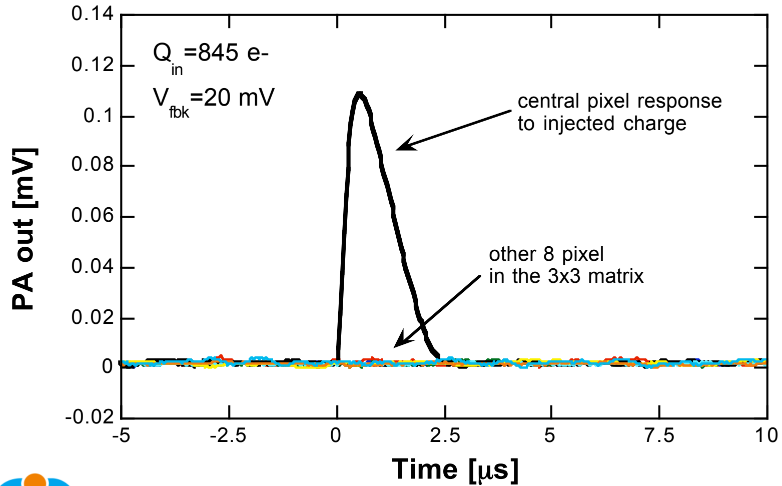
PA response to an external calibration signal



Pixel output vs injected charge



No crosstalk among pixels



Average charge sensitivity: 680 mV/fC

Threshold dispersion: 45 e-

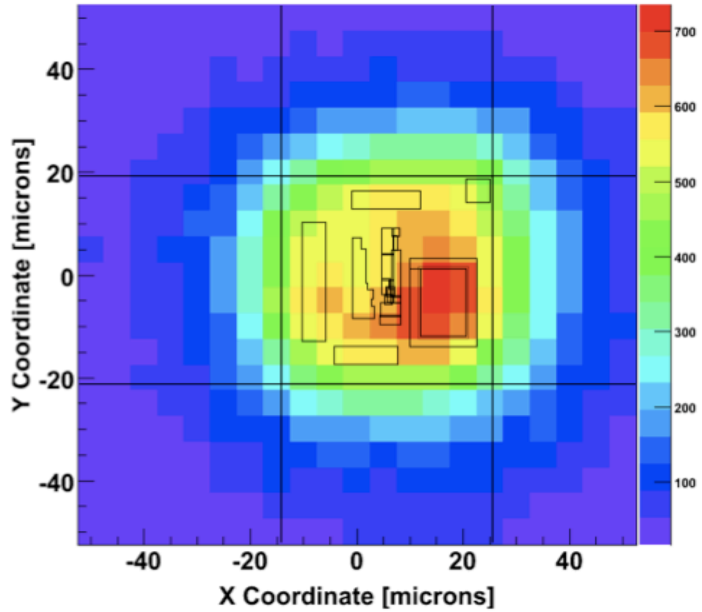
Pixel	Chip 3 - ENC [e-]
22 M1	45
22 M2	53
17 M3	53

Plans for the next weeks:

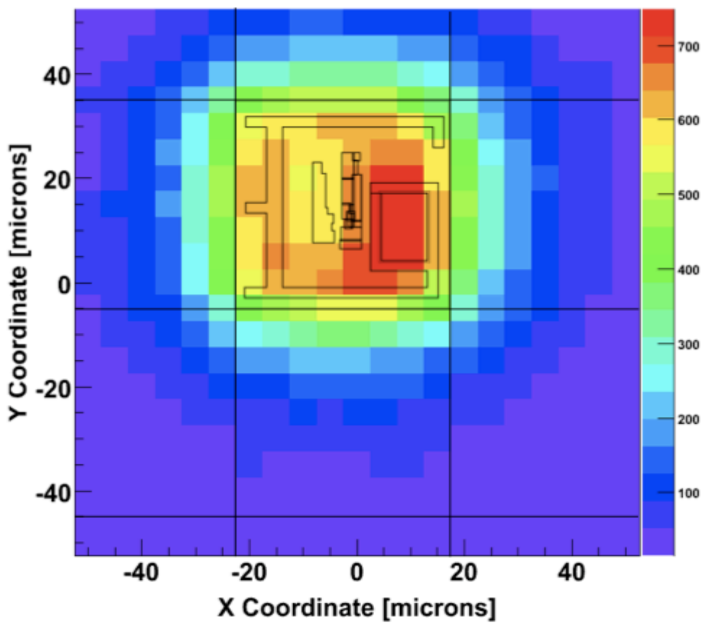
- Absolute calibration with a ^{55}Fe source
- Tests with ^{90}Sr source

Apsel5T: laser measurements

- Charge collected by the central pixel of M1 and M2 matrix as a function of the laser position
- Signal magnitude (e-) is plotted in the z (colour) axis for each position of the laser spot
- 5um step in X and Y (1064nm wavelength)
- The layout of the n-well layers and the dimension of the pixel pitch has been superimposed (exact position unknown)
- σ_{xy} of the laser ≈ 20um
- The main purpose of this measurement is to show the relative charge collection versus position (the amount of charge that is deposited has not been calibrated)
- Small reduction of the collected charge in the central region of the competitive n-wells
- Annular shape sensor with yellow and red area larger than main body + satellites

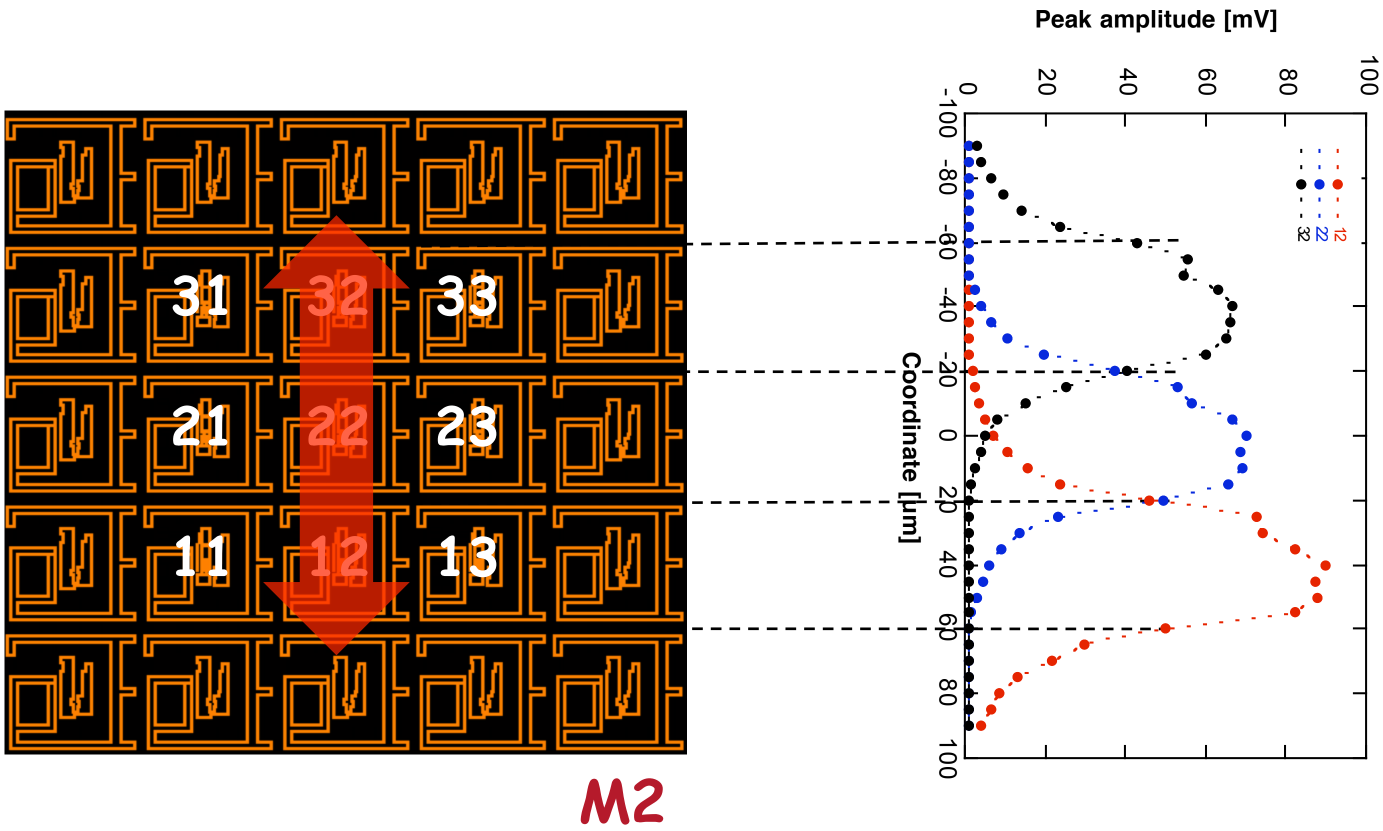


Sensor layout: main body + satellites



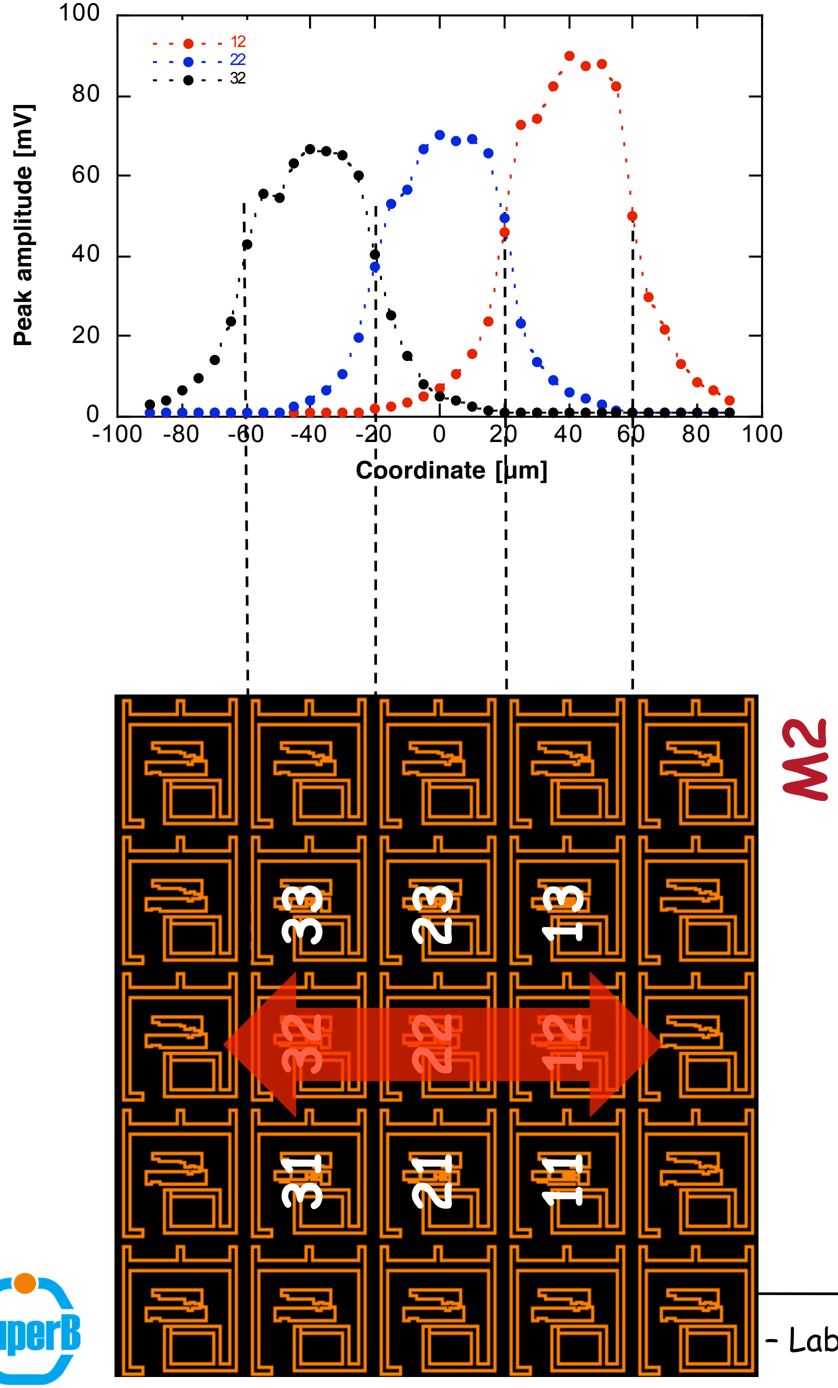
Sensor layout: circular shaped

Apsel5T: laser measurements



- X=0 is set at the maximum of 22, Y=0 is set at the 22 maximum and 12, 32 minimum
- The peak amplitude of 12, 22, 32 measured at the same time for each laser spot
- Spot size ≈ 20um
- 5um step in X and Y
- chip 2

Apsel5T: laser measurements



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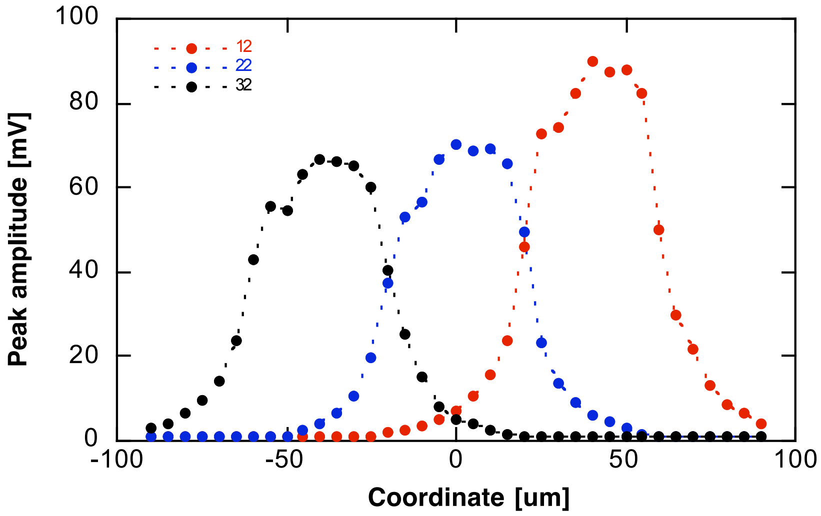
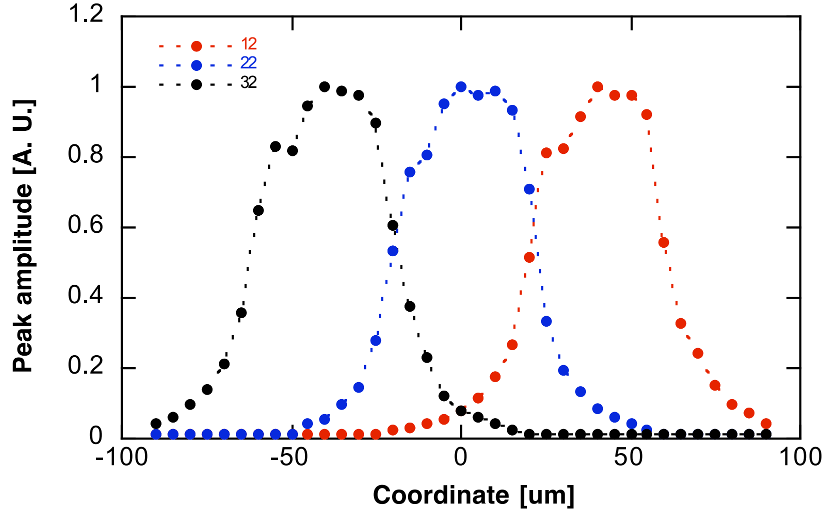
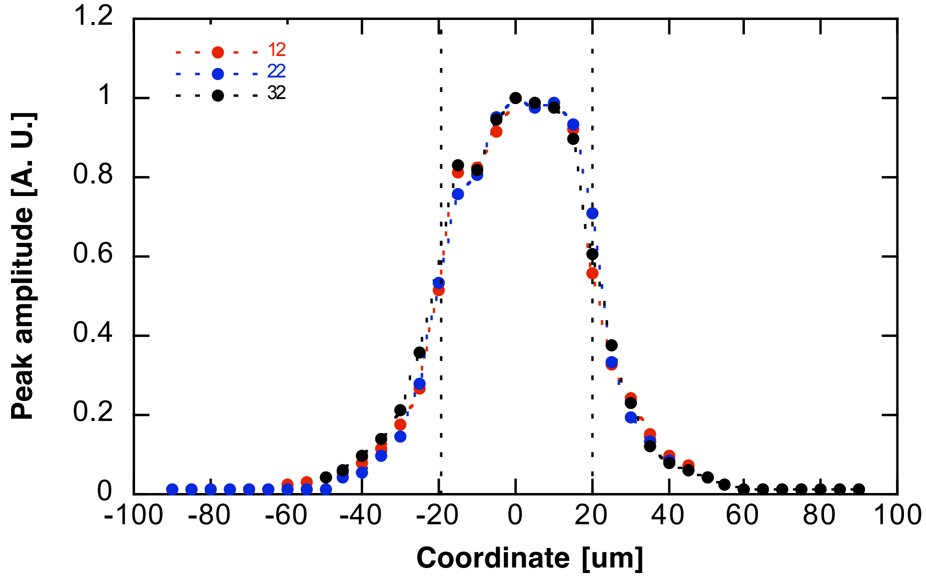
Apsel5T: laser measurements

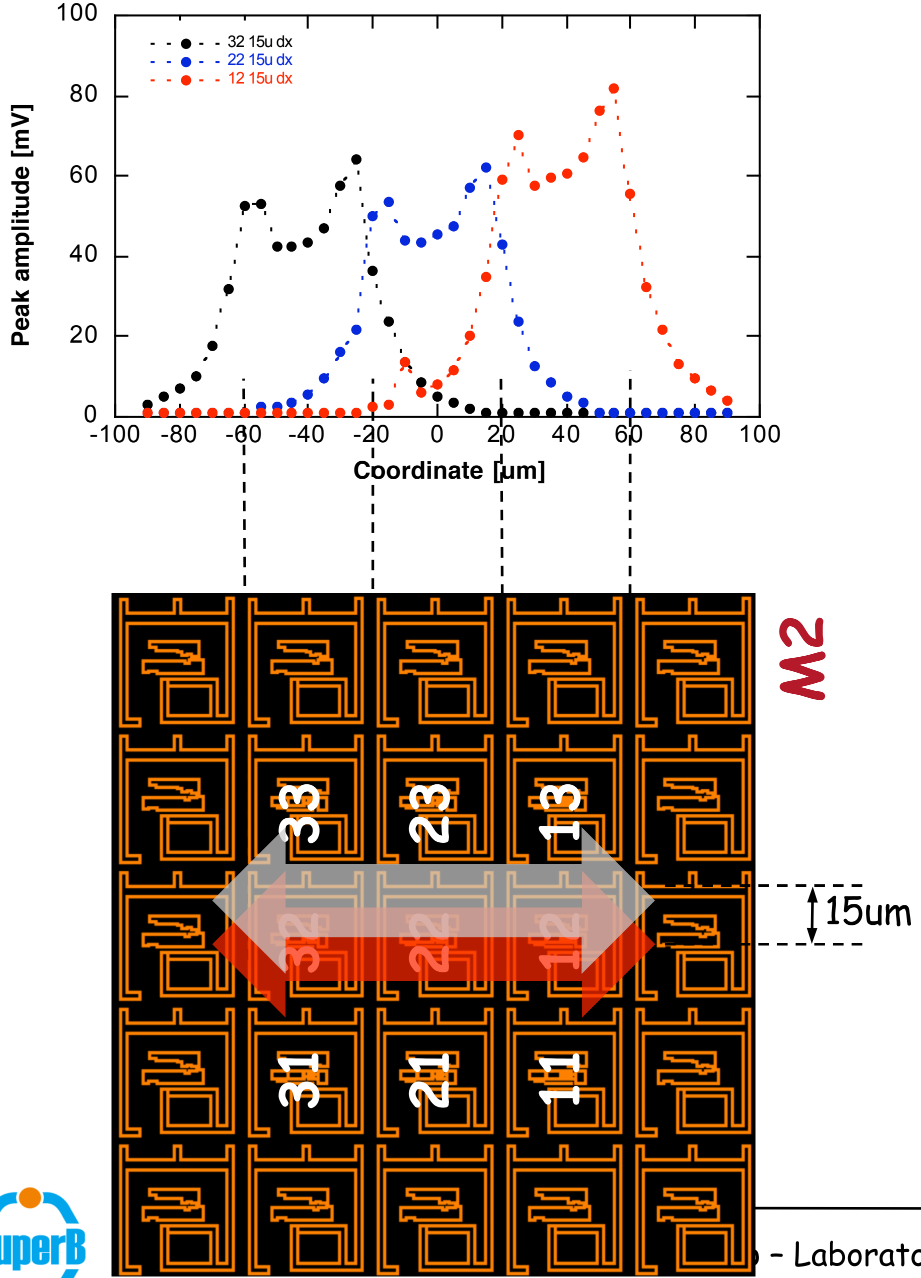


normalized gains →



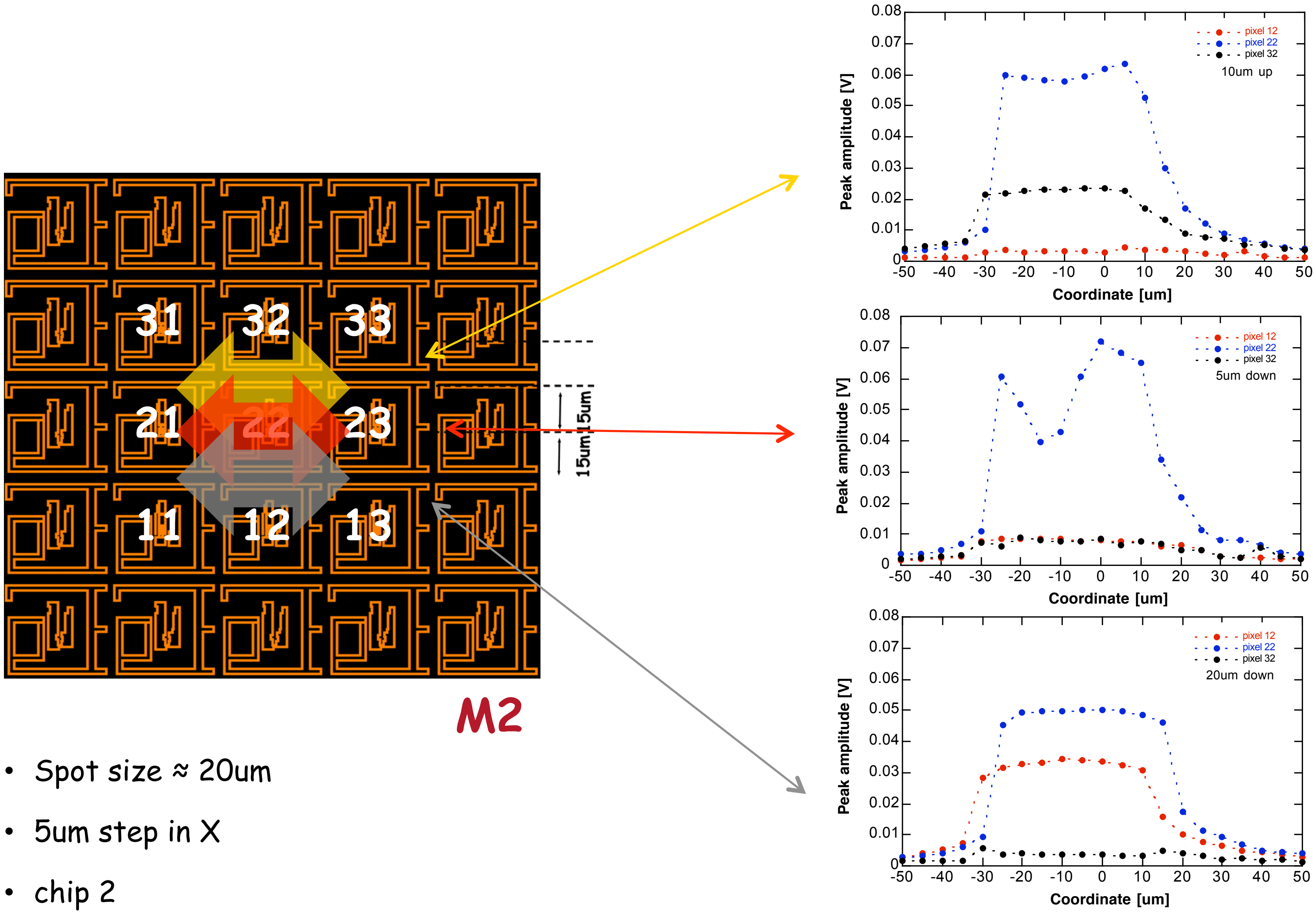


Apsel5T: laser measurements



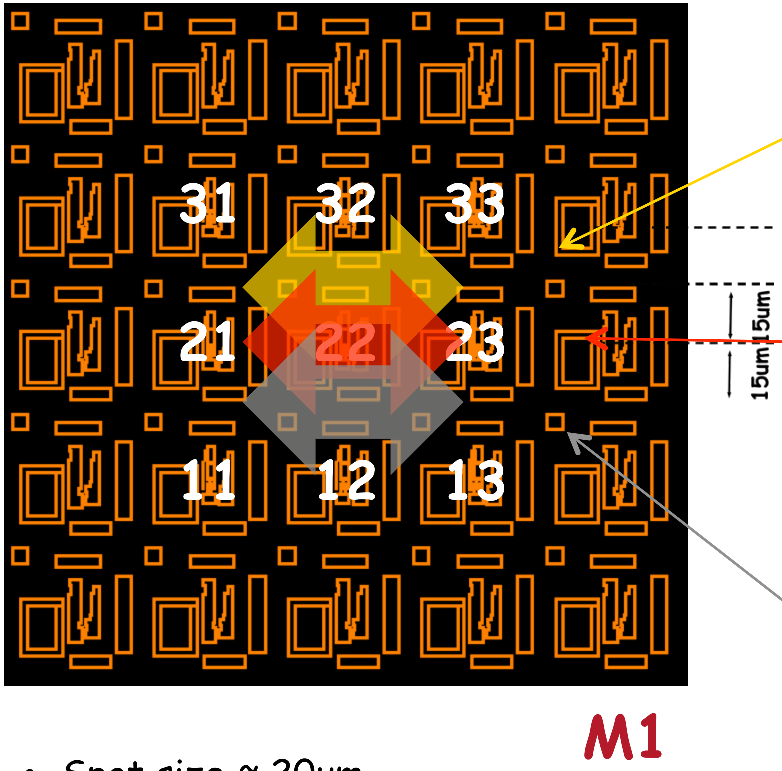
- X=0 is set at the maximum of 22, Y=0 is set at the 22 maximum and 12, 32 minimum
- The peak amplitude of 12, 22, 32 measured at the same time for each laser spot
- Spot size ≈ 20um
- 5um step in X and Y
- chip 2

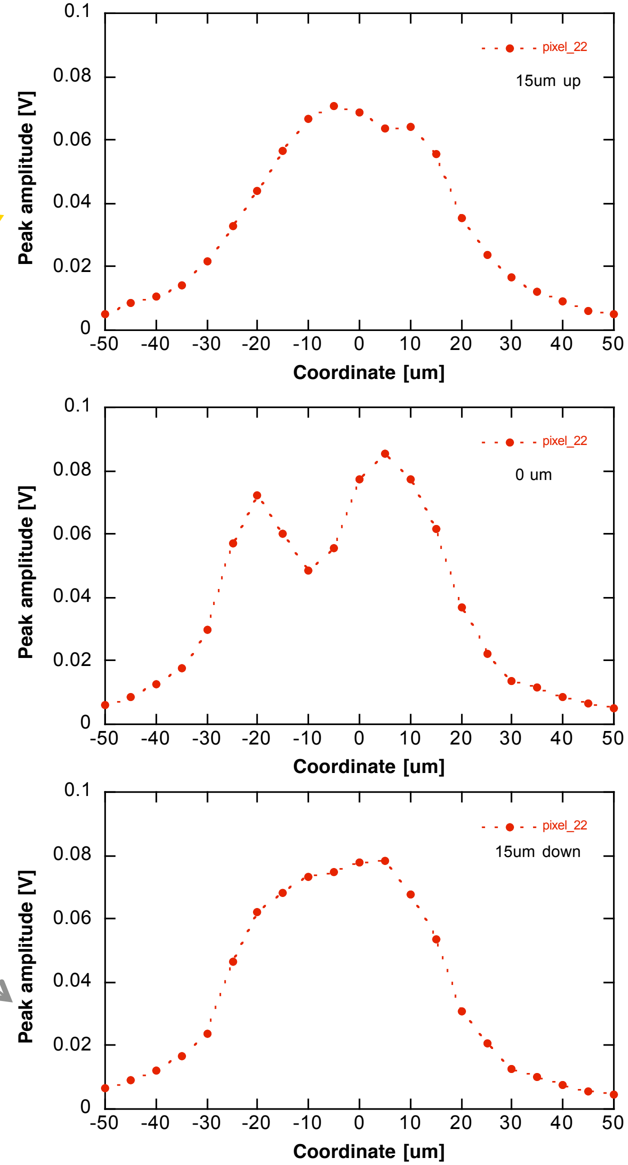
Apsel5T: laser measurements



- Spot size ≈ 20um
- 5um step in X
- chip 2

Apsel5T: laser measurements

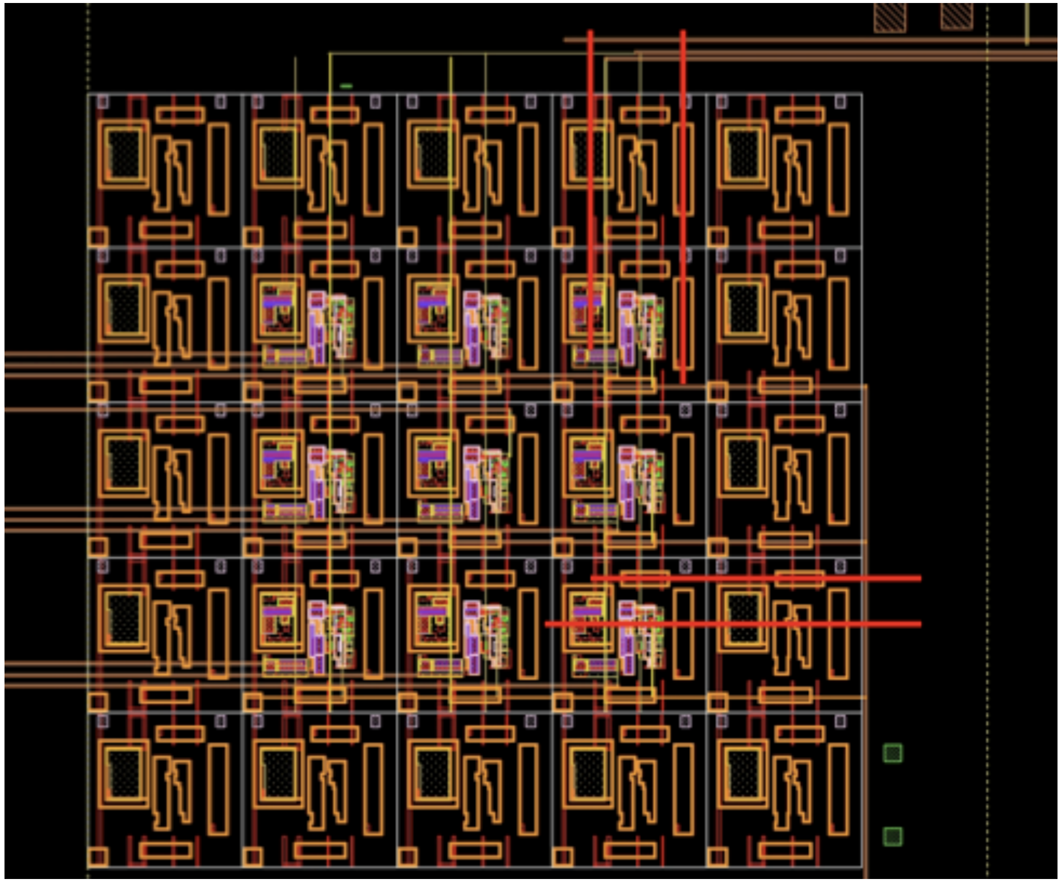


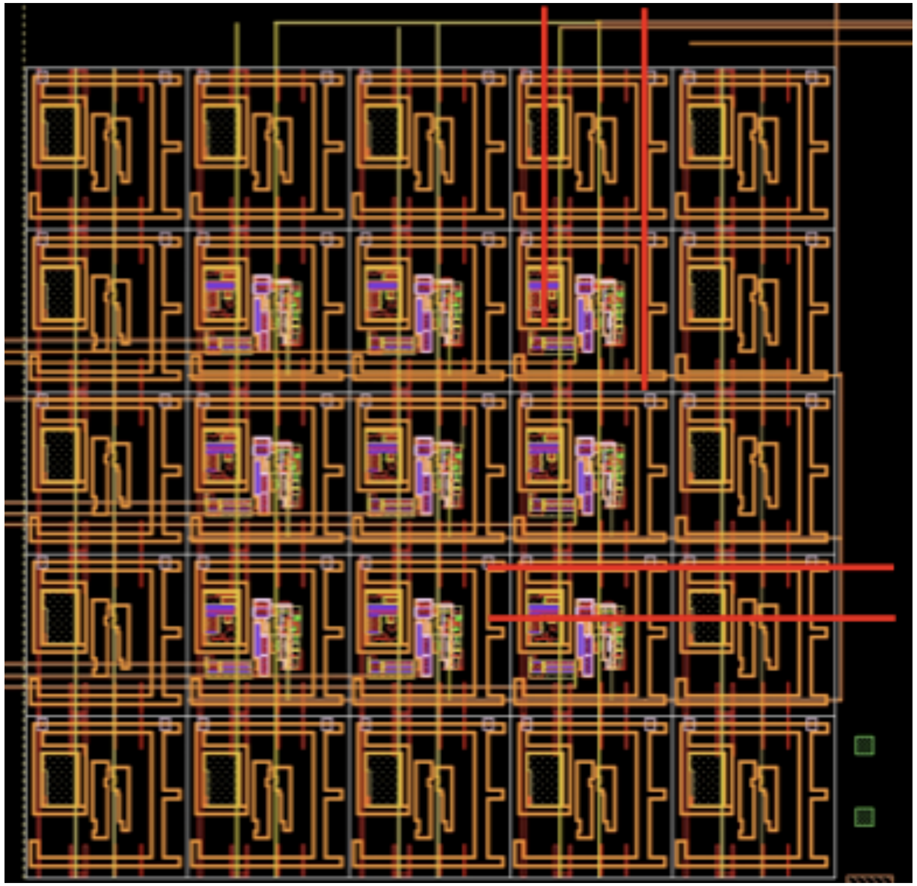


- Spot size ≈ 20um
- 5um step in X and Y
- chip 2

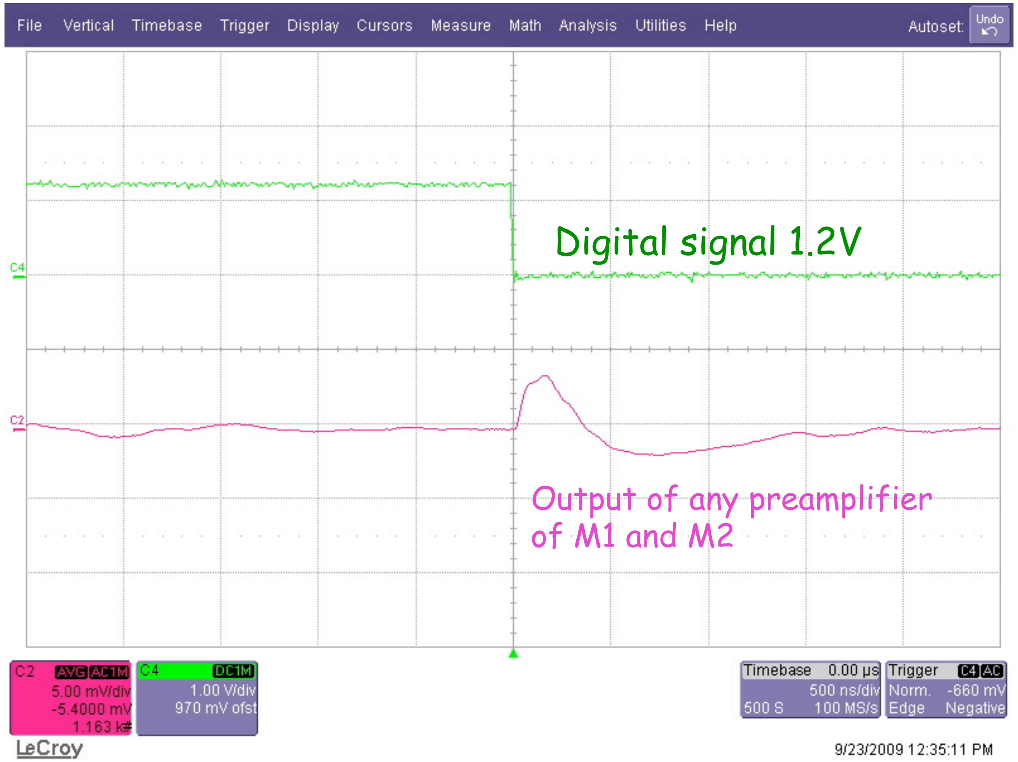
Metal3 and Metal4 shields

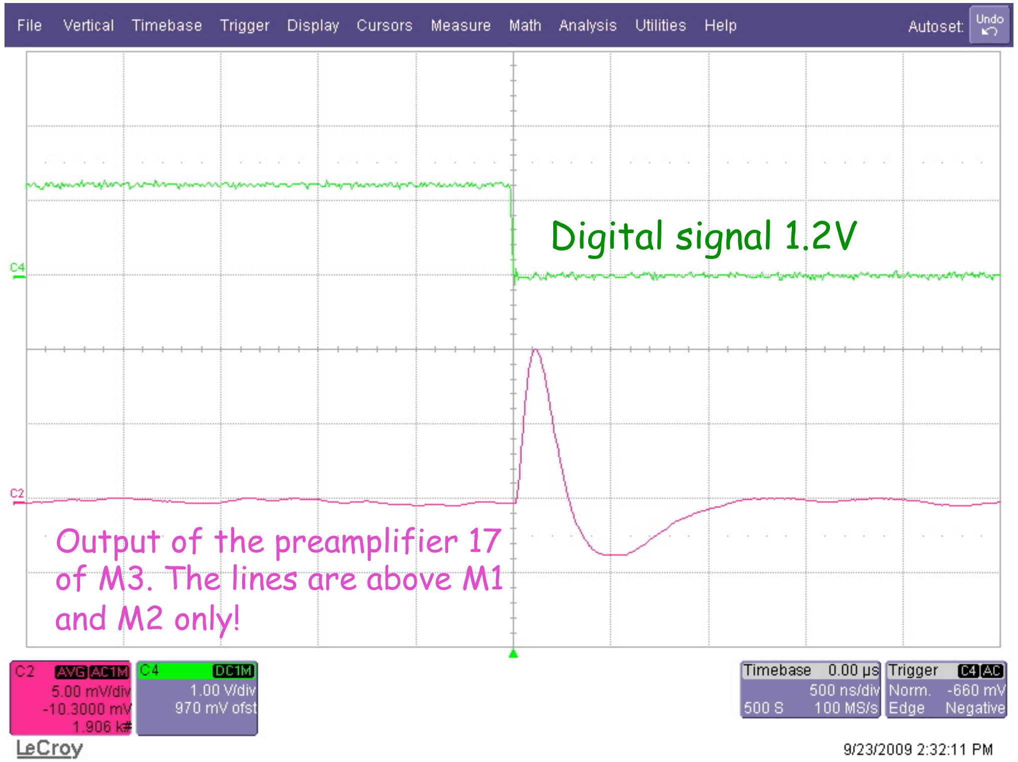
- We used M3 and M4 to distribute analog and digital power and to shield the sensor from the digital activity
- We routed M5 and M6 lines (as digital routing) above the sensor in different positions to test the shields





Metal3 and Metal4 shields





Conclusions

- Latest version of Apsel family chip (Apsel5T) has been fabricated in a planar 130nm DNW CMOS technology (STMicroelectronics)

- In view of the scaling to a larger matrix size, a compact, shaper-less design has been proposed for the analog front-end

- Non-negligible charge sensitivity variation among the pixels comes from device mismatch in the preamplifier feedback. A new improved feedback network is being prepared for the next version of the analog channel

- Laser measurements on the optimized layout of the sensor shows encouraging results in terms of charge collection properties

Backup Slides

Laser measurements

- Preamplifier outputs of the 3x3 matrices (the position of the laser is such to obtain the maximum amplitude)
- As shown in the previous slide there is a wide variation in the peak amplitude and in the return-to-baseline time
- Variations of the process parameters of the feedback network transistors could explain this effect