SuperB Workshop XI - LNF

Status report on CLUster COUnting activities

G. F. Tassielli
on behalf of CLUCOU group

INFN – Lecce
Dept. of Physics University of Salento
Dept. of Innovation Enginnering, University of Salento

A CMOS VLSI chip for Cluster Counting readout

- In order to instrument a full scale Drift Chamber a special readout electronics is needed;

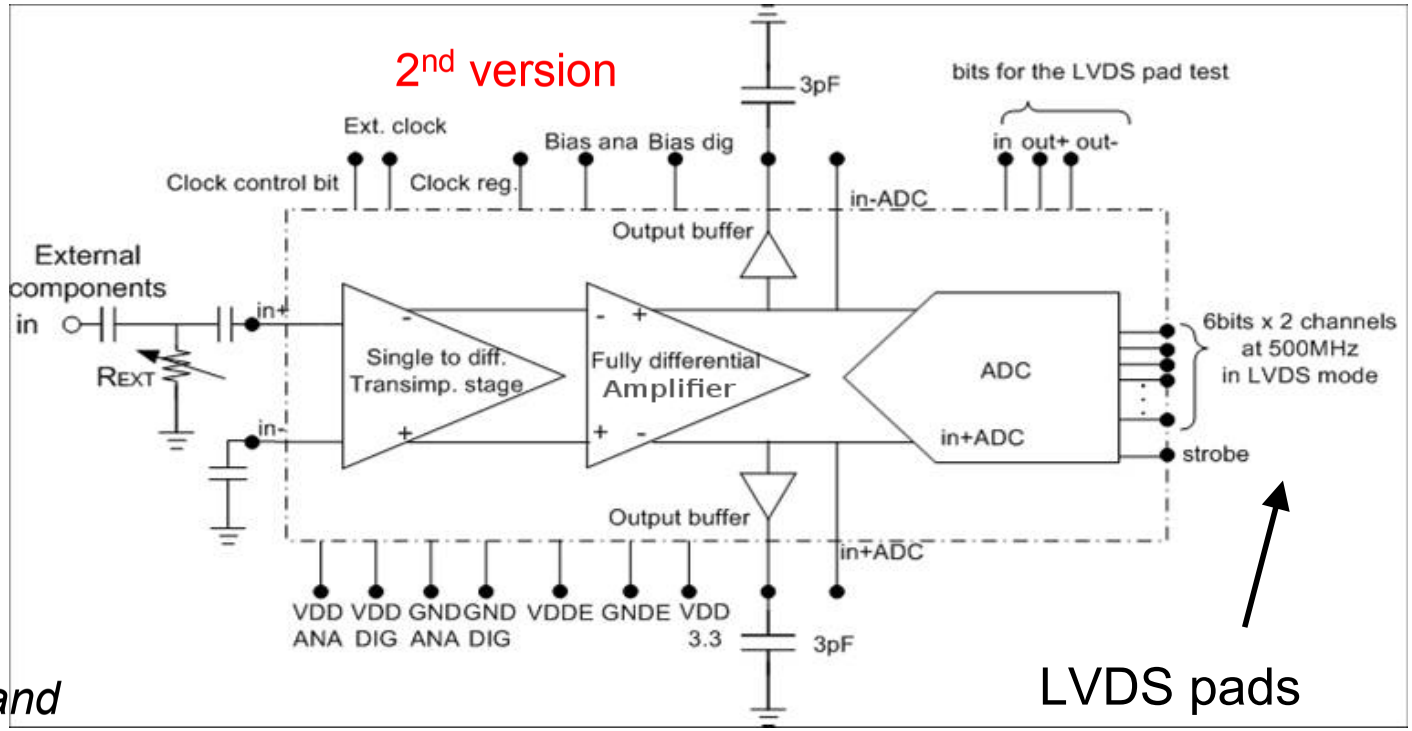
  goals:

  • fast (sampling rate ≥ 1Gsa/s, bandwidth > 500 MHz);

  • compact;

  • low cost in power and in money.

Overall architecture:



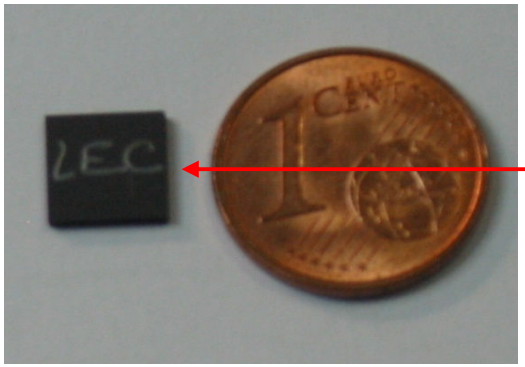
- designed in 0.13 μm CMOS technology;
- 1-2V and ~ 100 mW;
- Transimpedance preamplifier 26dB, -3dB @ 700 MHz;
- fast ADC 6 bit @ 1Gs/s;

Design and simulation using CADENCE 5.4.14

For the second chip version layout and MOS technology studied

A CMOS VLSI chip for Cluster Counting readout

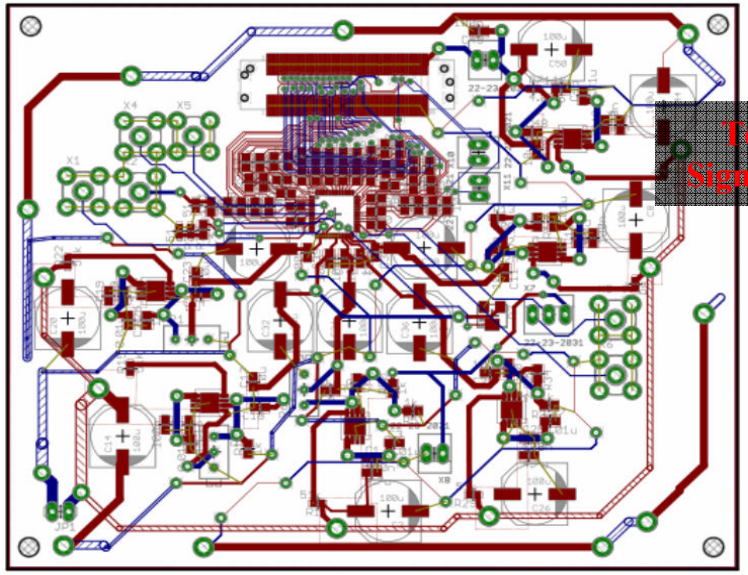
Preliminary Result from the 2st chip version

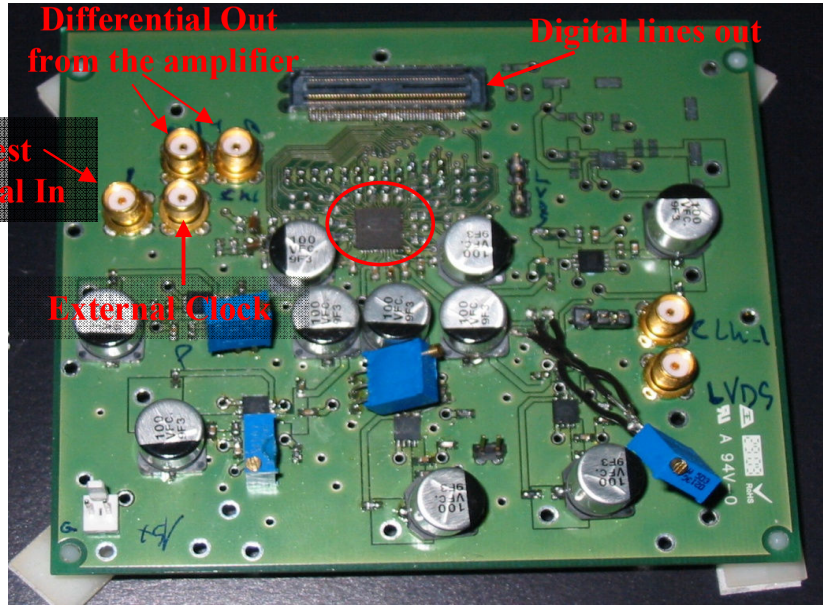


~20 chips delivered by the foundry at the end of September (9 of them are encapsulated)

The test started after the first two week of October when the testing PCB board was completely assembled

- Board designed on 4 layers;
- the distances between the layers chosen to have the right impedance matching;
- SMD components only;
- designed and test with *eagle 5.4.0 professional*;





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Preliminary Result from the 2st chip version

Before to continue:

All the measure that we are showing are very preliminary and not completed.
We apologize but we did not have enough luck so far:

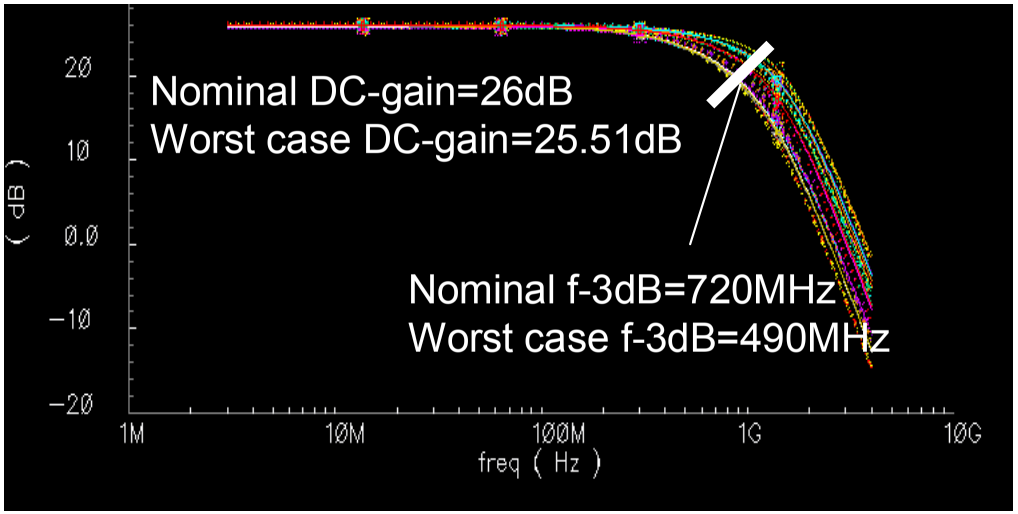
- the probe of the Logic State Analyzer had a fake channel, so we have spent time to find the problem and to find a temporary solution. Now the probe is under repair;
- during the test, in the first half of November, the oscilloscope probe crashed. Now it is under repair.

Due to these problems we had less that 1 month to test the chip and the PCB board and we had not the possibility to conclude systematic cycles of measurements.

A CMOS VLSI chip for Cluster Counting readout

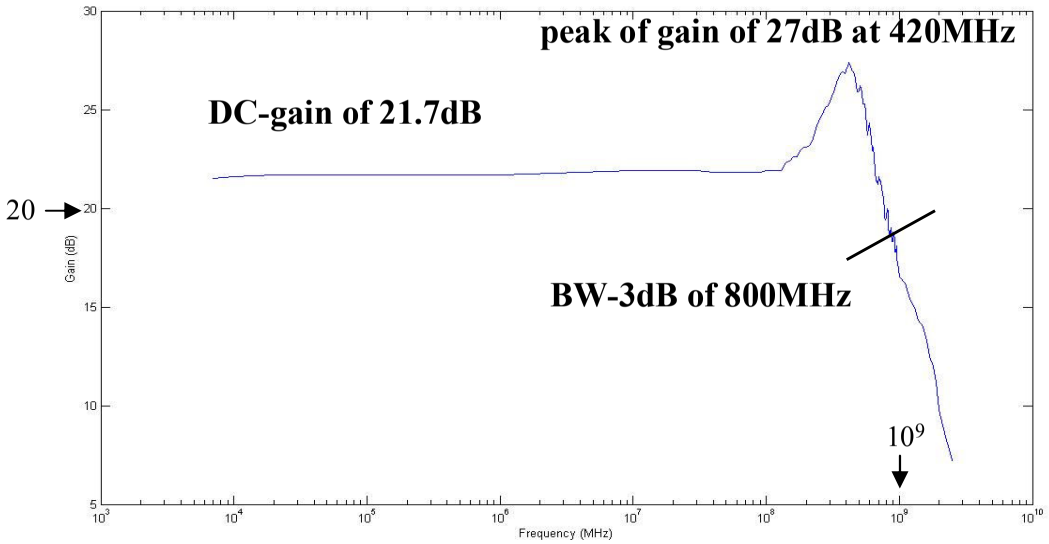
Preamplifier performance

Simulations



Parameter	Value
Input impedance	**50 Ω**
No. of stages	**2**
1st stage gain	**16 dB**
2nd stage gain	**10 dB**
Overall DC-gain amplifier	**26.12 dB**
Nominal -3dB Bandwidth amplifier	**735MHz**
Current consumption	**13.22 mA**
Noise	**81 µVrms**

Preliminary results

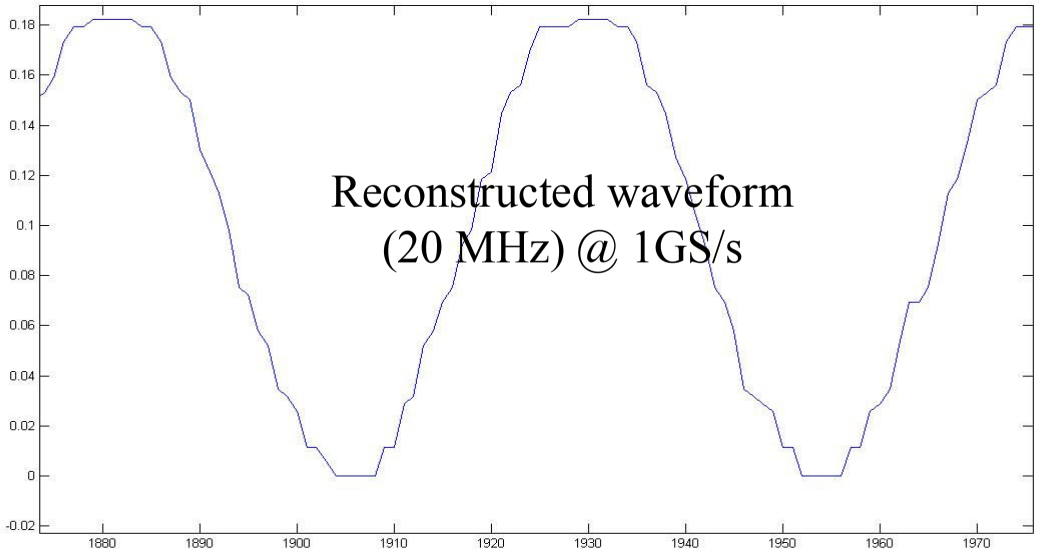


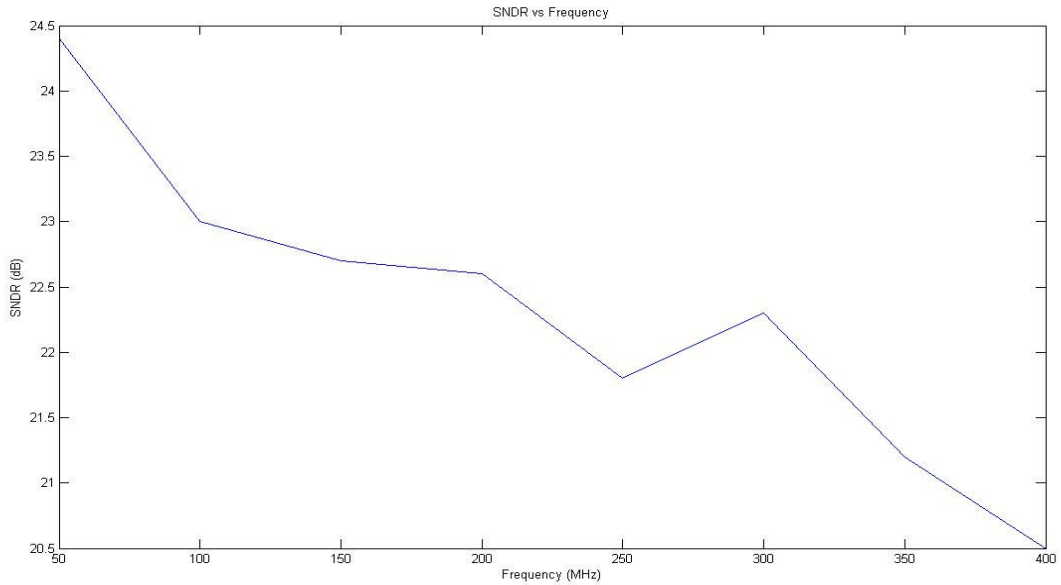
The transfer function is not very accurate, it has been obtained by measuring with the oscilloscope the value peak-to-peak of the output amplifier when the sinusoidal signal input is 20mV peak to peak as a function of the frequency.

Noise of Preamplifier + test board **0.258 mVrms**

A CMOS VLSI chip for Cluster Counting readout

ADC performance





The ADC lives! During these preliminary test we can reconstruct a digitized pattern but we cannot characterize and measure its performances.

INPUT FREQUENCY [MHz]	SNR [dB]	SNDR [dB]
30	26.9	23.9
100	26.1	23
150	24.3	22.7
200	26.9	22.6
250	24.4	21.8
300	26.55	22.3
350	23	21.2
400	22.6	20.6

SNR Signal-to-Noise Ratio
SNDR Signal to Noise-plus-Distortion Ratio

The Chip is fed at 1.2V, the LVDS pads are fed at 3.3 V. The whole of PCB board an the chip consumes 320mA.

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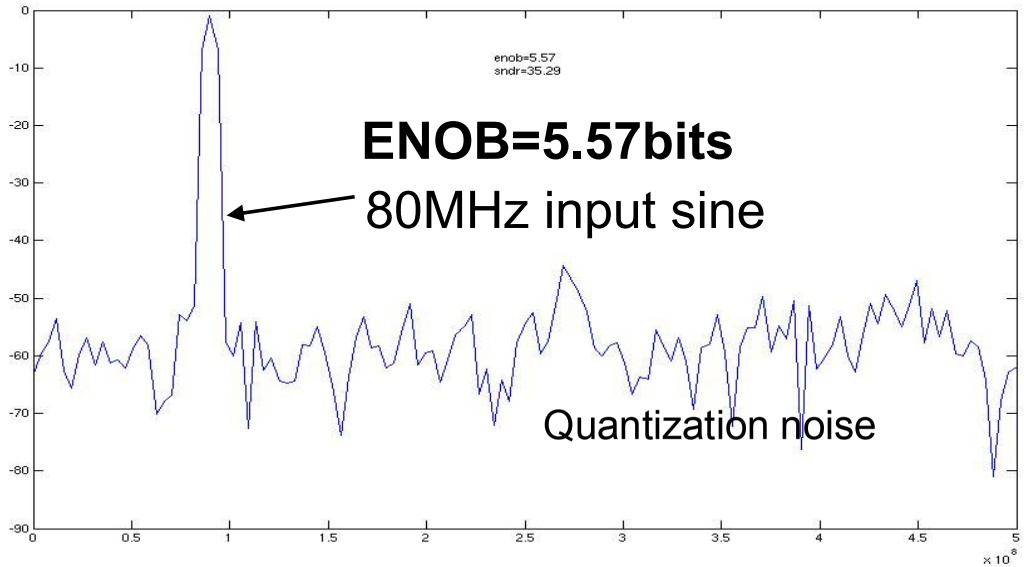
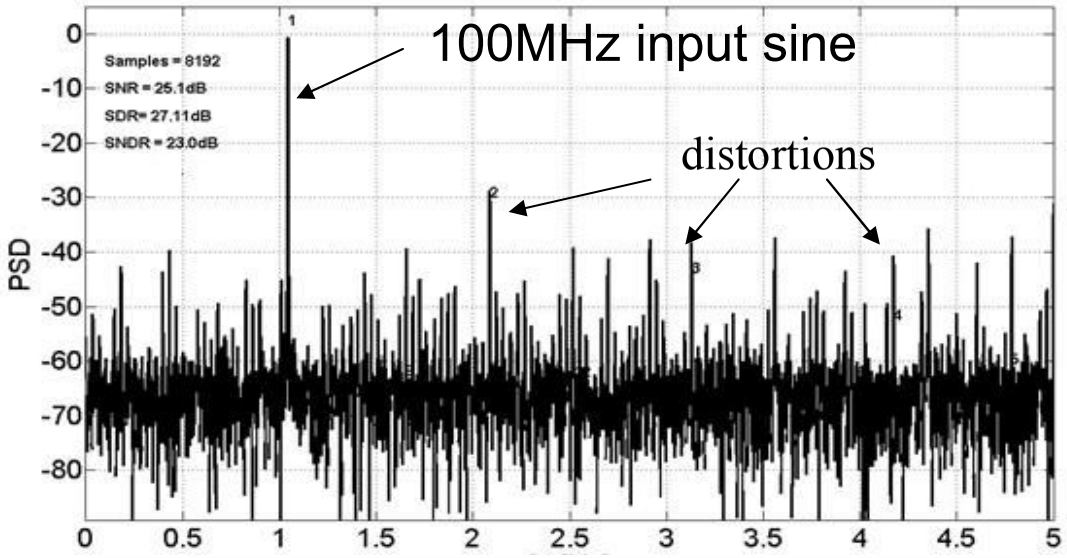
ADC performance

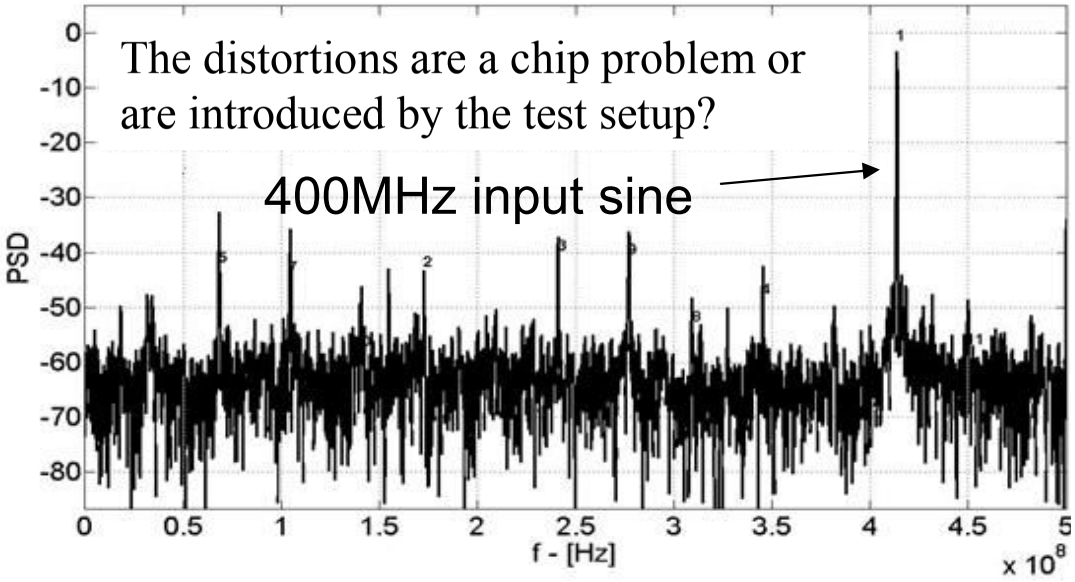
Simulations



Parameter	Values
Resolution	6 bits
Sample rate	1 Gs/s
Clock Frequency	1 GHz
ENOB	5.57 bits
Full scale	366 mV
LSB	6 mV
Current consumption	29mA
Quantization noise	1.73 mV_{rms}
Input referred quantization noise	86.5 μV_{rms}

Preliminary results



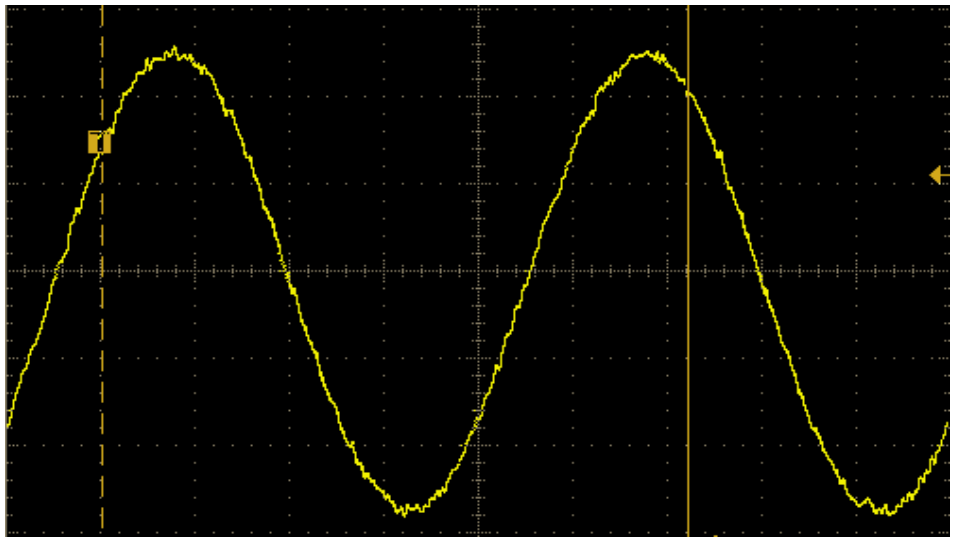


A CMOS VLSI chip for Cluster Counting readout

ADC performance

The following problem was found.
Starting up the ADC clock (internal/external) the signal out of the preamplifier results distorted.

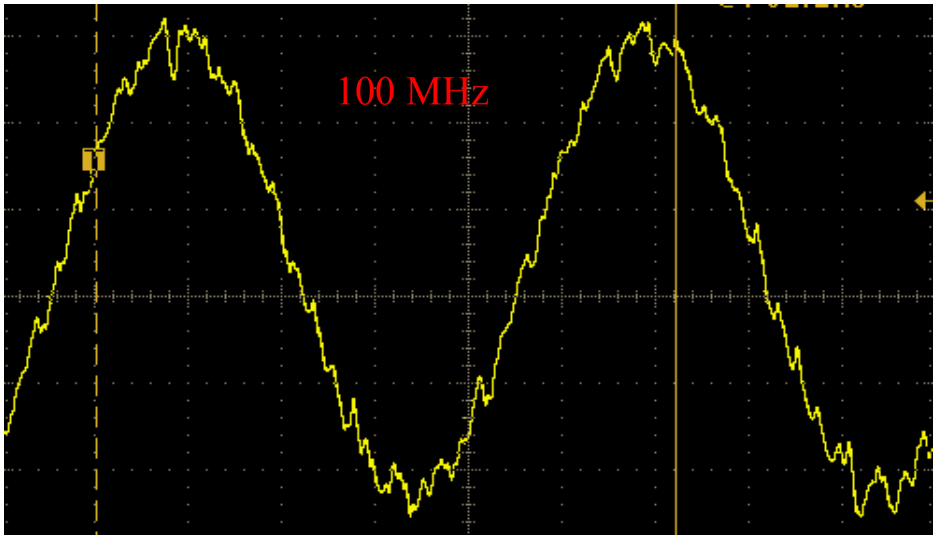
Signal out of the preamplifier without clock.

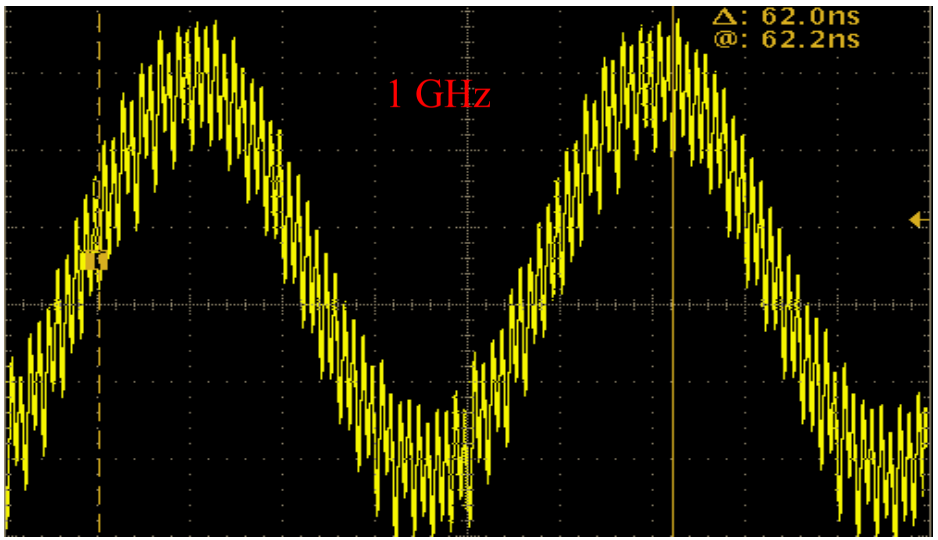


20MHz @ 4GS/s

Switching on the ADC clock

external clock at:





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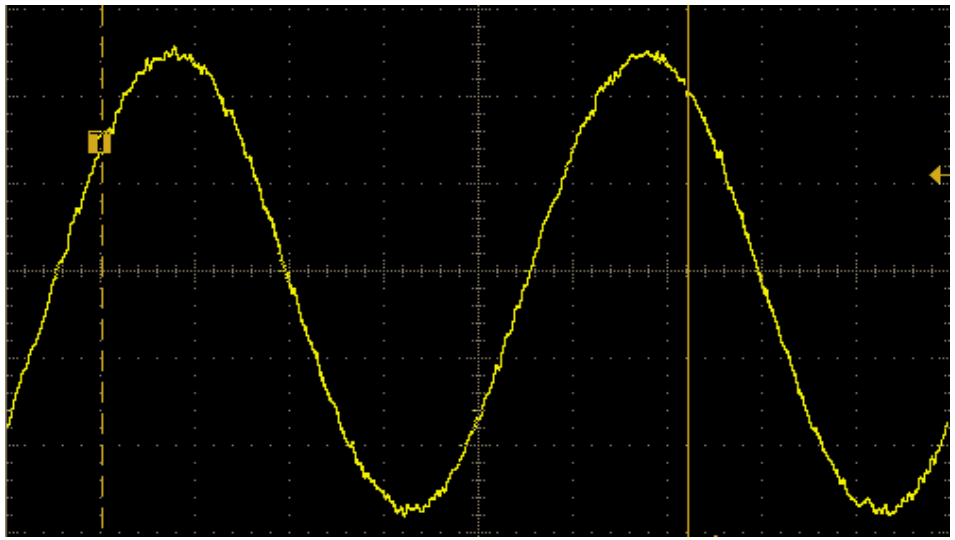
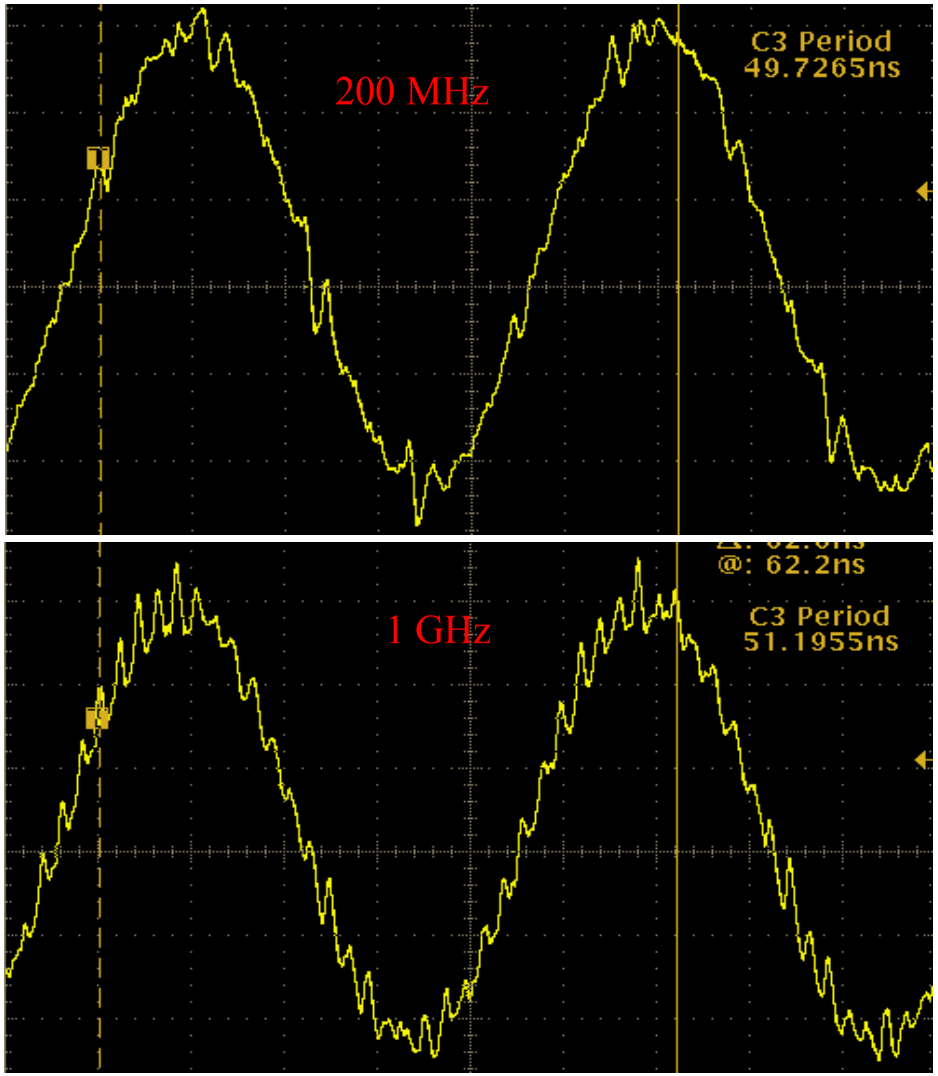


20MHz @ 4GS/s

Switching on the ADC clock

internal clock at:



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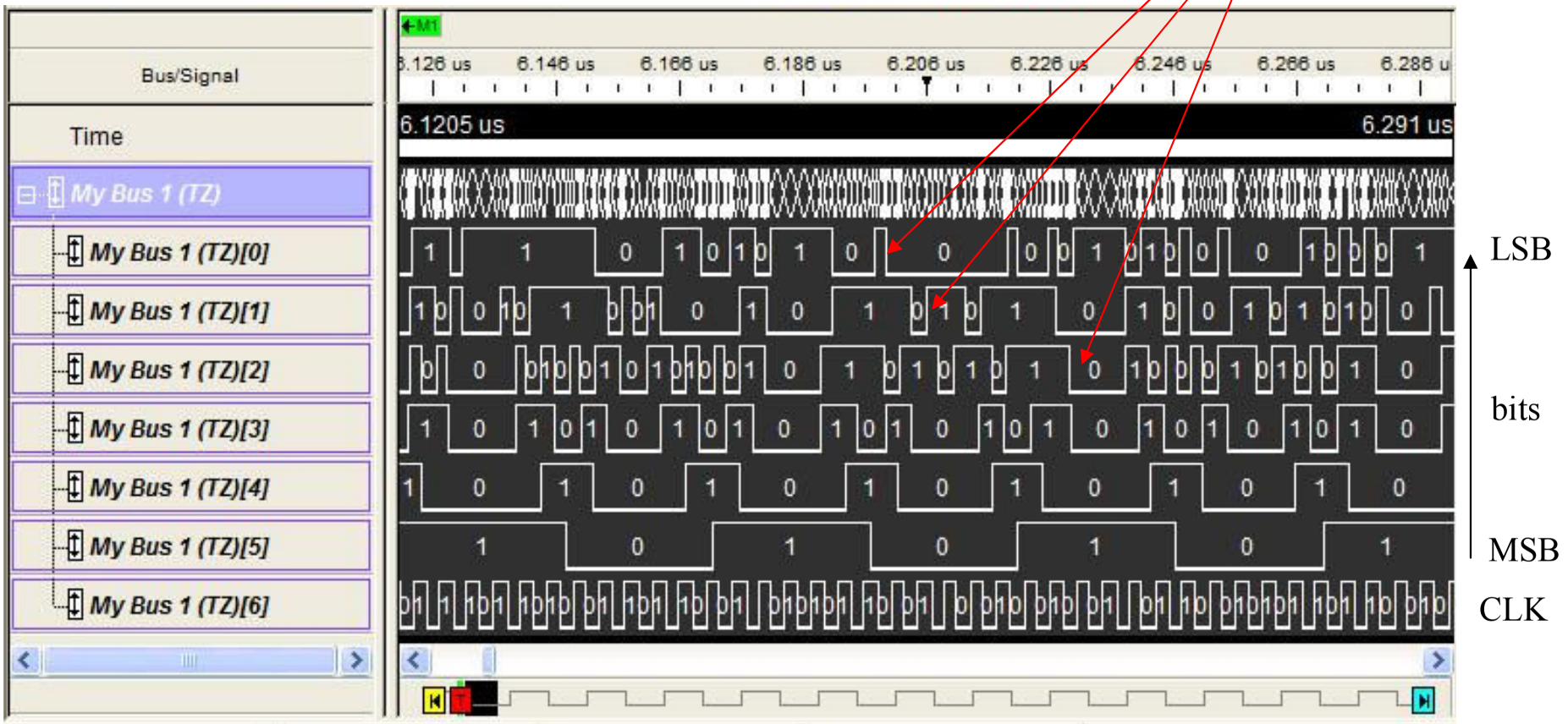
ADC performance

Due to the distortions the less significant bits are randomized

It is not easy to recognize a regular path.

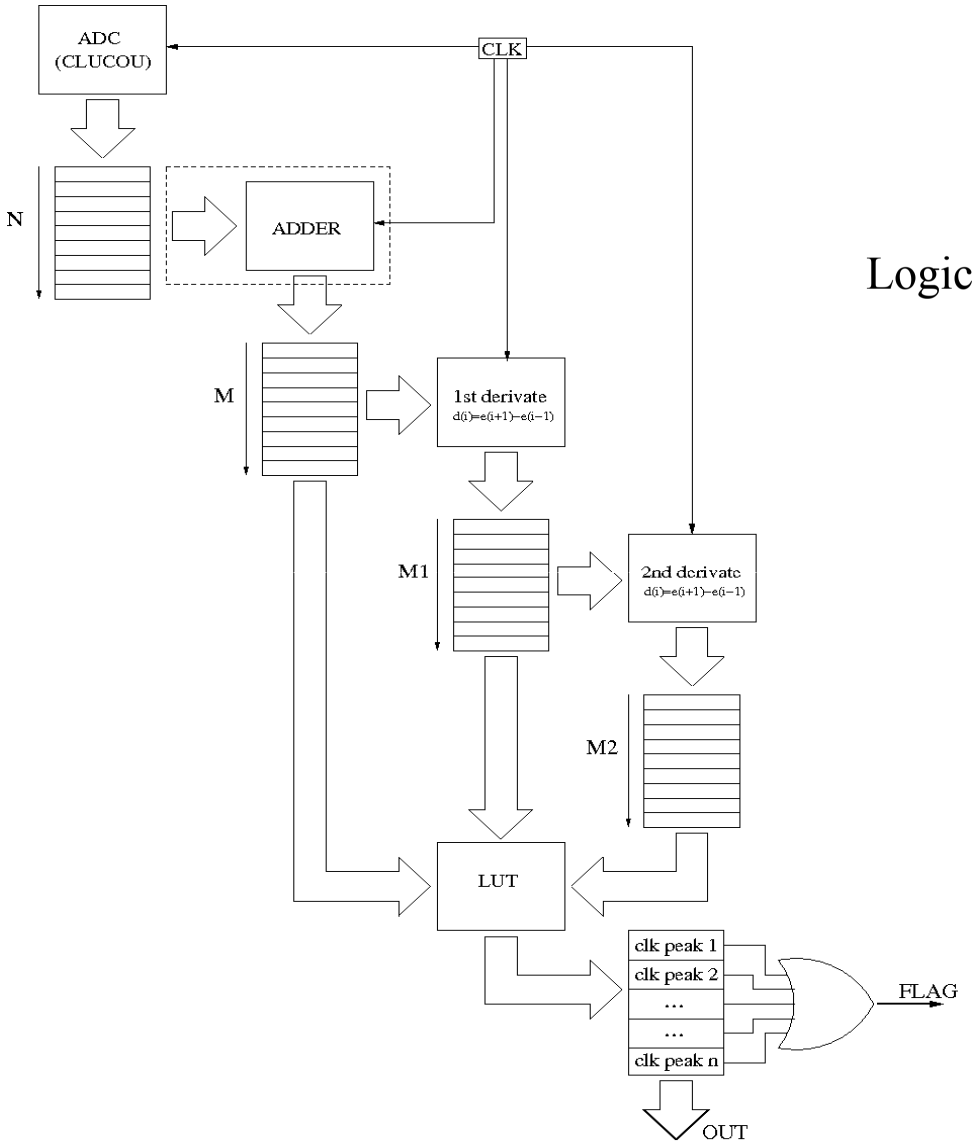


Conclusions and future planes

We think that the distortion introduced by switching on the clock are mostly due to some impedance mismatches, ringing and cross talk on the PCB;

- we are investigate the PCB, probably we have to redesign and rebuild it. We want to finish this stage before the end of January;
- restart the systematic test of the chip during January (if the probes will come back);
- try the chip on a drift tube and compare it with an high resolution oscilloscope, during February;
- we are investigating if we can use a general purpose acquisition board, made by Fermilab, to interface the PCB test board with it. In this manner it should be possible to instrument a few drift chamber prototype channels with the chip. We hope that we will able to do the first tests on January;
- It is reasonable that a usable system will be ready for the end of February-the start of March.

Backup



Logic scheme of a simple counting-timing algorithm that should be possible to implement in a FPGA