DCH Readout and Control System

A (very) preliminary study

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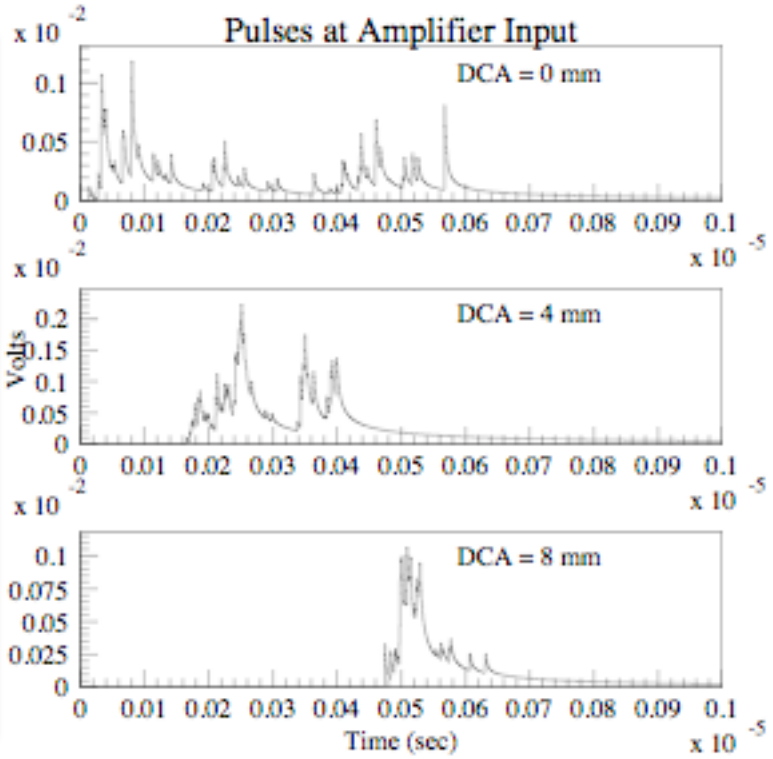
Outline

1. The DCH readout BABAR experience (a short review of the upgraded readout system)
2. OL – Super-B DCH vs BABAR DCH
3. Super-B DCH FEE possible scenarios
4. Power dissipation, radiation environment and material budget
5. Conclusions

DC numbers

- Cylindrical (≈ 1.6 m external diameter, ≈ 2.75 m length)
- Hex-cells (≈ 1.2 cm (radial dir) x 1.7 cm (azimuthal dir)
- 10 superlayers (4 layer each) – 4 axial – 6 stereo
- 7104 cells
- He:Isobutane (80%/20%) gas mixture - 22 i.p./cm per mip - 44 electrons (total ionization)
- Average charge per electron ≈ 8 fC (20% collected in first 10 ns)



BABAR FEE – Block Diagram

Requirements

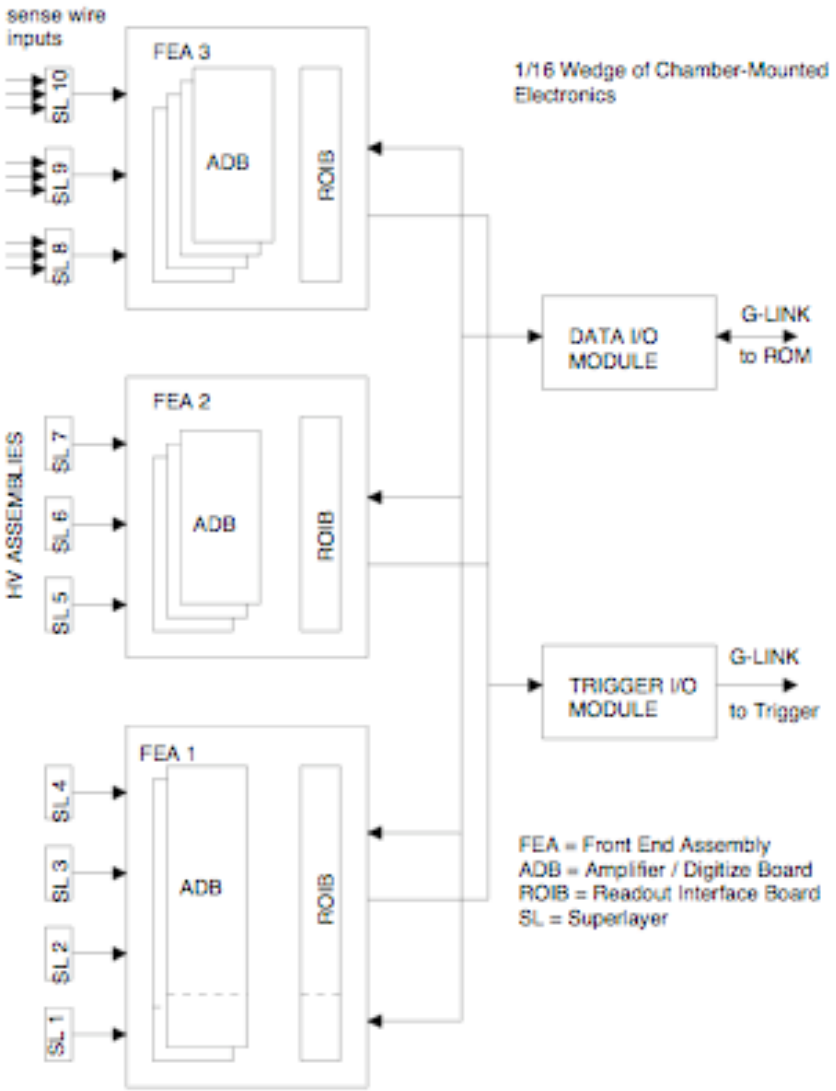
- Tracking (charged-particle momentum and event reconstruction)
- dE/dx (particle identification)
- Trigger (multi-charged-particle trigger for the BABAR detector)

DATA
- 4 - 1 Gbits/sec OL

TRIGGER
- 24 - 1.2 Gbits/sec OL

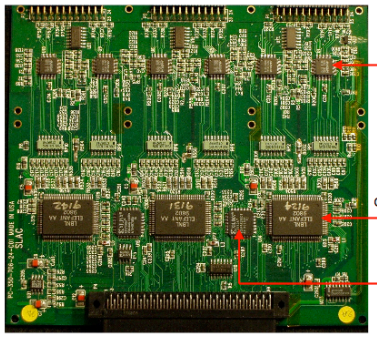
ECS
- Managed by DATA I/O modules (CAN standard)

COMMANDS (sync, L1_accept, read_event, cal_Strobe
- Managed by DATA I/O modules (1 Gbits/sec OL from ROM)



BABAR FEE – Analog to Digital Board (ADB)

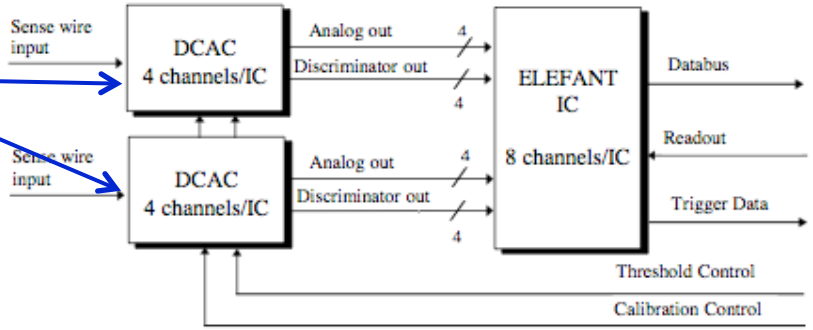
High-bandwidth transimpedance amplifier (input impedance adjusted to terminate the sense wire transmission line impedance) + Discriminator



"DCAC"
Commercial amplifier & calibration

"ELEFANT"
8 channel 6b TDC/ADC ASIC
Buffers 32 15MHz samples/ch on L1A
4 events deep
Generates untriggered waveforms @15MHz

TRIG_MUX FPGA
Stretches untriggered wavet
to 3.7MHz sampling an
serializes 4 channels
onto 1 output stream (15M



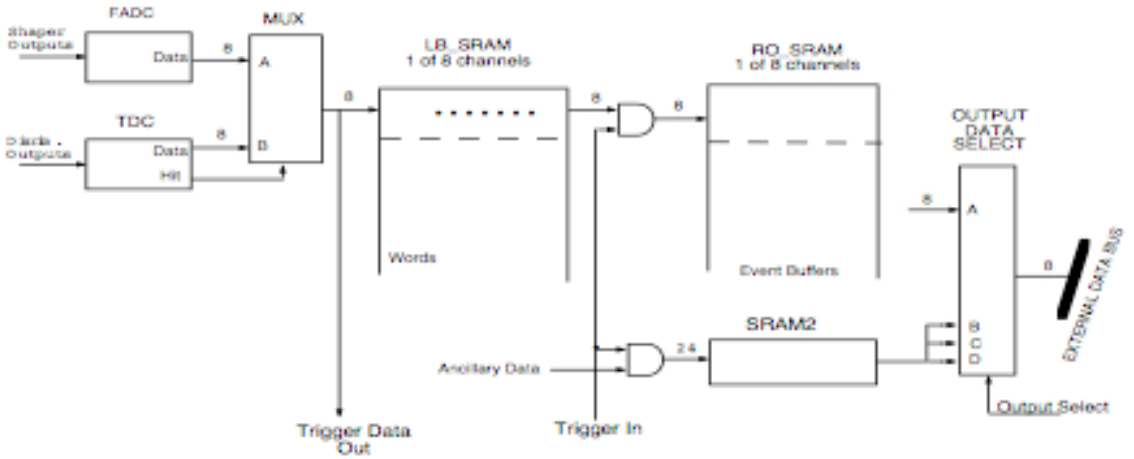
BUFFER
hold data 12.9 µs *(192 sample clock cycle)*

8 complete channels (amplitude + timing)

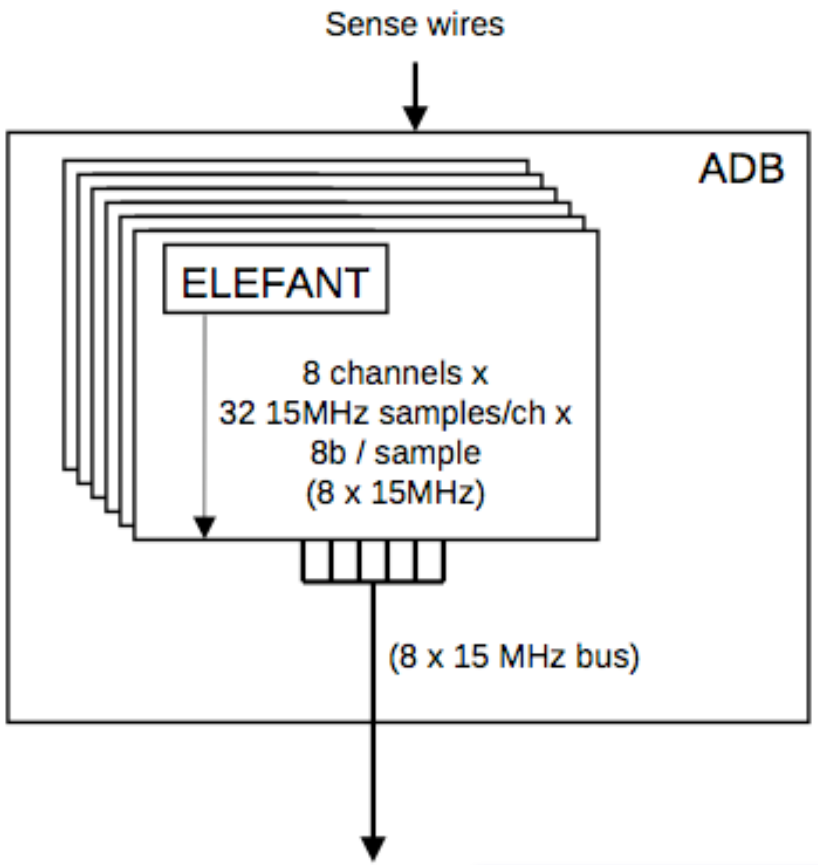
RO BUFFER (4 events)
2.2 µs (32 samples)

8 complete channels (amplitude + timing)

6 bits - 14.875 MHz



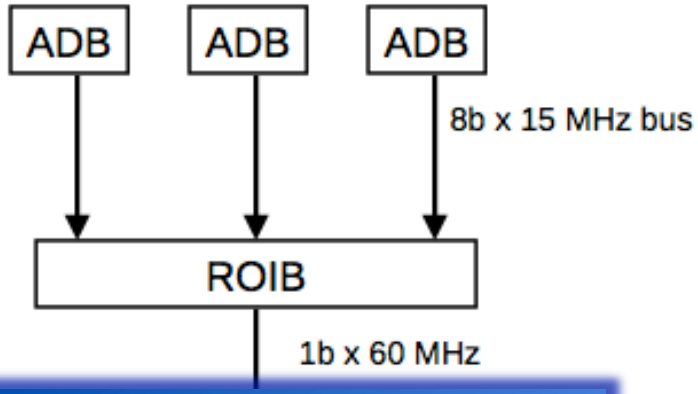
BABAR FEE – ReadOut Interface Board

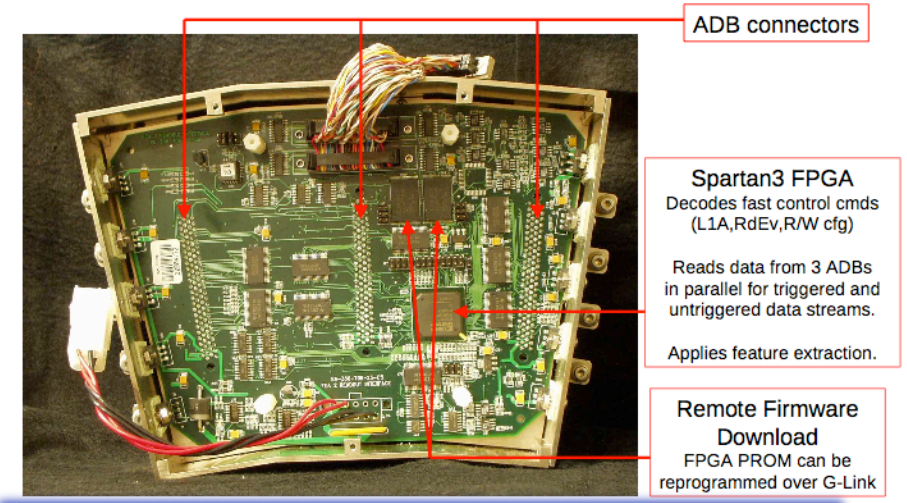


- ELEFANT continuously buffers data for 12 µsec (L1A latency)
- On L1A ELEFANT moves data to event buffer
  - 32 samples/ch x 8 channels
- Event buffers are drained via an 8b 15 MHz bus
- 256 bytes / ADB → 17 µsec + up to 17 µsec overhead
- Number of channels/ADB = 45/48/60 (outer/middle/ inner assemblies)

48 chs → 48 x 32 Bytes ≈ 100 µsec ≈ 10 kHz
(Real BW < 10 kHz because overhead)

BABAR FEE – ReadOut Interface Board





READOUT PROCEDURE

1. Readout ELEFANT chip into local FIFOs
2. After a fixed delay the master data controller starts FIFO data readout
3. Data are sent out on a 2-bit 30 MHz connection to the Data I/O

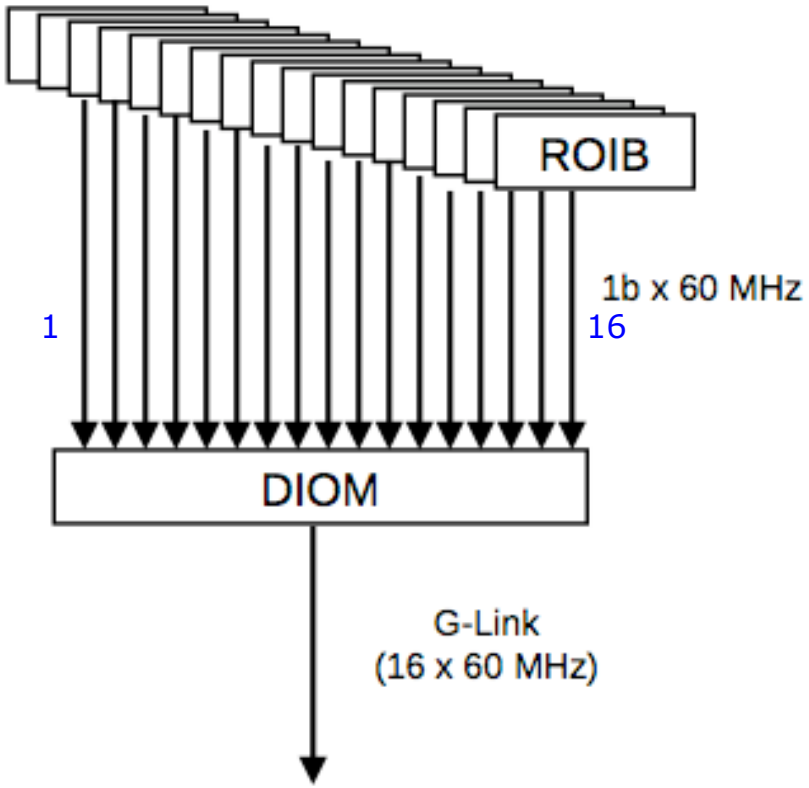
- Decode commands from Fast Control and perform appropriate operation
  - L1 Accept
  - Event Read
  - Sync & Calibration
  - ...
  - Subsystem specific commands
    - ELEFANT IC configuration & calibration
    - ....

Feature EXtraction

Data Reduction: 32 Bytes → 8 Bytes
- 2 Bytes status word
- 2 Bytes charge
- List of 2 Bytes TDC hits (over threshold signals

NO Zero Suppression
48 chs → 48x8 Bytes (average) → 3072 bits @ 60 Mbits/sec ≈ 50 µsec ≈ 20 kHz
(Real BW < 20 kHz because overhead)

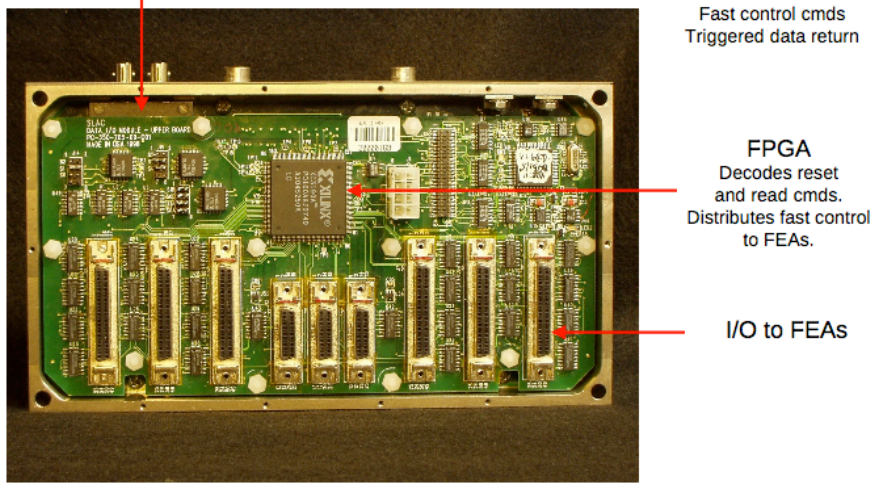
BABAR FEE – Data Input/Output Module (DIOM)



DATA INPUT/OUTPUT MODULE

1. Decode the READ EVENT and propagates it to FEAs
2. ELEFANT chips are readout into local FIFOs
3. After ≈ 20 μs (fixed delay) a GRANT signal is issued for each FEA
4. The FEA begins the synchronous data transfer from internal FIFOs to the G-link

4 Modules

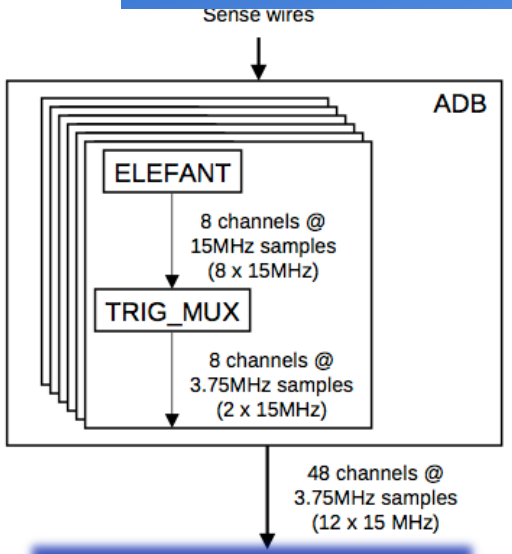


NO Zero Suppression
16 x 60 Mbits/sec → 960 Mbits/sec → manages ROIB DAQ rate (≈ 20 kHz)

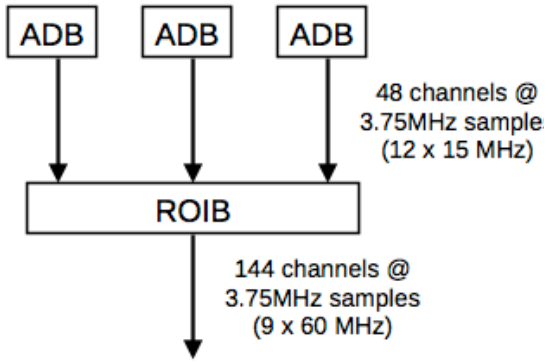
BABAR FEE – DC Trigger

Chain

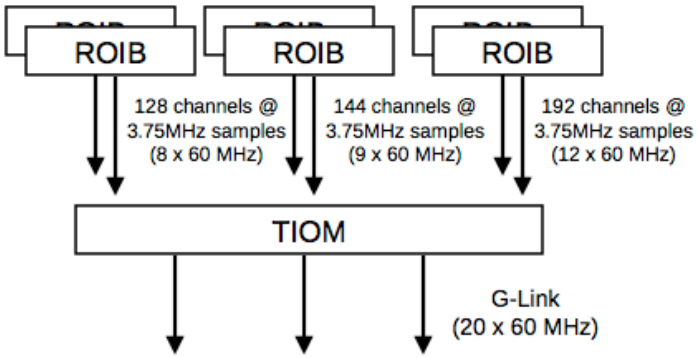
- Trigger interface require hit information from every channel at a trigger rate of 3.7 MHz
- The ELEFANT presents on 8 output pins the status of readout buffer at a sample rate of 14.873 MHz
  - Presence of TDC data in the sampling period or over-threshold signal from ADC
- A dedicated FPGA in ADB board provide down sample of ELEFANT trigger data output (by stretching and multiplexing) to 3.7 MHz and serialized on the ROIB on a 59.5 MHz line.
- 16 data channels are sent out on each 59.5 MHz trigger link to the Trigger Input/Output Module (TIOM).
- The TIOM multiplexes 20 links on a fiber that is sent to the trigger system



48 chs @ 3.75 Mbits/sec → 12.8 µsec ≈ 78 kHz



3.75 Mbits/sec → 38 µsec ≈ 26 kHz



464 chs @ 3.75 Mbits/sec ≈ 1.74 Gbits/sec

OL - SuperB DCH vs BABAR DCH

BaBar DAQ/Trigger numbers

- 2.5 kHz L1 (average) trigger rate @ 10^{34}
- 7104 cells
- ≈ 10% occupancy
- DAQ ≈ 8 bytes/ch (average)
- Trigger ≈ 1 bit/ch @ 3.75 MHz

Super-B DAQ/Trigger numbers

- 150 kHz L1 (average) trigger rate
- ≈ 10000 cells
- ≈ 20% occupancy (1 μs time window)
- DAQ ≈ 8 bytes/ch (average)
- Trigger ≈ 1 bit/ch @ 7 MHz

OL Estimation according to the BW

DAQ → 150×10^{3}(L1 rate)$\times10^{4}$ (N. of cells)$\times0.2$(occupancy)$\times8$(N. of bytes/ev)$\times8$(1 byte = 8 bits) → 19.2 Gbits/sec (average)

TRIGGER → 10^{4} (N. of cells)$\times7\times10^{6}$ → 70 Gbits/sec

OL Estimation according to the BABAR experience

BABAR DAQ/Trigger OL (1.2 Gbits/sec)

DATA
- 4 OL (layout requirement) ≈ 8 X L1 trigger rate requirement)

TRIGGER
- 24 OL

ECS
- Managed by DATA I/O modules (CAN standard)

Super-B DAQ/Trigger OL (2 Gbits/sec)

DATA
- 30 OL (including a x3 safety factor)

TRIGGER
- 35 OL (increase of sampling frequency & channels)

ECS
- 8 OL (layout driven)

FEE architecture – Scenario1

SCENARIO 1

ONLY HV distribution and preamplifier boards located on the end-plate

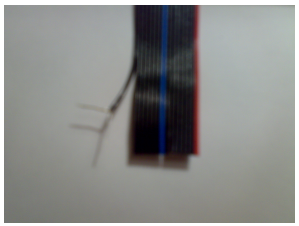
Pros :

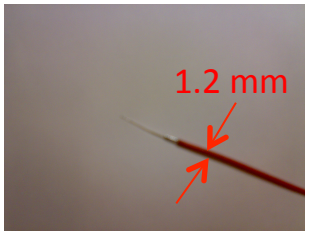
- minimization of the material added to the end-plate
- reduction of the power dissipation on the end plate (no cooling required or low airflow)
- minimization of the radiation environment issue
- possibility of using commercial available devices for data conversion
- Full system reliability

Cons :

- 10k cables required to extract signals (either micro-coax or twisted)

18 mm
12 coax-cables + 2 PS





Material Budget

- HV distribution board and Preamplifier input signals routing
  - 0.5 mm FR4
  - 70 µm copper (not homogeneous)
  - smd components and connectors (not homogeneous)
- Preamplifier boards
  - 0.5 mm FR4
  - 70 µm copper (not homogeneous)
  - smd components and connectors (not homogeneous)
- Cables (coaxial)
  - Shield : 150 µm copper

Min: 1 mm FR4
Max: 1 mm FR4 + 440 µm copper + 3 mm ceramics

FEE components – Scenario2

SCENARIO 2

Full FEE chain located on the end-plate

Pros :

- reduction of the number of connections between DCH and DAQ

Cons :

- two layers of boards plus shielding must be placed on the end-plate with not negligible increase of the material added to the end-plate (shielding is required as digital logic is continuously working for data conversion and serialization)
- power dissipation is increased and cooling is required
- to limit power dissipation dedicated radiation tolerant devices (ASIC) are required and ASIC design is a time consuming and expensive task.
- Power supply cables must delivery more current → bigger sections are required
- Reliability of the full system

Material Budget

- HV distribution board and Preamplifier input signals routing
  - 0.5 mm FR4
  - 70 µm copper (not homogeneous)
  - smd components and connectors (not homogeneous)
- Preamplifier boards
  - 0.5 mm FR4
  - 70 µm copper (not homogeneous)
  - smd components and connectors (not homogeneous)
- ReadOut Board
  - Multi-Layer PCB (8 layers)
    - 1.6 mm FR4
    - 280 µm copper (not homogeneous)
- Concentrators (Data I/O module)
  - Multi-Layer PCB (8 layers)
    - 1.4 mm FR4
    - 280 µm copper (not homogeneous)
- Shield to avoid interference from ReadOut Boards and Concentrators (≈ 300 µm copper)
- Cooling ??? (the thickest part in BABAR)

Min: 2.6 mm FR4 + 280 µm copper
Max: 2.6 mm FR4 + 720 µm copper + 3 mm ceramics + cooling

DCH FEE Power Dissipation & Radiation Environment

BABAR

DCH Power Dissipation

Component	Number	Total Power (W)
Front End Assemblies	48	1300
Data I/O Modules	4	100
Trigger I/O Modules	8	260

→ ≈ 1.7 kW

Radiation Environment

- Spartan 3 XC3S1500 → SEU (neutrons) ≈ 2kHz/cm2 estimated rate → FPGA must be reconfigured

→ 2/days

Material Budget

→ Nobody cares

Super-B (Estimate)

On Detector FEE - Scenario1

- Pd < 300 W * (including some shaping/amplification)
- No cooling required (or low air flush)
- Radiation Environment : low sensitivity (no FPGA)
- Material budget: low

* In KLOE (12k channels) was 100W

On Detector FEE - Scenario2

- Pd ≈ 1.5/2 kW
- Cooling required
- Radiation Environment : large use of FPGA → SEU problems
- Material budget: high

Conclusions

1. BABAR used 4 – 1 Gibits/sec OL for DAQ and 24 – 1.2 Gbits/sec for Trigger @ L1 rate = 2.5kHz
2. Our estimate based on a L1 trigger rate of 150 kHz and 10k DCH is about 30 - 2Gbits/sec OL for DAQ and about 35 - 2Gbits/sec OL for trigger
3. ECS number of links is mainly driven by layout considerations. 4 OL should be enough
4. Power dissipation, radiation environment and material budget are real issues if the full FEE chain will be located on the DCH end-plates