

The Belle II Detector at SuperKEKB

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• General Overview

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K_L detector (KLM) Electromagnetic Calorimeter (ECL)

Particle ID System (PID)

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Central Drift Chamber (CDC)







Silicon Strip detector (SVD) Si-Pixel Detector (PXD)



Super

iest for BSM

Summary & Conclusions



Detector: Baseline Design

Belle T







- Two independent (x and y) layers in one superlayer made of orthogonal scintillator strips with WLS read out
- Photo-detector: avalanche photodiode in Geiger mode (SiPM)
- ~120 strips in one 90° sector • y-strip (max L=280cm, w=25mm) plane ~30000 read out channels Geometrical acceptance > 99% Iron plate x-strip plane 3M mirror. **Optical glue** TiO₂ reflector Aluminum WLS fibre frame Kurary Y1 Scintillator: green photon blue photon to photodetector polysteren + 1.5%PTP + 0.01%POPOP SiPM, e.g. Hamamatsu 676 pixels (20x20µm²) 1.3x1.3 mm²





- Increase of dark current due to neutron flux
- Fake clusters & pile-up noise

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Barrel:
500 ns shaping + 2MHz w.f. sampling.
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Endcap:

rad. hard crystals with short decay time (e.g. pure CsI) + photopentodes 30ns shaping + 43MHz w.f. sampling











Upgrade: Particle Identification





Baseline Design for Barrel PID





Ring imaging with :

- One coordinate with a few mm precision
- Time-of-arrival
- → Excellent time resolution < ~40ps efficient single photon detection in 1.5 T field

Baseline Design for Endcap PID





encouraging beam tests: Ch-photons ~ 14/track angluar res./tr. 4 mrad Position sensitive PD In the B field of 1.5Tesla (HAPD's or SiPM's)



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	Belle	Belle-II
Radius of inner boundary (mm)	77	160
Radius of outer boundary (mm)	880	1096
Radius of inner most sense wire (mm)	88	168
Radius of outer most sense wire (mm)	863	1082
Number of layers	50	58
Number of total sense wires	8400	15104
Effective radius of dE/dx measurement (mm)	752	928
Gas	He-C ₂ H ₆	He-C ₂ H ₆
Diameter of sense wire (µm)	30	30



normal cell: 13.3 x 16 mm²



z-coordinate via standard stereo wire arrangement, charge division planned

New Si System for Belle-II : SuperSVD



Layer	# Ladders	Rect. Sensors [50µm]	Rect. Sensors [75µm]	Wedge Sensors	APVs
6	17	0	68	17	850
5	14	0	42	14	560
4	10	0	20	10	300
3	8	16	0	0	192
Sum:	49	16	130	41	1902

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Super

uest for BSA

Chip on Sensor: The Origami Concept (SVD)

zylon rib



- Strips of bottom side are • connected by flex fanouts wrapped around the edge
- All readout chips are aligned \rightarrow single cooling pipe
- Shortest possible connections • \rightarrow high signal-to-noise ratio



3-layer kapton hybrid

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Super

cooling pipe

SVD Mechanics and Material Budget









Gen: Charged Particles (e[±], μ[±], π[±], K[±], p[±])



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p-channel FET on a completely depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate ("internal gate")

Signal electrons accumulate in the internal gate and modulate the transistor current $(g_q \sim 400 \text{ pA/e}^-)$

Accumulated charge can be removed by a clear contact ("reset")

Fully depleted:

large signal, fast signal collection

Small capacitance, internal amplification — low noise

Depleted p-channel FET



Transistor on only during readout: low power



Thinning Technology



sensor wafer	handle wafer			
1. implant backside on sensor wafer	2. bond sensor wafer to handle wafer	3. thin sensor side to desired thickness	4. process DEPFETs on top	5. structure resist, etch backside up to oxide/implant

- Sensor wafer bonded on "handle" wafer.
- Rigid frame for handling and mechanical stiffness
- 50 μm thickness has been produced
- Samples of 10x1.3 cm² & frame of 1 & 3 mm width
- Electrical properties OK (diodes)







Row wise read-out ("rolling shutter")

- select row with external gate read current, clear DEPFET, read current again
 - \rightarrow the difference is the signal
- only one row active → low power consumption
- two different auxiliary ASICs needed



→ DCD (drain current digitizer)







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DHP = Data Handling Processor (zero-suppression)

DHH = Data Handling Hybrid (buffer readout, slow control etc.)









Expected Performance with PXD









Near-term plan

- Detector proposals (by Dec. 2009)
- Decisions on technology choices (Barrel PID configuration/photon detector, ECL endcap crystalls and photosensors)
- TDR by March 2010













2004.06: LoI for SuperKEKB 2008.01: KEK Roadmap \rightarrow identified as high priority project at KEK 2008.12: New collaboration (Belle-II) officially formed

✤ 13 countries/region, 43 institutes, ~300 members

Organization:

Executive Board (Chair: H. Aihara) Spokesperson: P. Križan Project manager: M. Yamauchi

Institutional Board (Chair: L. Piilonen)

Physics coordinator: B. Golob

Technical coordinator: Y. Ushiroda

Software /computing coordinators: T. Hara / T. Kuhr

2009.11: 4th Open Collaboration Meeting



European Participation in Belle-II

- •Austria: HEPHY (Vienna)
- •Czech republic: Charles University in Prague
- •Germany: U. Bonn, KIT Karlsruhe, MPI Munich, U. Giessen
- •Poland: INP Krakow
- •Russia: ITEP (Moscow), BINP (Novosibirsk),
- •Slovenia: J. Stefan Institute, U. Ljubljana, U. Maribor, U. Nova Gorica

Sizeable fraction of the collaboration: in total 100 collaborators out of 287!



Members of the DEPFET Collaboration:

- + Heidelberg, Göttingen
- + 5 Spanish groups





- SuperKEKB and Belle-II are priorities of KEK
- The Japanese government has allocated 32 oku-yen (32 M\$) for upgrade R&D in FY 2009, as a part of its economic stimulus package. This is considered as a very important sign in Japan.
- KEK has submitted to the Ministry of education, science, and technology (MEXT) a budget request for FY 2010 and beyond for 350 M\$ for the construction of SuperKEKB. MEXT submitted a request for the upgrade budget to the Ministry of finance.
- The Japanese government is currently reviewing all major projects. The decision concerning SuperKEKB and Belle-II is expected by the end of this year.
- Several non-Japanese funding agencies have already allocated sizable funds for the upgrade.





- B factories have proven to be an excellent tool for flavour physics, with reliable long term operation, constant improvement of the performance.
- Major upgrade at KEK in 2010-13 \rightarrow Super B factory, L x 40
- The Belle-II detector is essentially a new project, all components have to be replaced, options to be frozen in the next few months
- The project has a strong European participation (about 1/3!)
- A physics reach update is being prepared to be made public soon
- Expect a new, exciting era of discoveries, complementary to LHC





Backup























Original Collaboration: DEPFET pixel detector @ ILC (since 2002) now: Unite efforts to deliver a REAL PXD by 2013 for Belle-II

University of Barcelona, Spain CNM, Barcelona, Spain Universitat Ramon Llull, Barcelona, Spain Bonn University, Germany Heidelberg University, Germany Giessen University, Germany Goettingen University, Germany Karlsruhe University, Germany IFJ PAN, Krakow, Poland MPI Munich, Germany Charles University, Prague, Czech Republic University of Santiago de Compostela, Spain IFIC, Valencia, Spain

with important help from Hawaii, KEK, Vienna

DEPFET@Belle-II

Management:

• IB- Board

- Project Leader
 C. Kiesling
- Technical Coord.
 H.-G. Moser
- Integration Coordinator Shuji Tanaka (KEK)





Sensors:	pixel geometry -> parameter studies prototyping, radiation hardness inter-connections, thinning technology
Read-out ASICs:	Drain Current Digitizer chip (DCD): prototyping Switcher: rad-hard design
DHP & DHH: :	Zero-suppr: 400 Gpx/s -> 2 Gpx/s (trigger, occ) -> 1.6 Gb/s per half module
DAQ:	~200 Gb/s total (zero-suppressed!)
Mechanics, Cooling:	Mounting, thermal coupling, alignment,
Test Procedures:	System / beam tests



Prototype Sensors for PXD





4 big chips

- half modules
- bump bonded
- 4 different design options
- 2 inner
- 2 outer

8 standard BB (128 x 16) same design options as for the big chips (2 of each)

85 standard WireBonded (128 x 8 or 16)
8 of them on thin oxide
6 ILC (128x128)
2 of them on thin oxide
9 mini matrices
2 of them on thin oxide
4 single trans. Chips
24 DEPFET pairs with varied channel and clear gate geometry

Test structures







outer sensor must be in two parts (limitation of wafer size)













- debugging ongoing incl. development and testing of FPGA-to-FPGA communication a.) onboard b.) board-to-board
 - (via backplane) (via
- preparation for beamtime (readout with 1 ATCA shelf) at HADES test experiment at GSI in 2010
- main priority right now: trigger and event builder algorithms for HADES







Hough

transform

SVD

Claudio Heller (MPI)

 2D pattern recognition in z-r-plane using SVD data: Hough-transform with fast peak finding algorithm

•SVD hits are divided into 3 x 40 overlapping sectors in r-phi rotated with $\Delta \Phi = 9^{\circ}$

 different shaped sectors for low momentum particles and nearly straight tracks in r-phi-



r-axis





