"Overview of the readout system for the TDCpix ASICs in the NA62 Gigatracker detector"

"Overview of the readout system for the TDCpix ASICs in the NA62 Gigatracker detector"

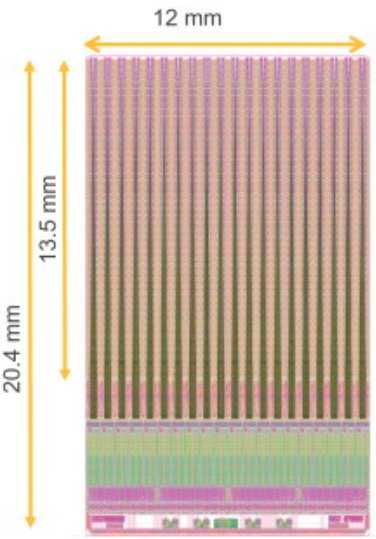
The goal of this presentation is to give a concise overview of a state-of-the-art device for the readout of silicon pixel detectors, the TDPpix ASIC developed at CERN for NA62, and of the readout system developed for it by the INFN / Dipartimento di Fisica e Scienze della Terra for the NA62 GigaTracker detector in which the TDCpix are installed.

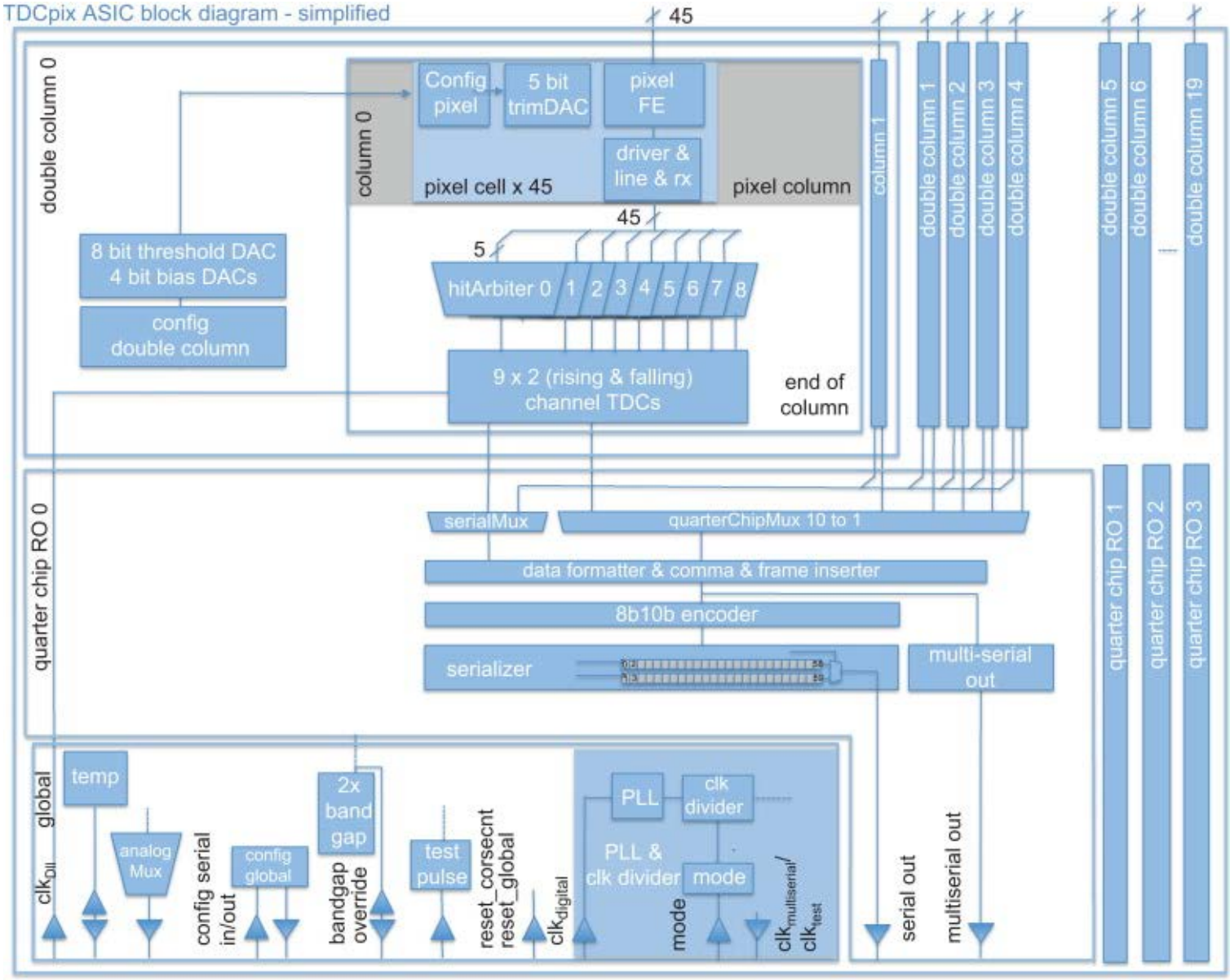
The connection with this workshop lies in the fact that assemblies based on TDCpix ASICs could be used in this project to characterize the high performance pixel detectors object of this research project while the dedicated ASIC is being developed.

Summary:

- TDCpix overview
- The GTKRO (GigaTracker Read Out) card
- The TDCpix single chip assembly
- The minimal DAQ system for the TDCpix single chip assembly

- TDCpix overview





The TDCpix readout ASIC: A 75 ps resolution timing front-end for the NA62 Gigatracker hybrid pixel detector
NIM A, Volume 732, 21 December 2013, Pages 511–514; Vienna Conference on Instrumentation 2013
A. Kluge, G. Aglieri Rinella, S. Bonacini, P. Jarron, J. Kaplon, M. Morel, M. Noy, L. Perktold, K. Poltorak

- TDCpix overview

G. Aglieri Rinella et al. / Physics Procedia 37 (2012) 1608 – 1617

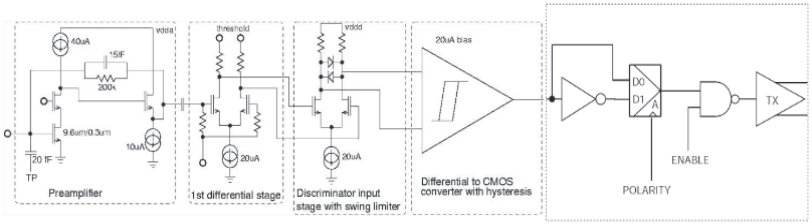
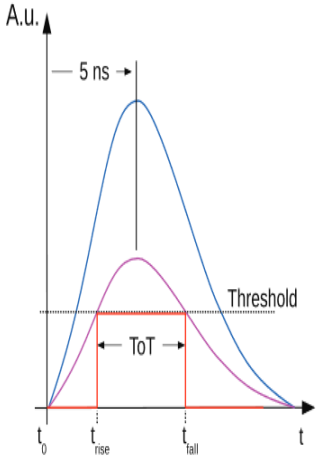


Fig. 3: Block diagram of a pixel cell of the TDCpix.

Dynamic range	0.6-10 fC/3600-60000 *e*
Gain	75 mV/fC
Peaking time	5 ns
ENC (no sensor)	130 *e*
FE consumption	130 μA (56%)
TX line driver consumption	100 μA (44%)

Table 1: Main electrical characteristics of the front-end pixel channel.



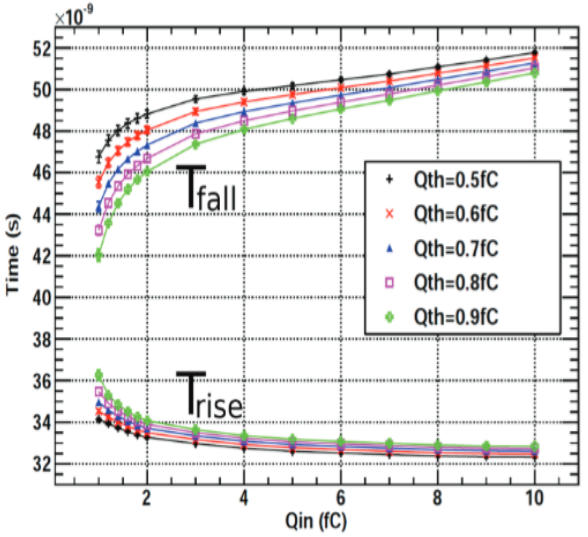


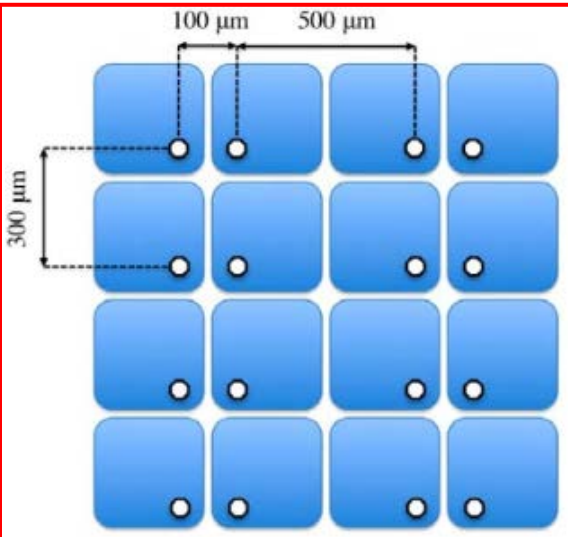
Fig. 5: Measured timings of the leading and trailing edges as a function of input charge.

Measurements with laser pulses showed that the timing resolution, including the time-walk correction by the ToT technique, is better than 75 ps rms when the pulse shapes are constant and for charges larger than 2 fC. The overall timing performance of the prototype assemblies with particles in a beam test is better than 175 ps rms when a bias voltage larger than 300 V is applied to the 200 μm thick sensor. The difference between the timing uncertainty with constant shape pulses and beam particles is linked to the mechanisms of charge generation and signal induction in the sensor. It derives from the fluctuation of the shape of the sensor current pulses due to the random position of the particle hit and to the randomness of the density of the charge carriers released across the sensor thickness.

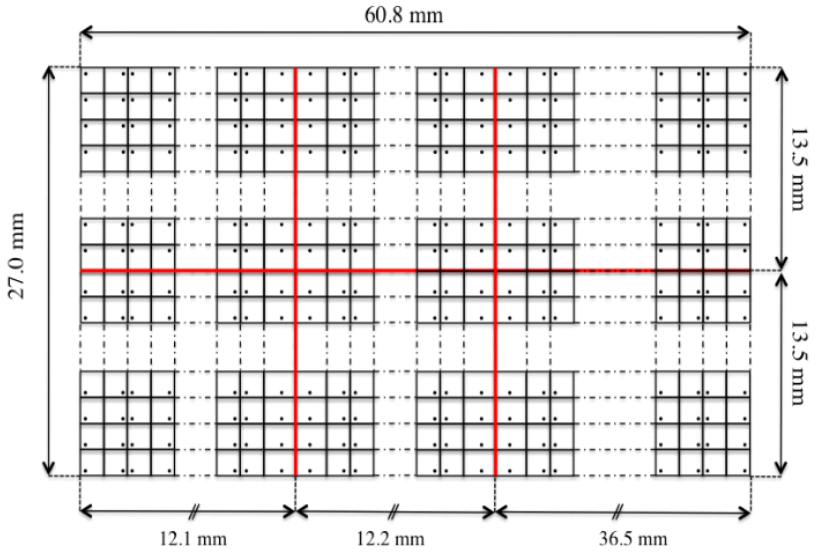
The TDCpix Readout ASIC: A 75 ps Resolution Timing Front-End for the Gigatracker of the NA62 Experiment
G. Aglieri Rinella, M. Fiorini, P. Jarron, J. Kaplon, A. Kluge, E. Martin, M. Morel, M. Noy, L. Perktold, K. Poltorak (CERN)
Phys.Procedia 37 (2012) 1608-1617

- TDCpix overview

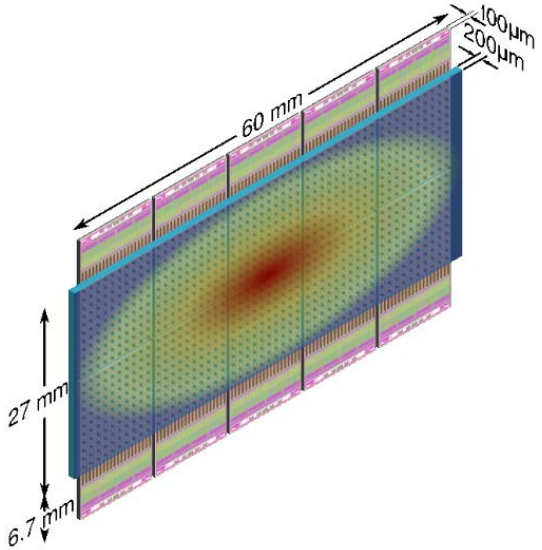
From NA62 TDR

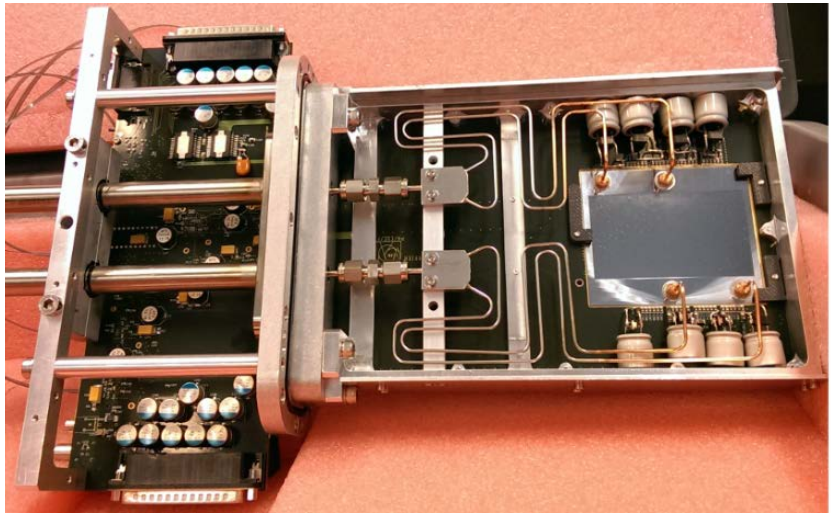


Bump pads arrangement scheme.



Schematic layout of the full-size sensor. Enlarged pixel cells (300 µm x 400 µm) are put in the border region between neighboring read-out chips.

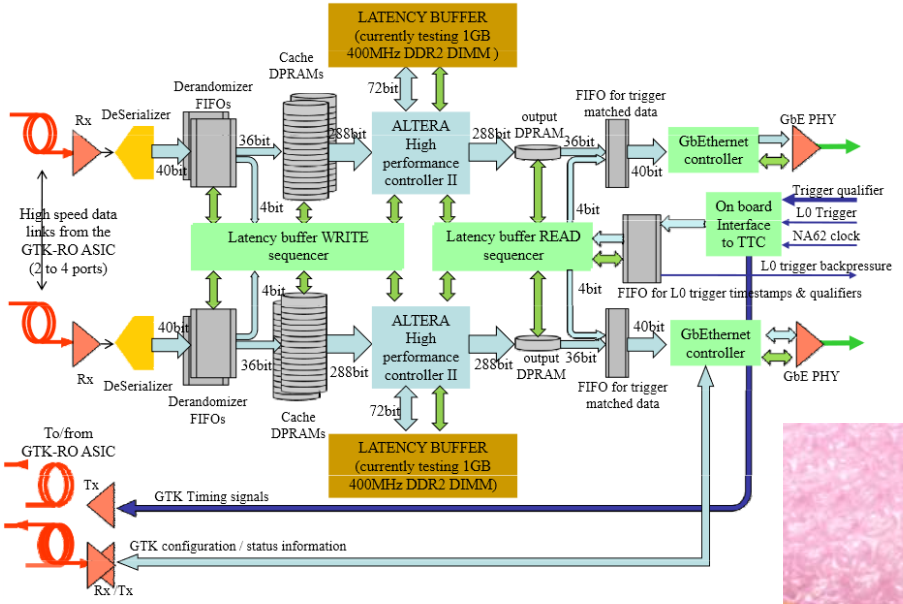




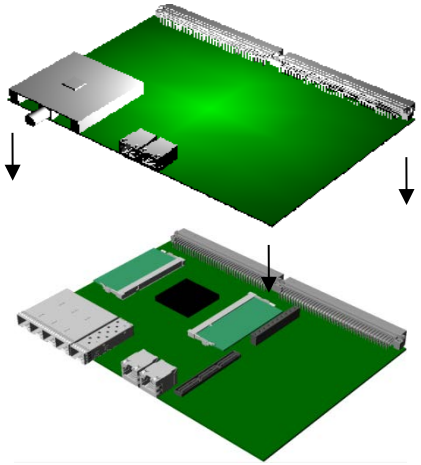
The NA62 GigaTracker
Mathieu Perrin-Terrin
24th International Workshop on Vertex Detector -VERTEX2015, 1-5 June 2015 Santa Fe, New Mexico, USA

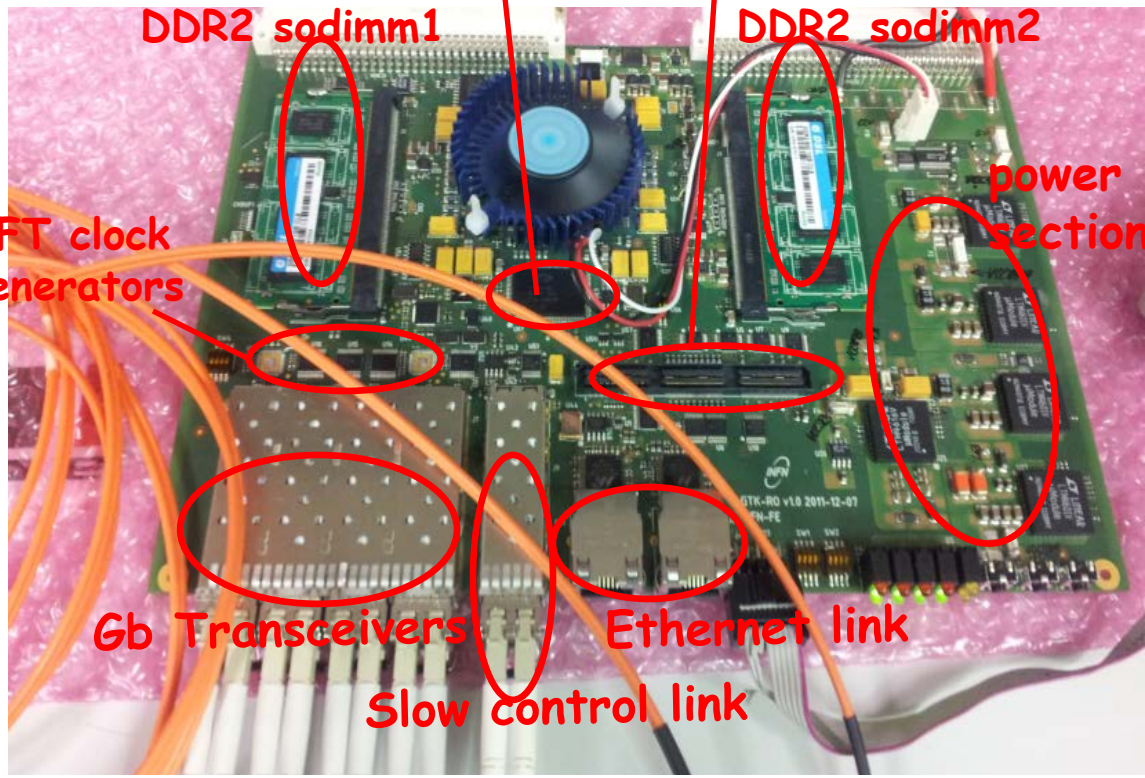
Figure 2: The TDCPix assembly is composed of a 60.8mm×27mm sensor bump-bonded onto 5×2 TDCPix chips. The chip digital and time-to-digital converters logic is located in the 6.7 mm extending outside the sensor.

- The GTKRO (GigaTracker Read Out) card

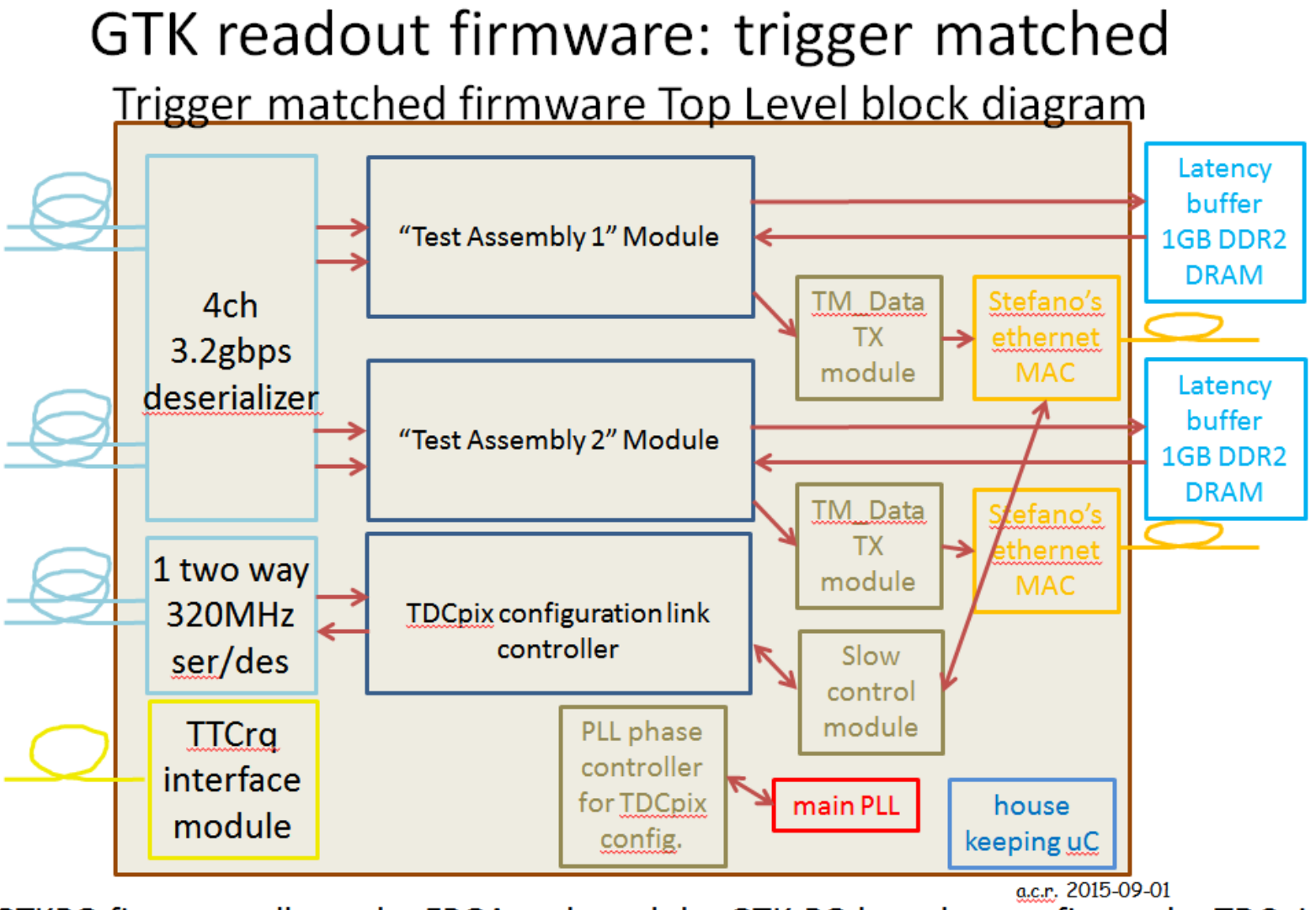


HSMC port to GTK-TTC daughter card





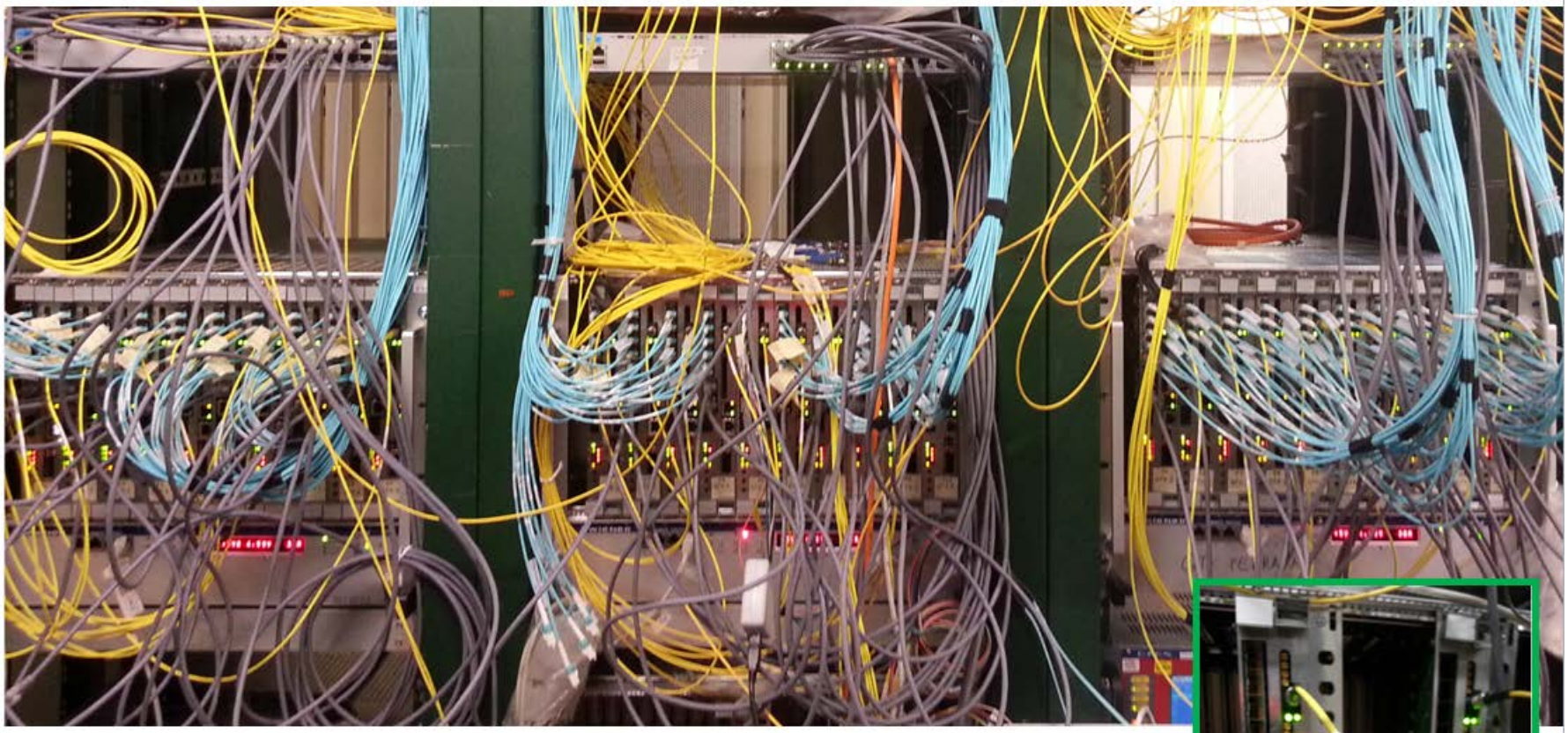
- The GTKRO (GigaTracker Read Out) card



The GTKRO firmware allows the FPGA on board the GTK-RO board to configure the TDCpix controlled by it and to collects its output data, storing it into the DRAM buffer and retrieving it when required by the trigger received through the TTCrq

- The GTKRO (GigaTracker Read Out) card

GTK readout hardware



- The GTK_RO hardware has been delivered for the start of the 2015 run. The readout boards are equipped with the final TTC_rq interface and the timing to the Gigatracker detectors is provided by the final GTK_TTC unit (one spare is also installed and used to supply timing to the single chip assembly)

Angelo Cotta Ramusino INFN-FE, for GTK_WG meeting, Prague 2015-09-01

- The TDCpix single chip assembly

The TDCPix may be operated through a small set of signals:

- DIG_CLK: (currently set at 8x the bunch crossing frequency of 40.08MHz) it is the clock for the TDCpix synchronous serial configuration link (see next slide)
- CONF_IN: it is input to the TDCpix synchronous serial configuration link
- CONF_OUT: it is output from the TDCpix synchronous serial configuration link
- DLL_CLK: (currently set at 8x the bunch crossing frequency of 40.08MHz) it is the clock for the TDCpix TDC units (potentially uncorrelated to the DIG_CLK signal)
- CFC_Rst: (Coarse Frame Counter Reset) it is the reset signal for the TDC units and the downstream processing chain
- T_PULSE

Optical fiber links are used in NA62 to connect the TDCpix of the Gigatracker assembly to the GTK-RO cards.

Single chip assemblies, some of which equipped with a silicon pixel detector bonded to the TDCpix, have been prepared by the designer team for preliminary testing, along with a dedicated readout system based on a Xilinx FPGA (Matt Noy, CERN).

The (unbonded) assemblies are of potential interest for the 4D Tracking project.

- The TDCpix single chip assembly

As the ASIC will be placed in a relatively harsh radiation environment, all state and configuration registers have been triplicated. In the end of column region, the schemes use free running clocks, whereas in the pixel matrix, a combinatorial SEU error indicator is propagated to the end of column region, where it can be monitored by the off detector electronics.

The TDCpix chip was designed in a 130 *nm* commercial CMOS process, and manufactured during the latter part of 2013. Chips became available for testing at the beginning of December 2013 and have been under test since January 2014. A photo of the chip bonded to the test system is shown in Figure 2. No bugs have been detected so far and a re-spin of the design is currently not anticipated. Consequently, sensor assemblies are being bump bonded at the time of writing and delivery is expected at the end of June 2014.

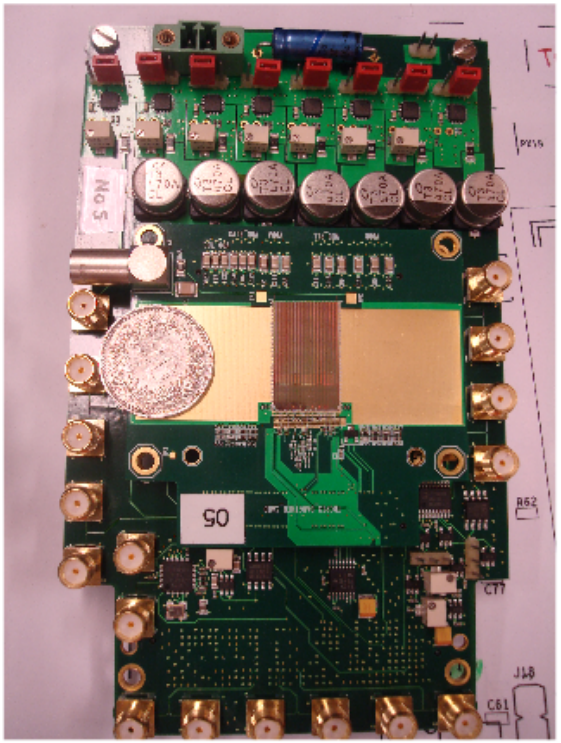
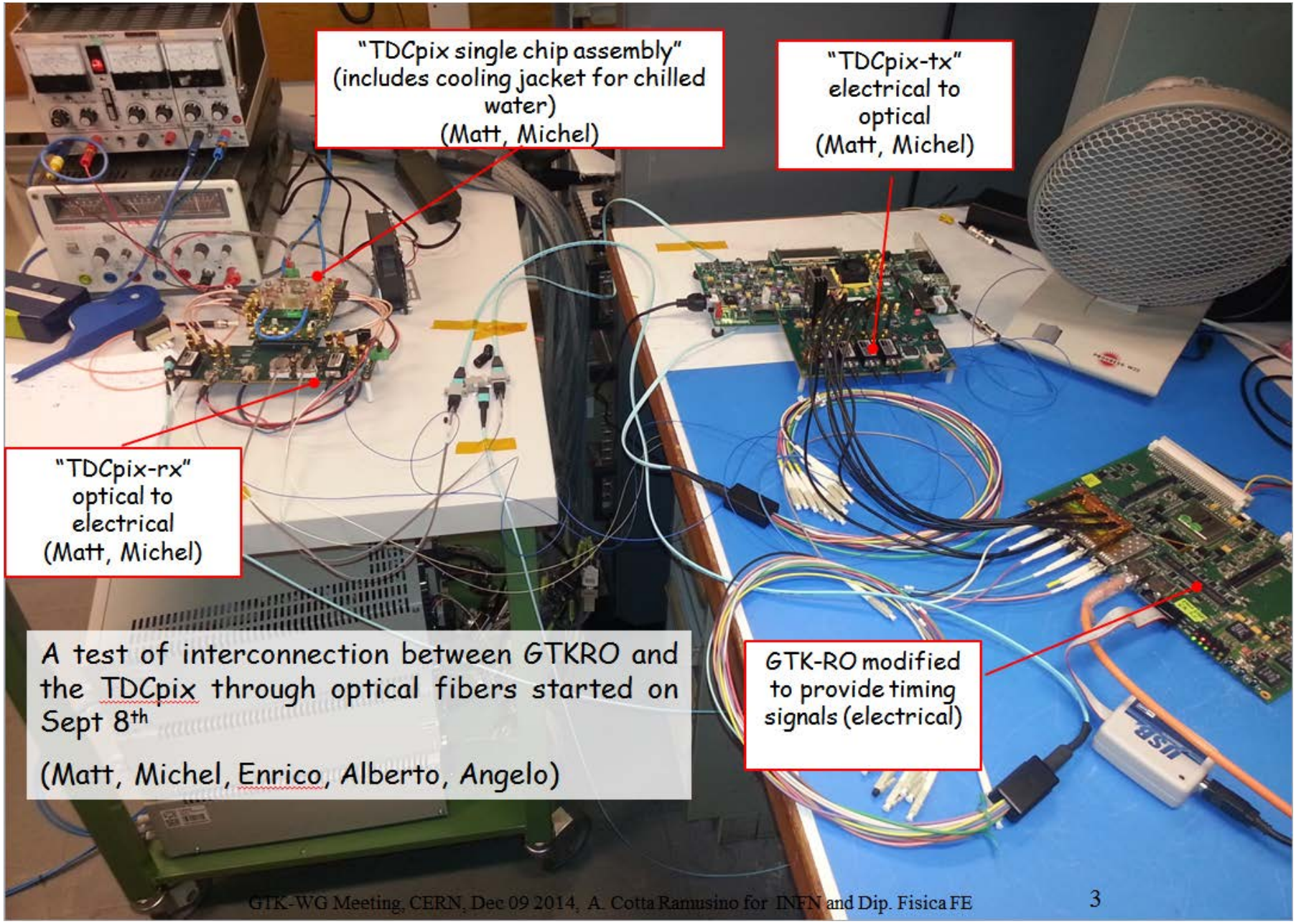


Figure 2: The TDCPix Chip bonded to the test card.

The TDCPix ASIC: Tracking for the NA62 GigaTracker
M. Noy, G. Aglieri Rinella, S. Bonacini, J. Kaplon, A. Kluge, M. Morel, L. Perktold, K. Poltorak
Technology and Instrumentation in Particle Physics 2014, 2-6 June, 2014, Amsterdam, the Netherlands

- The minimal (GTK-RO based) DAQ system for the TDCpix single chip assembly



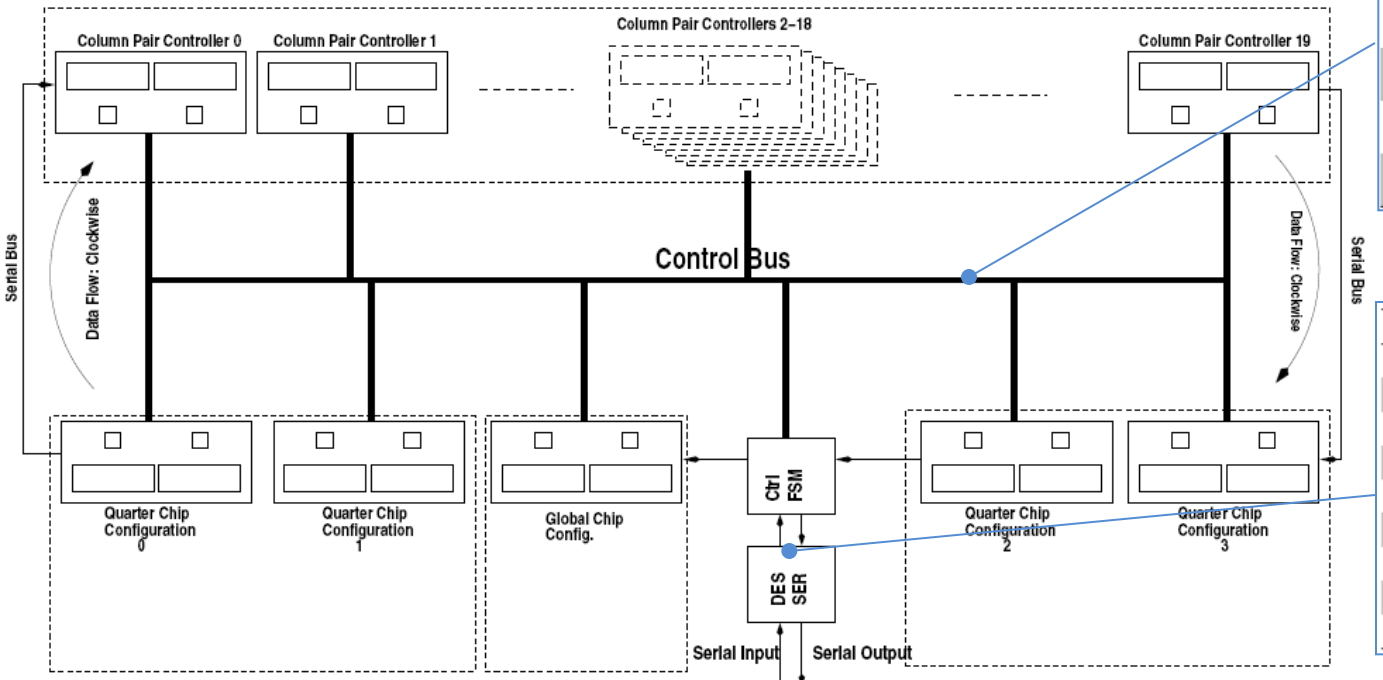
- The minimal (GTK-RO based) DAQ system for the TDCpix single chip assembly

Shown in the previous picture are some of the elements needed to setup a DAQ system exploiting the GTK-RO card for reading one TDCpix single chip assembly eventually bonded to the candidate detector for the 4D Tracking project:

- the TDCpix single chip assembly (CERN) with the ancillary:
    - "TDCpix-tx" and "TDCpix-tx" board (CERN)
    - water chiller (not shown), providing refrigeration to the TDCpix assembly
- One GTK-RO mother board modified to provide the LVDS signals DIG_CLK, DLL_CLK, CFC_RST and T_PULSE converted by the "TDCpix-tx"
- an host PC (not shown) running the configuration and DAQ software
- ancillary instrumentation and daughter cards are needed to synchronize the operation of more GTK-RO if needed (as in a beam test for instance)

- Extra slides:

From: "The TDCPix Design Manual", v. 1.2, 24 Feb 2013):
" The main configuration block (tdcpix_config_block) through which all configuration functions are accessed exists as one monolithic block that spans almost the whole width of the chip, leaving 50um on either side for test signals to be passed. The block is 500um high and occupies metal layers M1, M2 and M3.
Within this block the configuration is organised into several logically distinct components, listed below:
•the interface to the outside world;
•main loop controller state machine and control loop;
•global chip configuration;
•quarter chip configuration;
•column pair configuration;"



Signal	Name	Function
SRST	Synchronous Reset	Resets all registers to '0'.
SCLK	System Clock	Loop system clock $F_{SCLK} = F_{clk-dig}/4$.
PLF	Parallel Load Forwards	Loads data from the loop shift register to the storage register.
PLB	Parallel Load Backwards	Loads data into the loop shift register in combination with SSE.
SSE0	Data Serial Shift Enable	Shifts data around the loop shift register.
SSE1	Bypass Serial Shift Enable	Shifts data around the bypass shift register.

Bit	Symbol	Name
0	SD0	Serial Datum 0
1	SD1	Serial Datum 1
2	SS0	Serial Shift Enable 0
3	SS1	Serial Shift Enable 1
4	PLB	Parallel Load Backwards
5	PLF	Parallel Load Forwards
6	SAS	Serial Array Select
7	SRST	Synchronous Reset
8	K	K-Code Indicator

Fig. 1 An overview of the control loop showing the individual blocks, the order in which they are linked together to form the loop, and the position of the control state machine (Ctrl FSM). The control bus is also shown, broadcast to all slave block. (from: "The TDCPix Design Manual", v. 1.2, 24 Feb 2013)