Elettronica CMOS 65 nm

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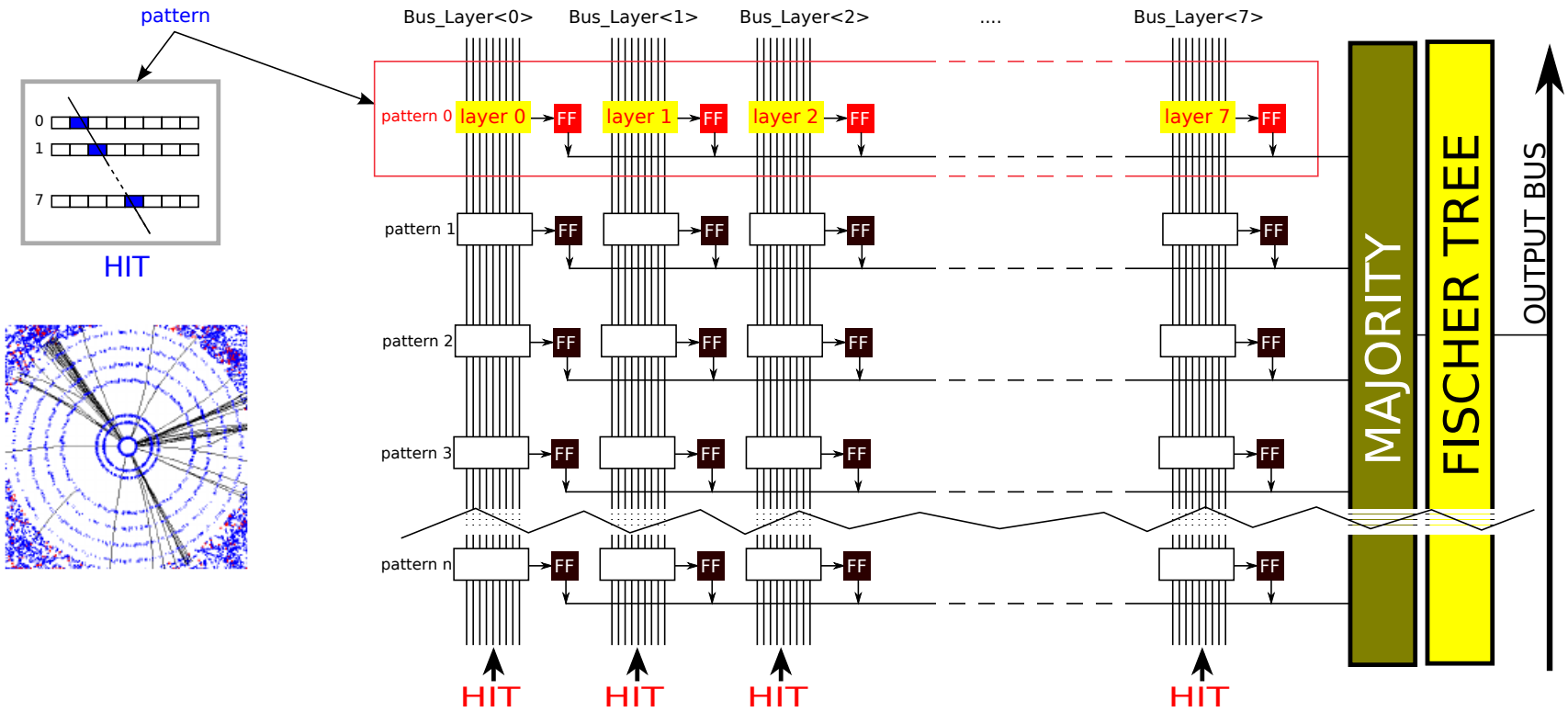
UNIVERSITÀ DEGLI STUDI
DI MILANO

Bologna, June 2016

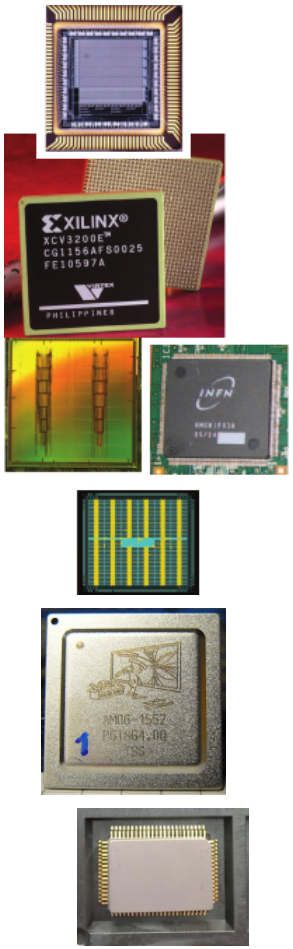
Overview

The Associative Memory working principle



- Small Content-Addressable Memory (CAM) cell for each bus and for each pattern
- The CAM cell compares its own content with the hits received
- Matching result (1 or 0) is stored into a Flip-flop (FF)
- Partial matches are analyzed by the majority logic and compared to the desired threshold
- A priority encoder reads the matched patterns in order

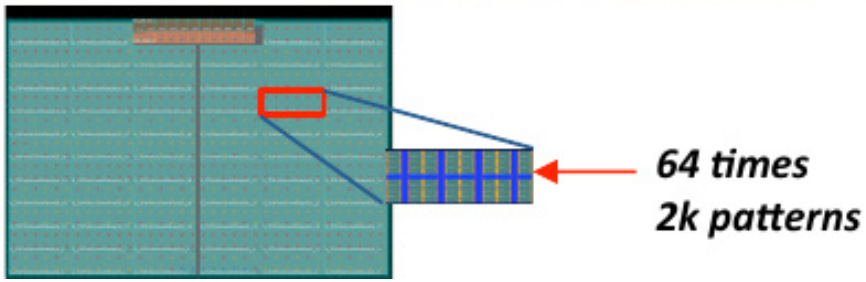
AM Chip History



Vers.	*Design*	*Tech.*	*Area*	*Patterns*	*Package*
1	Full custom	700 nm		128	QFP
2	FPGA	350 nm		128	QFP
3	Std cells	180 nm	100 mm^2	5 k	QFP
4	Std cells + Full custom	65 nm	14 mm^2	8 k	QFP
mini-5	Std cells + Full custom	65 nm	4 mm^2	0,5 k	QFP
5	+ IP blocks		12 mm^2	3 k	BGA
6	Std cells + Full custom + IP blocks	65 nm	168 mm^2	128 k	BGA
7a	**Full custom**	**28 nm**	**0,6 mm^2**	**2,3 k**	**CQFP**
7b	**Full custom + Std cells**		**9,7 mm^2**	**38 k**	**SIP BGA**

blue = under design (figures are estimated)

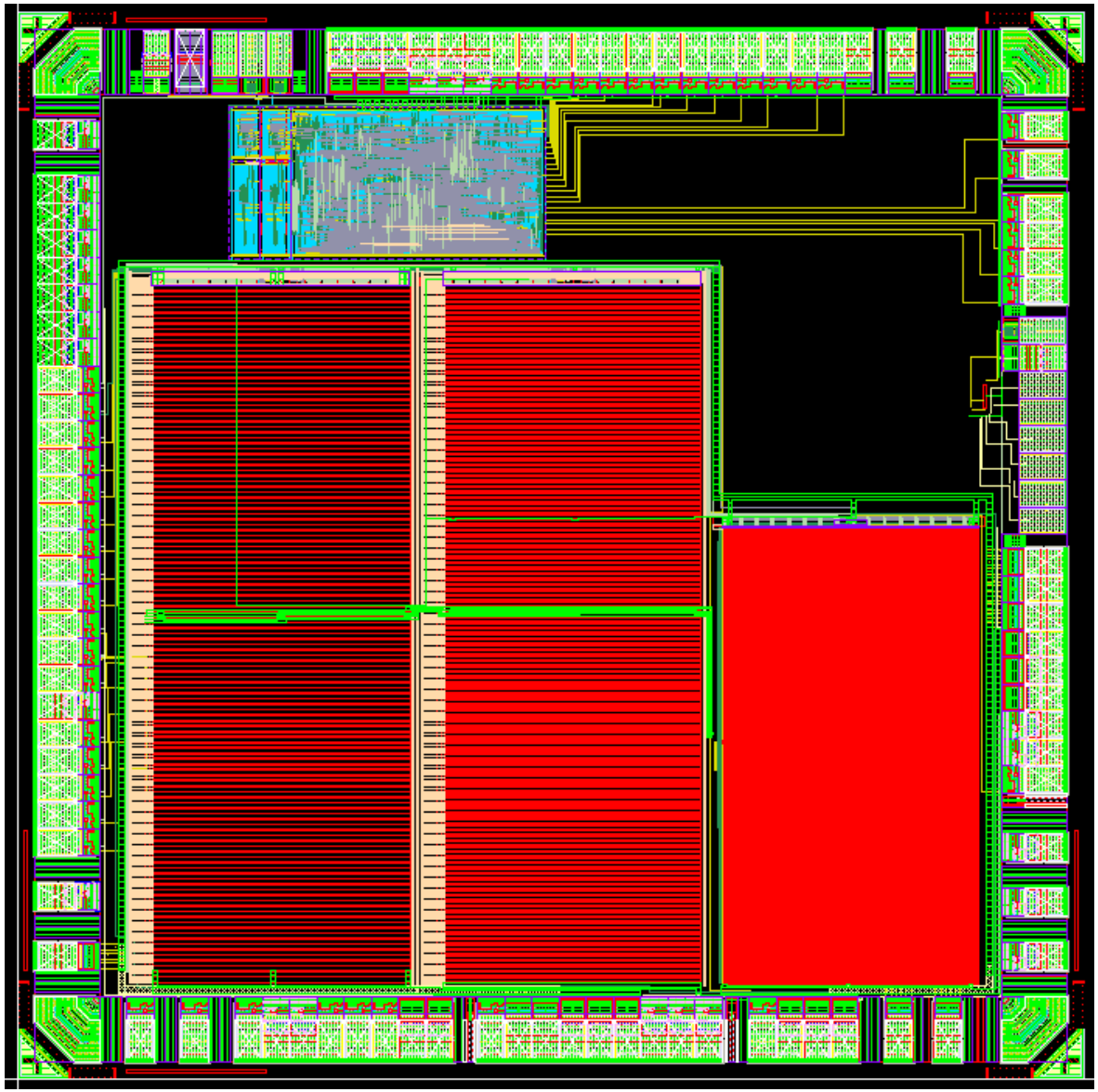
The AM06 Chip



AM06 is a **large** silicon chip in TSMC CMOS 65 nm technology:

- 168 mm^2
- 421 M transistors
- 64 blocks, each of them containing 2 kbit of Associative Memory (AM), designed with full-custom approach and employing a new AM cell (XORAM) specifically optimized for FTK
- SERDES (serializer/deserializer) IP blocks from Silicon Creations, for serial I/O at 2 Gbit/s
- Standard cell 'glue' logic, JTAG interface, and BIST (CRC)

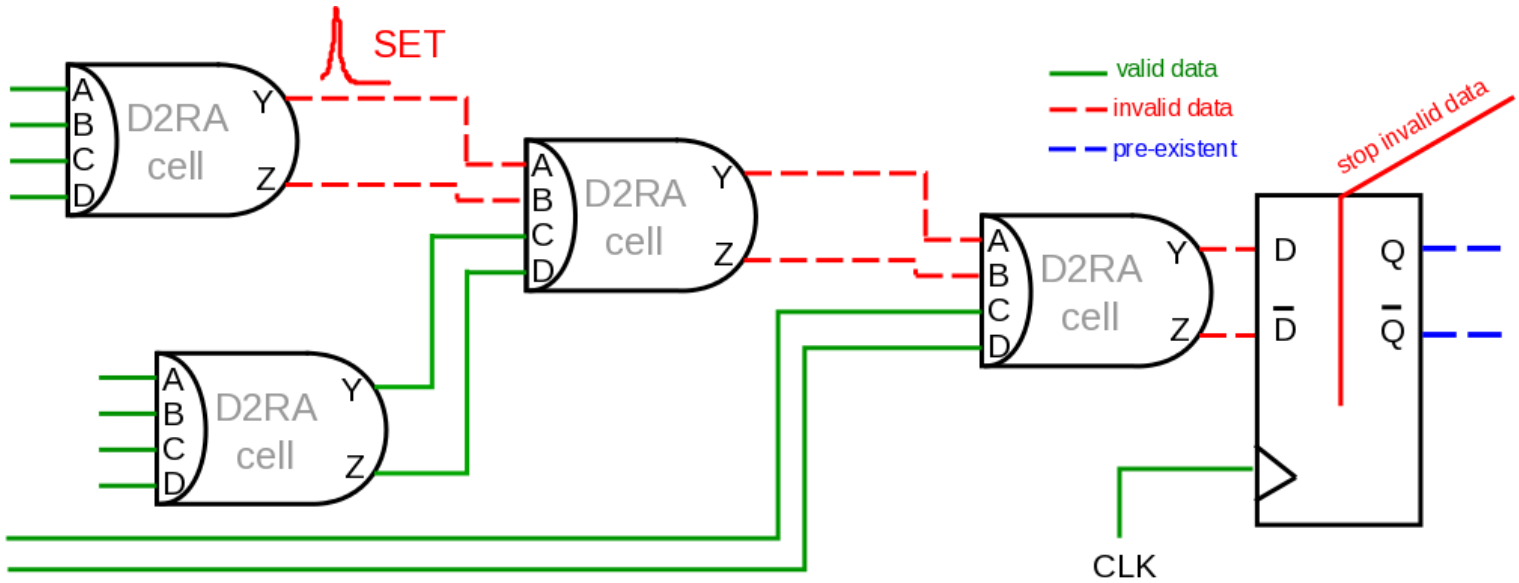
CHIPIX65 1st demonstrator chip



Layout:
3 256 $\times$ 256 SRAM arrays based on DICE (Dual Interlocked CEll) + other cells

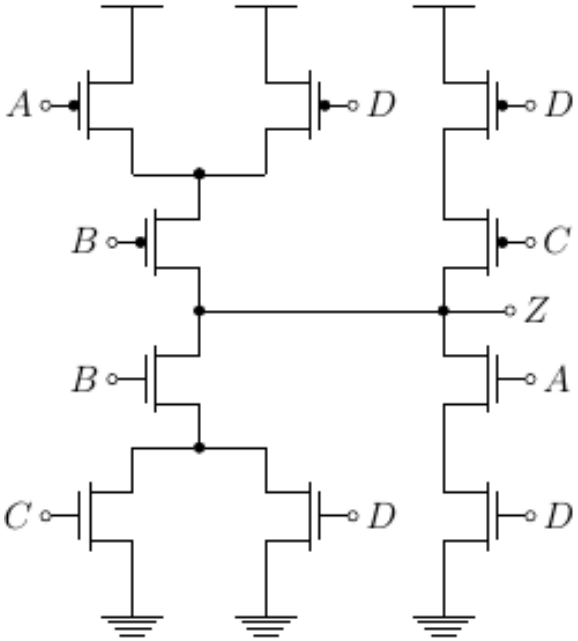
D2RA: Double-Rail Redundant Approach

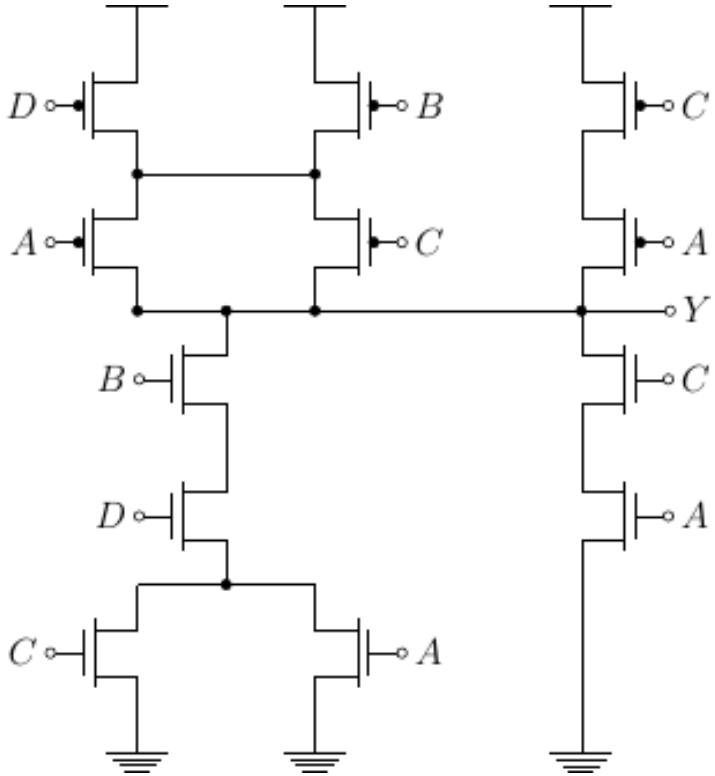
Idea: uso di logica ridondante con bit e bit negato



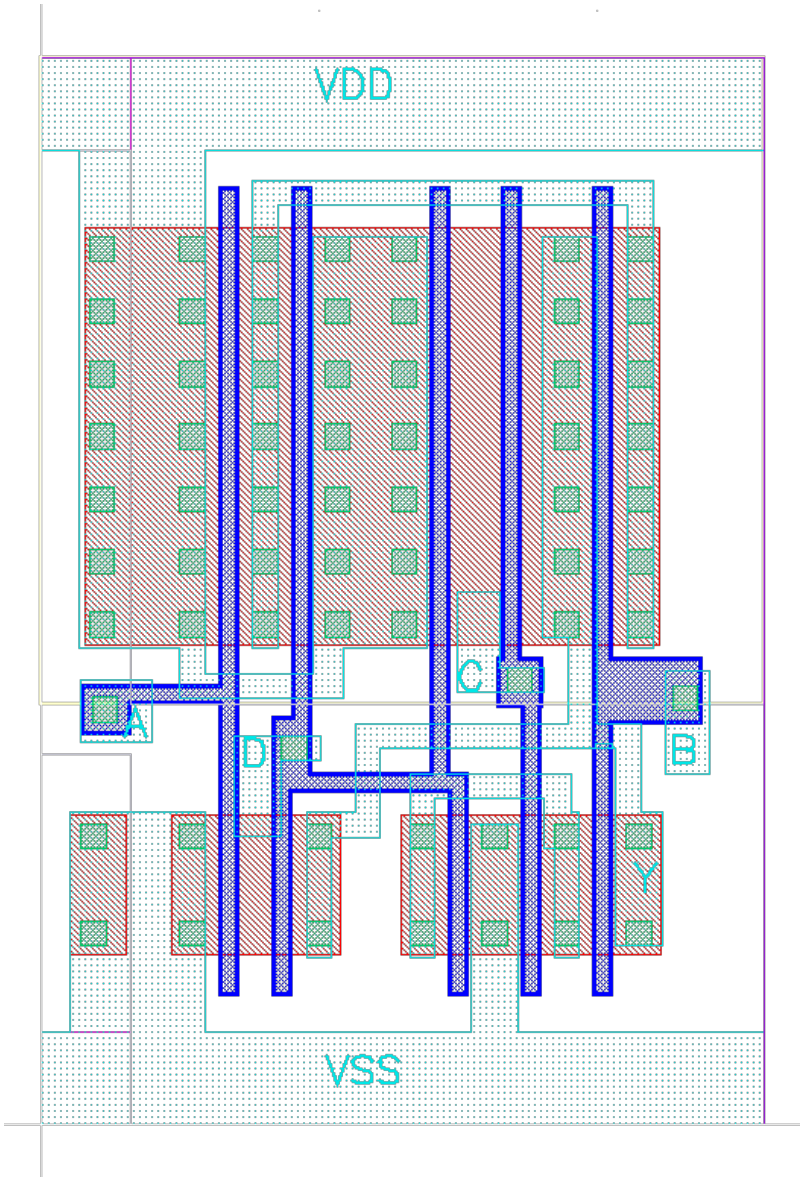
V. Ciriani, L. Frontini, V. Liberali, S. Shojaii, A. Stabile, G. Trucco: "Radiation-tolerant standard cell synthesis using double-rail redundant approach", in *Proc. of Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Sept. 2014, `http://dx.doi.org/10.1109/ICECS.2014.7050063`

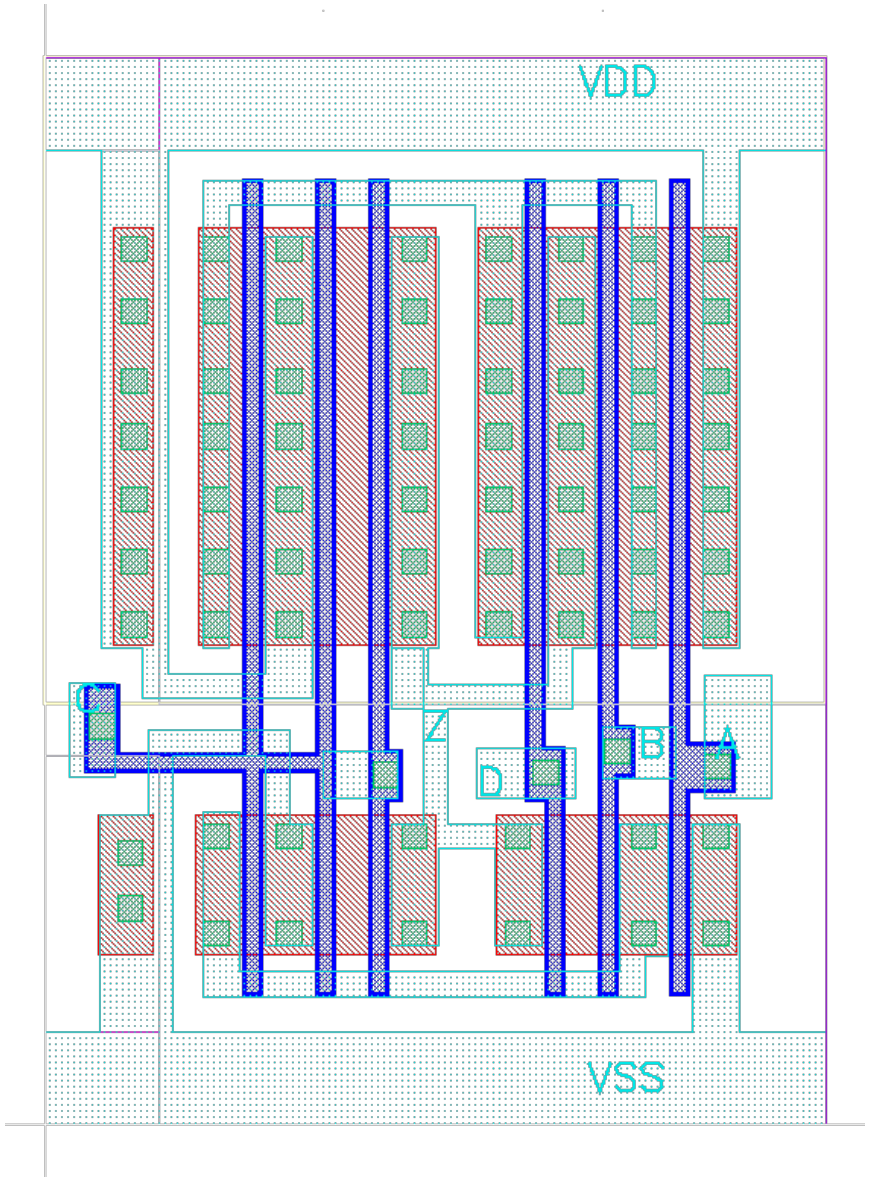
Porte logiche D2RA: AND / NAND schematic





Porte logiche D2RA: AND / NAND layout





Complex Design rules

65 nm gates require PCM (Phase Change Masks)

Conventional masks for photolithography are *binary* masks:

- 0 = opaque
- 1 = transparent

Phase Change Masks are *ternary* masks:

- 0 = opaque
- 1 = transparent with phase = 0 ◦
- –1 = transparent with phase = 180 ◦

The 65 nm gate is defined by an opaque strip, with **two different phases** on the S and D sides
$\longrightarrow$ ALL transistor gates MUST have the same orientation!

Parasitic Capacitances and Resistances

Reduction of transistor size requires the reduction of metal width for scaling
Consequences:

- The metal height is larger than width
- Metal resistance cannot be neglected (tens of milliohm per square)
- Lateral capacitance is much larger than vertical capacitance

Propagation delay is limited by RC parasitics of interconnections

Power Consumption

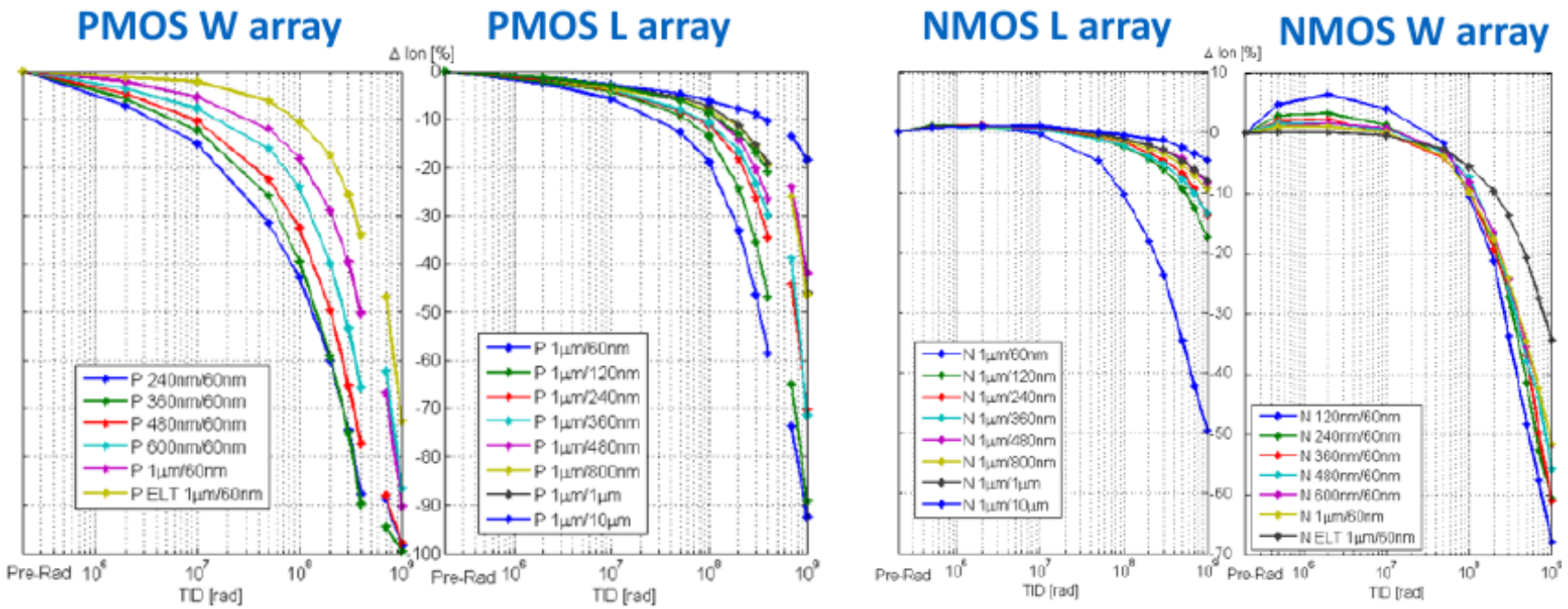
Dynamic power consumption due to interconnection does not scale (and will increase for ultra-scaled technologies.
An example: at 20 nm technology node

- the energy required for boolean operations is about one attojoule per bit
- The energy required to transport 1 bit of information is about one picojoule per millimeter

Total Dose Effects

From Federico Faccio's talk at the RD53 meeting (CERN, Apr. 2016):

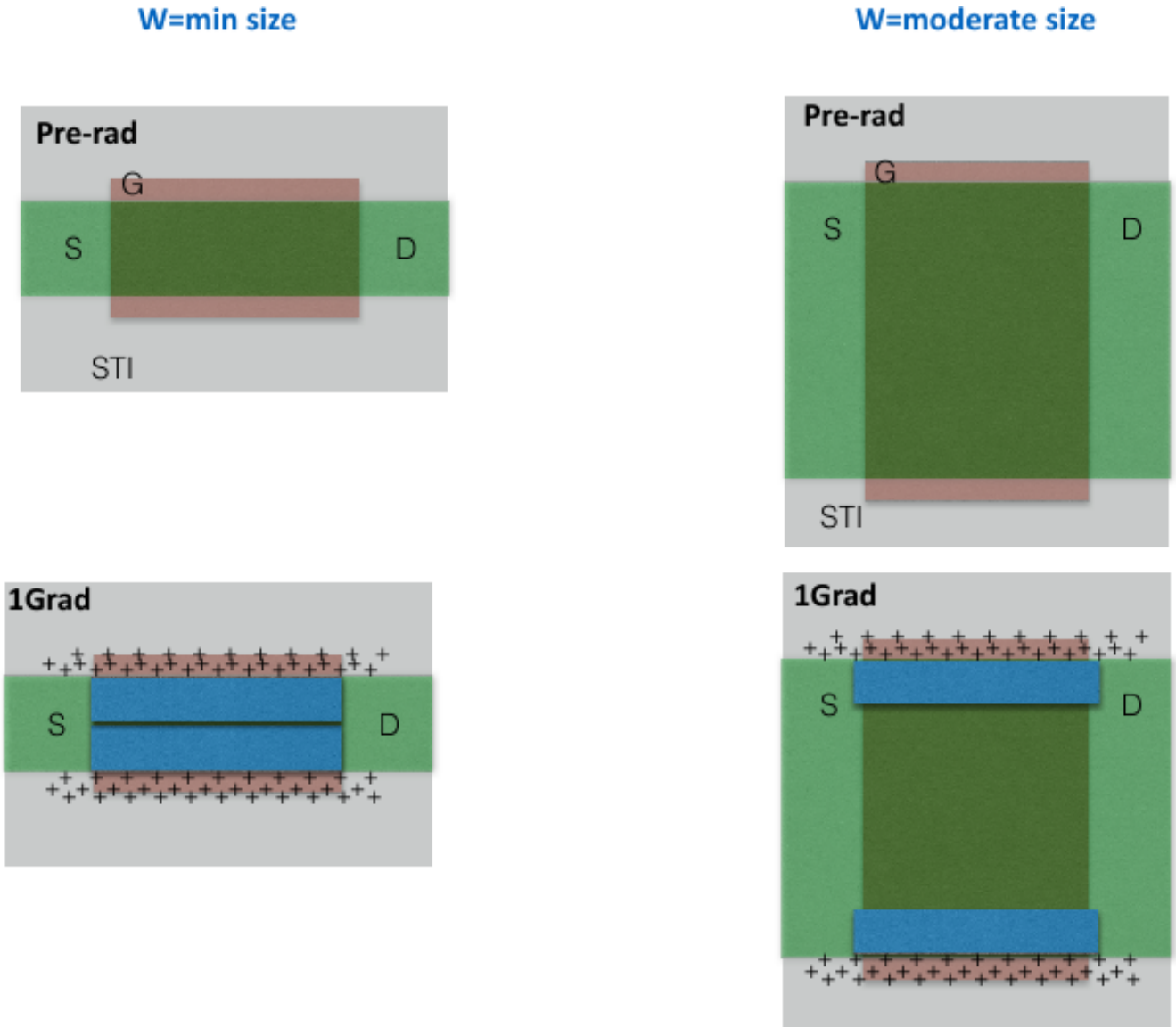
Radiation-Induced Narrow Channel Effect (RINCE)
Radiation-Induced Short Channel Effect (RISCE)



Vertical axis: % loss of current (–100% $\longrightarrow$ transistor is died!)
Narrow and short transitors are more damaged by total dose!

RINCE: Radiation Induced Narrow Channel Effect

From Federico Faccio's talk at the RD53 meeting (CERN, Apr. 2016):



RISCE: Radiation Induced Short Channel Effect

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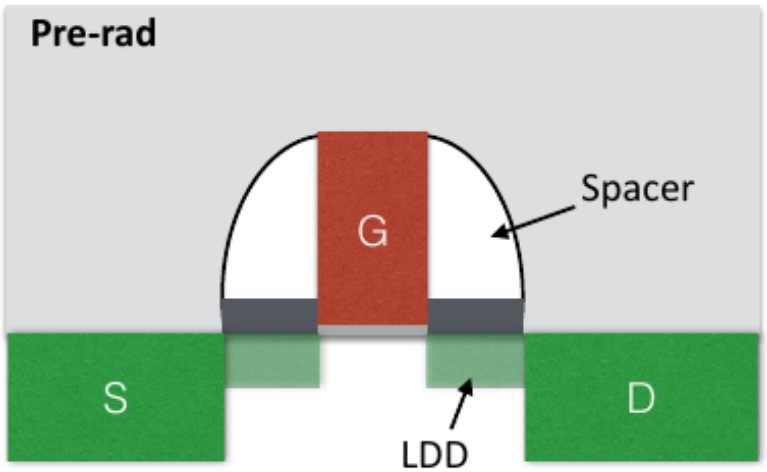
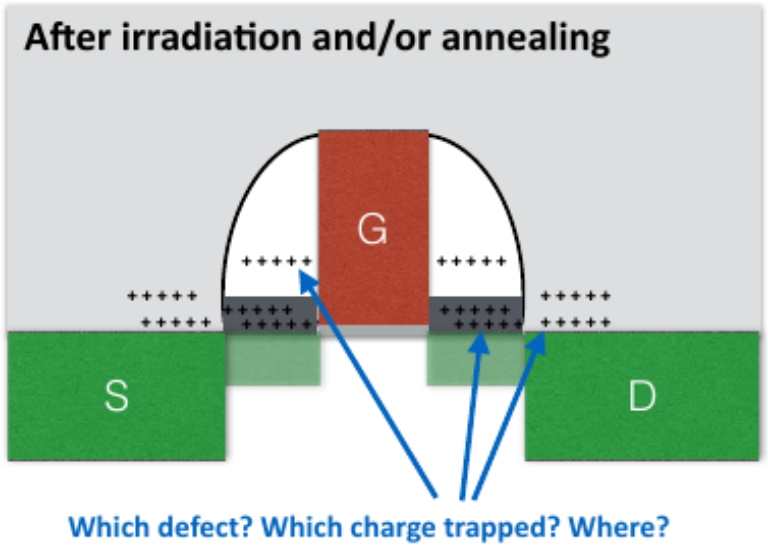
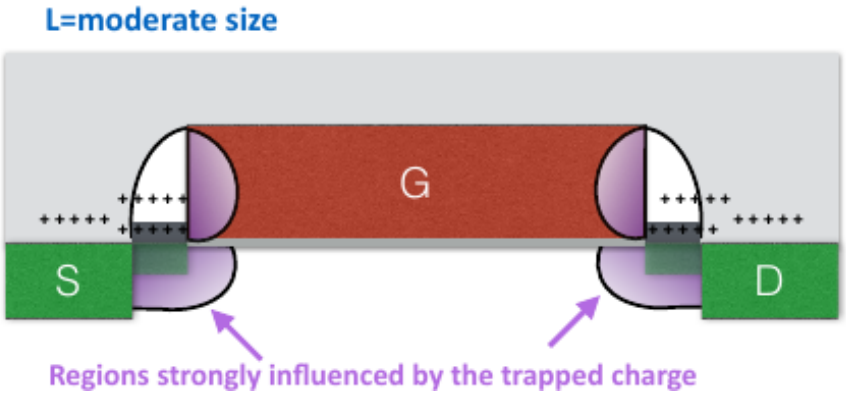
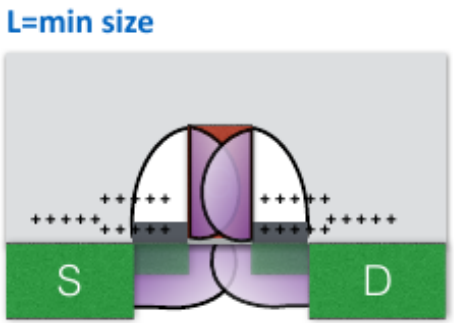


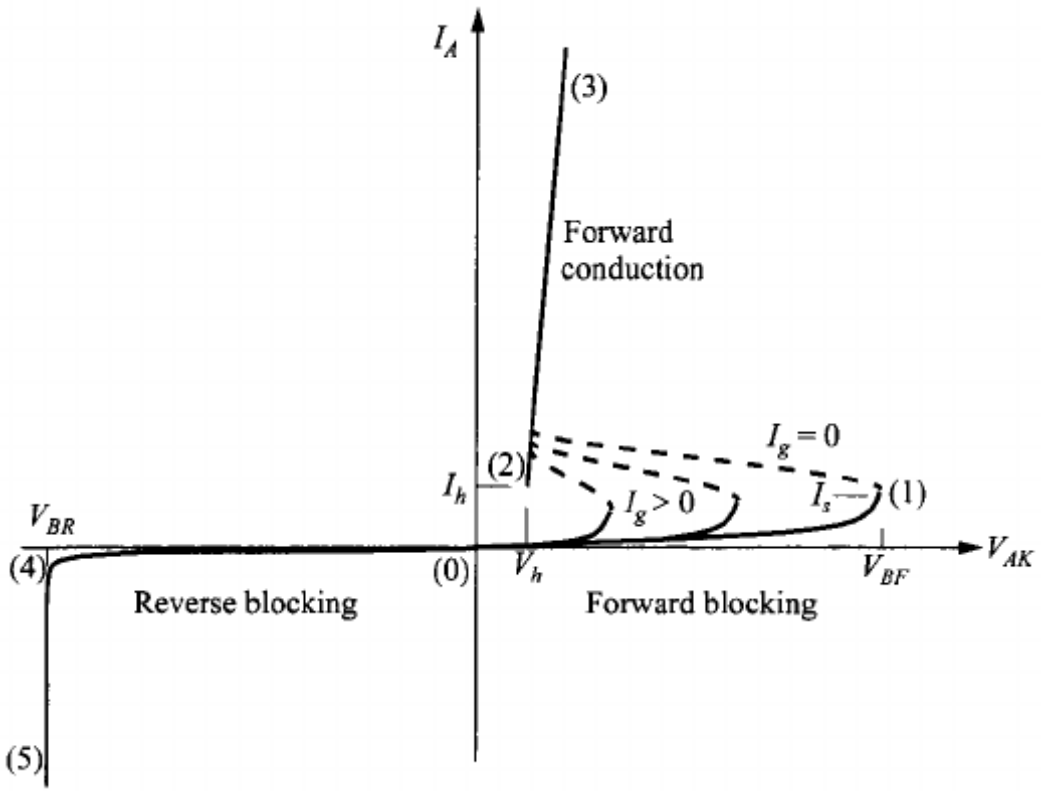






Latch-up

Warning! For very high radiation hardness, guard rings must be placed **all around active devices**, to block parasitic currents. Remember that the latch-up can be triggered **either** by the voltage **or** by the current. Low V_{DD} (≈ 1 V) helps, but does not guarantee latch-up immunity!



Thyristor or SCR (silicon-controlled rectifier) *VI* characteristics, from: *S.M. Sze and K.K. Ng, Physics of Semiconductor Devices, John Wiley & Sons, 2007.*

Common design problems and some solutions

Main issues:

- ☹ Chip composition and design verification require **time**!
  - Our experience: about two working days are required for the chip composition and the final verfication of a small design (2 mm $\times$ 2 mm)
  - A large chip requires at least one week, or more
- ☺ Very powerful **new CAD tools**!
  - EAD (Electrical Advanced Design) provides **semi-automatic routing**, **on-line LVS and DRC**, and information on **interconnection parasitics** during layout design
  - Powerful sign-off tools: **Voltus** (*IR* drop) and **Tempus** (timing)
  - Caution: for designs with mixed approach (e.g., full custom + standard cells), 'Liberty' files should be provided for all blocks
- ☺ The complete **TSMC 65 nm library provided by CERN** is very helpful!
  - Full DRC and LVS are possible (including transistors in std cells)
  - ESD protection check can be performed (included in DRC)
  - Caution: design rules are different for devices directly connected to pads