Fast Timing with Silicon Pixel Detectors

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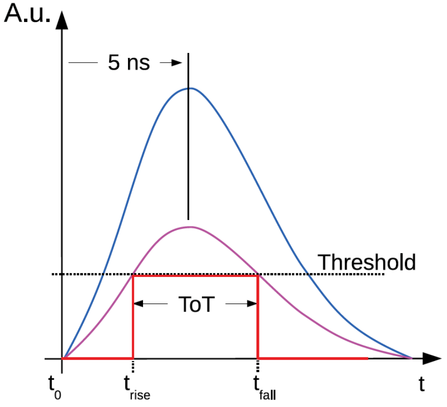
Timing detector

- In timing measurements the slope-to-noise ratio has to be optimized rather than the signal-to noise ratio alone
  - ❑ Very low r.m.s. noise σ_n
  - ❑ Very steep signal at threshold level $(dV/dt)_{thr}$
- Time resolution is given by the ratio: $\sigma_t = \frac{\sigma_n}{(dV/dt)_{thr}}$
- Many contributing factors to consider:
  - ❑ Need large signals, and fast "signal collection"
  - ❑ Reduce input capacitance, match amplifier bandwidth
  - ❑ Electric (weighting) field uniformity
  - ❑ Energy release (total, straggling, direction)
  - ❑ Time-walk correction
  - ❑ Digitization (e.g. TDC bin size and linearity)
  - ❑ …



Time-walk correction

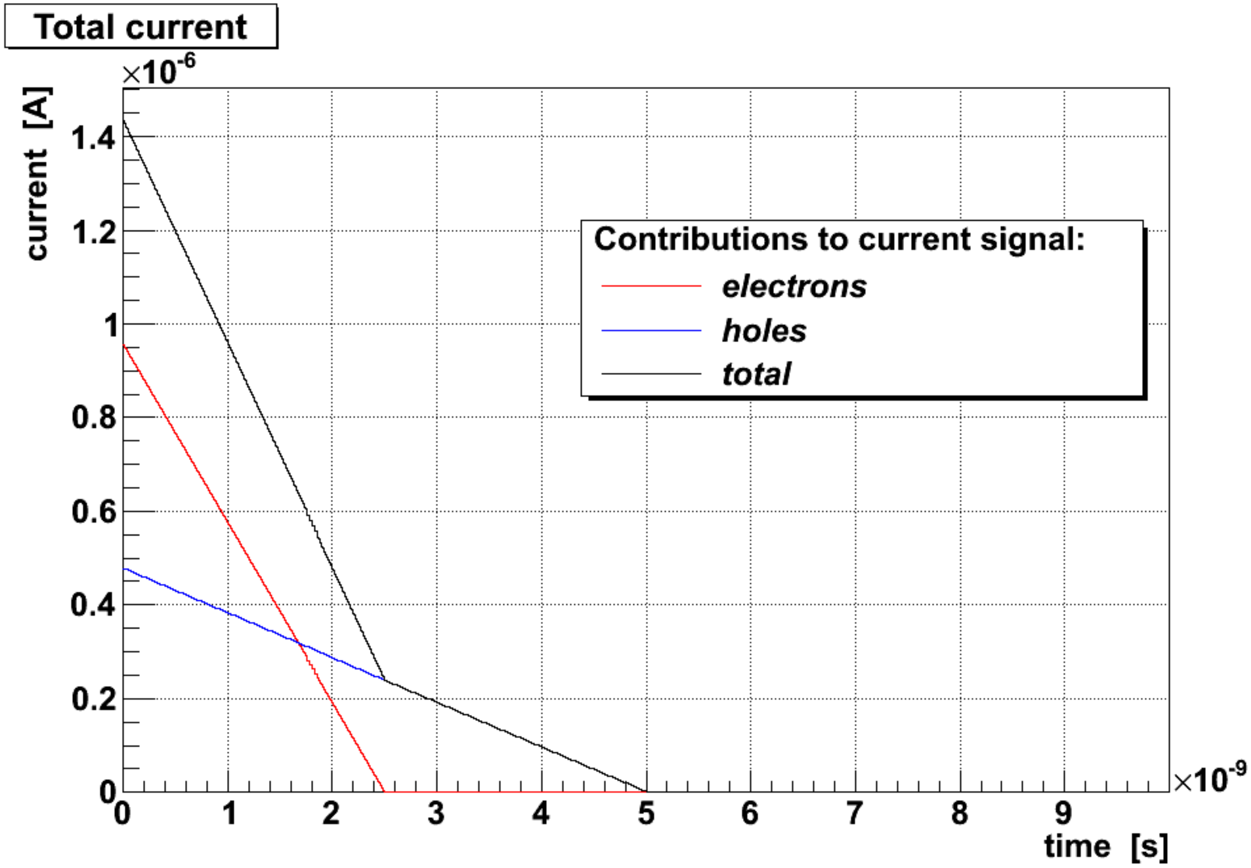
- To achieve excellent timing accuracy, a careful time-walk compensation has to be applied:

Some alternatives:

- Single threshold discriminator and Time over Threshold
  - Time-walk correction algorithm based on the signal time over threshold (pulse width), obtained by measuring leading and trailing edges of the pulse
  - Accurate calibration needed to define correction algorithm
- Use of a Constant Fraction Discriminator (CFD)
  - Analog signal processing technique of time information
  - Single time measurement, complicated analog design
- Digitizer
- Multiple thresholds discriminator

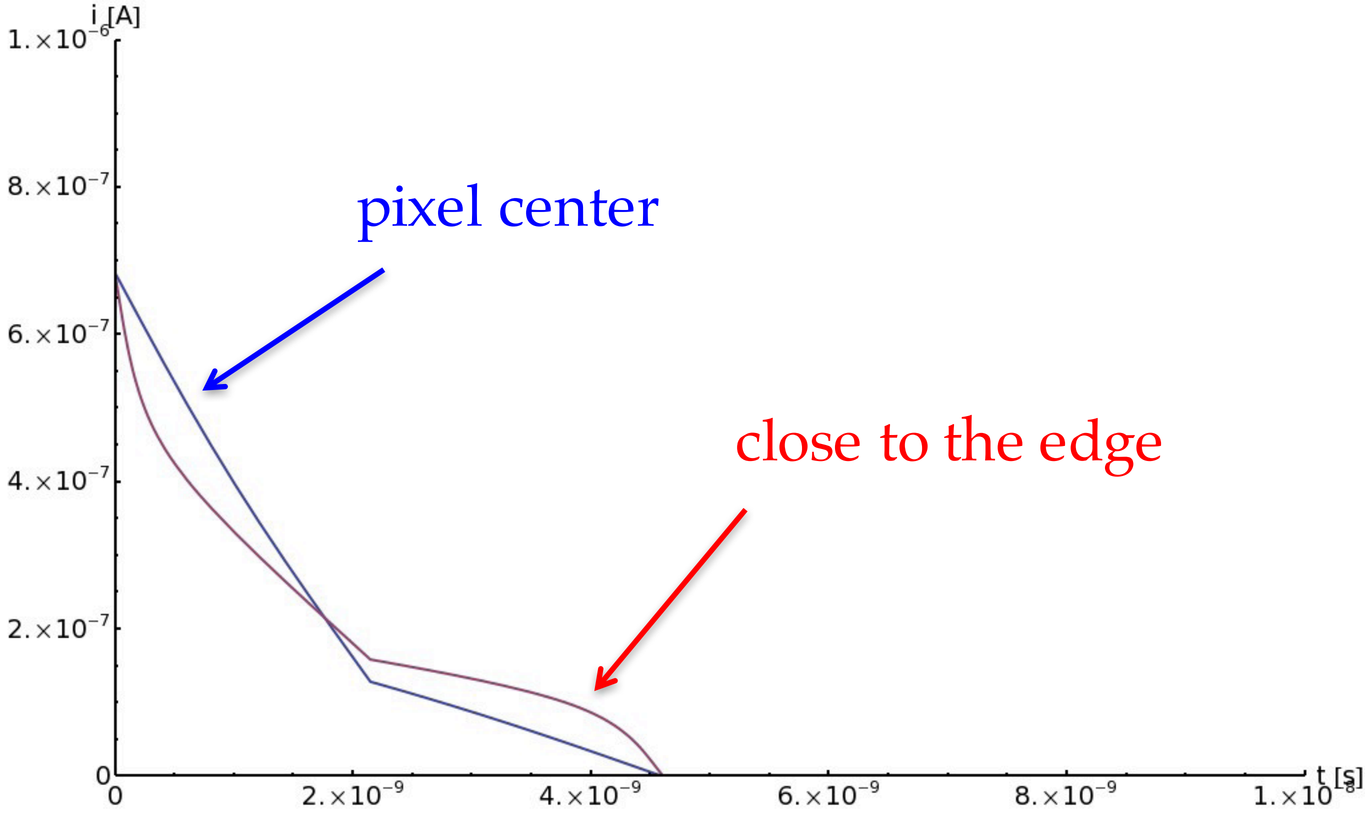
Sensor: signal formation

- Ramo-Shockley theorem
  - $i = q\,\mathbf{v} \bullet \mathbf{E}_w$
- Example: uniform release of 2.4 fC (MPV) along a 200 μm thick planar sensor
  - Assuming uniform weighting field



Sensor: weighting field effect

- Uniform charge release along the sensor thickness
- Charge injection at pixel center and close to the edge

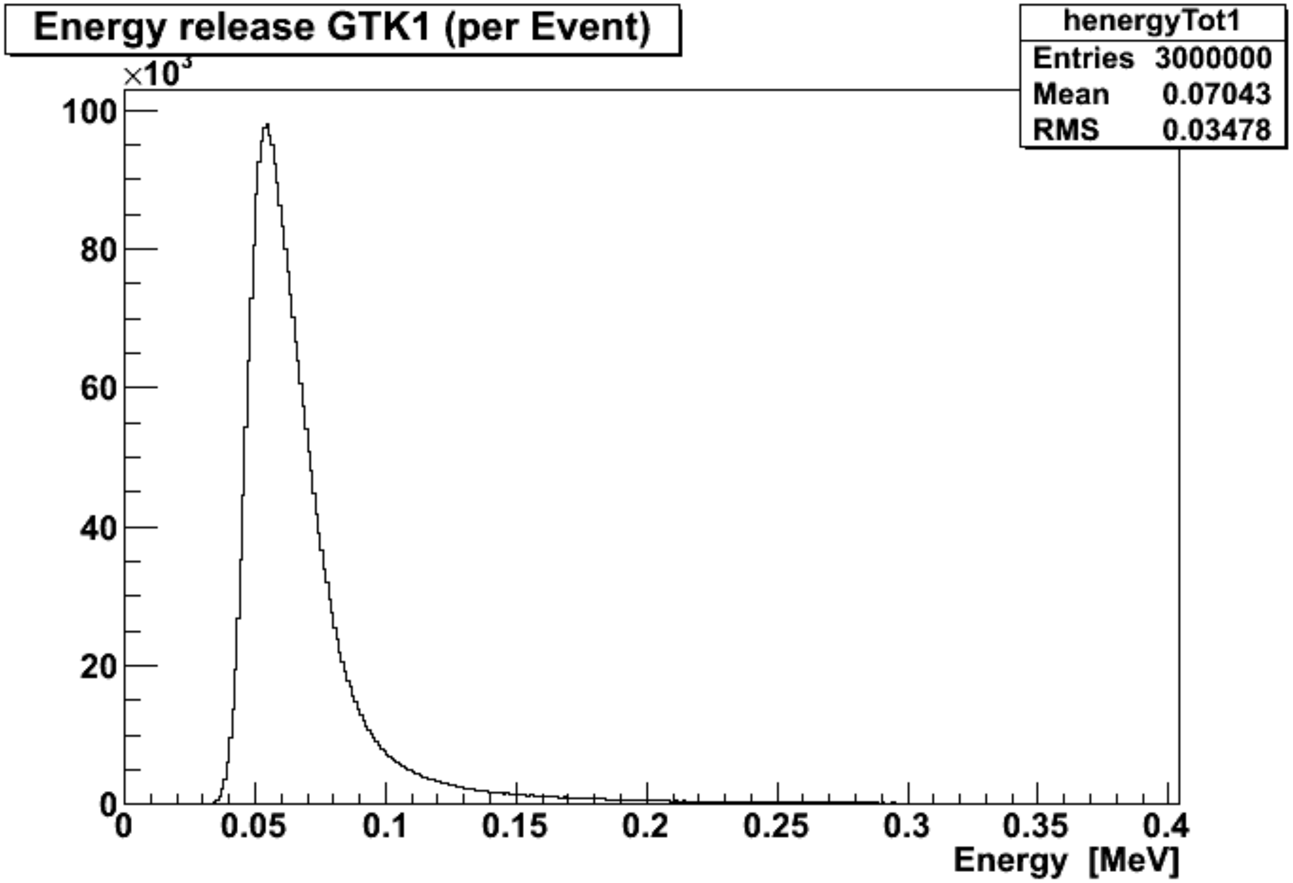


pixel center

close to the edge

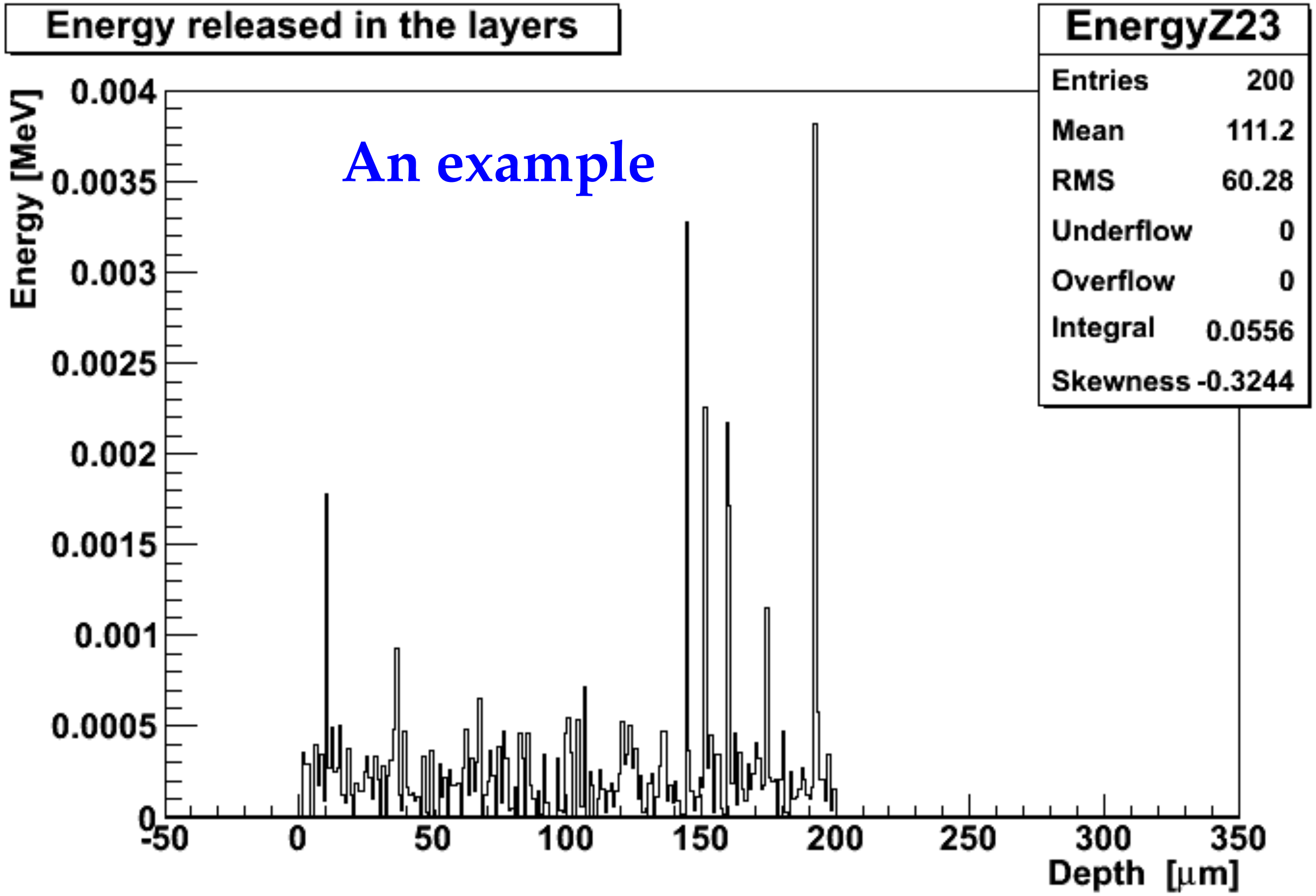
Sensor: energy deposition

- Simulation of energy deposited in 200 μm silicon
  - GEANT4
- Mean energy: 72 keV (~20 k e-h) → 3.2 fC
- Most probable energy: 54 keV (~15 k e-h) → 2.4 fC



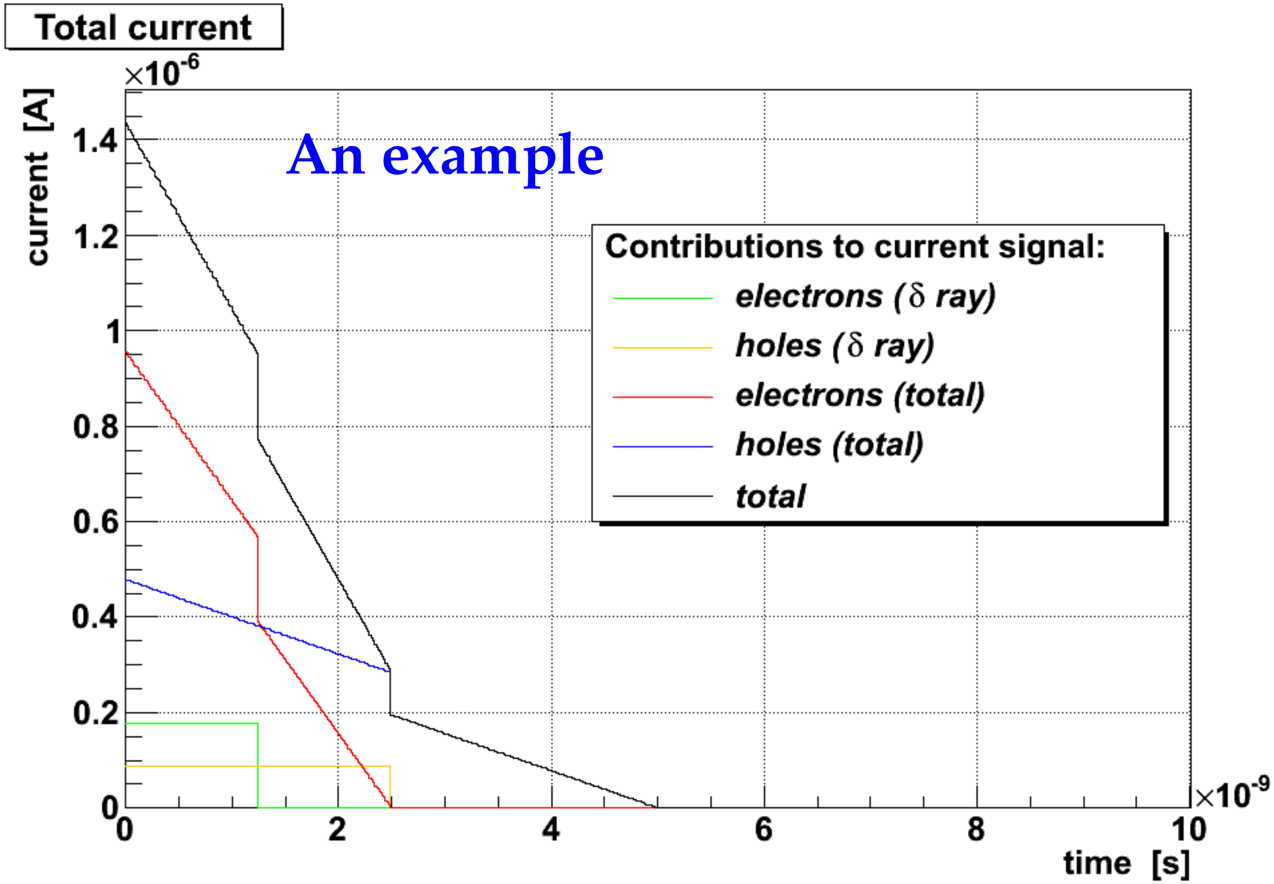
Sensor: energy straggling (1)

- Energy released as a function of depth in silicon
- 200 µm thick silicon divided in 200 layers (1 µm each)
  - GEANT4



Sensor: energy straggling (2)

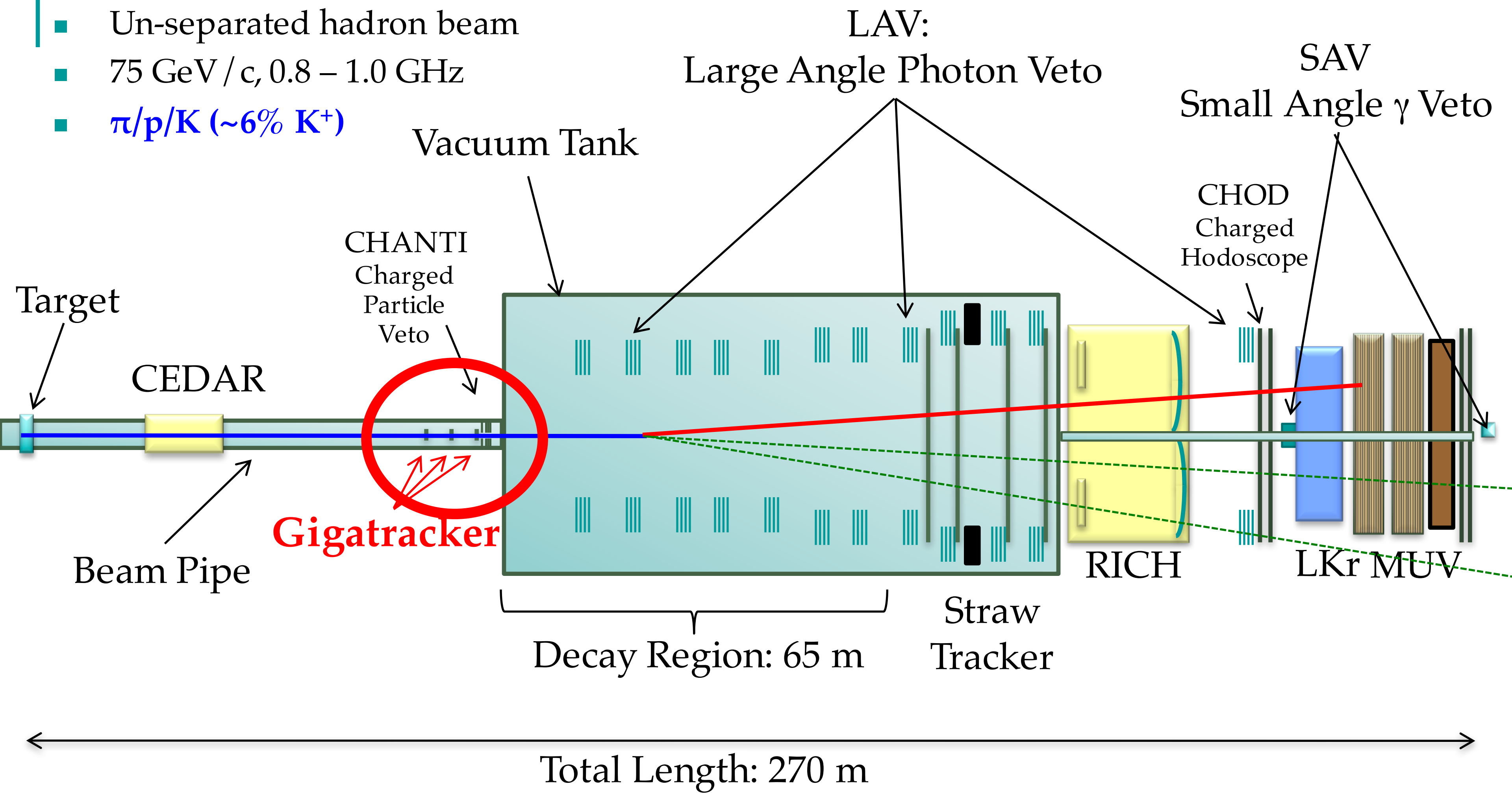
- Total charge release of 54 keV (2.4 fC)
- One δ ray emitted at 100 μm
- δ ray energy is 10 keV (~0.4 fC)



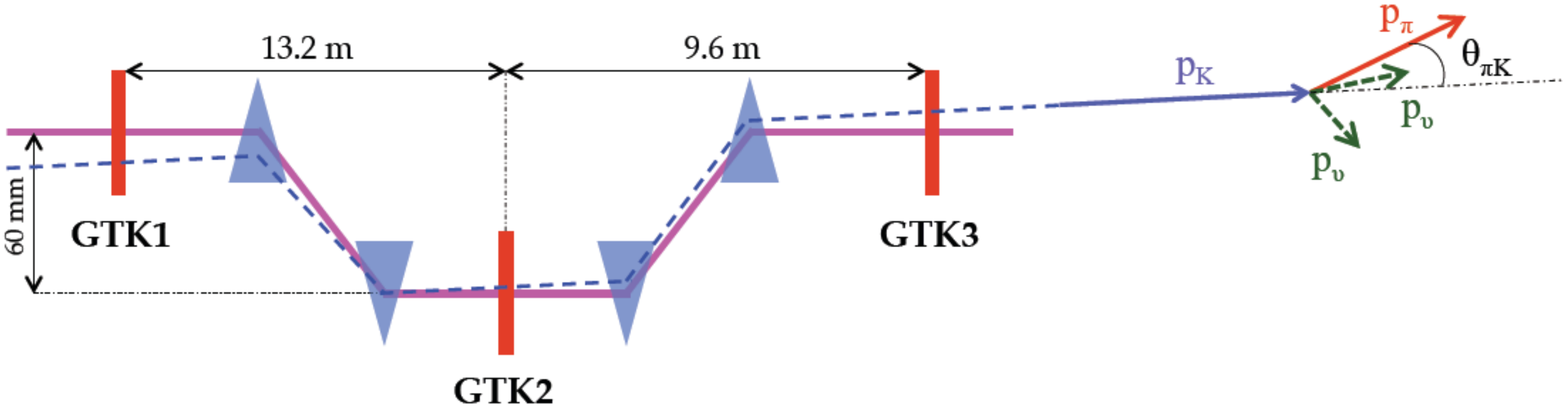
The NA62 Gigatracker

The NA62 experiment

- Measurement of **$K^+ \rightarrow \pi^+ \nu\bar{\nu}$** at the CERN SPS
- Un-separated hadron beam
- 75 GeV / c, 0.8 – 1.0 GHz
- **π/p/K (~6% K^+)**



The GigaTracKer (GTK)

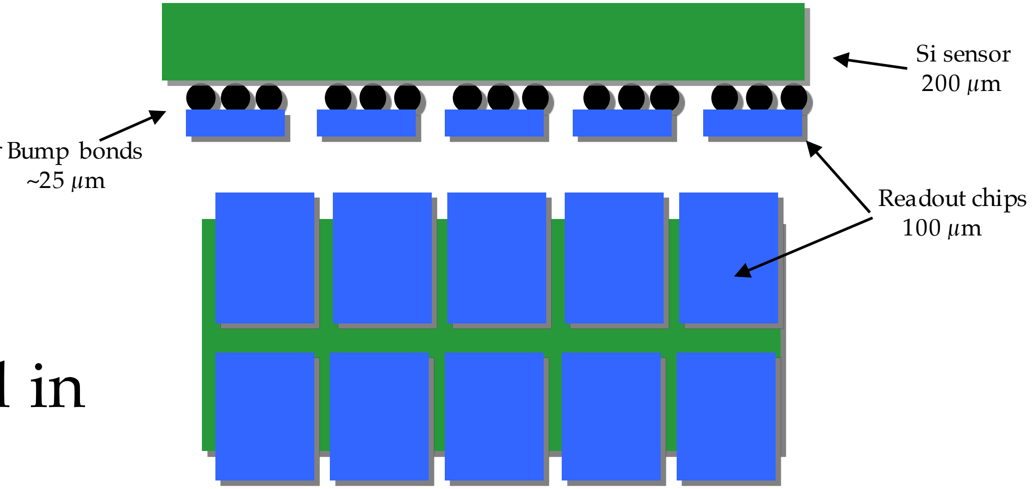


- Beam spectrometer
  - Provides precise momentum, time and angular measurements on all beam tracks
  - Sustains high and non-uniform rate (~1.5 MHz/mm^2 in the center, 0.8-1.0 GHz total)
  - Reduces multiple scattering and beam hadronic interactions

- X/X_0 ~0.5% per station
- $\sigma(p_K)/p_K$ ~0.2%
- $\sigma(\theta_K)$ ~16 μrad
- pixel size
  300 μm × 300 μm
- **$\sigma(t)$~150 ps** on single track

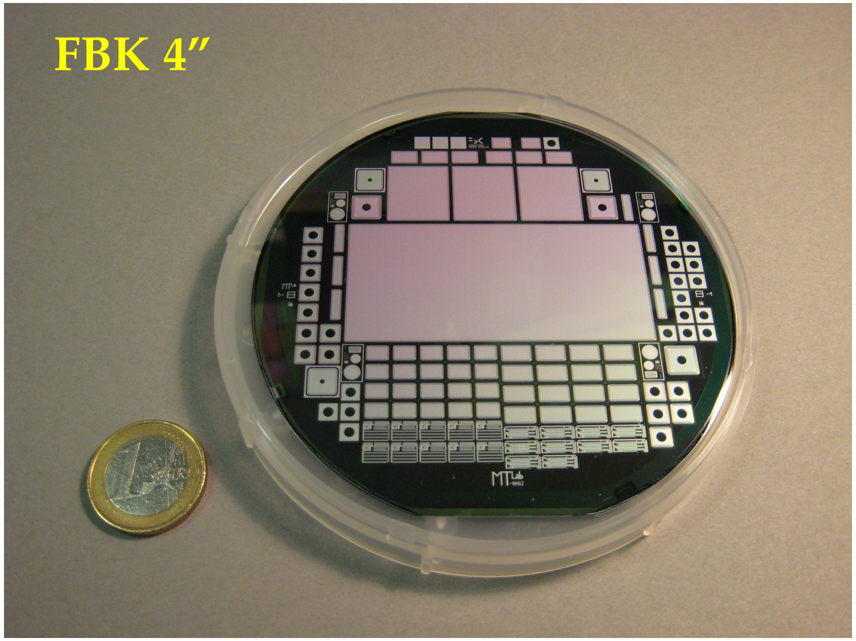
Gigatracker assembly

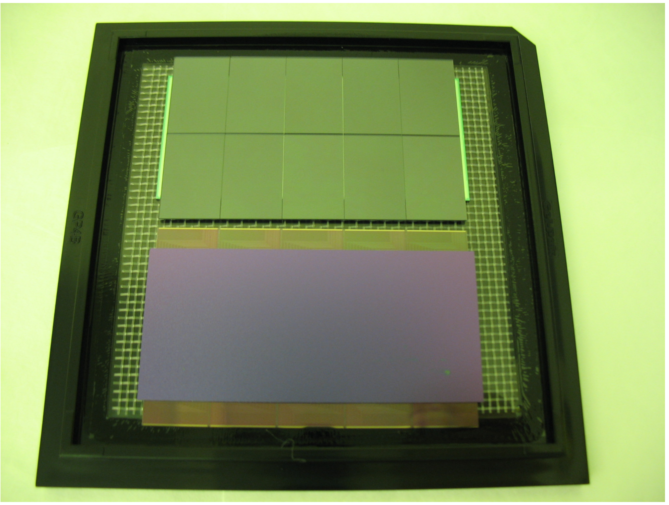
- Hybrid pixel detector
  - **300 μm × 300 μm** pixels
  - 1 sensor (~6×3 cm^2) bump-bonded to 10 read-out chips
- Material budget:
  - 200 μm sensor + 100 μm read-out chip → ~0.32% X_0
  - Bump bonds ~0.01% X_0
  - Mechanical support and cooling ~0.15% X_0
  - **<u>Total</u> < 0.5% X_0**
- Minimization of material in active beam area
  - Beam profile adapted: two rows of read-out chips
  - Wire connections to R/O chip outside active area



Sensors and bump-bonding

- 200 μm thick p-in-n and n-in-p planar sensors (FBK, CiS)
- Over-depleted operation of the detector required to achieve target time resolution (300 V over-bias)
    - Fast charge collection
- Irradiation of test structures
    - Annealing study following expected run scenario





- Flip-chip bonding and read-out wafer thinning (100 μm) done at IZM

Read-out specifications

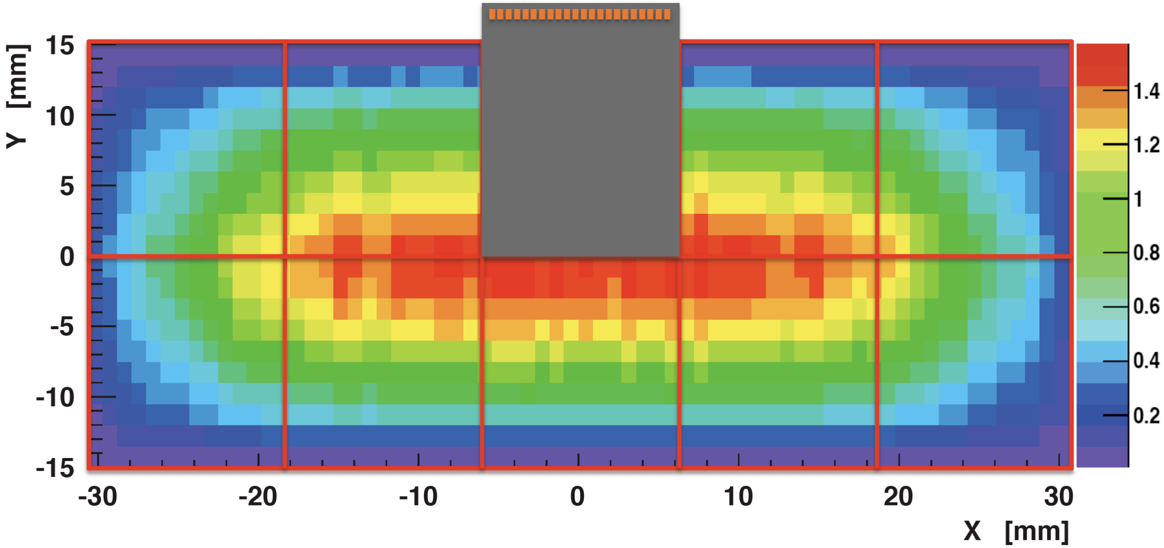
Pixels per chip	$40 \times 45 = 1800$
Chip size	12 mm × 20.4 mm
Dissipated power	~2 W/cm^2
Dynamic range	3600 – 60000 e^- (0.6 – 10 fC)
Total dose in 1 year	~10^5 Gy
Time resolution	< 200 ps
Peaking time	5 ns
TDC bin size	100 ps
Efficiency per station	> 99%
Particle rate per (central) pixel	140 kHz
Particle rate per chip	130 MHz
Data bandwidth	4 × 3.2 Gb/s

The TDCpix ASIC

- IBM 130 nm CMOS technology
- 1800 pixels
- On-pixel fast preamplifier and discriminator
- Asynchronous transmission lines from pixels
- Data driven architecture
- Digital signal from 5 pixels in a column (45 pixels) are sent to a multiplexer ("hit arbiter")
- A TDC pair is connected to each "hit arbiter" to measure leading and trailing edge times
  - 360 TDC pairs/chip
- Four 3.2 Gb/s serializers used to send the data off-chip
- Triplicated digital logic (SEU protection)

Operating environment

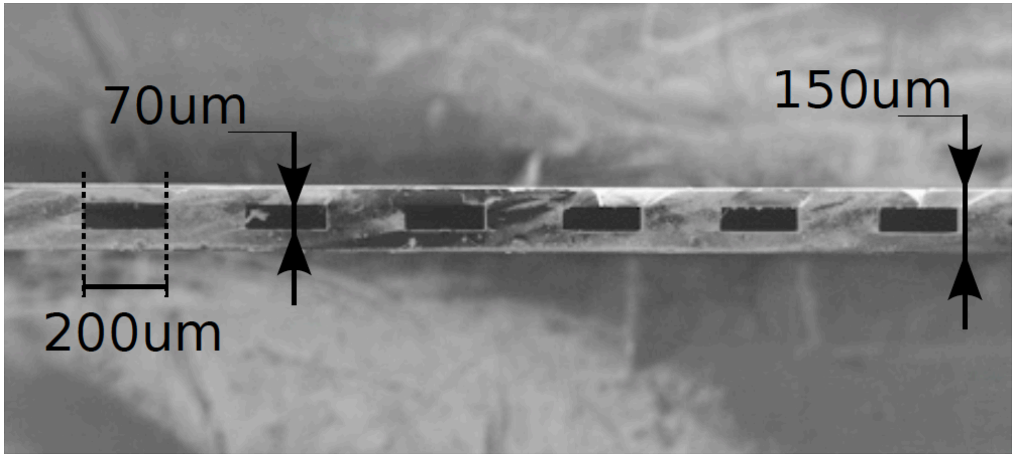
- GTK stations installed in **vacuum**
- High and non-uniform radiation levels
  - Expected fluence is **~2 × 10^{14} (1 MeV n_{eq}/cm^2)** during one year of operation (100 days) in the sensor center
- Efficient cooling necessary for stable detector operation
  - **35 W** per station
  - Very low material budget (**~0.15% X_0**) in the active beam area

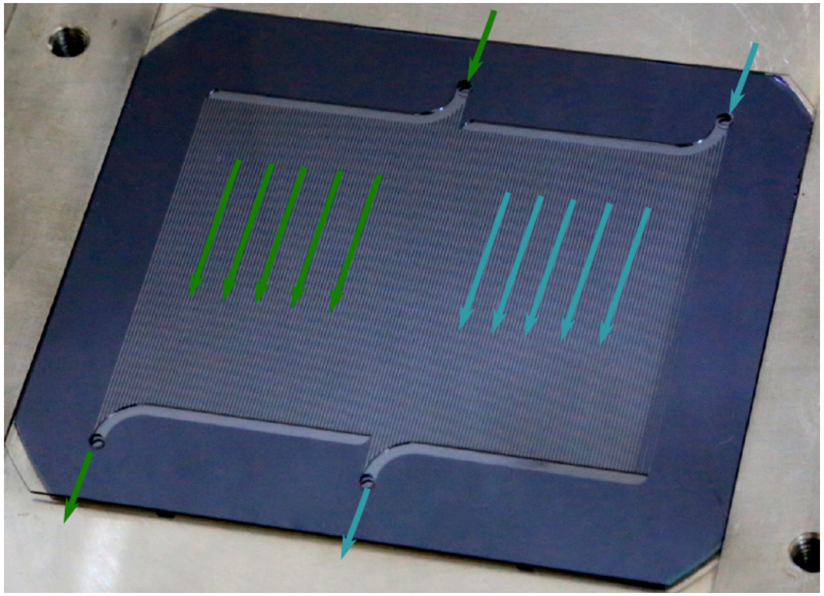


- Micro-channel cooling plate:
  - First application of this technique to a HEP experiment

Micro-channel cooling

- Micro-channel cooling plates (CEA Leti)
    - 150 μm (210-280) thick in the active detector area
    - Channels plus opening for inlets and outlets

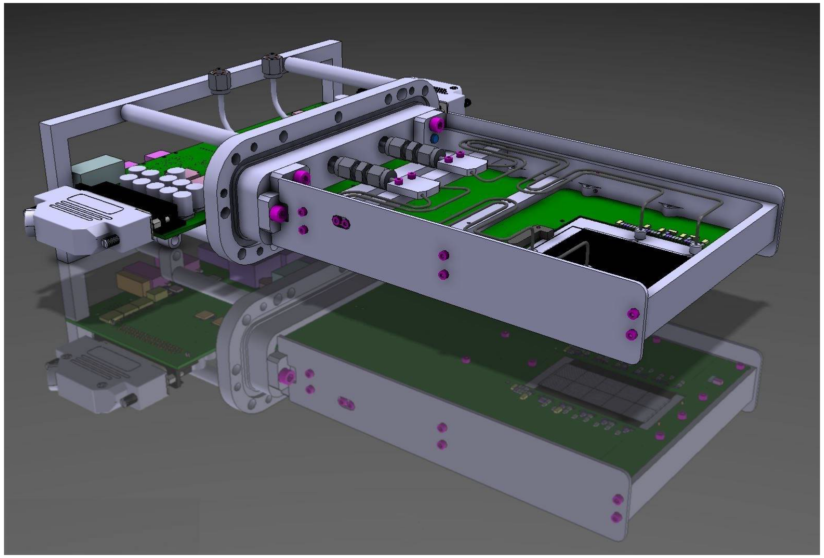


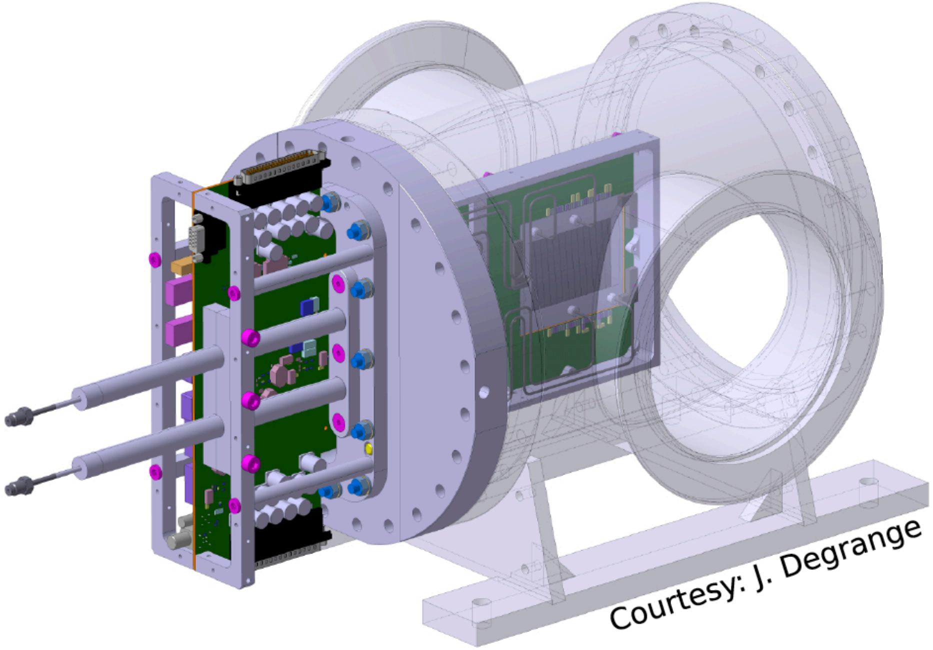


- 70 μm × 200 μm micro-channels
- C_6F_{14} liquid coolant
    - 3.5 bar pressure
    - 3 g/s flow
    - Temperature down to -25 °C
- Two cooling circuits

Mechanical integration

- Hybrid pixel detector glued on cooling plate
- Cooling plate clamped on PCB
- PCB glued into frame and flange



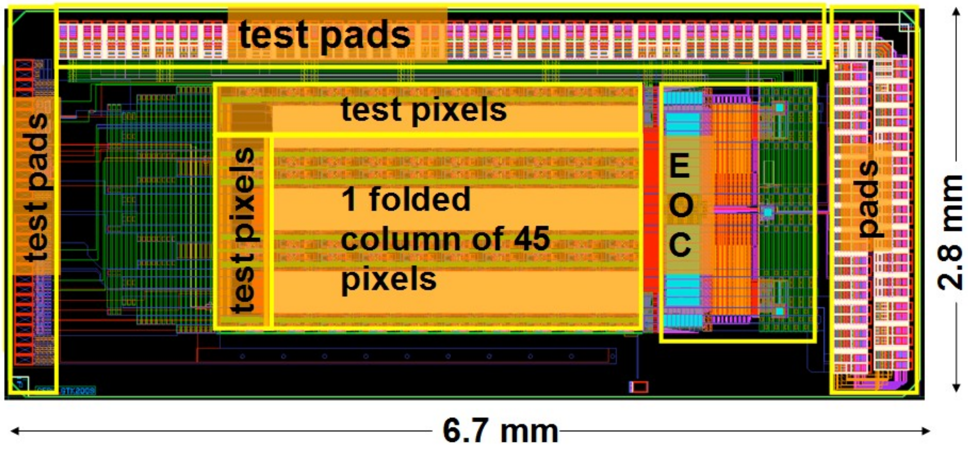


Courtesy: J. Degrange

- Flange closes the vacuum vessel
- Easy access to the detector for intervention
  - Detector is replaced every ~100 days of running

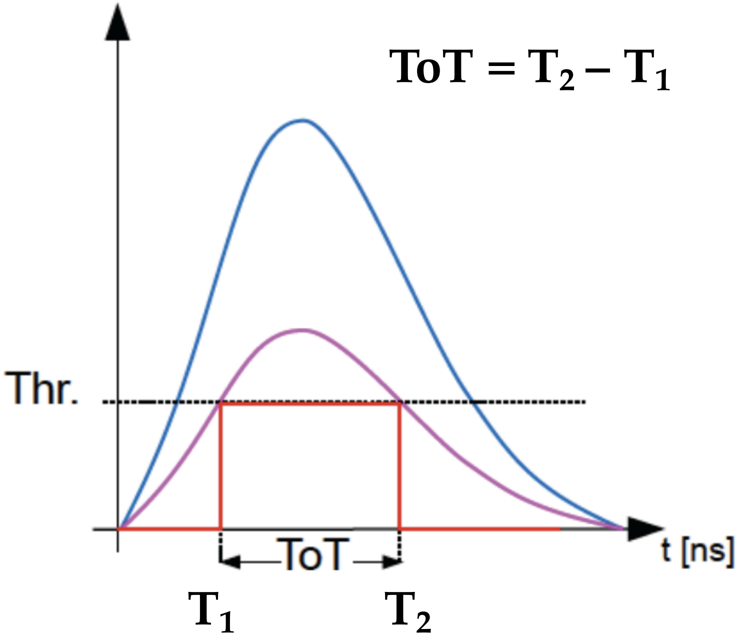
Prototype read-out ASIC

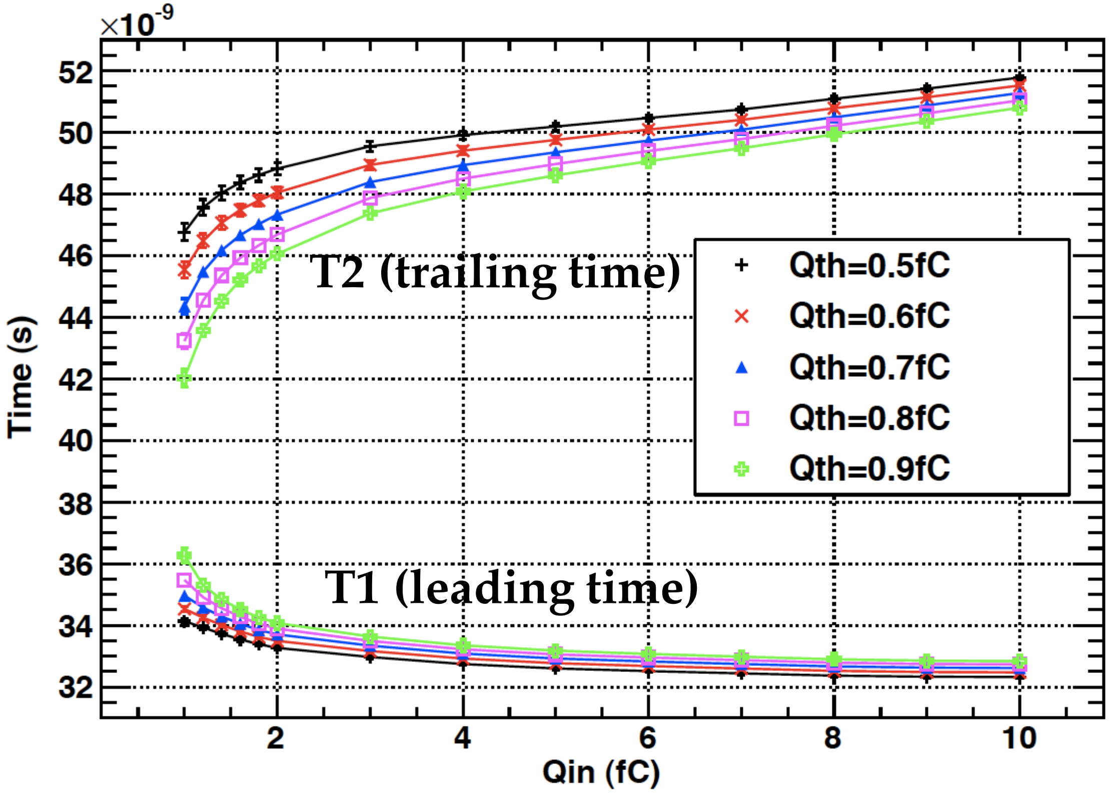
- IBM 130 nm, 2.8mm × 6.7mm total size, 320 MHz clock
- 60 pixels divided into 3 groups
  - 45 pixels with 9 read-out blocks, each one serving the 5 pixels through the “hit arbiter” block
  - Small array: 9 pixels
  - Test column: 6 pixels with analog output
- Extensively characterized with laser and beam particles
- Measured ~180 e^- (ENC) with sensor (~130 e^- without)



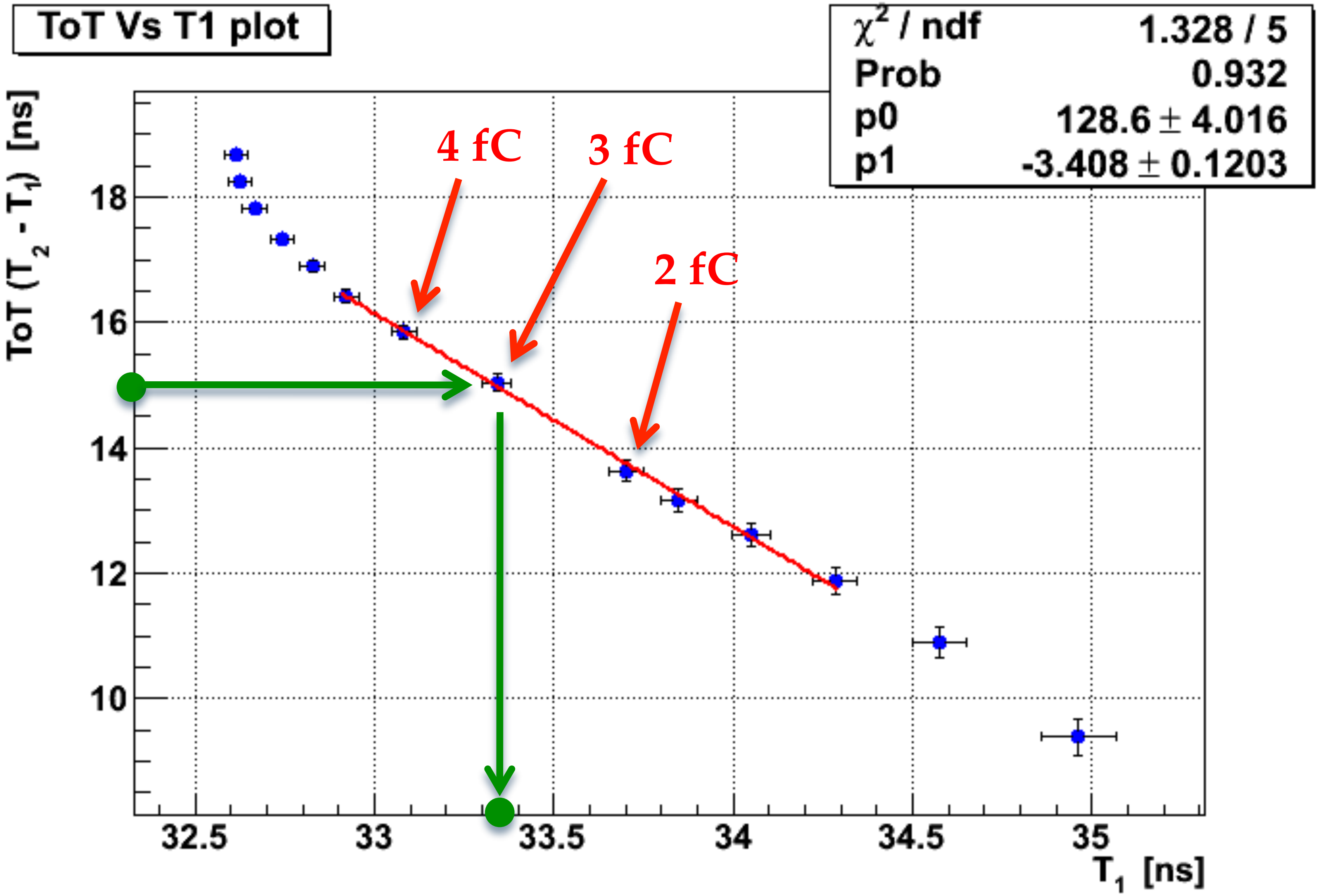
Time-walk

- ~2.5 ns walk of leading time (1.0 – 10.0 fC range)
- Time-over-Threshold used for correction of time-walk effect
  - ToT Vs T_1 (leading time) is monotonic function



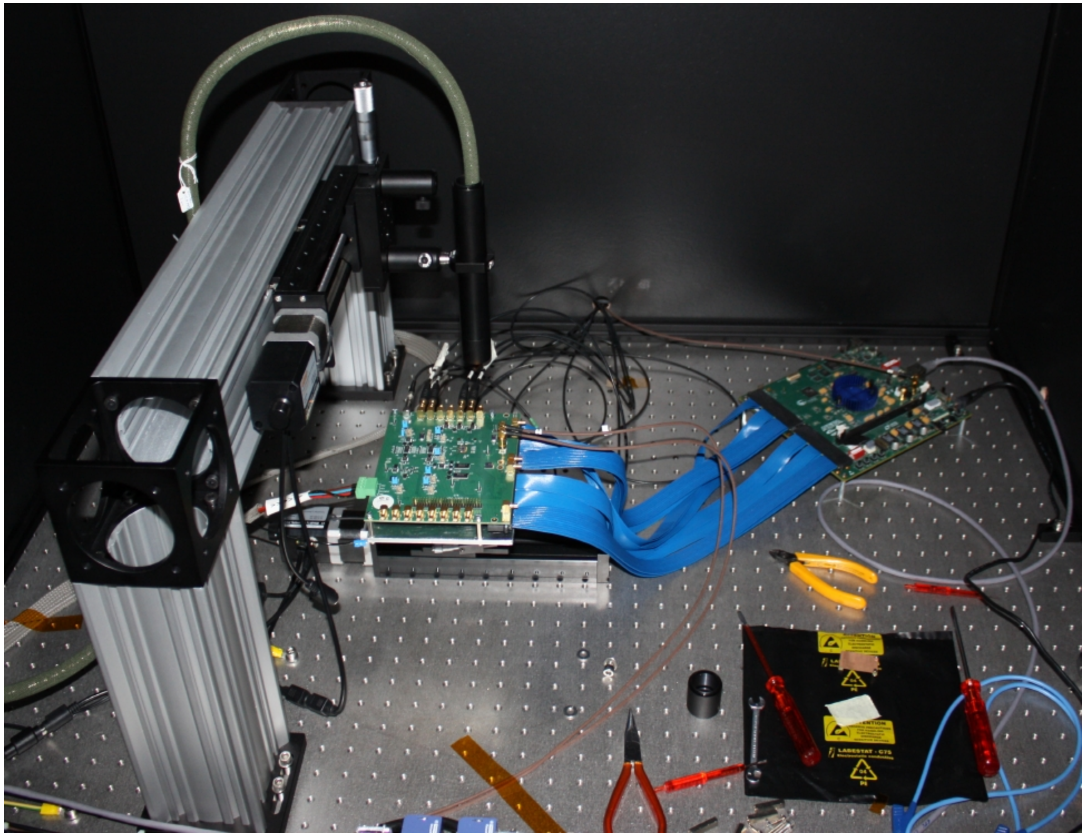


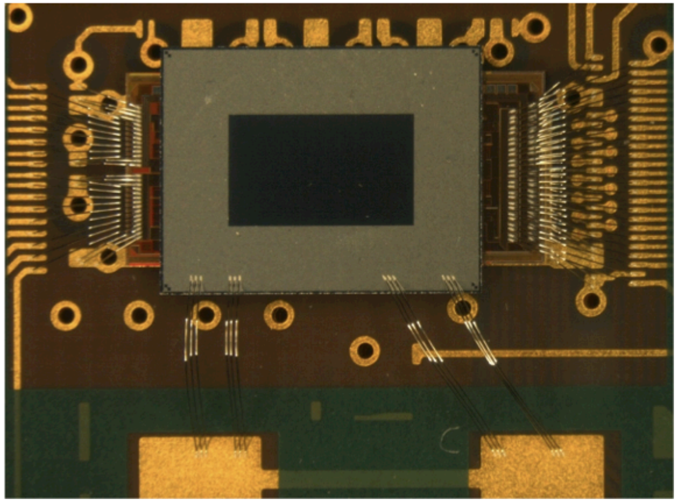
Time-walk correction



Laser test setup

- IR light (1060 nm) to mimic minimum ionizing particles
- Characterize GTK bump-bonded assemblies on laboratory bench

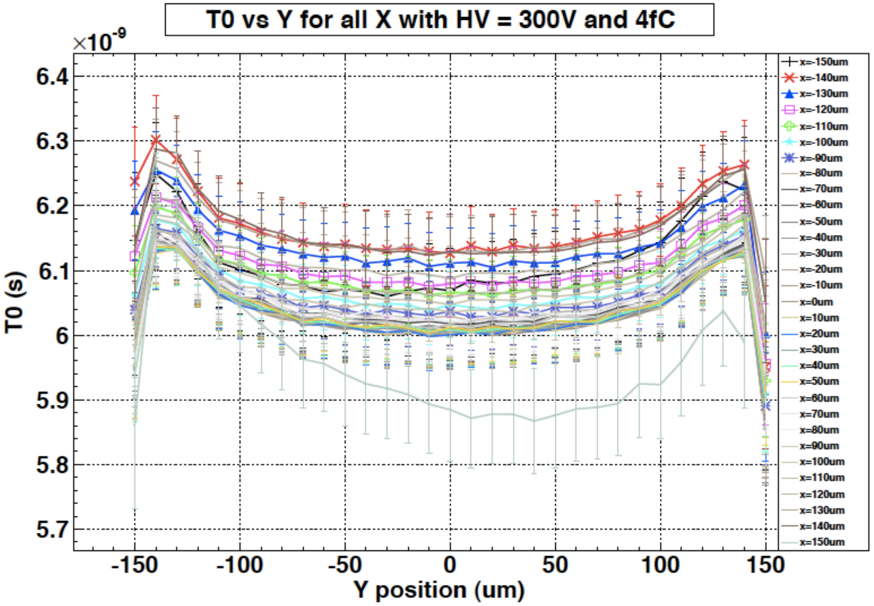


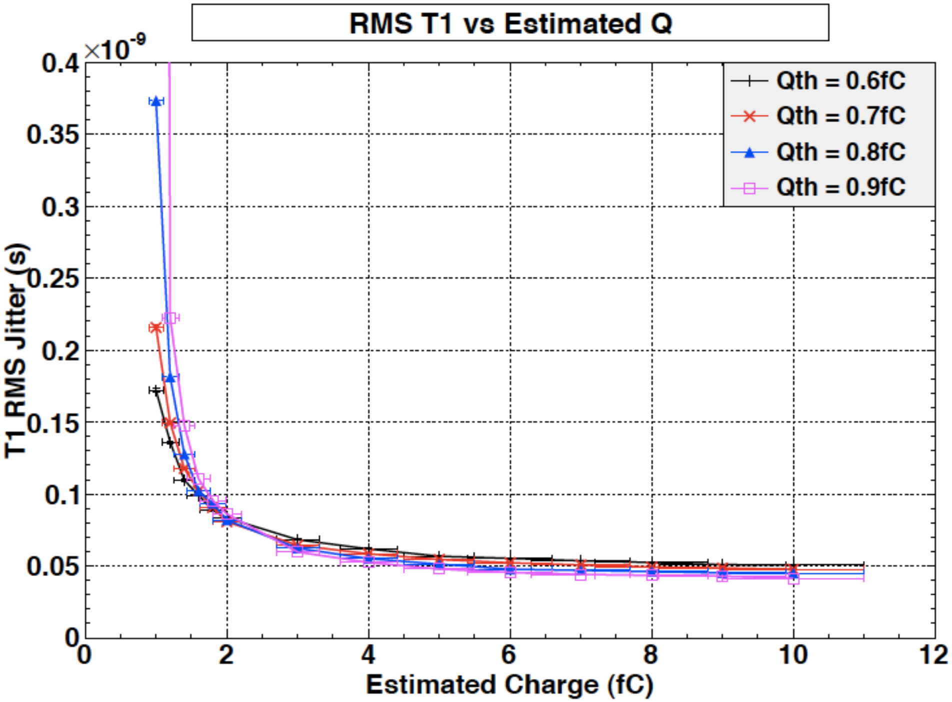


- 5 ps time precision
- Absolute calibration of injected charge
  - Radioactive sources (^{241}Am, ^{109}Cd)

Results from laser test

- Time resolution of ~75 ps at 3 fC (average charge created by minimum ionizing particle)
  - Charge injected at the pixel center

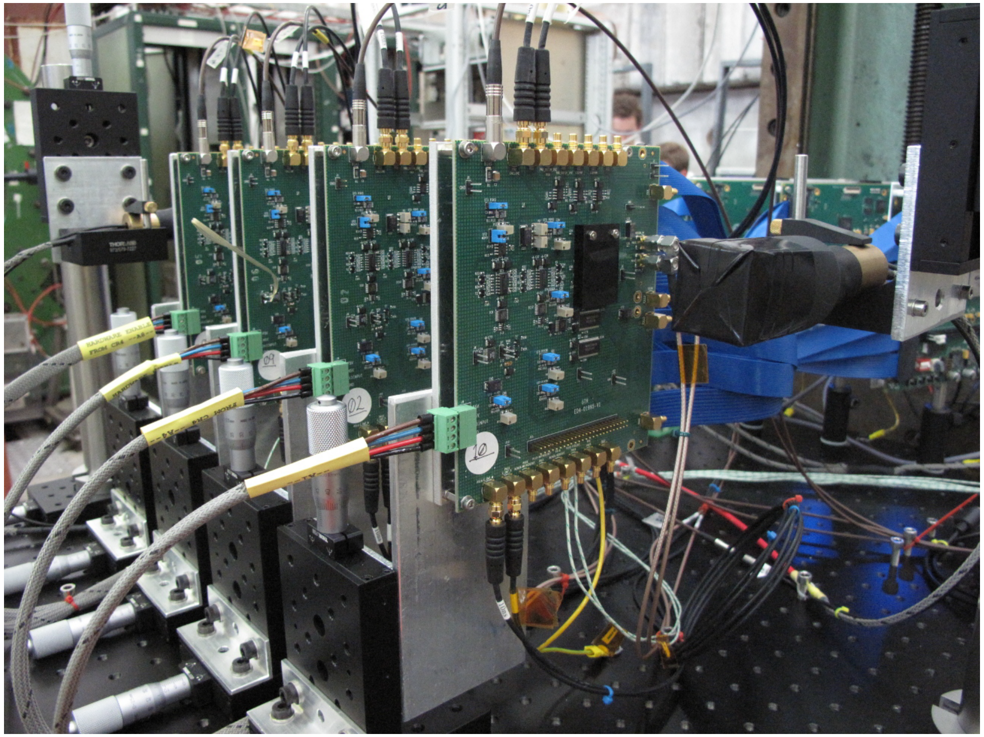




- X-Y position scan of pixel matrix
  - Variation of measured time with impact position inside pixel
  - Geometrical effect (weighting field)

Test-beam at CERN

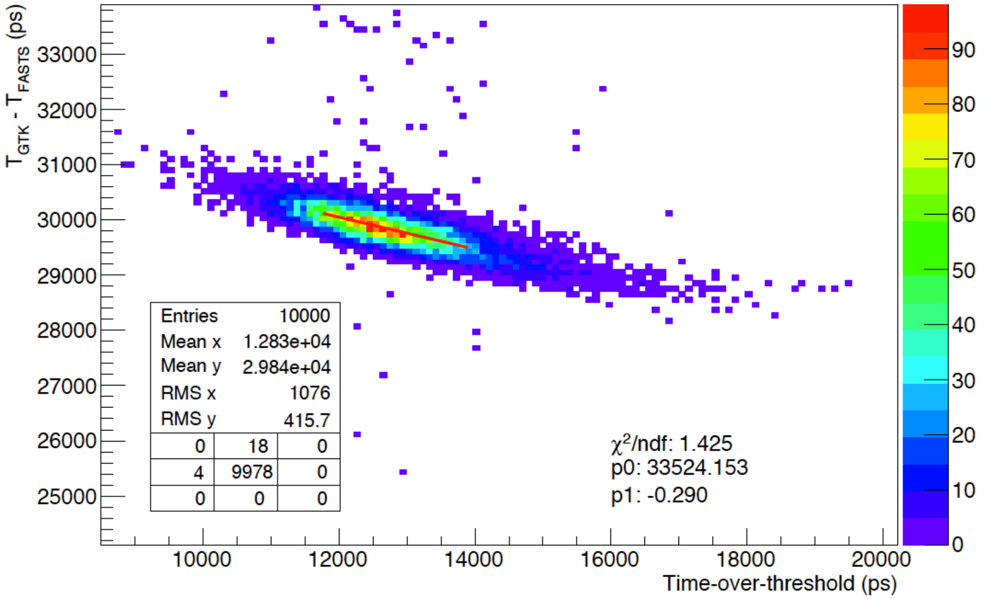
- Test-beam at the T9 beam-line (CERN PS East Hall)
  - 10 GeV/c π^+ and p
- 4 consecutive prototype detector planes
- Fast scintillators used for timing reference
  - Synchronized 25 ps TDC independent read-out

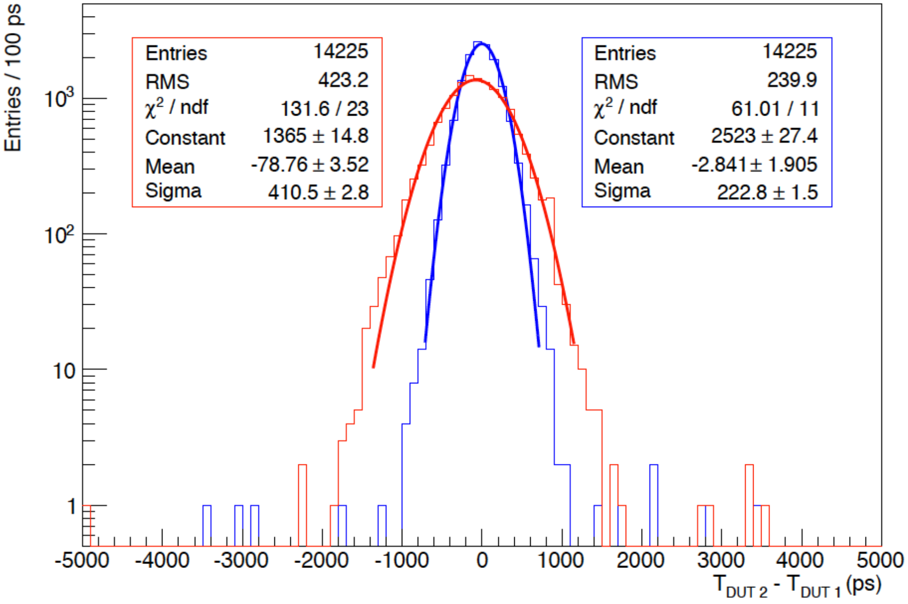


- Very precise mechanical supports and pre-alignment at the 150 μm level
- Operation in air (no cooling, no dry air circulation)
- Results published on JINST 10 P12016 (2015)

Time-walk correction

- Time-walk correction evaluated using fast scintillators for time reference and time-over-threshold information
  - ❑ Linear fit or look-up table

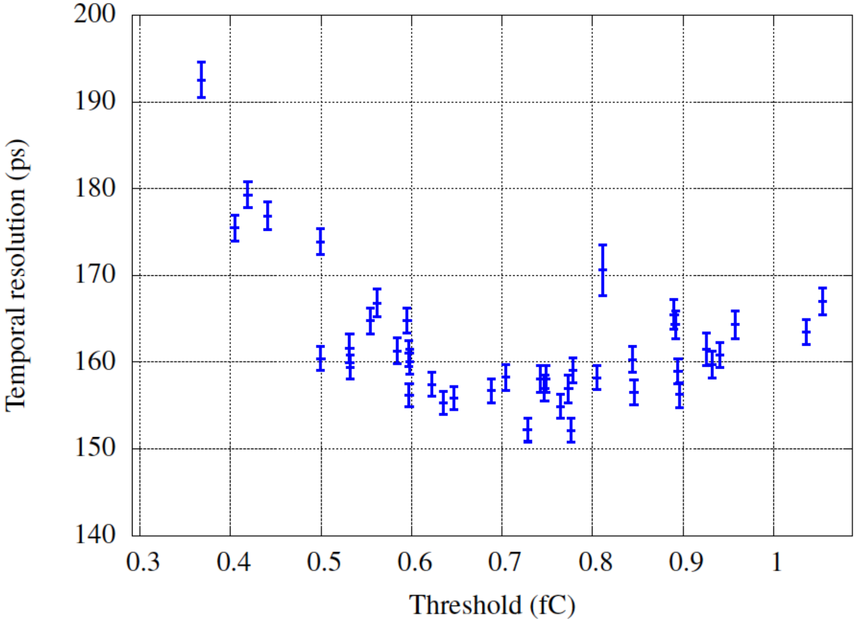


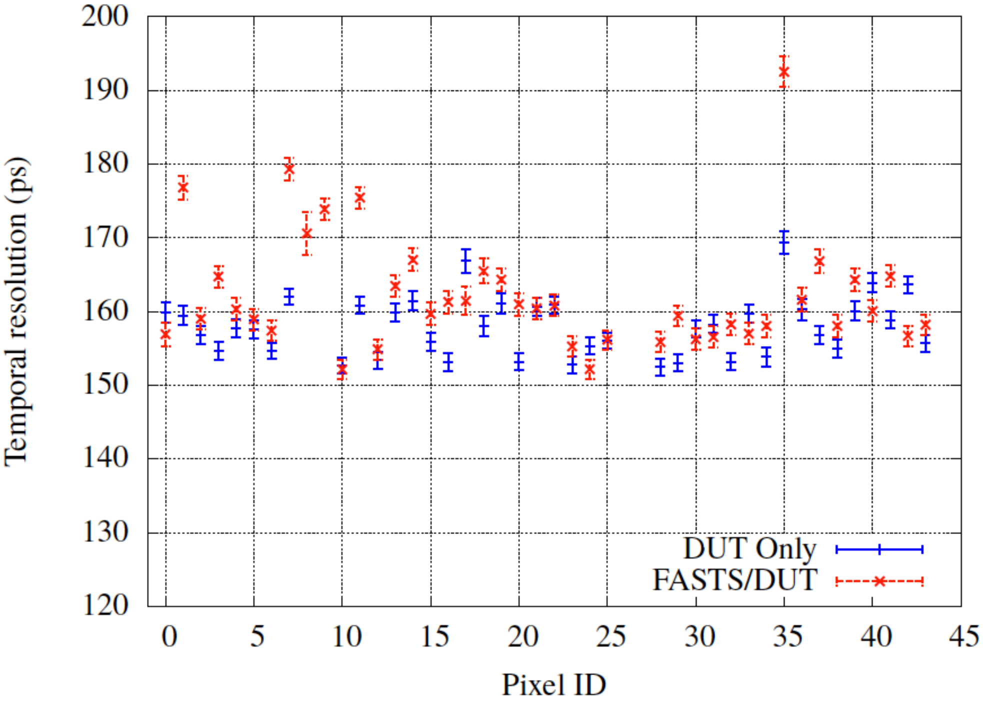


- Discriminator thresholds set by unique digital-to-analog converter for all pixels
  - ❑ (0.70±0.14) fC
- Time resolution after correction is ~160 ps (for 300 V bias)

Time resolution

- Time resolution measured for all 45 pixels per chip
  - Shown for 300 V bias
  - Variations mainly due to pixel-by-pixel threshold variation

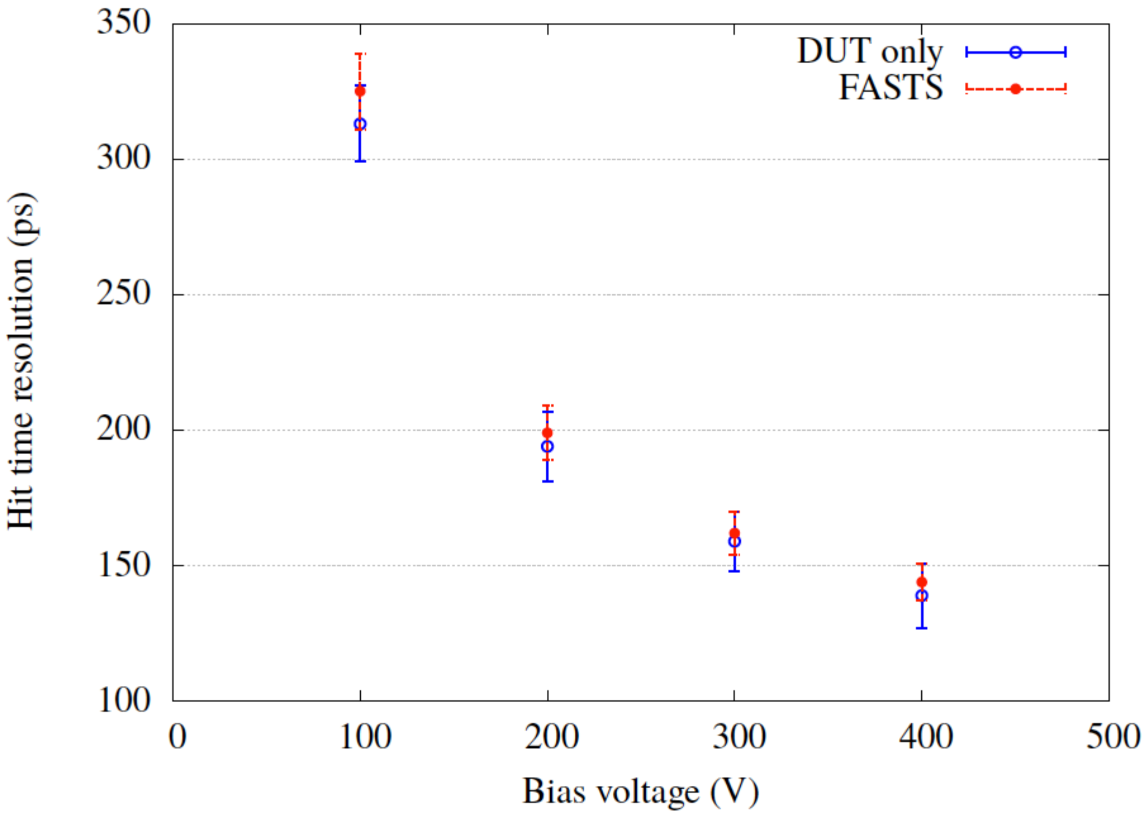




- Clear threshold dependence
  - Worse resolution for small threshold values (smaller signal slope)

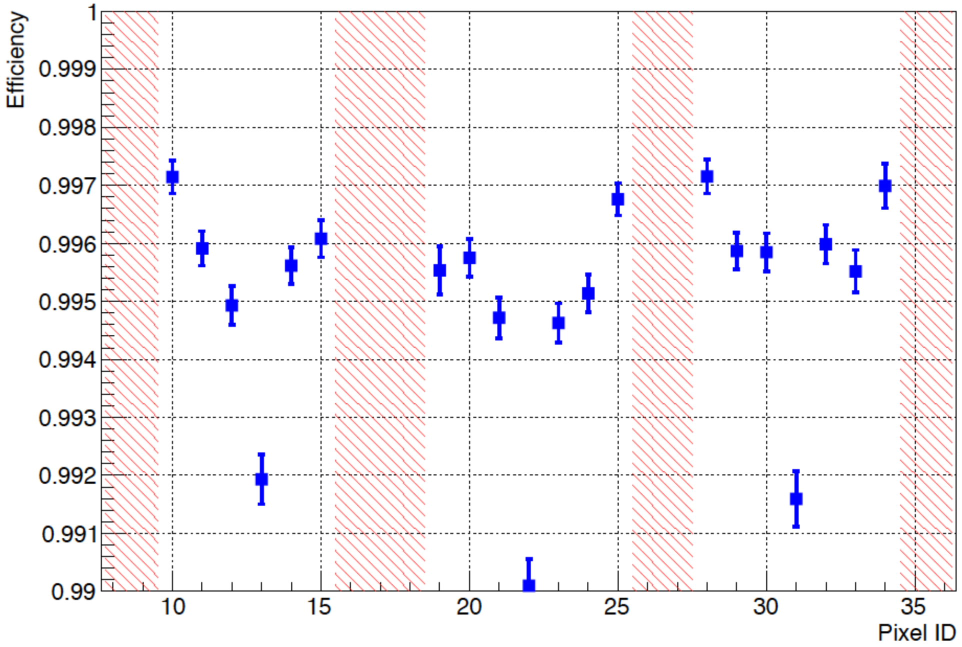
Bias voltage variation

- Time resolution measured as a function of bias
- Better than **150 ps** at 400 V
  - Still room for improvement at higher voltages



Detection efficiency

- Track fitting and extrapolated track impact position to the target detector calculated
- Very high efficiency (>99%)
  - Pixels in the outer region and dead pixels have been excluded (red hatched area)



Summary

- Excellent timing performance measured on thin hybrid pixel detectors (200 μm planar sensors)
- Time resolution better than 150 ps measured at 400 V with prototype ASIC
- Clear trend with bias voltage suggests that even smaller values can be obtained approaching carriers saturation
- Detection efficiency higher than 99%

3D sensors for timing

- Many interesting features compared to planar sensors:
  - Active thickness and collection distance are decoupled
  - Very low depletion voltage
  - Higher electric fields and charge carriers saturation achieved at very low voltage
  - Fast signal development, more "concentrated" in time, energy fluctuations collected almost simultaneously
  - Radiation hard
- but…
  - Larger capacitance
  - Columns not fully active (tilt angle to recover efficiency)
- S. Parker et al, IEEE Trans.Nucl.Sci. 58 (2011) 404-417

SPARES

Carriers drift velocity

- In “nominal” conditions we apply 300 V over 200 μm
- Electric field $1.5 \times 10^4\ \mathrm{V/cm}$
- Close to saturation but still room for improvement