IX SuperB General Meeting - Perugia

Thursday, 18 June 2009

Parallel - ETD I (09:00 - 10:30)

time	[id] title	presenter
09:00	[150] Fixed latency high-speed serial links with embedded SerDes.	RAFFAELE GIORDANO
09:20	[151] Jitter analysis on the recovered clock of Xilinx Virtex-5 embedded SerDes.	ALBERTO ALOISIO
09:40	[152] A possible readout interface.	MARCO BELLATO
09:55	[153] The SPECS field bus: a possible solution for on-detector ECS.	DANIEL CHARLET
10:10	[154] Discussion about ETD architecture	ALL