XIPE GPD BEE

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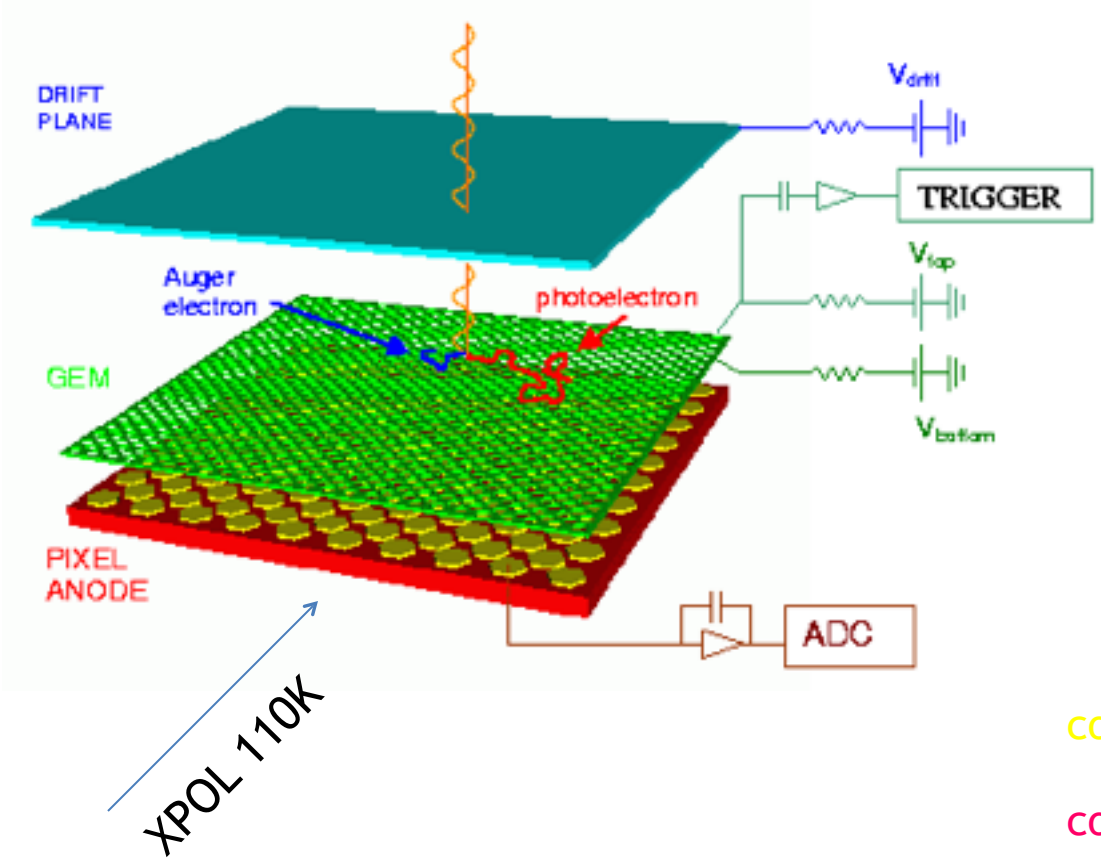
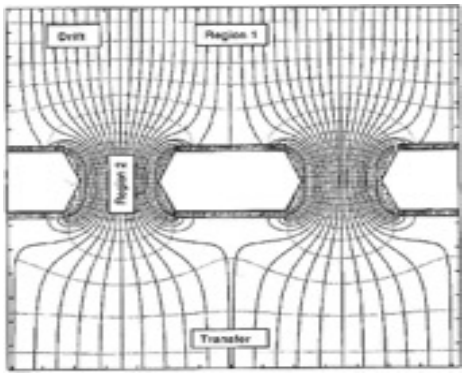
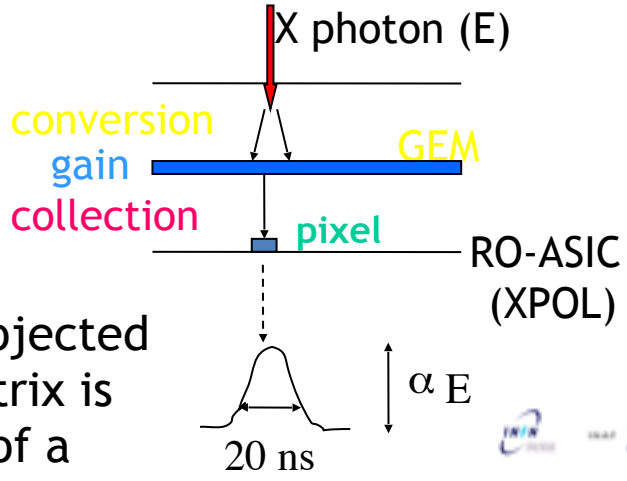
GPD RO ASIC



GEM electric field

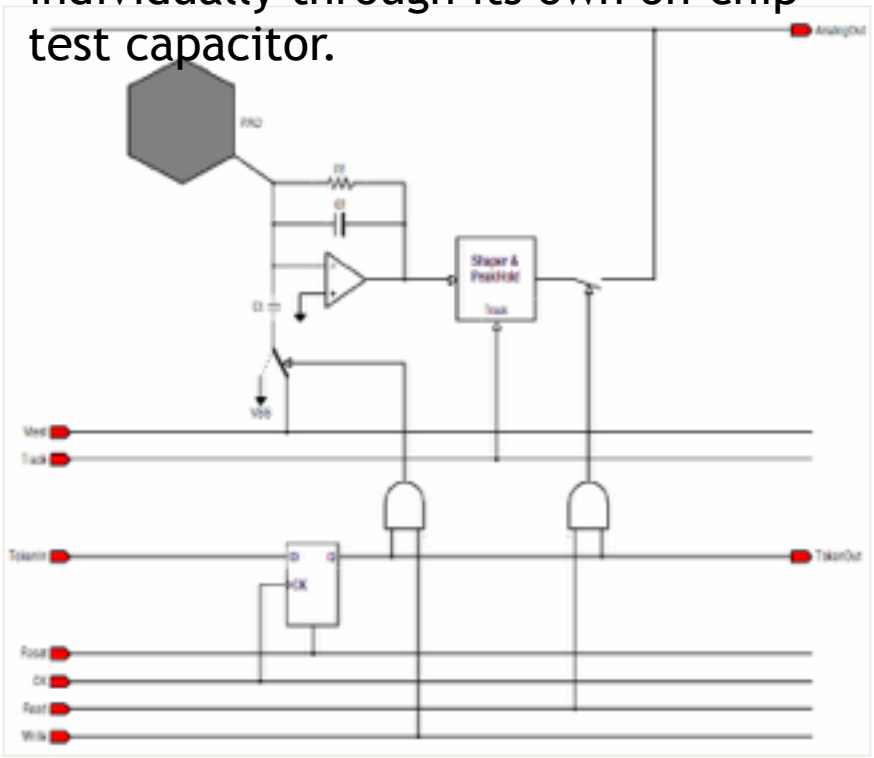


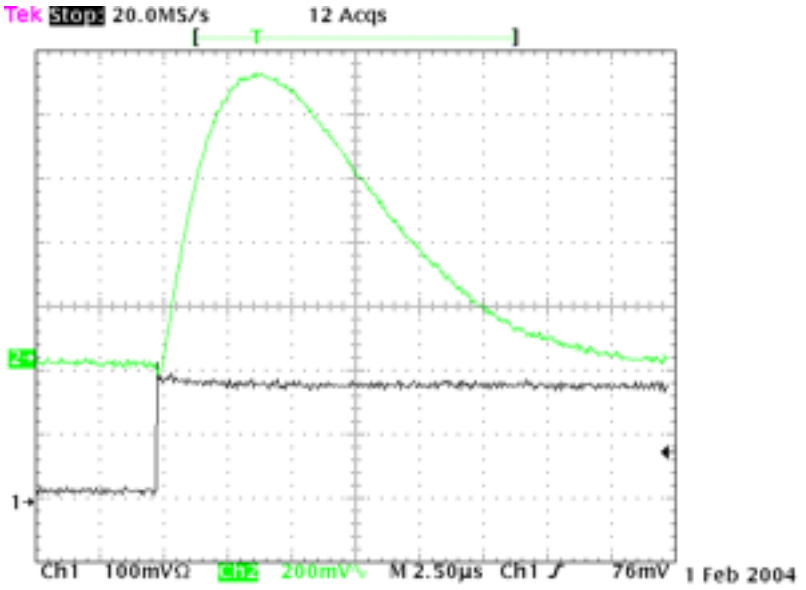


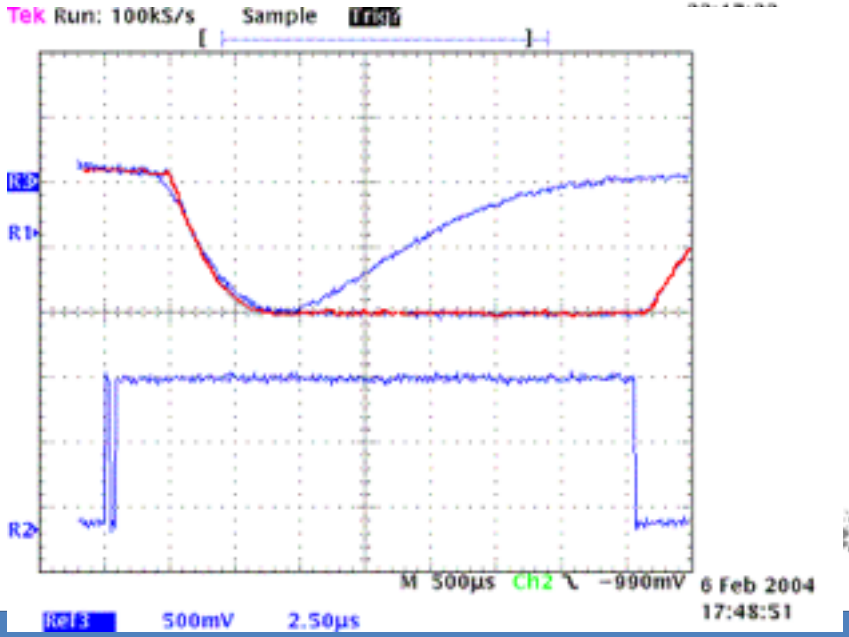
The charge (e-) genareted in the avalanche is projected onto the 50um pitch active pixel matrix. The matrix is indeed formed with the upper-most metal layer of a 0.18um CMOS ASIC

GPD RO ASIC

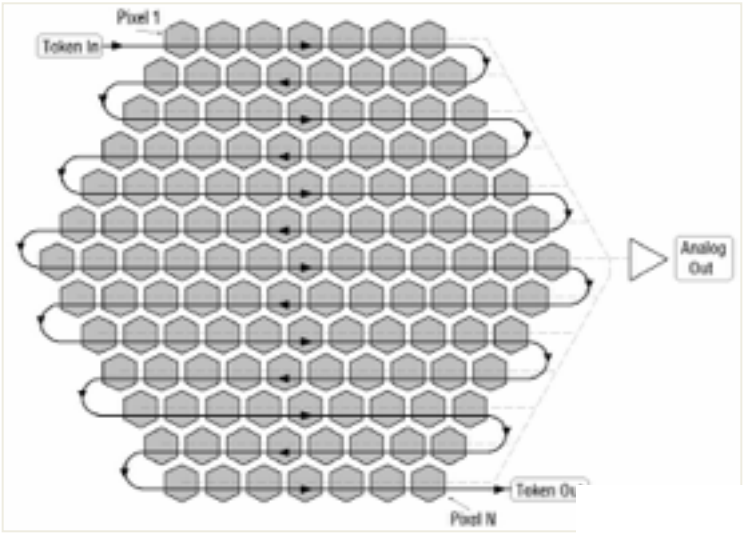
The matrix is made up of 105K active pixels. Each pixel is equipped with its own shaping chain, a Peak-Hold circuit can be triggered either from external trigger signal or internally by an auxiliary faster chain. A test charge can be injected in each pixel individually through its own on-chip test capacitor.



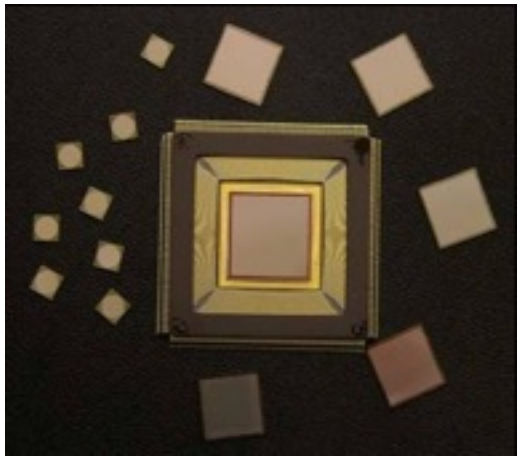


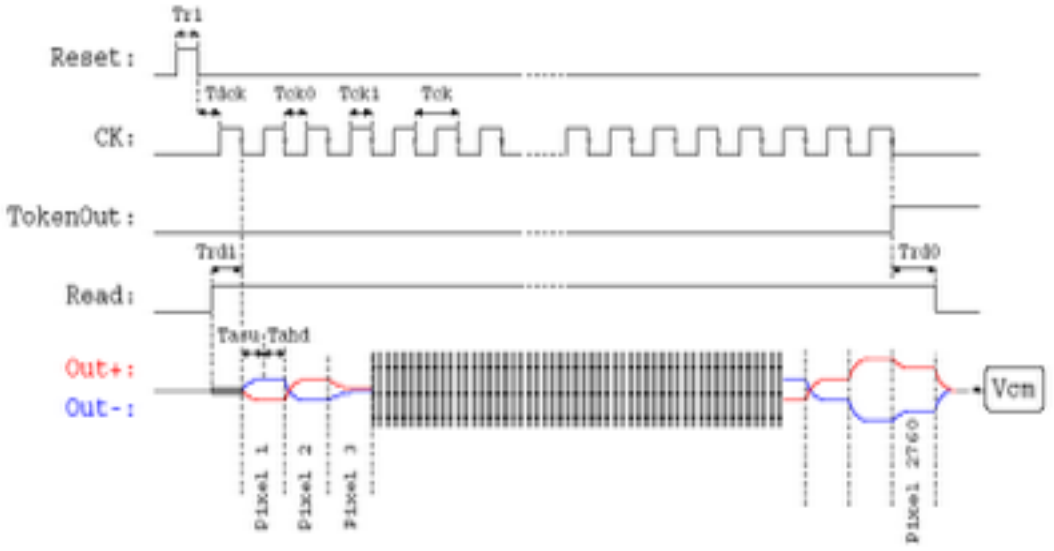


GPD RO ASIC

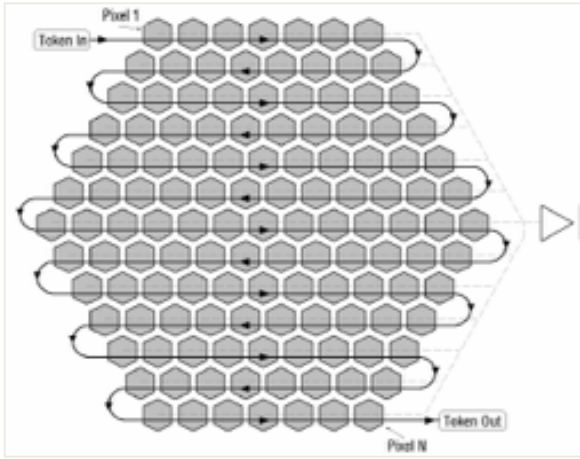


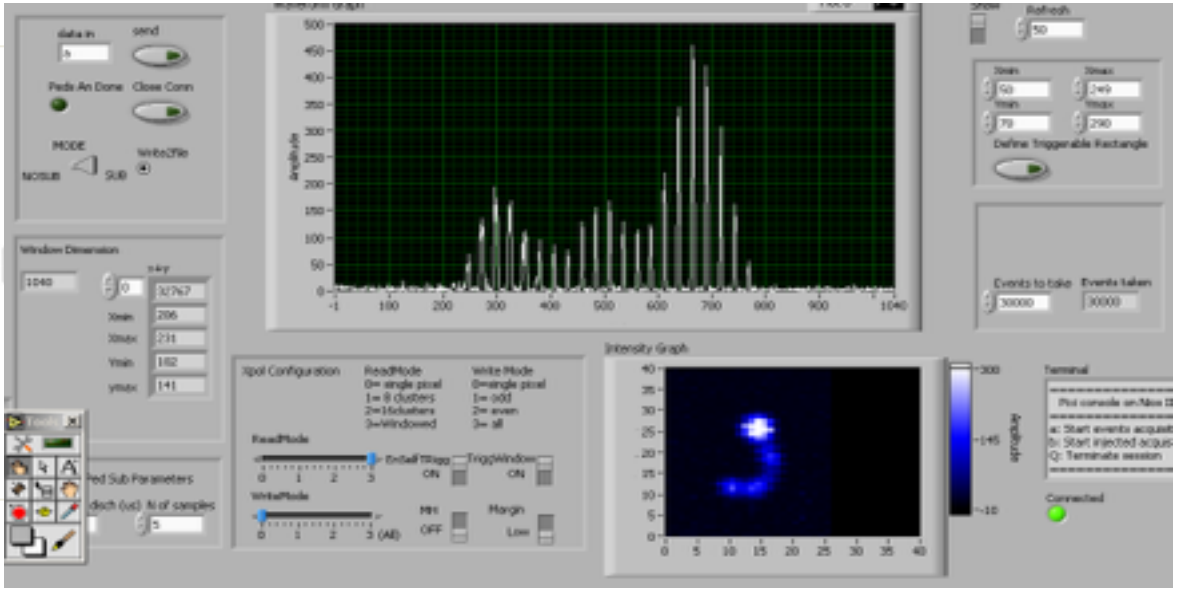
Once the signal peak has been captured, Pixels charge “content” can be retrieved in the
ReadOut sequence. During RO the Pixels amplifier outputs are “serially” connected to drive a differential output driver.
All the readout signal must be driven from outside (BEE).

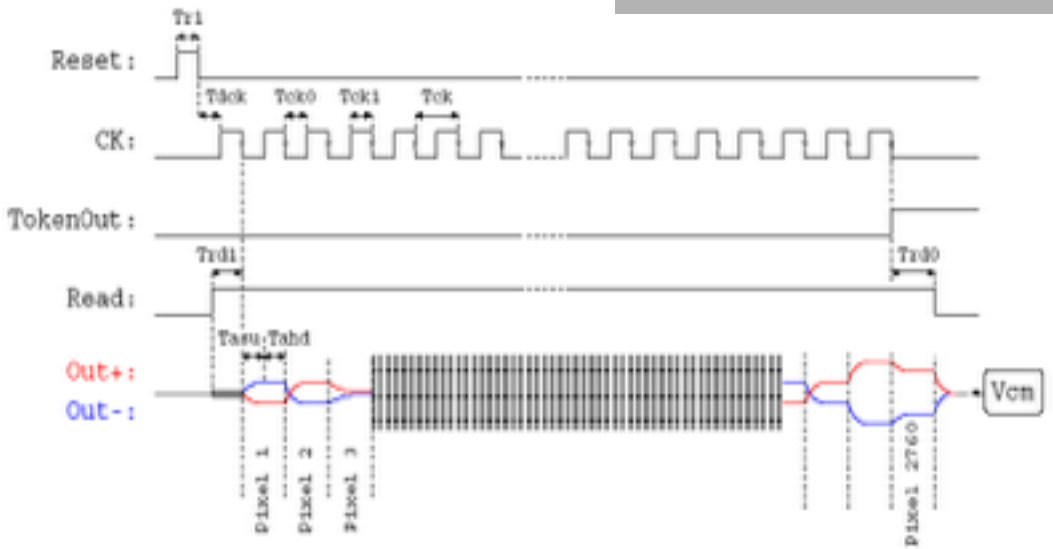




GPD RO ASIC


Pixel 1
Token In
Token Out
Pixel N




Tri
Reset:
Tack
Tok0
Tok1
Tck
CK:
TokenOut:
Trdi
Trd0
Read:
Tasu
Tahd
Out+:
Out-:
Vcm
Pixel 1
Pixel 2
Pixel 3
Pixel 2760

GPD RO ASIC

Pixel:
shaping time: 3-10us (externally adjustable)
full-scale linear range: FS = 5fC (30ke-)
line/column addressing
electrical stimulation for test purposes

Matrix organization:
300 (width=300x50um=15mm) x 352 (height=352x43.3=15.24mm) pixels
16 clusters of 300 x 22 = 6600 pixels each or 8 clusters of 300 x 44 = 13200 pixels each

Trigger:
user-selectable internal/external

Internal trigger functionality:
every 4 pixels (1 mini-cluster) contribute to a local trigger with a dedicated shaping amplifier
each pixel includes a masking function to disable its contribution to the trigger function

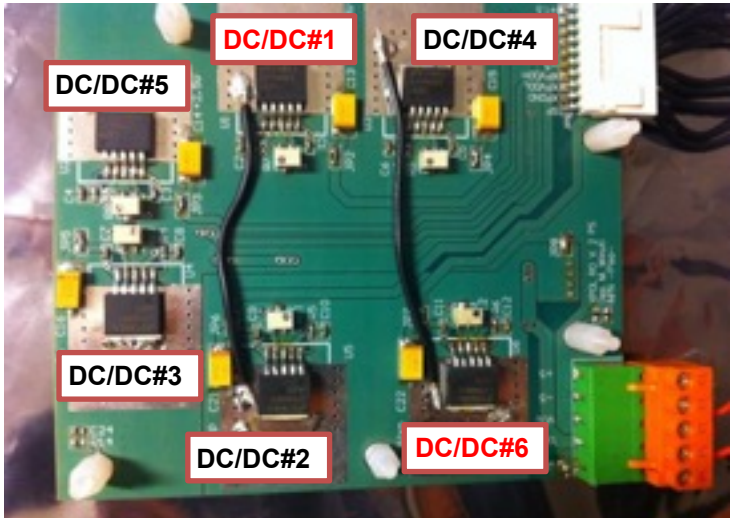
each of the 16 clusters' trigger level is defined independently to accommodate possible "region" offset the event is localized in a rectangle containing all triggered mini-clusters plus a user-selectable margin of 10 or 20 pixels (0.5mm or 1.0mm)
the chip calculates the resulting area of interest defined with coordinates (Xmin,Ymin) & (Xmax,Ymax) corresponding to the upper-left & lower-right corners, respectively.

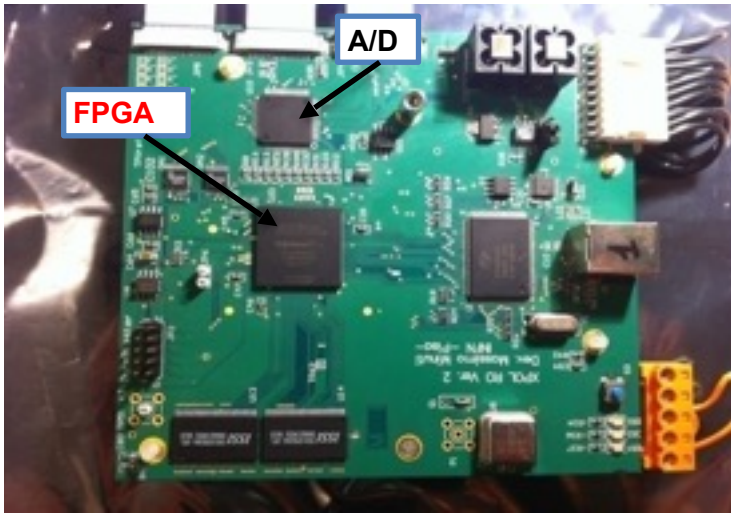
GPD RO ASIC

Readout:
Read mode 0 (direct addressing): the pixel is selected with its (X,Y) coordinates by entering its column (X) & line (Y) index binary code. This is the preferred readout mode during the electrical test of a single pixel.
Read modes 1 & 2 (standard readout): sequential within each cluster (line-by-line from top left down to bottom right), all 8 (mode 1) or 16 clusters (mode 2) read out in parallel (1 buffer amplifier per cluster).
Read mode 3 (advanced readout): sequential within the area of interest defined by coordinates (Xmin,Ymin) & (Xmax,Ymax).

Masking function:
the trigger contribution of any pixel can be disabled by direct addressing (the pixel address is entered with **Read mode 0 & Write mode 0**)
the masking bits are to be set at each power-up of the circuit
Analog outputs:
balanced output buffer (+/-1V) compatible with TI ADC ADS572x.
read mode 1, respectively 2 & 3 uses 8, respectively 16 & 1 analog buffer(s)
unused buffers are disabled to minimize power consumption
Digital controls:
a common TTL-compatible serial interface is used both to configure the chip and enter any (X,Y) address and to read out the impact rectangle coordinates (Xmin,Ymin) & (Xmax,Ymax)
external digital controls to be applied within the analog data acquisition timeframe (Write, TrigWindow, MaxHold) or analog readout process (Read, CK) use LVDS interfaces

GPD EGSE 0.0 (INFN Pisa)



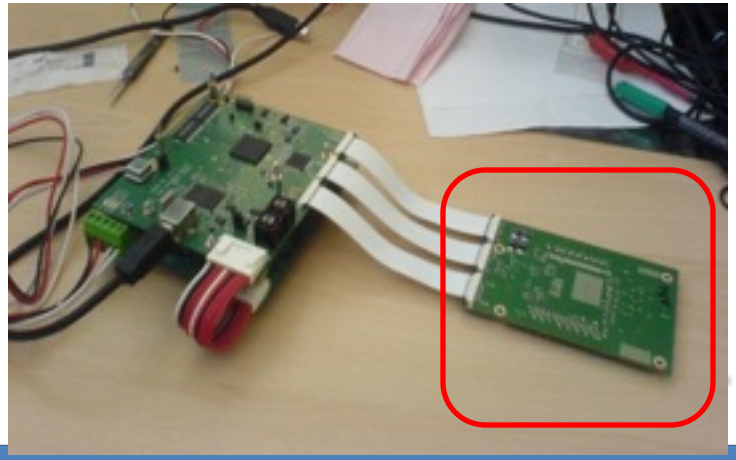


A first implementation of the GPD DAQ has been developed.

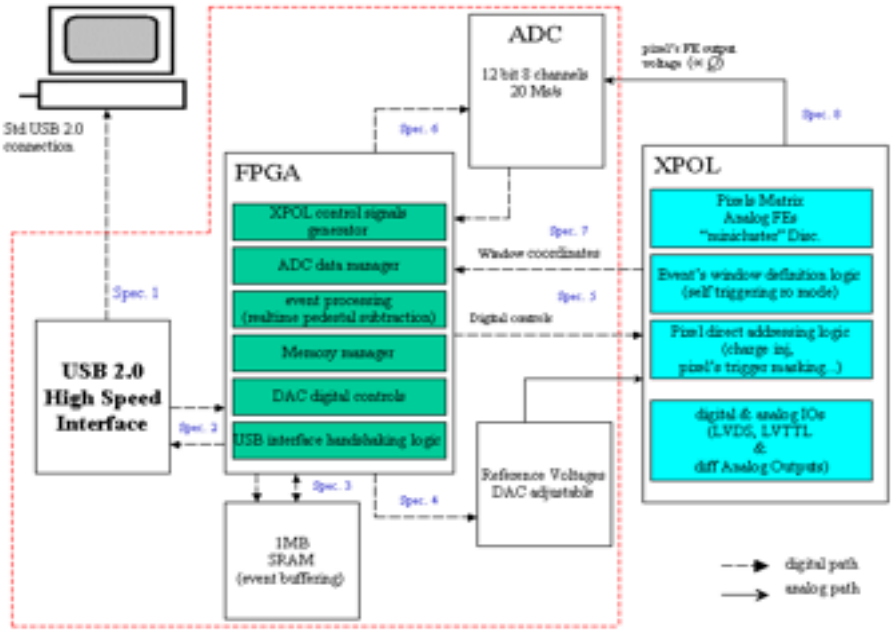
The EGSE ver. 0.0 is made up of two stacked boards (~10 cm X 10cm):

- Power Supply distribution Unit; mostly Linear Low drop-out voltage regulators;

- Sequencer Logic, Memories, AD conversions and references are non-space-qualified devices;



GPD EGSE 0.0 (INFN Pisa)

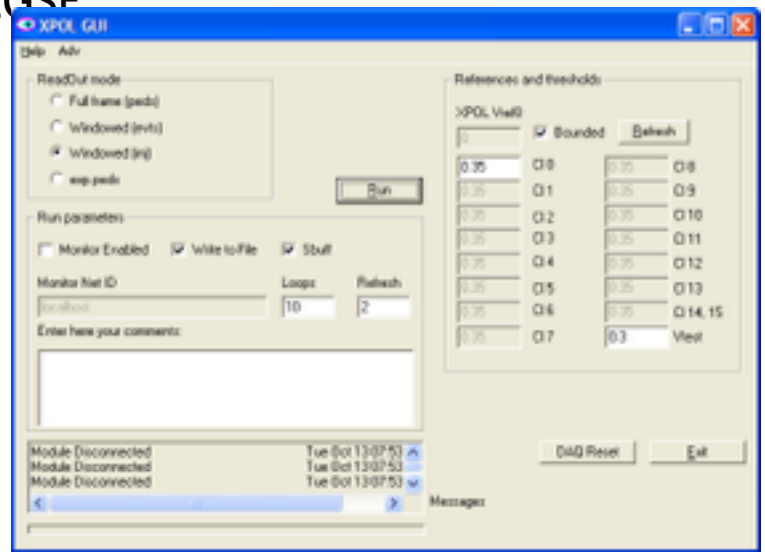


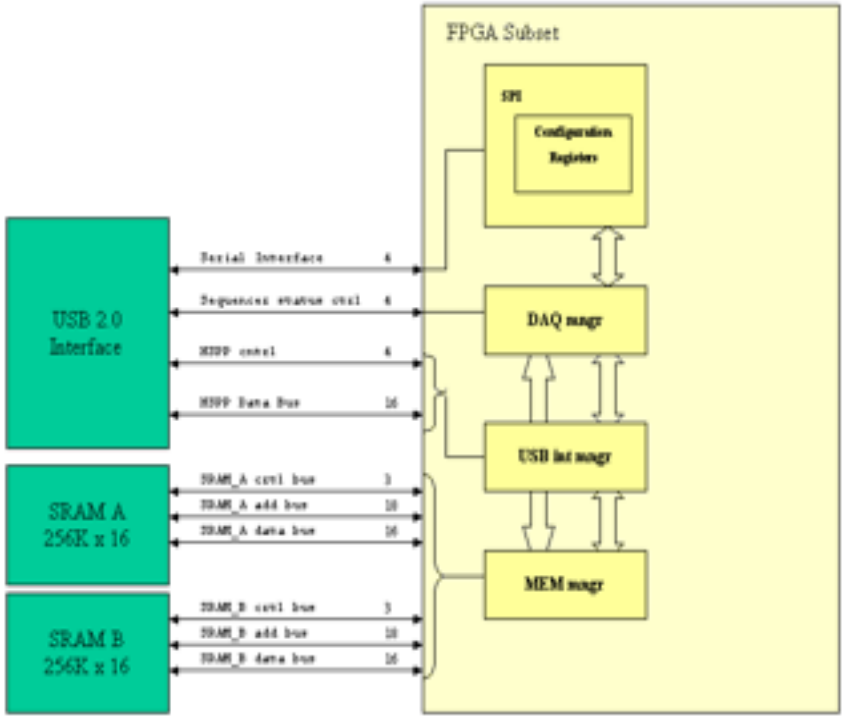
An FPGA is the core of the whole EGSE 0.0
It contains the logic to synchronize the XPOL readout sequence and A/D conversion. DACs
Are provided to set the discriminating thresholds levels. Additional functions for on-line pedestal subtraction are provided.
An on board 1MB SRAM memory is used for event buffering.
A 12 bit 20 Msps ADC is used for XPOL output A/D conversion.

Link	Type	Function	Wire counts
Spec 1	USB 2.0 High Speed	PC Link	4
Spec 2	LVTTL IO	High Speed Parallel Port	20
Spec 2	LVTTL IO	SPI	8
Spec 3	LVTTL IO	address, data & control BUS	74
Spec 4	LVTTL IO	DAC Controls	5
Spec 5,7	LVTTL IO	XPOL Interface	13
Spec 5	LVDS	XPOL Interface	14
Spec 6	LVDS	ADC dig. output	20
Spec 6	LVTTL	ADC controls	5
Spec 8	Analog differential (Vcm=1.5)	XPOL analog output	16

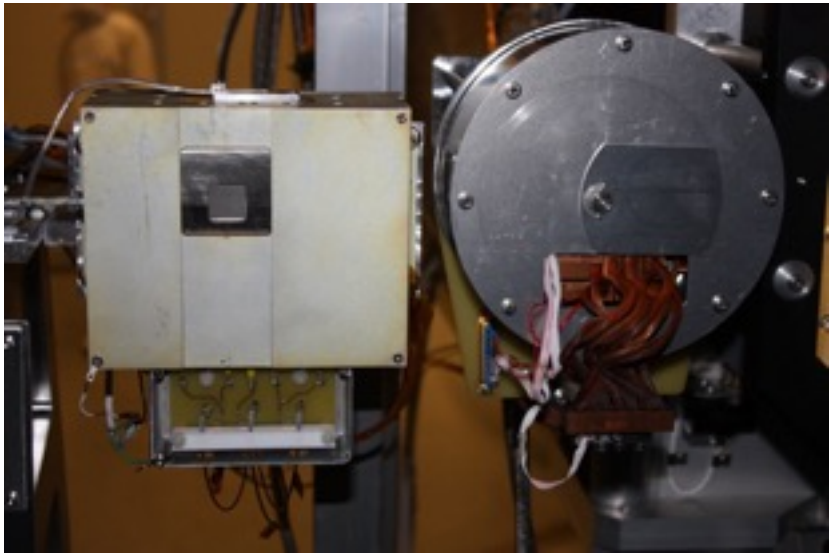
GPD EGSE 0.0 (INFN Pisa)

The EGSE 0.0 interfaces the world through a USB 2.0 High Speed interface, providing a 12MB/s data tranfer rate.
A register R/W access oriented interface allows interactions between a standard PC and the EGSE.





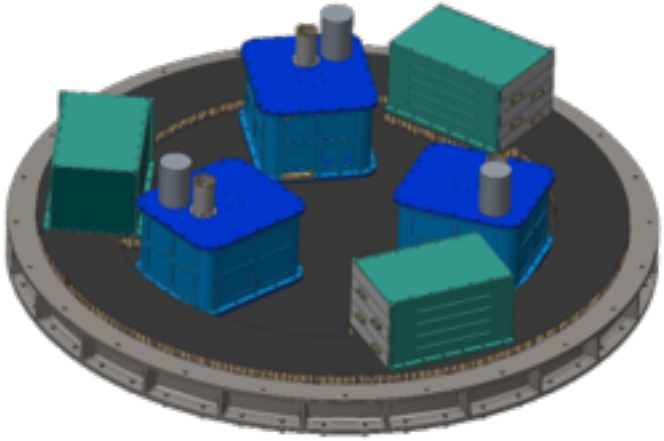
GPD EGSE 0.0 (INFN Pisa)

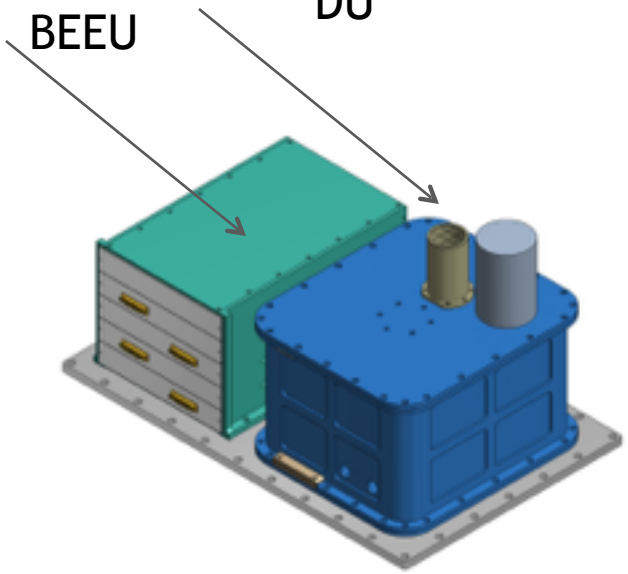


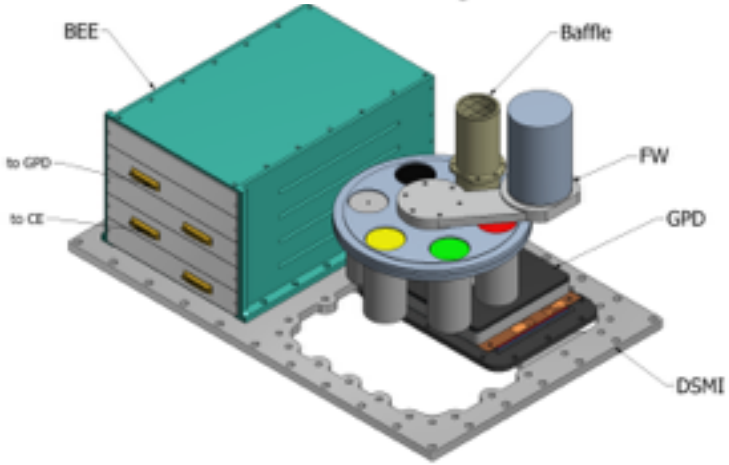
EGSE 0.0 successfully accompanied the GPD through all the Environmental test performed so far: Thermal cycles, Thermo-Vacuum (10-6 mbar), Heavy-Ions survival test…

XIPE Instrument Electronics

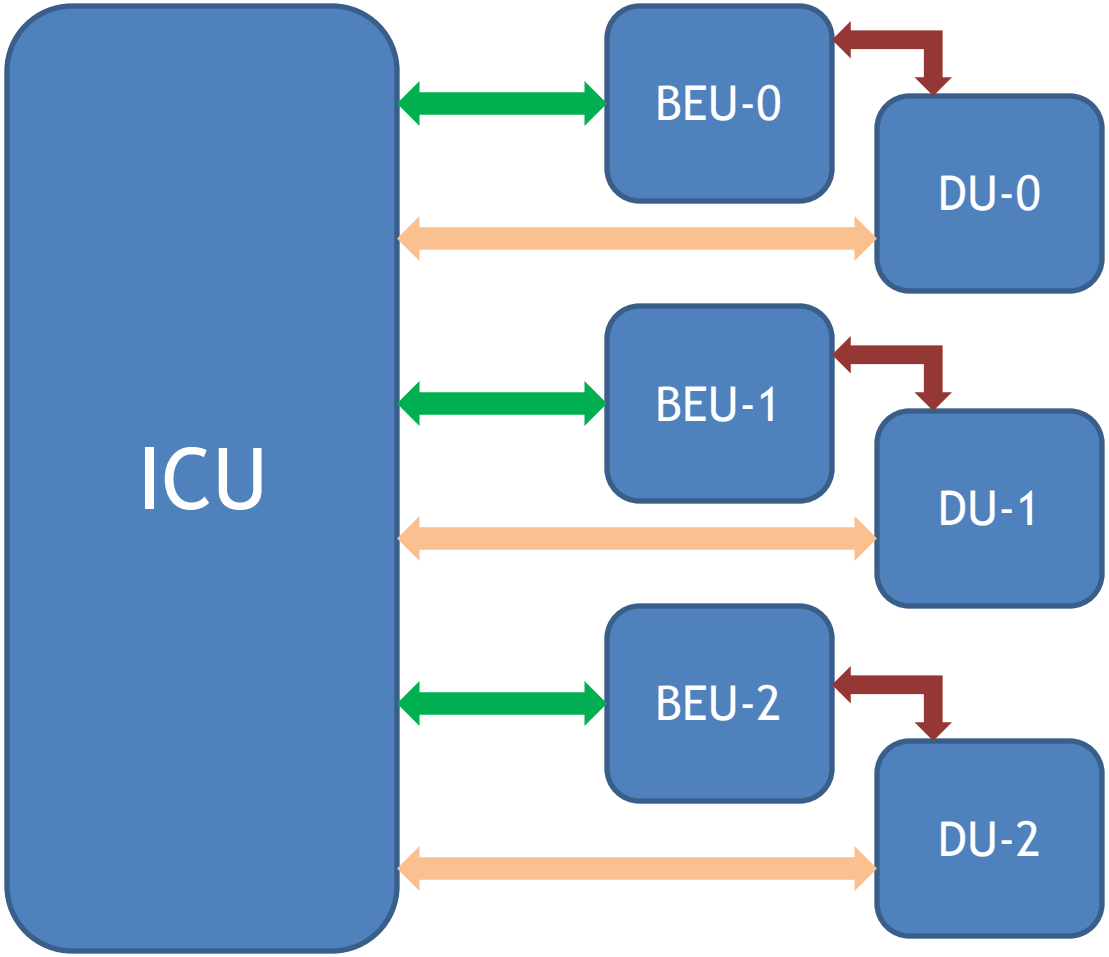
The XIPE focal plane



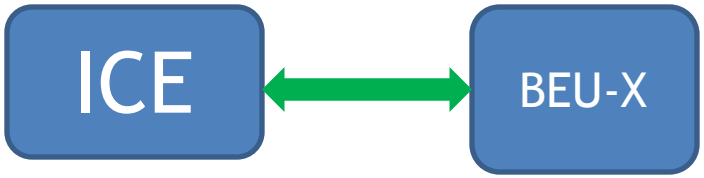




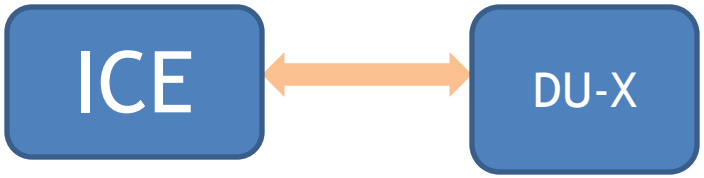
Electrical Interfaces



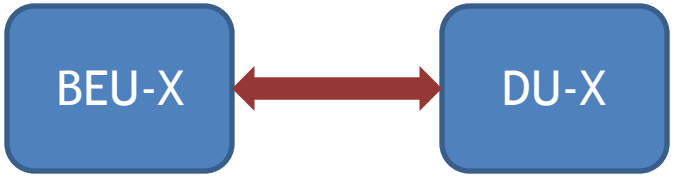
Electrical Interfaces



-) 2 X SpaceWire (Science DL + TCM Link)
-) OBT
-) Power Supplies (+/-15V, +/-5V)

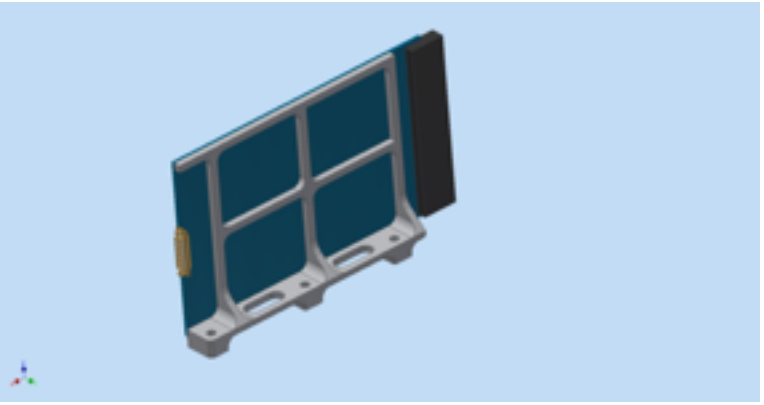


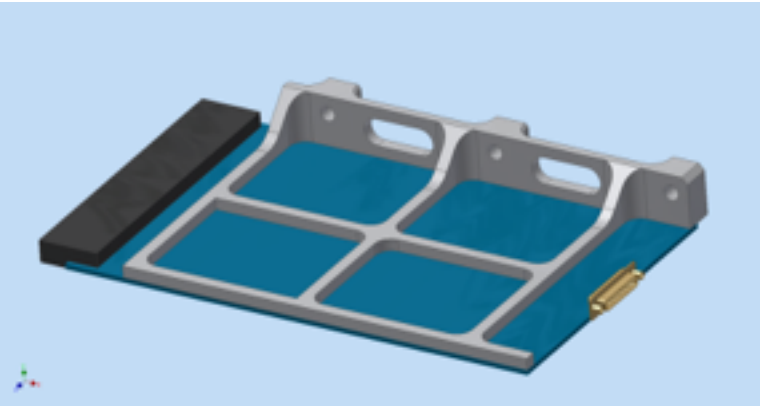
-) HKP (Temperature Sensors + Peltier Driving)
-) FW driving + Position Sensors (Hall + optical)

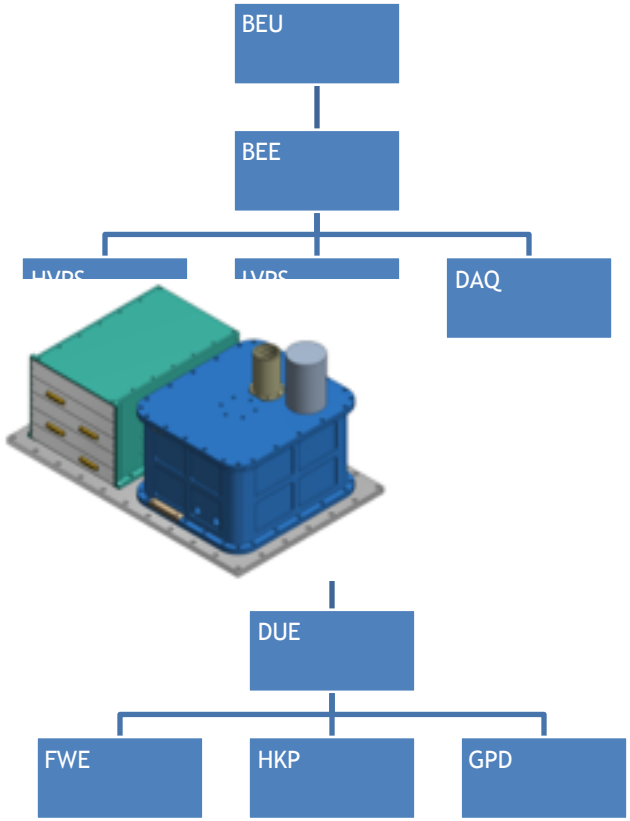


-) GPD Science Data Interface
-) GPD Configuration
-) GPD Bias (Gas Cell)
-) GPD LV Power Supplies

XIPE Instrument Electronics







SRC-PAS

INFN-PI

INFN-PI

UCL-MSSL

INFN-PI

INFN-PI

BEE electronics boards are uPCI 3U standard (20mm X 160mm X 100mm) . Bottom side is expected to be dedicated to Mechanical and Thermal interfaces.

BEE - HVPS

-) generates VTop, VBottom, VDrift;
-) hardware constraining of Vtop, (VTop - VBottom) to have inherent limits for the High Voltages;
-) Current Voltages Monitors
-) manages ramping up/down
-) manages S/C survival modes

Location:
2 uPCI slots in BEEU

Responsibility:
Space Research Centre of Polish Academy of Sciences (Poland)

Typical Output Voltage

V_{drift}= -2670 V
V_{bottom} = -400 V
ΔV_{t-b}= -470 V

Ranges

V_{drift}= -2000 / -3500 V
V_{bottom}= -100 / -600 V
ΔV_{t-b}= -300 / -550 V
(TBV)

BEE - LVPS

-) generates the BEEU supply low voltages from the ICU regulated +/-15, +-/5V;
-) [current monitors]
-) [manages S/C survival modes]

Location:
1 uPCI slot in BEEU;

Responsibility:
INFN-Pisa

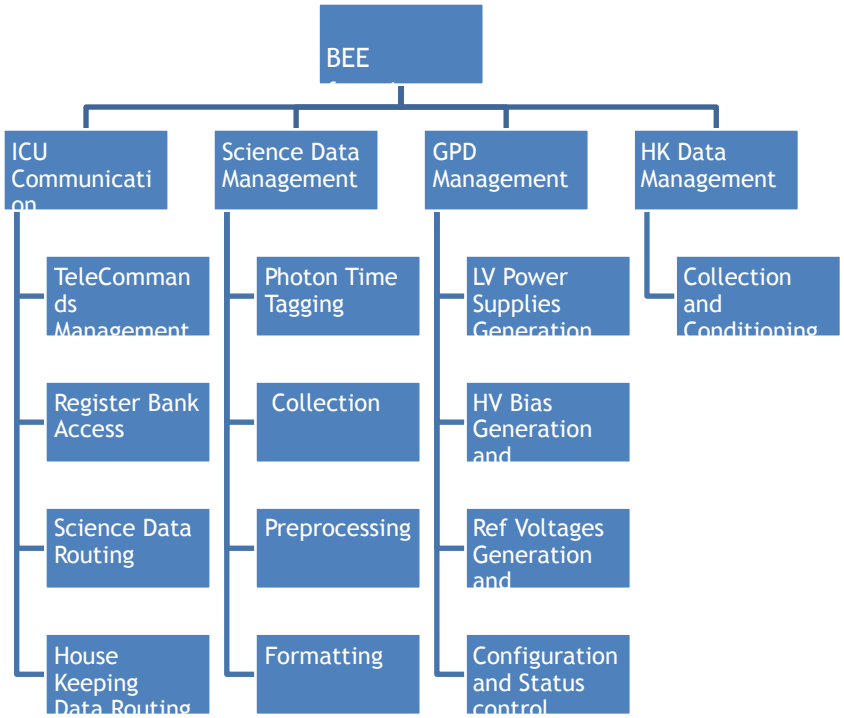
BEE - DAQ

-)ICU communication management;
-)Science data management;
-)House-Keeping data management;
-)GPD configuration, biasing and monitoring;

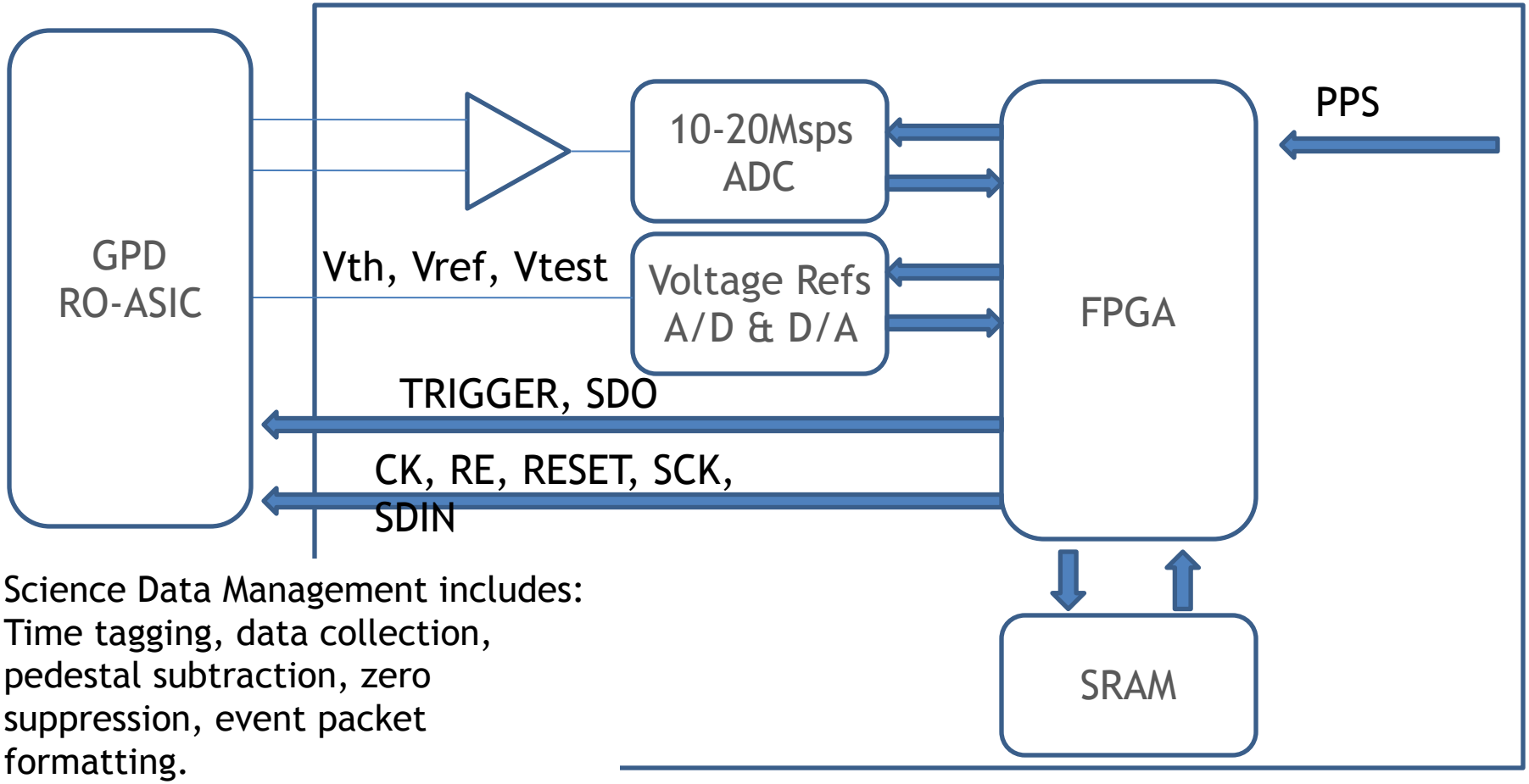
Location:
1 uPCI slot in BEEU

Responsibility:
INFN-Pisa

BEE – Functions Break Down

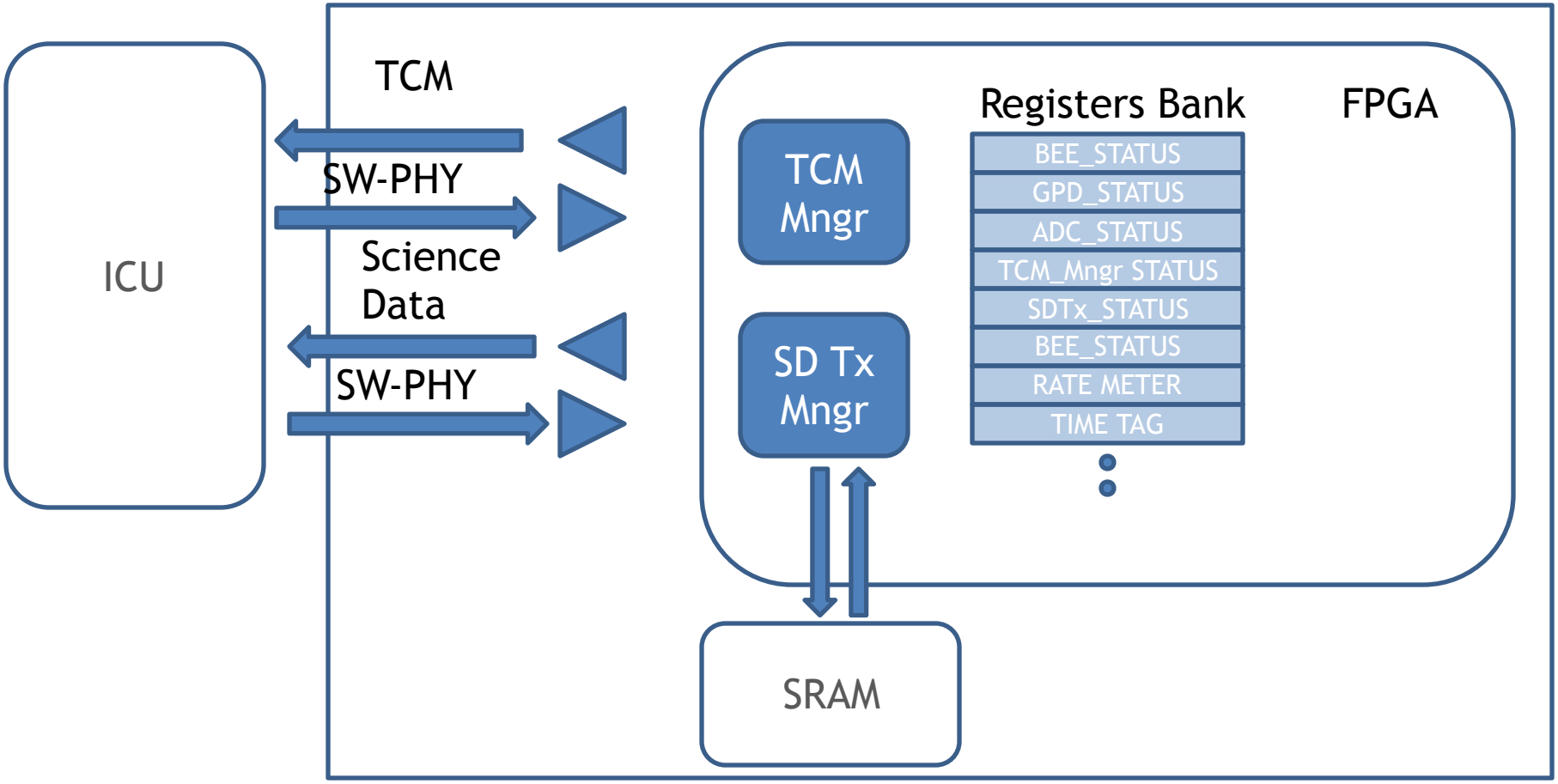


BEE – DAQ



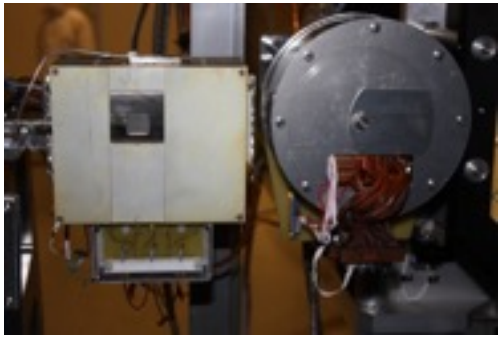
Science Data Management includes: Time tagging, data collection, pedestal subtraction, zero suppression, event packet formatting.

BEE – DAQ

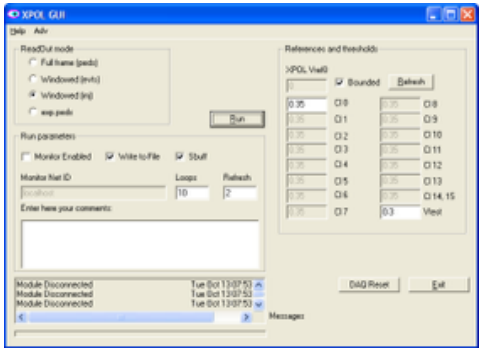

ICU
TCM
SW-PHY
Science Data
SW-PHY
FPGA
TCM Mngr
SD Tx Mngr
Registers Bank
BEE_STATUS
GPD_STATUS
ADC_STATUS
TCM_Mngr STATUS
SDTx_STATUS
BEE_STATUS
RATE METER
TIME TAG
SRAM

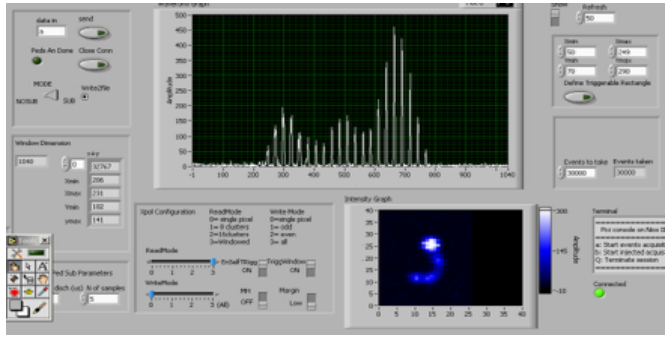
INFN PISA Activities

Site Visit (NASA) (Oct2016) goal:
-) GPD Assembly
-) DAQ software Update
-) GPD verification & tests



Further Goals (Nov2016):
-) FM BEE DAQ FPGA VHDL design and verification;
-) BEE DAQ schematics with SQ components;
-) BEE LVPS schematics with SQ components;
-) DU GPD RO board schematics with SQ components (Harnesses);
-) prototyping;





THANKS