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CiS Planar Sensor Technologies for Future High-Luminosity-LHC Upgrades

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Planar hybrid silicon sensors are a well proven technology for past and current particle tracking detectors in HEP experiments. However, the future high-luminosity upgrades of the inner trackers at the LHC experiments pose big challenges to the detectors. The first challenge is an expected radiation damage level of $2 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$. The second challenge is the large detector areas which have to be built as cost efficient as possible, i.e. it is aimed for low-cost and large-sized sensor material.

Various new wafer processing, electroplating or mask-less & electro-less Under-Bump-Metallization and bump deposition and mounting technologies are currently developed at CiS.

Our focus is to coordinate the technologies in order to cope with the application challenges on the one side and the cost efficiency on the other side. The target costs have to match with the full value chain of hybrid modules for inner tracker upgrades and industrial use.

The CiS research institute has accomplished a proof-of-principle run with n-in-p ATLAS-Pixel sensors where cavities are etched to the sensors back side to reduce its thickness. The membranes with areas of up to $\sim 4 \times 4 \text{ cm}^2$ and target thicknesses of 100 and $150 \mu\text{m}$ feature a sufficiently good homogeneity across the whole wafer area. Various technological approaches to realize edge-less sensor layouts, especially using active edges are developed.

For Pixel sensors different new concepts for “removable” bias grids will be investigated.

It will also be presented our new opportunities to realize under-bump-metallization, copper pillars, bump deposition using Lift-off mask or stencil printing or mask-less & electro-less processes.

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