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## Performance of thin n-in-p planar pixel modules with and without active edge

*Monday, 6 June 2016 15:00 (20 minutes)*

New productions of thin n-in-p pixel sensors designed at MPP will be presented. Sensors of thicknesses of 100 and 150  $\mu\text{m}$  have been produced at ADVACAM and CiS and interconnected to FE-I4 chips. At ADVACAM SOI wafers were employed, while at CiS anisotropic KOH etching was carried out to create backside cavities in the wafer leaving thicker frames around each single structure.

To maximize the active area of the thin sensors, slim and active edges were implemented in the sensors of the ADVACAM production. The evaluation assemblies have been measured by means of radioactive source scans and beam tests and the results on charge collection - and edge efficiency will be discussed. The power dissipation for thin sensors irradiated at a fluence of  $1\text{e}16$  will be evaluated and the performance after irradiation up to  $1\text{e}16$  in terms of hit efficiency of different sensor thicknesses in the range of 100 to 270  $\mu\text{m}$  will be discussed.

Previous investigations of different punch-through designs have led to the optimization of the pixel biasing structure to limit the related loss of efficiency at high levels of irradiation. This is particularly important for the sensors to be interconnected to the new RD53 chip, given the reduced cell size of  $25\times 100$  or  $50\times 50 \mu\text{m}^2$ . A pixel sensor production at HLL on SOI wafers where these changes were implemented has been recently completed and the preliminary electrical characterization of the RD53 sensors will be discussed.

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