Performance of thin n-in-p planar pixel sensors with and without active edge

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Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

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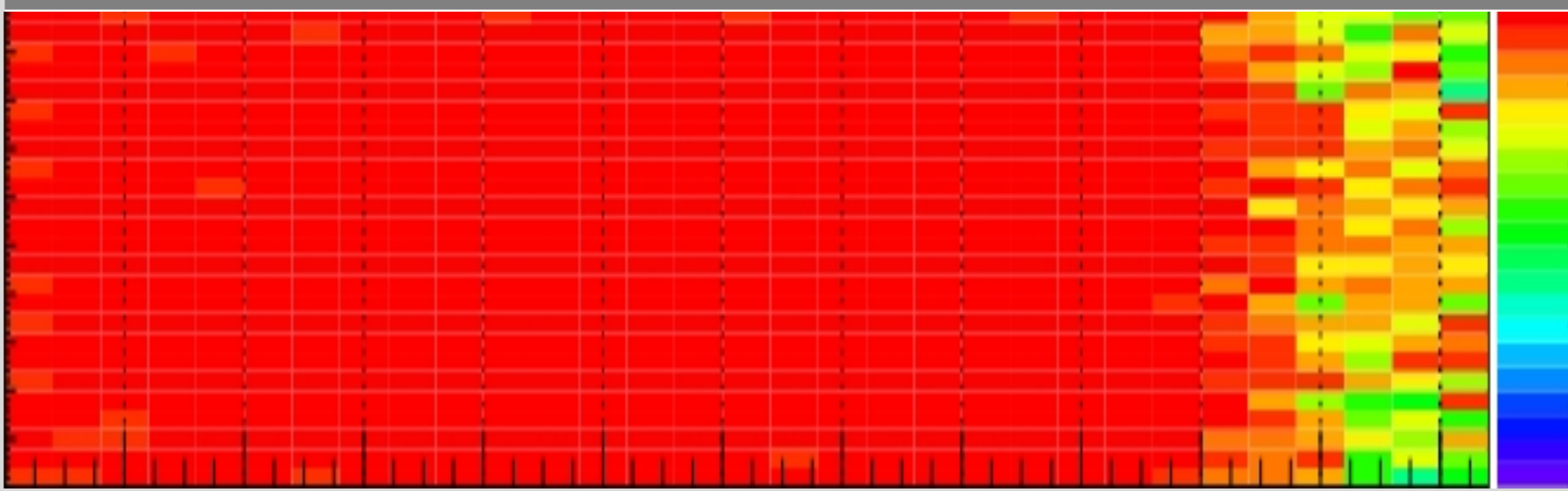

Overview

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- **New ADVACAM production for thin n-in-p planar pixels sensors with active edges**
  i. sensor thicknesses: 100 and 150 µm

- **Test-beam studies with n-in-p planar pixels in (un-) irradiated modules**
  i. with different sensor thicknesses from 100 to 270 µm
  ii. at different irradiation levels up to $1x10^{16}\ n_{eq}/cm^2$

- **Grazing angle studies with n-in-p planar pixels**
  i. unirradiated module at high Φ (80˚ incidence angle (η~2.4))

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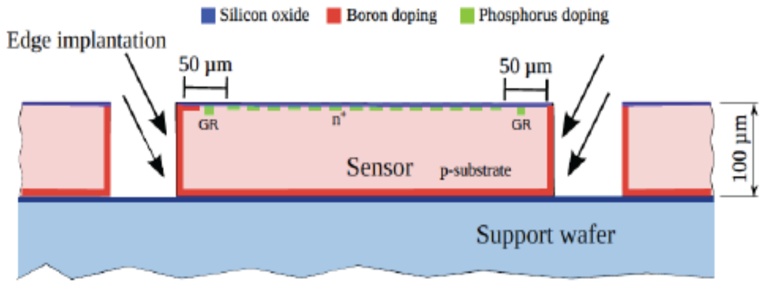
New thin production at ADVACAM

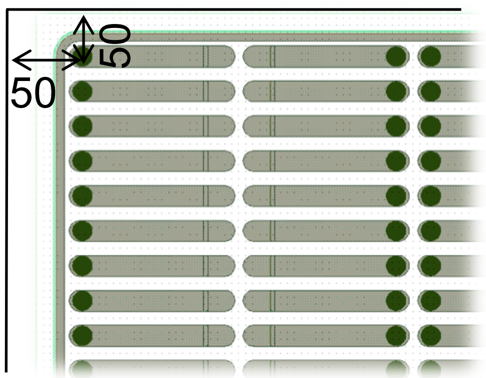
ADVACAM Production

- Second SOI production of active edge pixels at ADVACAM
- 15 6" wafers on p-type FZ material
- Thickness 50, 100 and 150 μm



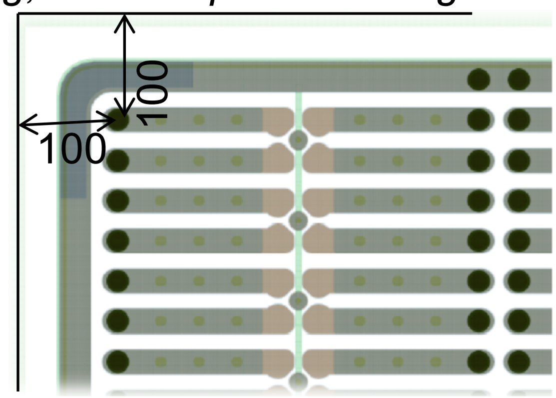
FE-I4s *with*
50 μm edge,
one GR, no punch-through structure

Active edge



100 μm edge,
Bias Ring, external punch-through structure

Slim edge



In Collaboration with Glasgow, Göttingen, LAL, CLIC and Geneva University

RD50 project: 2014/03

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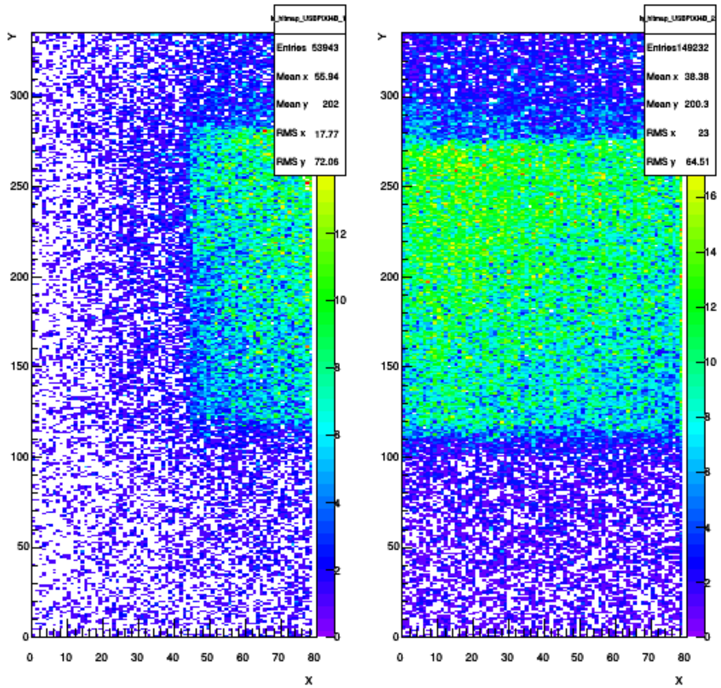
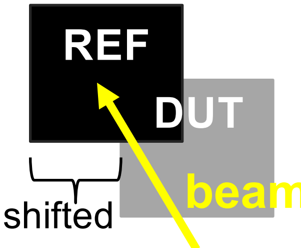
Testbeam studies of unirradiated modules (ADVACAM)

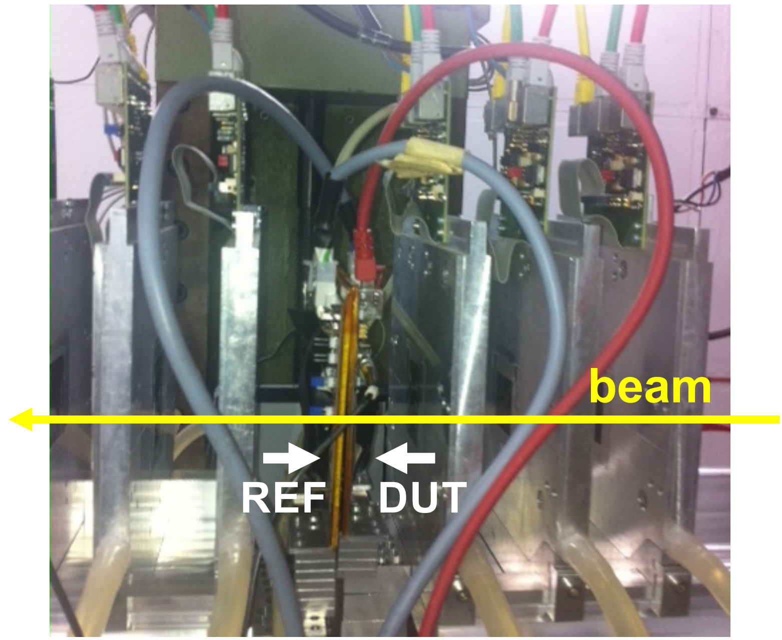
Test beam set-up (slim and active edge, 100 μm thickness)

- Hit map of the online monitor and photo of the set-up

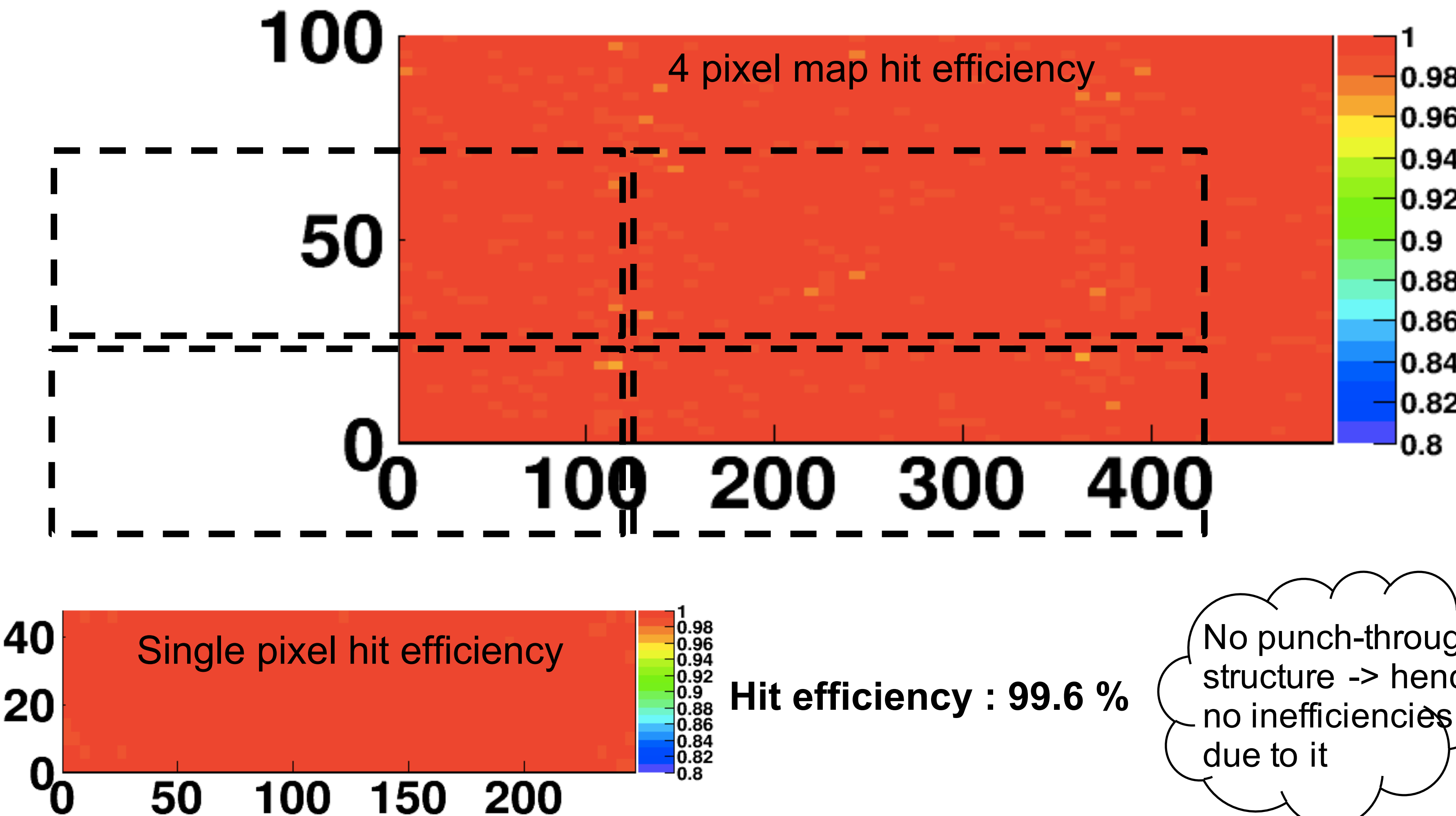




DUT is placed such that the beam only traverses the edge region



In-pixel hit efficiency at 40 V



Hit efficiency : 99.6 %

No punch-through structure -> hence no inefficiencies due to it

In-pixel hit efficiency at edge

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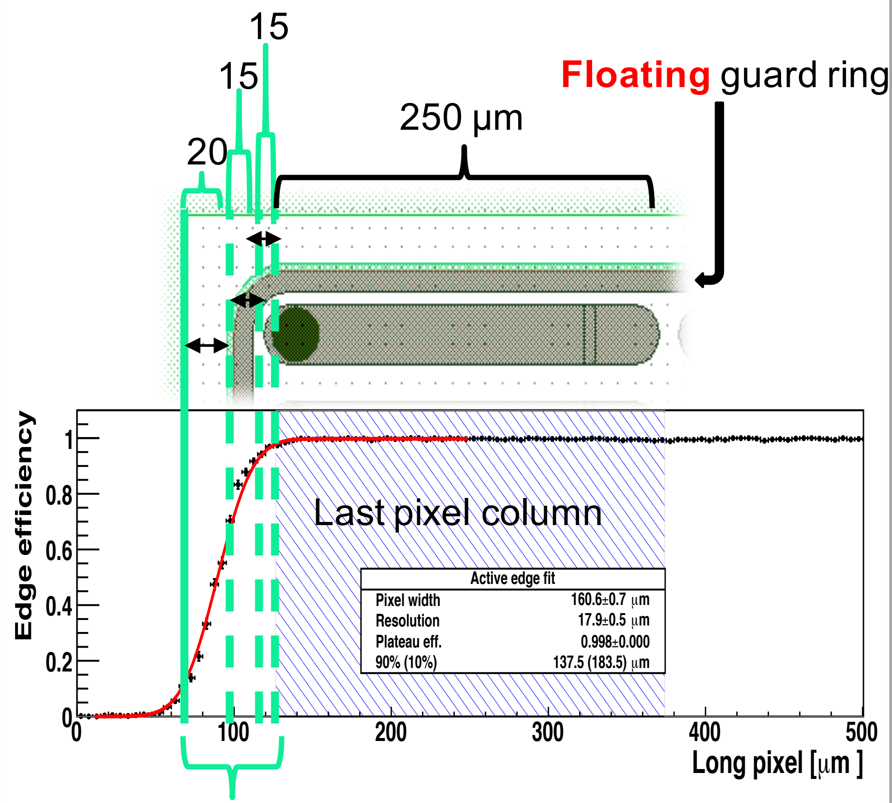
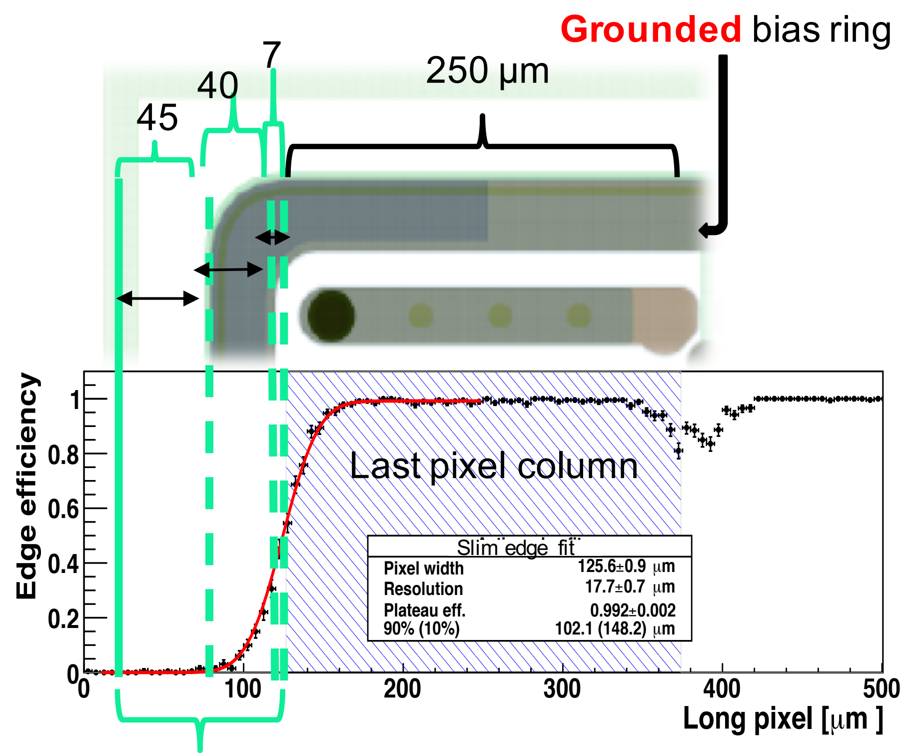
Active edge



Slim edge



Smearing due to resolution of ~18 µm

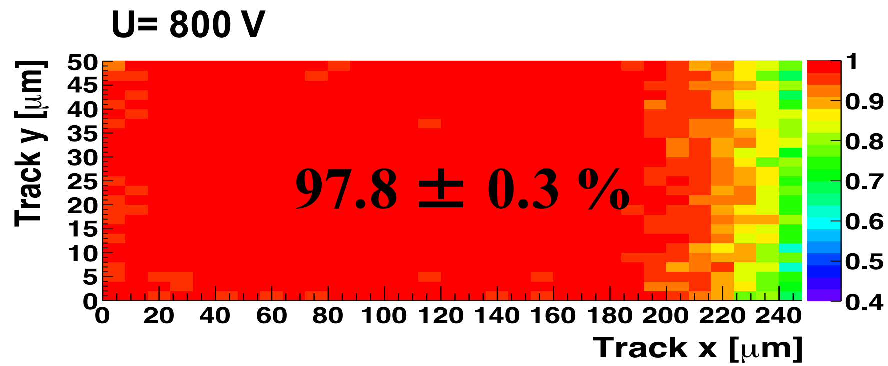
Testbeam studies of irradiated modules

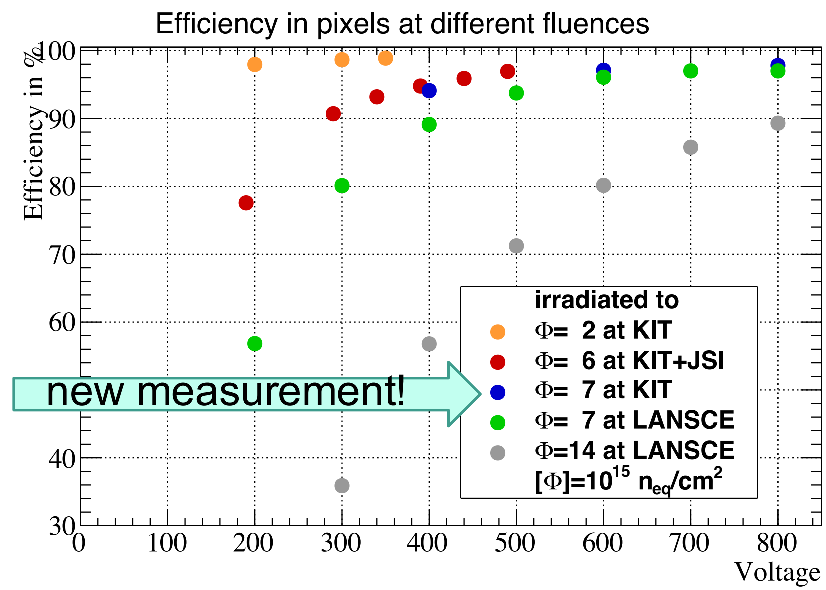
Comparison of performance at different fluences

In-pixel hit efficiency at $7x10^{15}$ n_{eq}/cm^2

CiS2 production:

- Geometry:
  - Thickness: **200 µm**
  - Standard punch-through design
- Tuning:
  - Threshold: 1400 ke
  - ToT: 6 to 4 ke
- Irradiated at $7x10^{15}$ n_{eq}/cm^2 at KIT



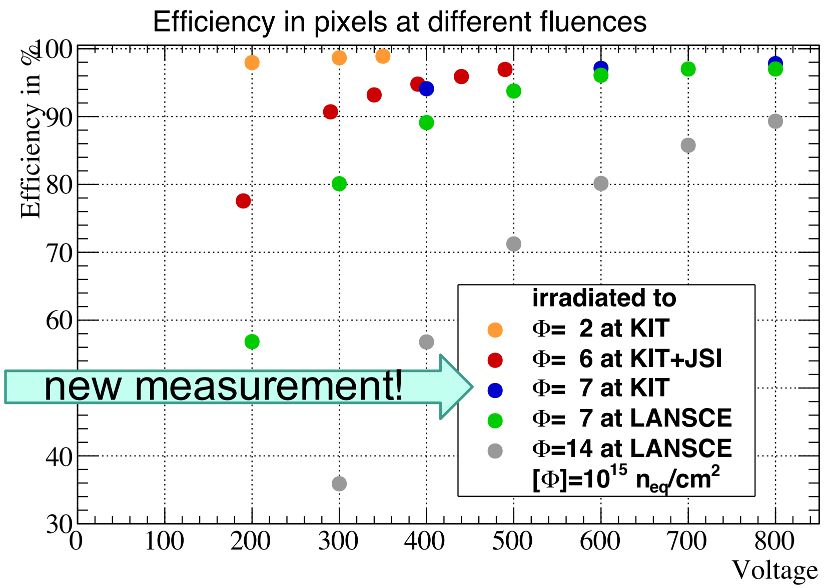


Comparison of efficiencies at 7×10^{15} n_{eq}/cm^2

Irradiation at KIT and LANSCE

	400 V	600 V	800 V
at KIT	94.1 %	97.1 %	97.7 %
at LANSCE	89.1 %	96.1 %	97.0 %

Δ=0.3 %



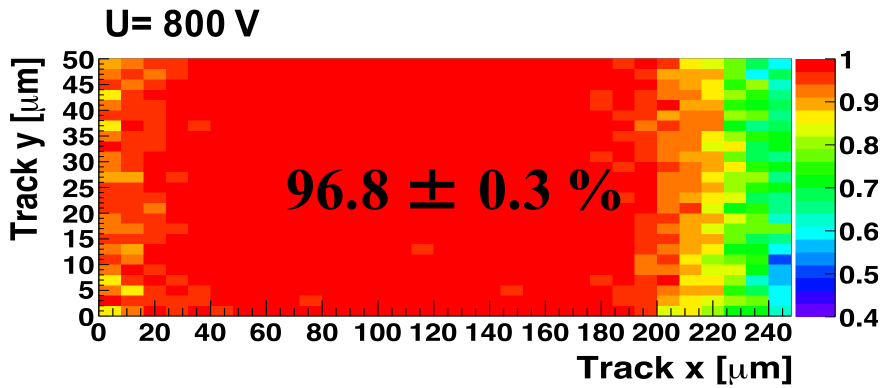
Slightly lower efficiency values achieved after irradiation at LANSCE

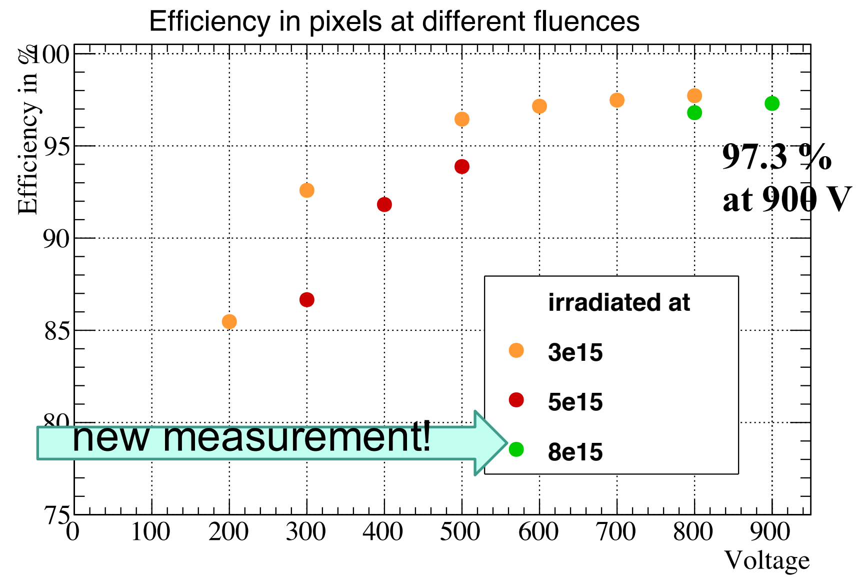
- probably caused by the non uniform and underestimated irradiation at LANSCE

In-pixel hit efficiency at 8×10^{15} n_{eq}/cm^2

CiS3 production:

- Geometry:
  - Thickness: **270 µm**
  - Standard punch-through design
- Tuning:
  - Threshold: 1400 ke
  - ToT: 6 to 4 ke
- Irradiated at 8×10^{15} n_{eq}/cm^2 at KIT

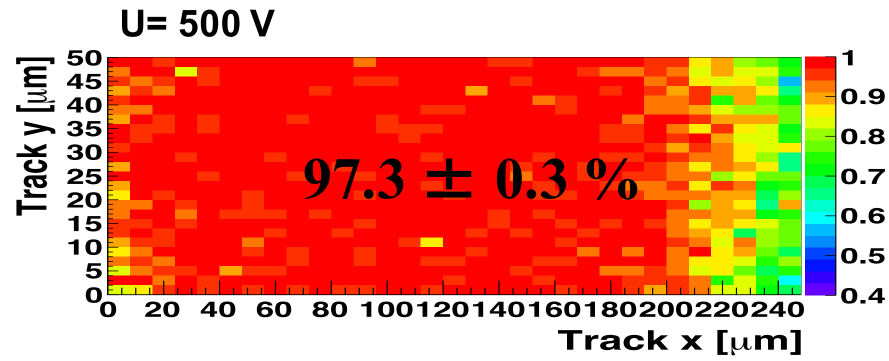


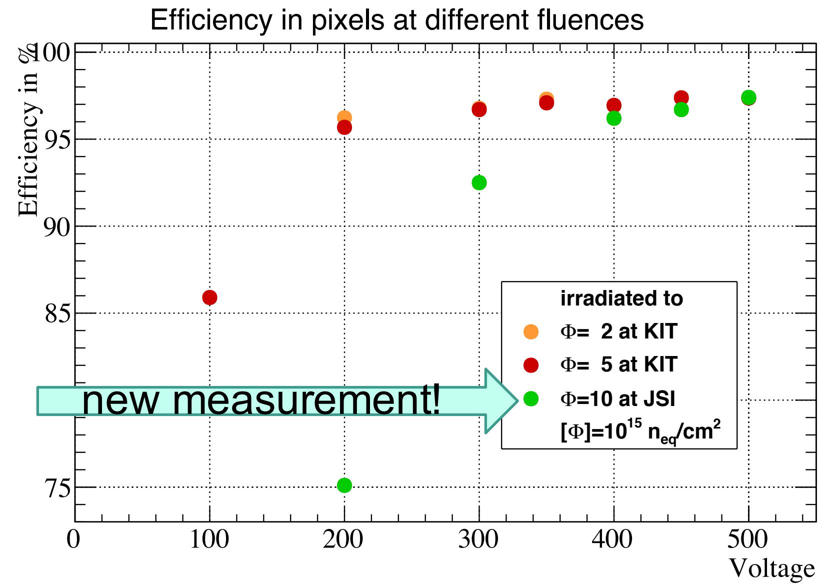


In-pixel hit efficiency at $1x10^{16}$ n_{eq}/cm^2

VTT production:

- Geometry:
  - Thickness: **100 µm**
  - Standard punch-through design
- Tuning:
  - Threshold: 1300 ke, ToT: 6 to 6 ke
- Irradiated at $1x10^{16}$ n_{eq}/cm^2 at JSI





- saturated efficiency values of 1e16 similar to values at lower fluences
- significantly lower efficiencies at 200 and 300 V for 1e16

Power dissipation at fluences up to $1x10^{16}$ n_{eq}/cm^2

for a 100 µm thick sensor

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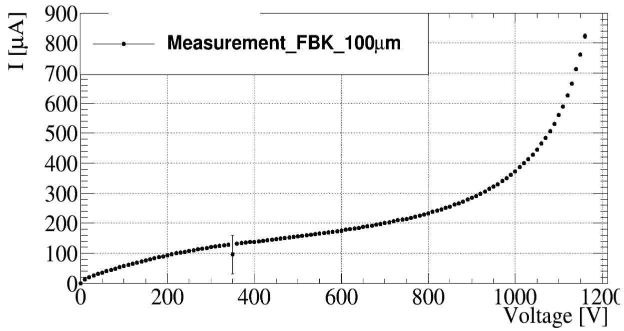
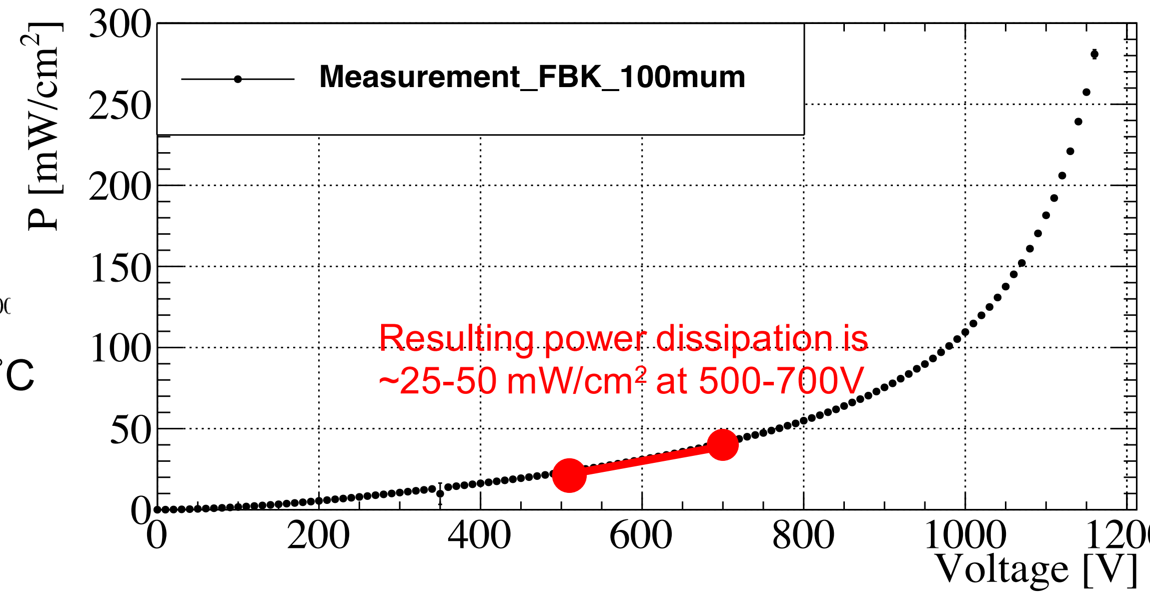


IV curve of bare sensor at -25˚C irradiated to **$1x10^{16}$ n_{eq}/cm^2** at JSI



Power dissipation per area curve of bare sensor at -25˚C irradiated to **$1x10^{16}$ n_{eq}/cm^2** at JSI

- The possible range of operation bias voltage for a pixel module with a 100 µm thick sensor is **500-700 V**
- The resulting power dissipation at 500-700 V is **~25-50 mW/cm^2** including safety factor at $1x10^{16}$ n_{eq}/cm^2 irradiation

Grazing angle technique employing modules with a 50x250 μm^2 pixel pitch

Testing at high phi

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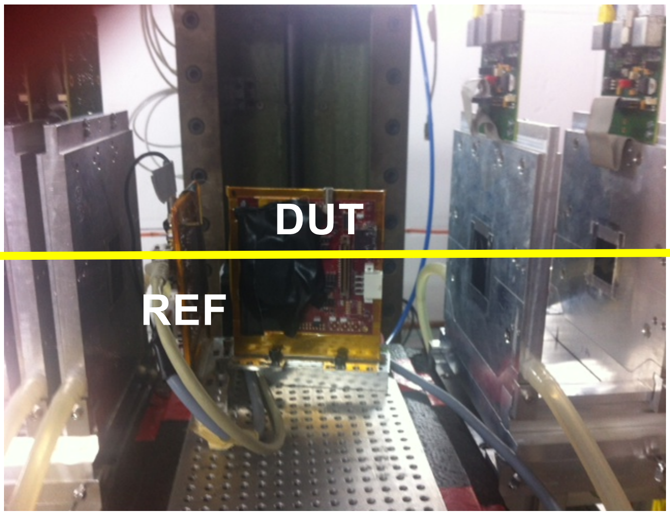
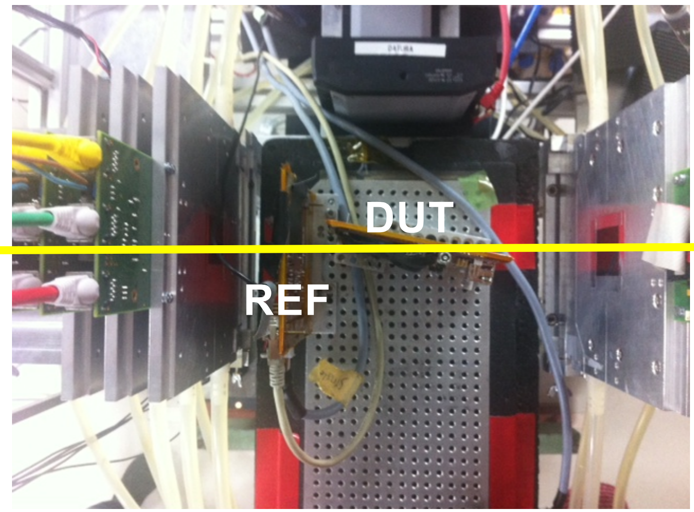
- High Φ set-up with a not irradiated n-in-p FE-I4 module of 150 μm sensor thickness at high Φ (80°) and a reference plane, perpendicular to the beam

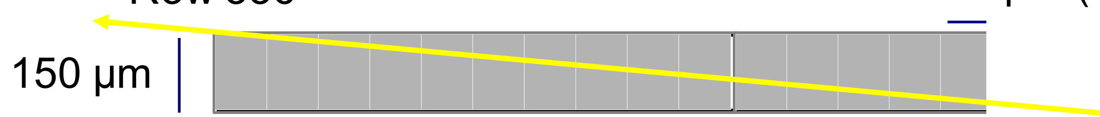


Side view



Top view

Back side of the sensor
Row 336



Front side of sensor
Row 0

TB DESY
March '16

Distribution of cluster width

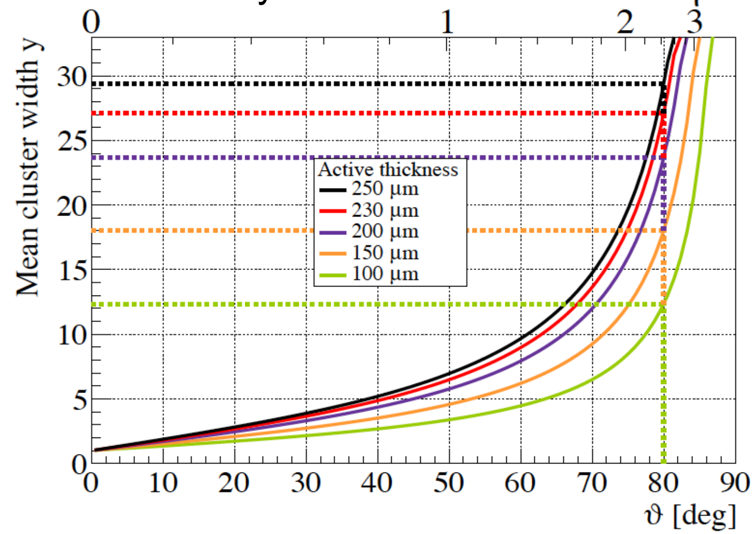
Cluster size dependent on sensor thickness

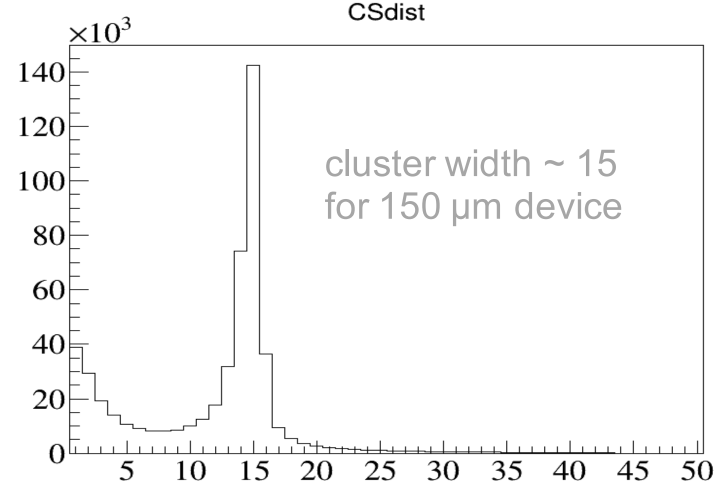
-> smaller cluster width for thinner sensors

Example on cluster width for 150 µm thick sensor

- Geometry : 150 µm thickness, 50x250 µm² pitch, placed at 80˚ in r-phi
- Expected cluster width from geometry ~ 18
- Measured cluster width at test beam ~ 15

Cluster width y for different sensor thicknesses

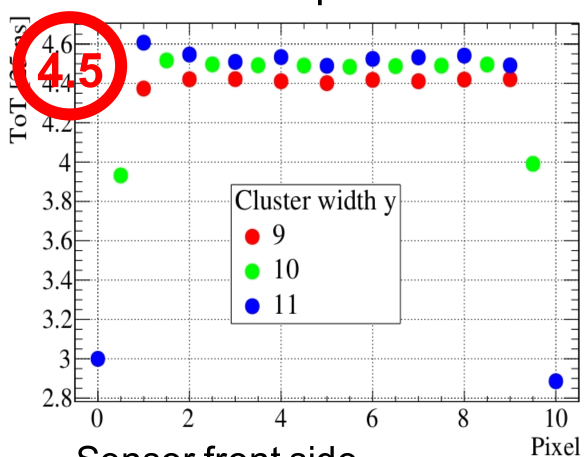




Charge Collection vs sensor thickness

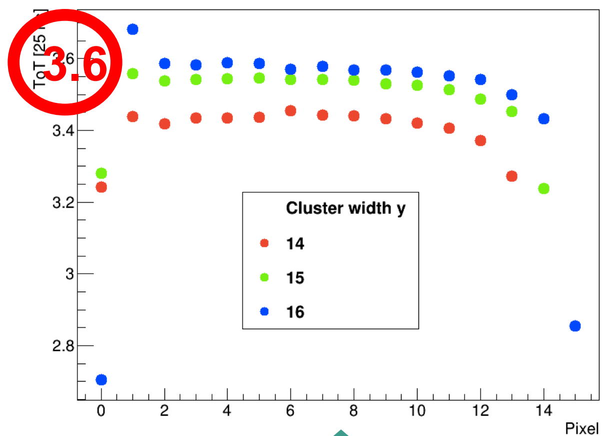
- Charge collection at threshold: 1000e and ToT: 6 to 4ke
- Module with 150 µm thick sensor compared to thicknesses of 100 and 200 µm

100 µm



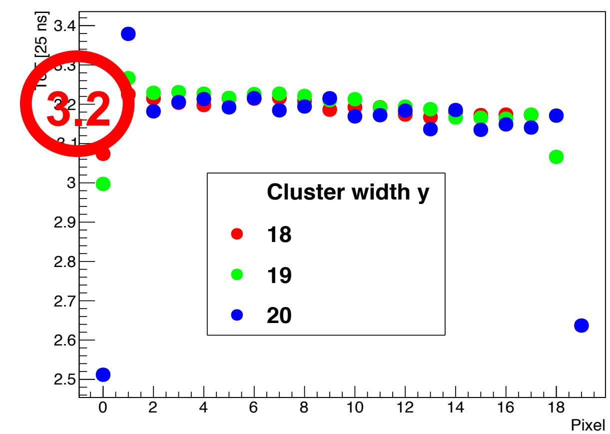
Sensor front side starting from row 0

150 µm



New measurement!

200 µm



Sensor back side starting from row 336

- Increasing cluster width for increasing sensor thickness
- Flat charge collection throughout the sensor depth for all thicknesses
- Increasing charge collection for decreasing sensor thickness

Charge Collection and efficiency vs threshold

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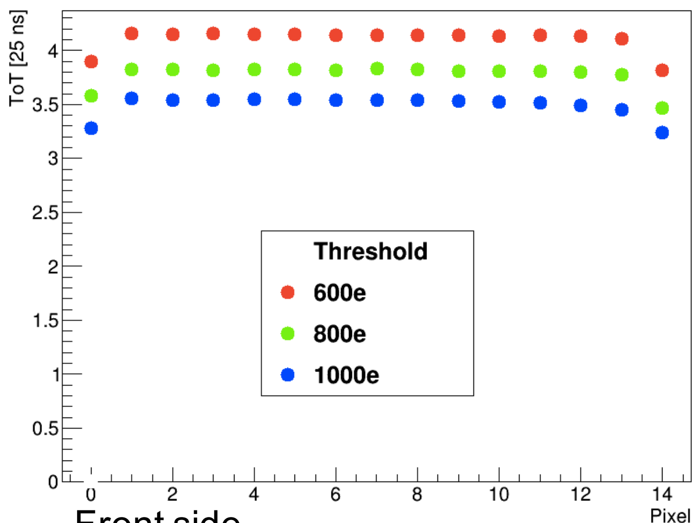
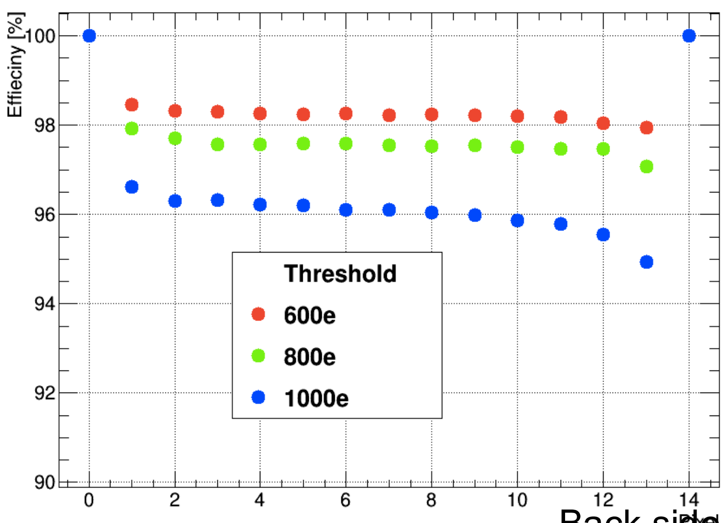
- Charge collection and efficiency at different threshold: 1000, 800 and 600e and ToT: 6 to 4ke

Charge collection per pixel



Front side

Efficiency per pixel



Back side

- First measurements at a threshold of 800 and 600e, in the range expected for the RD53A chip
- Increasing charge collection and efficiency for decreasing threshold values

Summary and Outlook

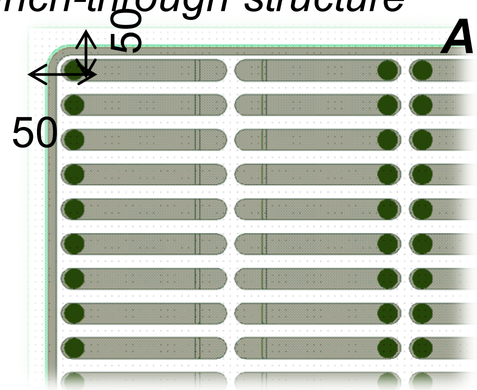
- **Thin sensors with slim and active edge**
  - Results on FE-I4 modules with 100 µm thick sensors and active edge show a hit efficiency of 99.6 %
  - Good hit efficiency up to the sensor edge
- **Performance at high fluences**
  - Hit efficiency for the VTT module with a 100 µm thick sensor is still 97.3 % after irradiation at $1 \cdot 10^{16}\ n_{eq}/cm^2$ -> for a moderate bias voltage of 500 V
- **Performance at high Φ**
  - Planar sensors tunable to a threshold of 600e
  - Increase of charge collection from 3.5ke to 4.1ke and increase of efficiency from 96% to 98% at a threshold of 600e instead of 1000e

Back-up

Different structures of bias ring and punch-through

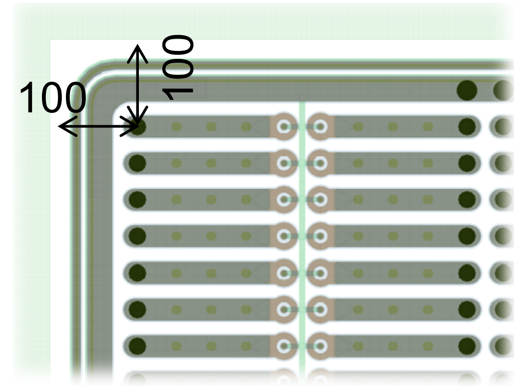
FE-I4 with
50 µm edge,
one GR,
no punch-through structure

Active edge



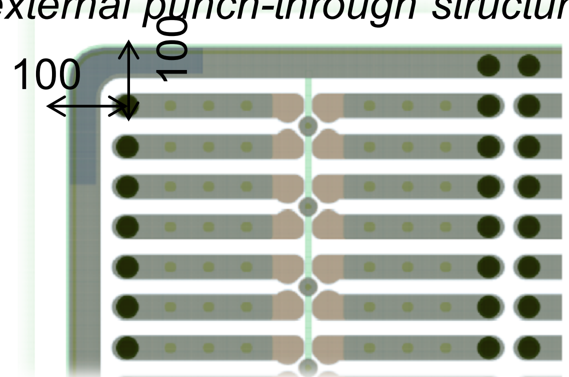
100 µm edge,
Bias Ring + Guard Ring,
std punch-through structure

Slim edge



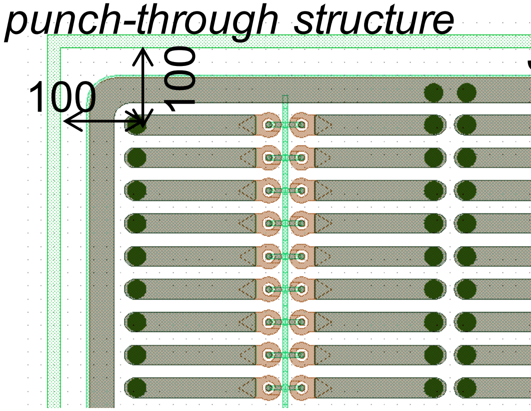
100 µm edge,
Bias Ring,
new external punch-through structure

Slim edge



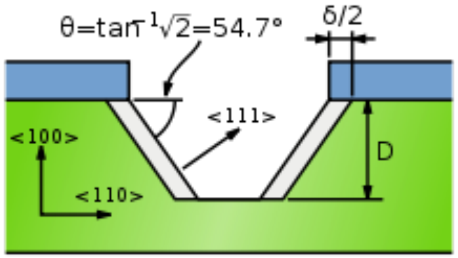
100 µm edge,
Bias Ring,
std punch-through structure

Slim edge

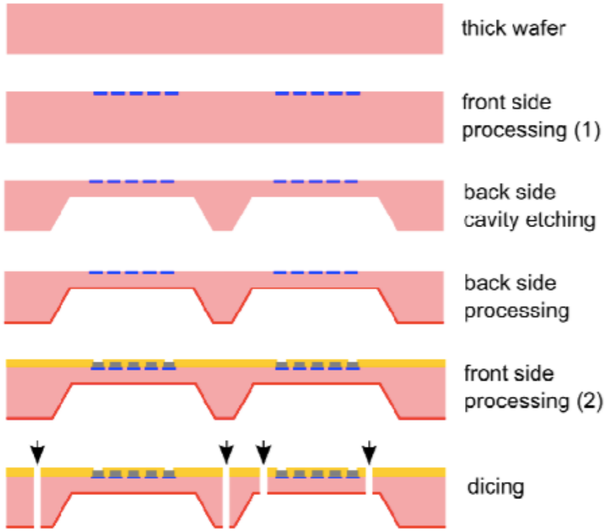


CiS Production

- First R&D production on 4‘‘ wafers for 100 and 150 µm thick sensors
- Thinning technology without using support/handling wafer by anisotropic wet etching (KOH)

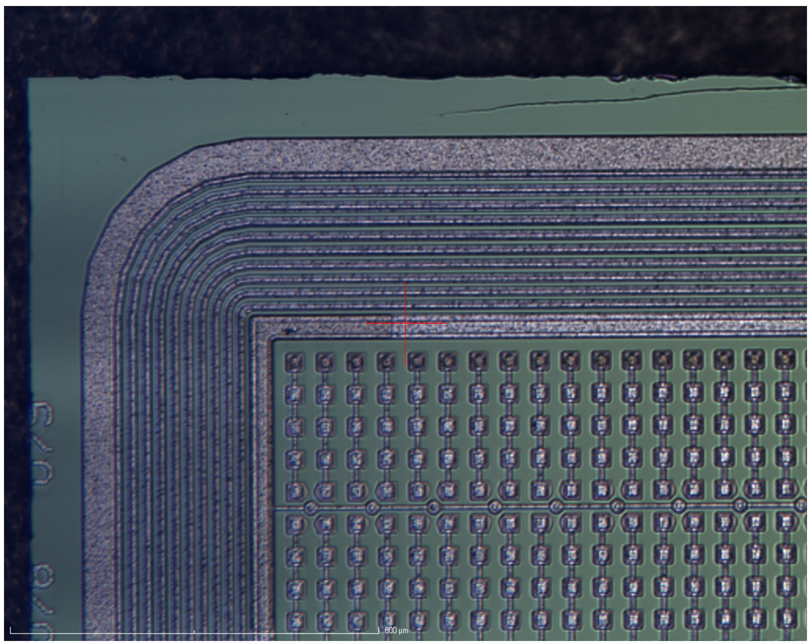


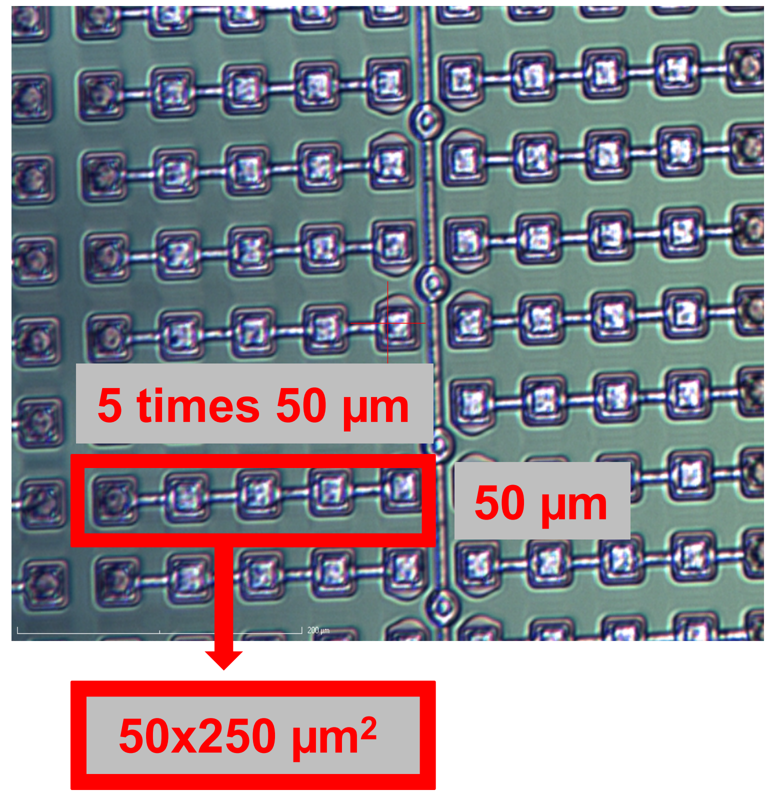
- Starting thickness 525 µm
- Front-side processing up to nitride depositions and patterning
- Back-side p+ implantation, top-side p-spray
- Metallization on the front and back side
- UBM (electroless Nickel at CiS or standard at IZM)
- dicing



CiS Production

- Sensor layout with 50x50 µm^2 pixel cells
- Implemented common punch-through design
- 5 pixel cells of 50 µm are connected with an extra rail to allow for a readout with the standard FE-I4 chip with 50x250 µm^2 pixel cells





New design for sensors compatible with the RD53 chip

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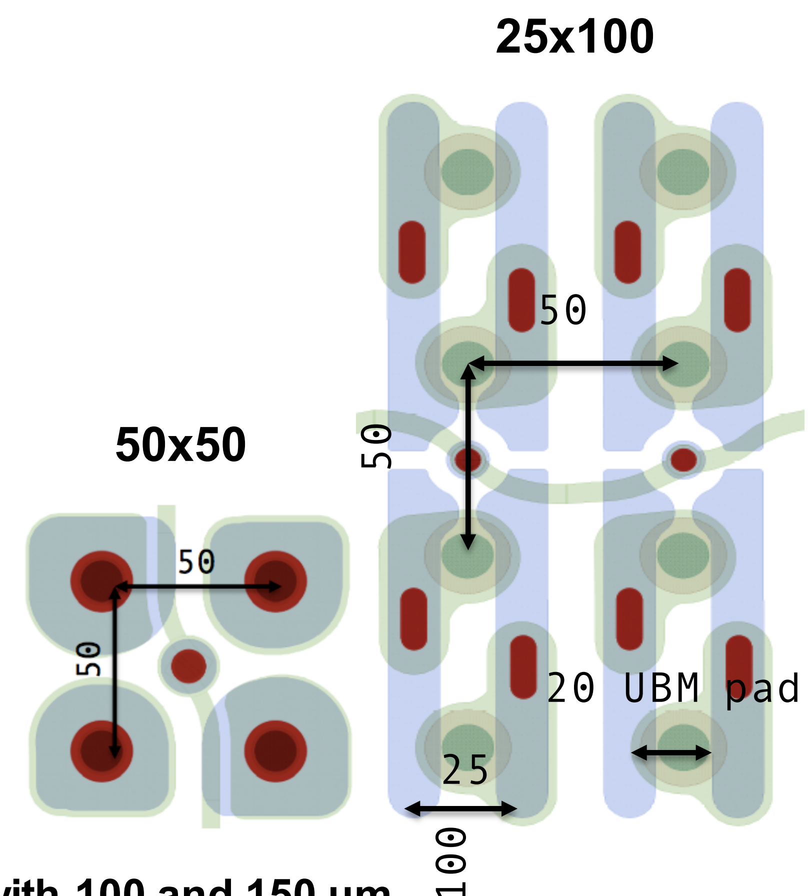
- Punch-through design adopted from the two best performing ones: combination of biasline over p-t dot and common p-t
- Alternative designs also implemented without any biasing structure

25x100 μm² pixel pitch

- Pixel staggered in such way to be compatible with a regular 50x50 μm² grid on the chip
- Design based on the existing prototype with 25x500 μm² pitch (results shown before)



- **New production on SOI wafers at MPG-HLL with 100 and 150 μm active thickness**
- **Alternative but similar design implement in new CiS production**

Not irradiated modules: Tuning for high phi

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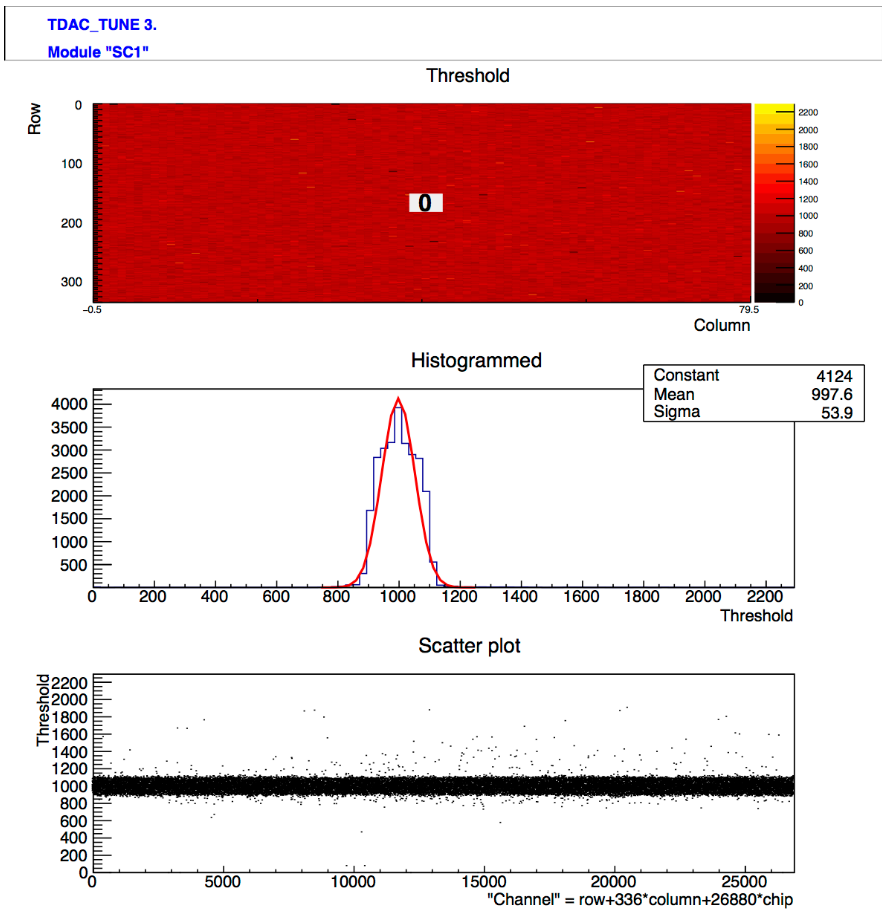
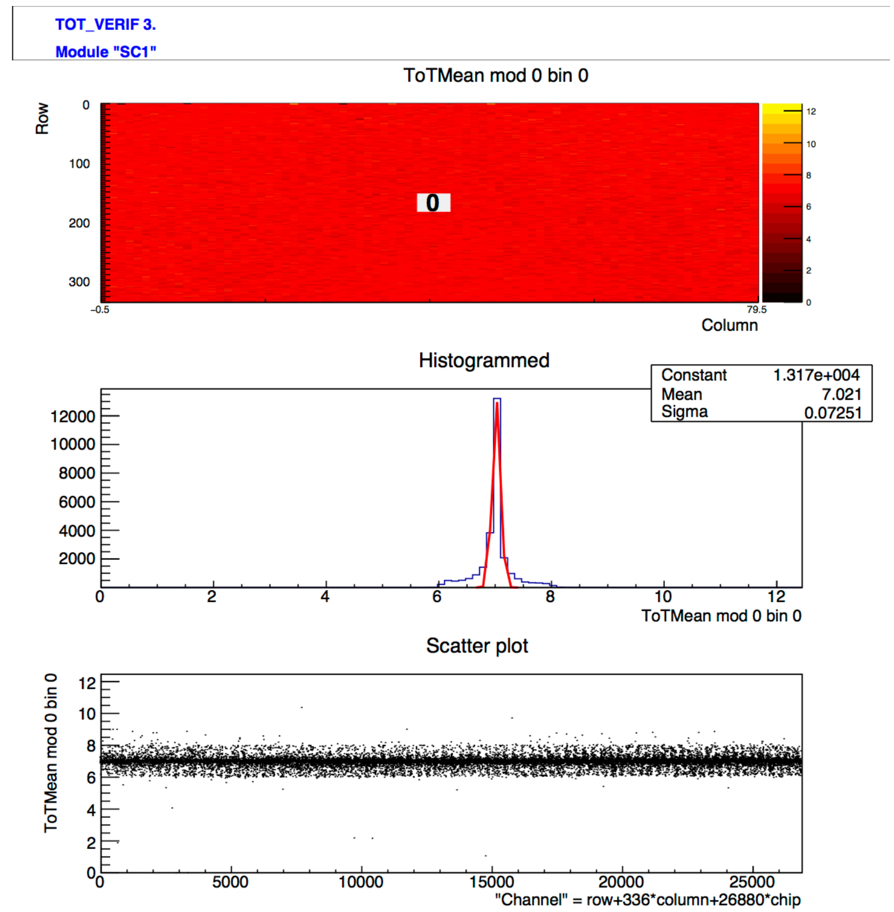
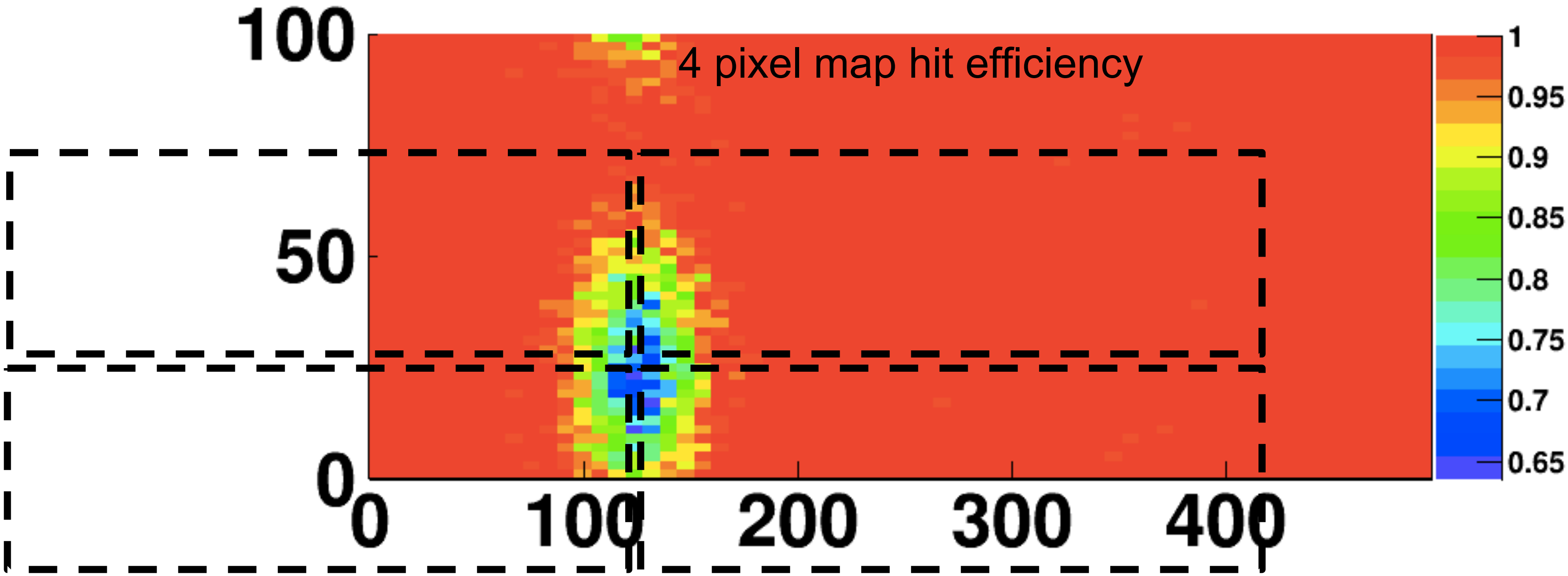
- NP150µm-5-4A (active edge) at **high phi**: Threshold: 1000e and ToT: 6 to 4ke

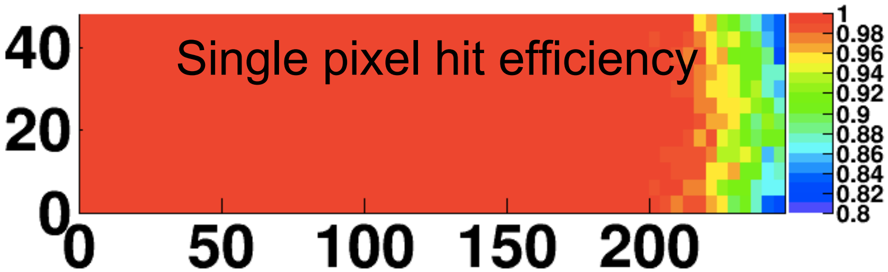




ADVACAM production (slim edge, 100 µm thickness)

In-pixel hit efficiency at 40 V





mirrored in x

Hit efficiency : 98.8 %

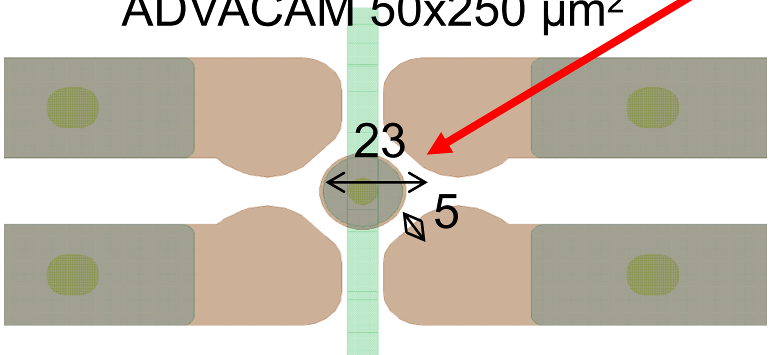
Relatively high inefficiency due to punch-through structure

New punch-through designs
in different productions

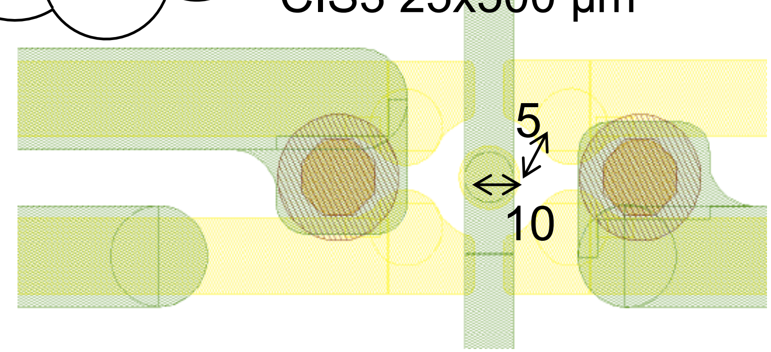
Possible reason for rather large inefficiencies: **large pt-dot**

New common PT

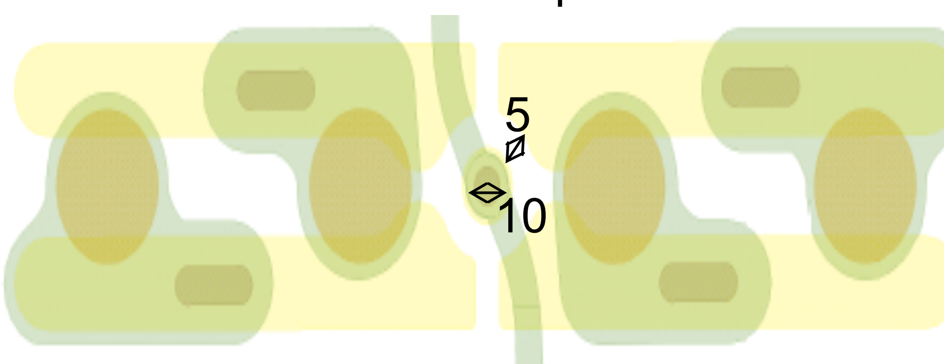
ADVACAM 50x250 μm²



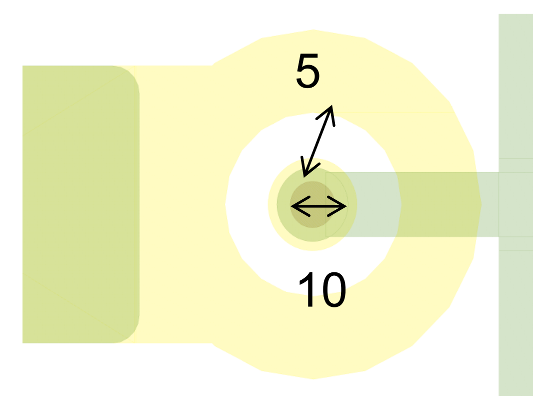
CIS3 25x500 μm²



RD53 25x100 μm²



Standard PT



Distribution of cluster width

- Cluster size dependant on sensor thickness -> smaller cluster width for thinner sensors

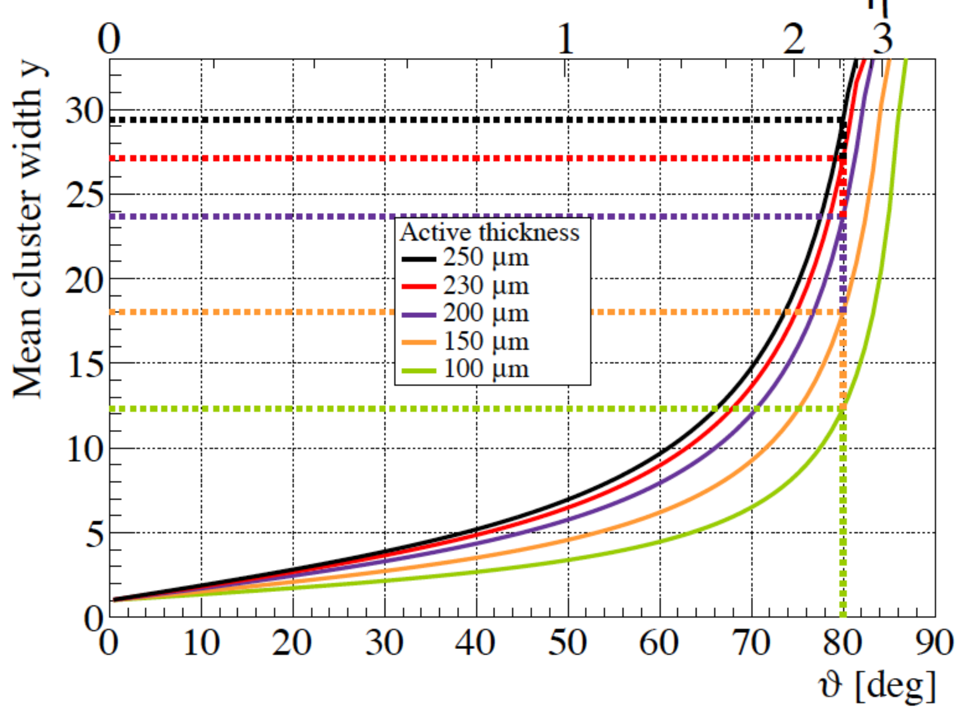
Example on cluster width for 150 µm thick sensor

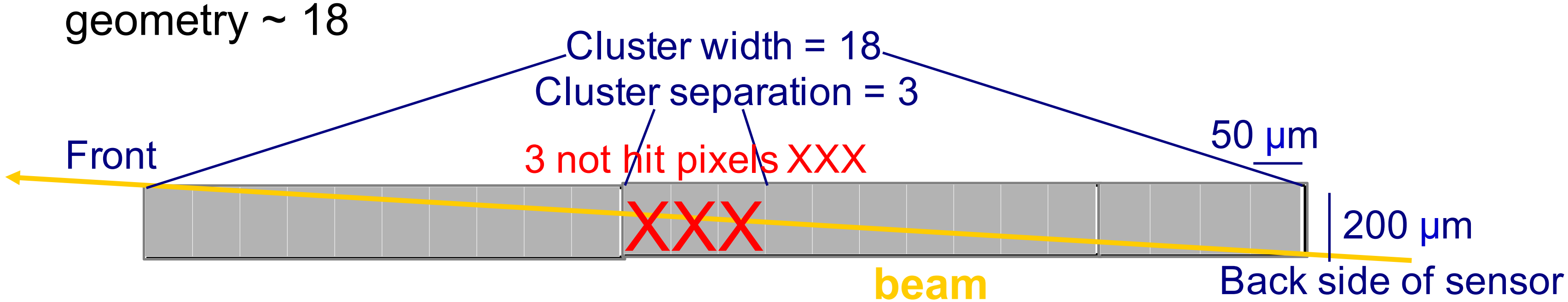
- Geometry :

  150 µm thickness,
  50x250 µm² pitch,
  placed at 80° in r-phi

- Expected cluster width from geometry ~ 18

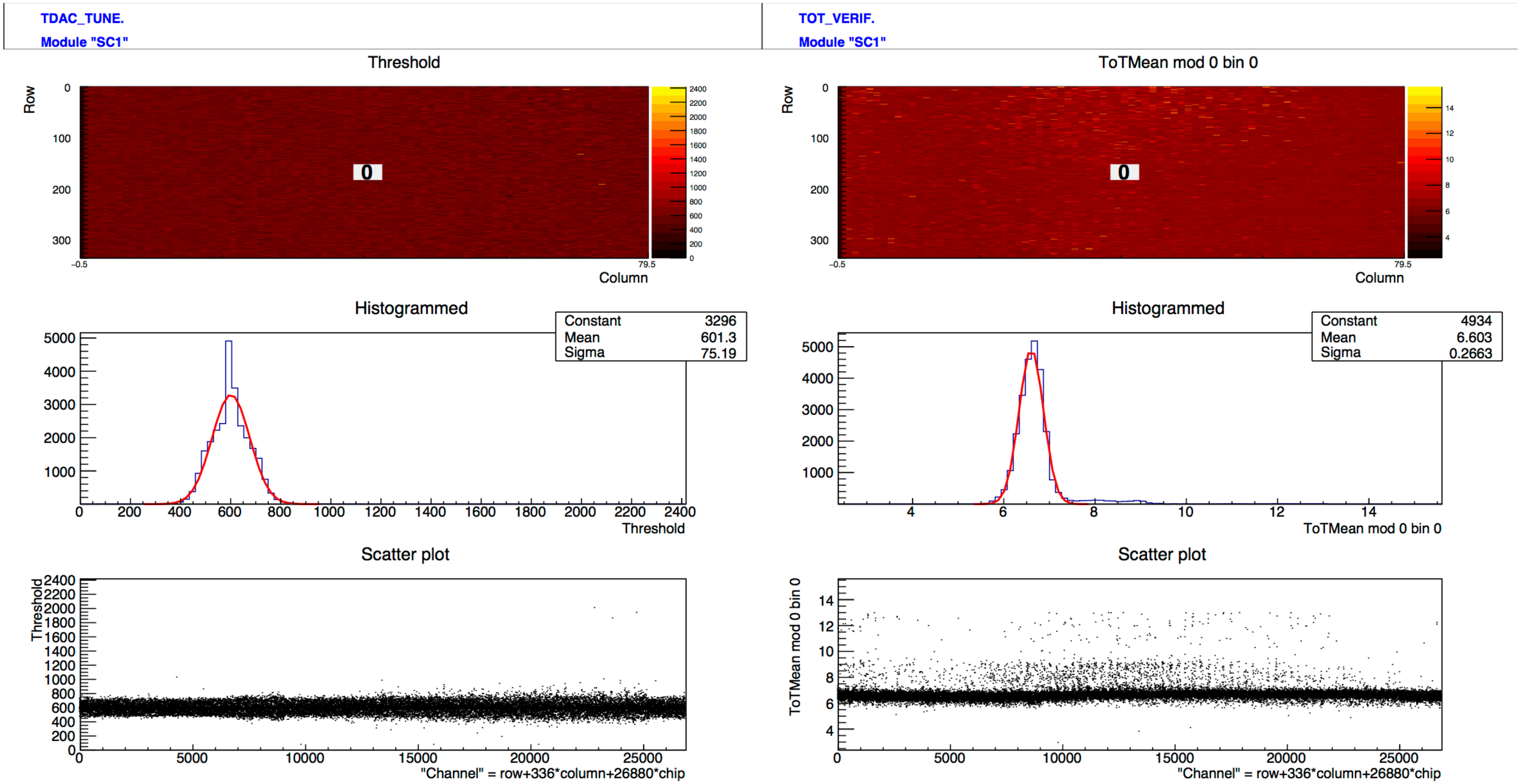
Cluster width y for different sensor thicknesses





Not irradiated modules: Tuning for high phi

- NP150µm-5-4A (active edge) at **high phi**: Threshold: **600e** and ToT: 6 to 4ke



Not irradiated modules: Cluster distances

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- NP150µm-5-4A (active edge) at **high phi**: Threshold: 600-1000e