The GigaTracKer: a silicon hybrid pixel detector with good timing resolution.

M. Noy[1] on behalf of the GTK Working Group

EP-ESE-FE Group, CERN

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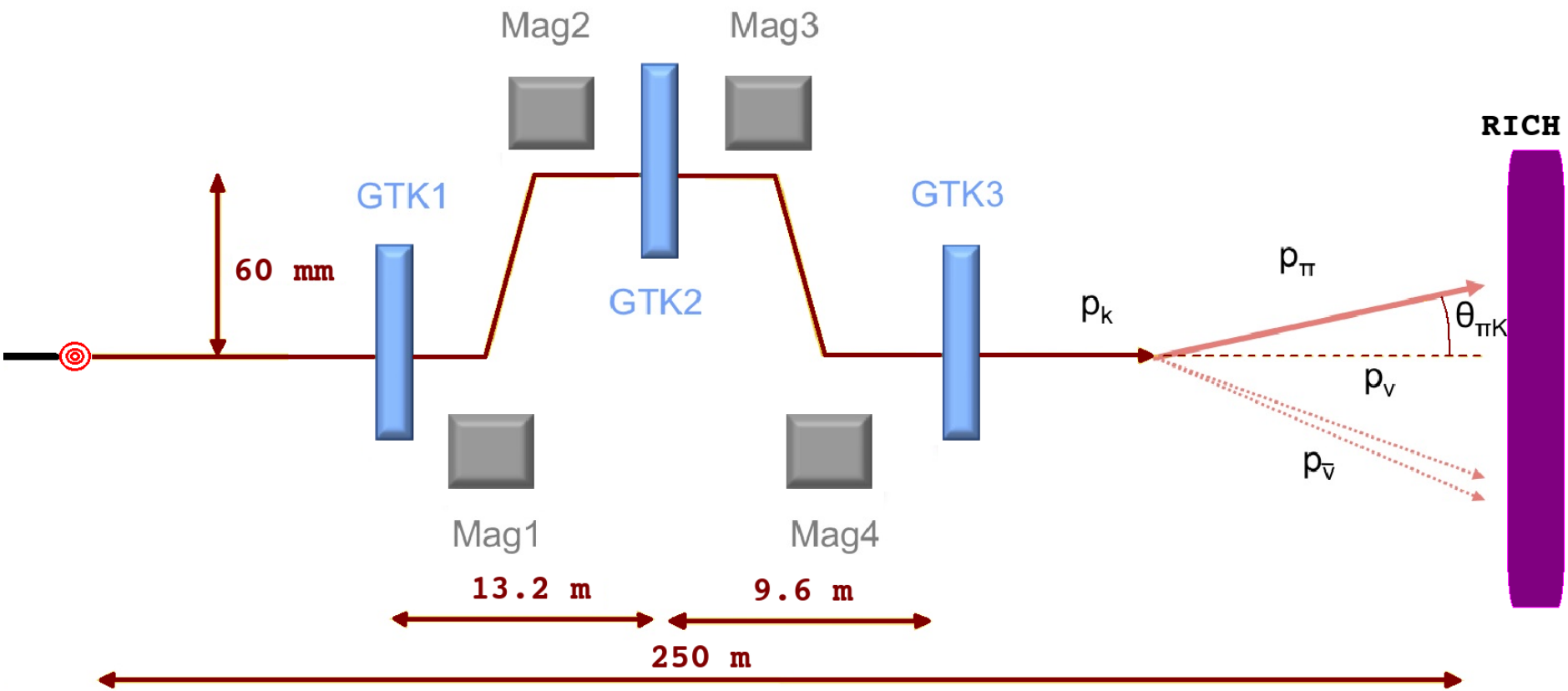
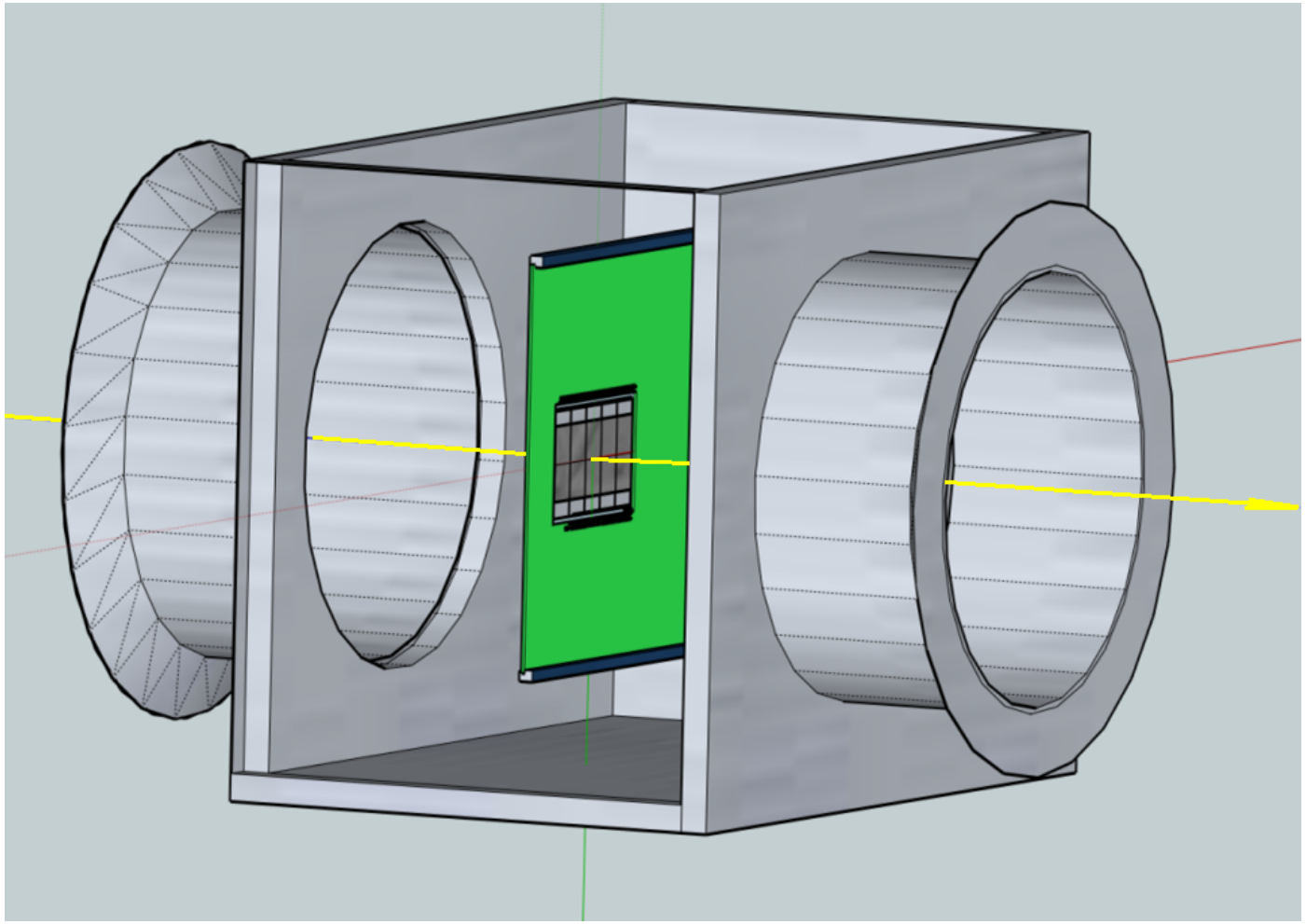
The NA62 Experiment



- Trajectory
  - momentum
  - angle
- Time
  - correlate hits with RICH
  - $\leq 200\,ps(RMS)$ per station

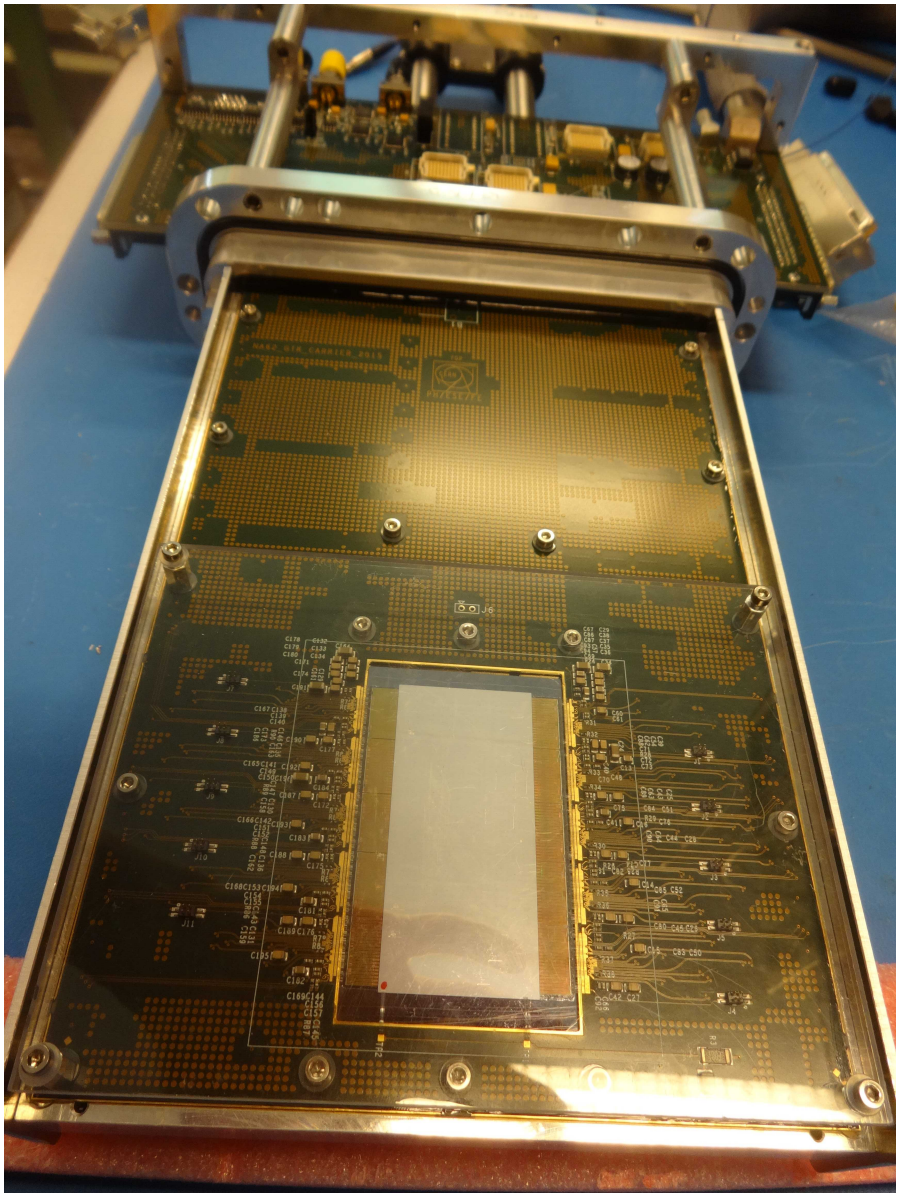
The NA62 Experiment

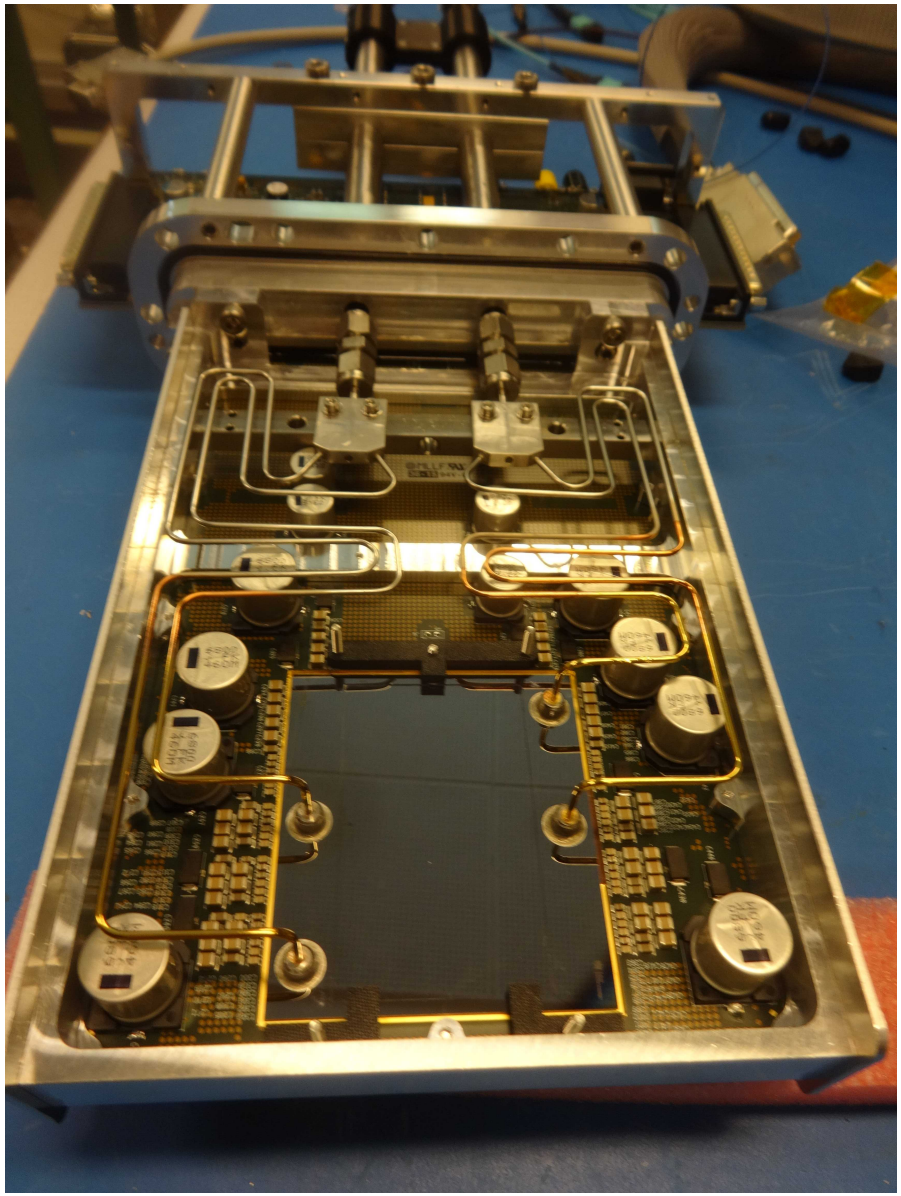
GTK Station in the Beam Line



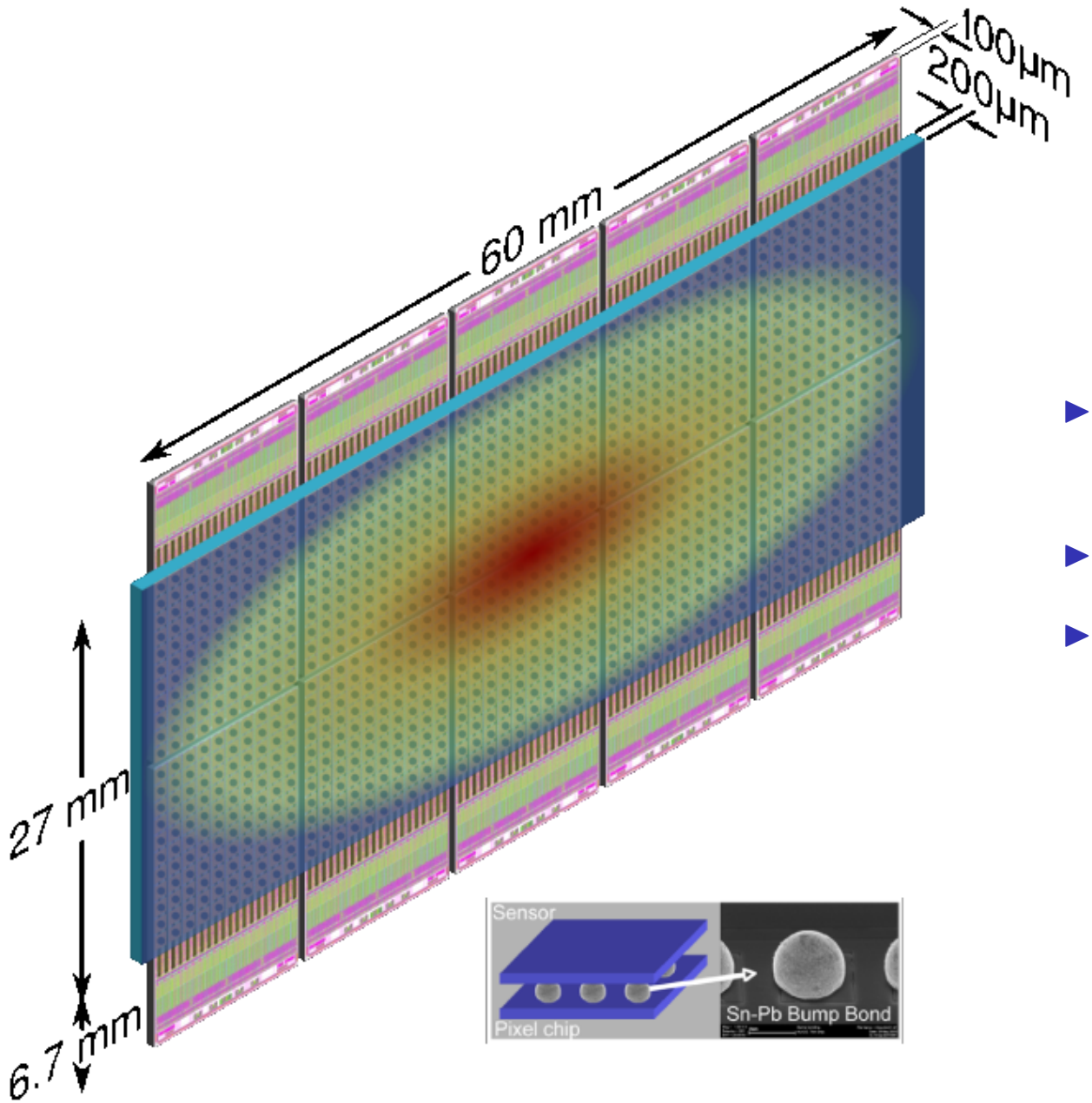
- in vacuum
- centred on the beam
- 0.8→1 GHz beam rate

The GTK Carrier Card



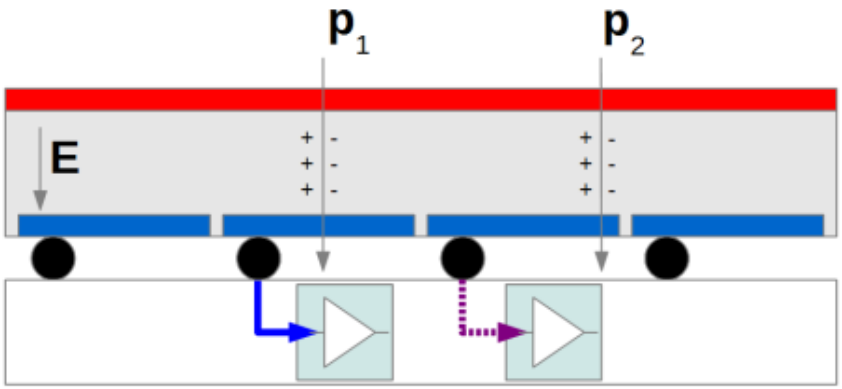


GigaTracker: Hybrid Pixel Detector

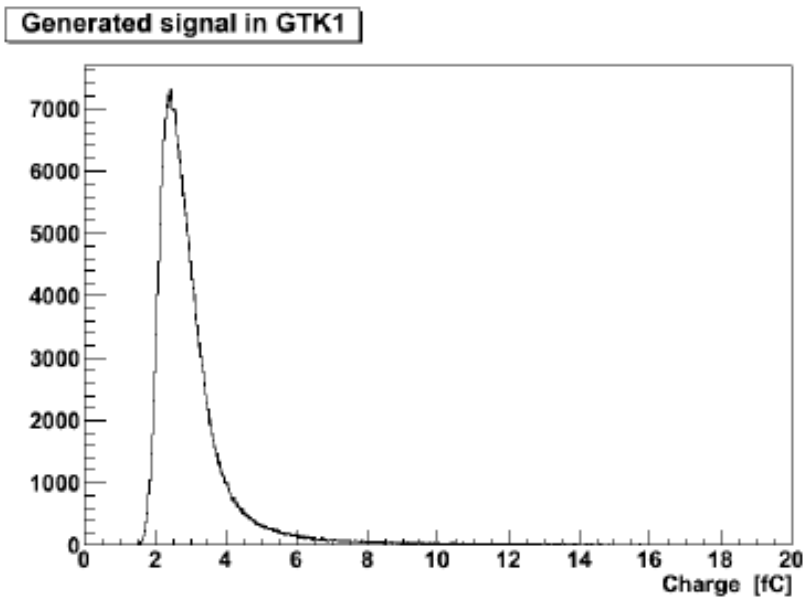


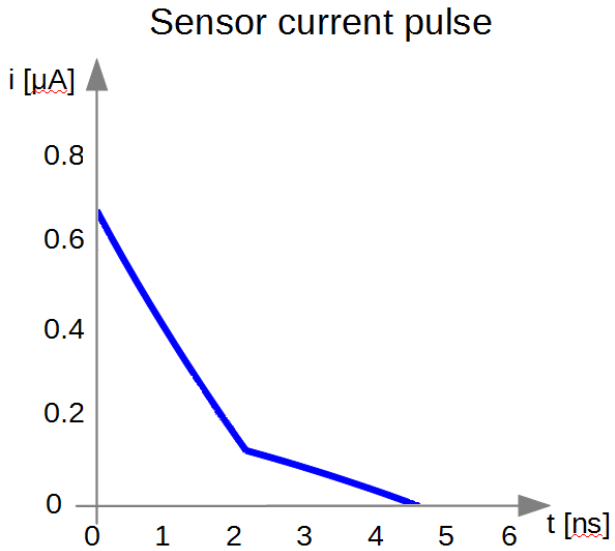
- non-uniform beam
- 6Mrad/year
- 0.5% X_0 per station

Sensor Parameters

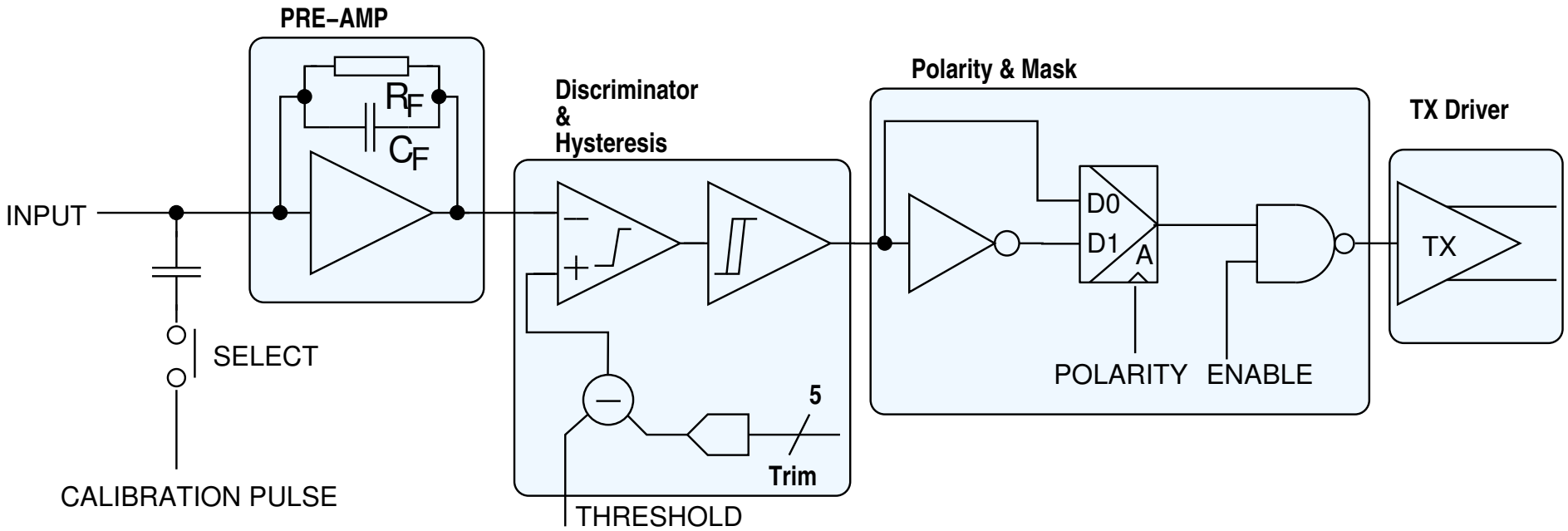


- $V_{bias} \sim$ 300-600V
- charge release mechanism is stochastic
- Landau distribution
  - $Q_{MP} = 2.4\,fC$
- 200μm thick
  - (signal size vs $T_{collection}$)



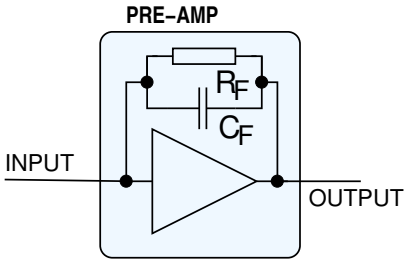


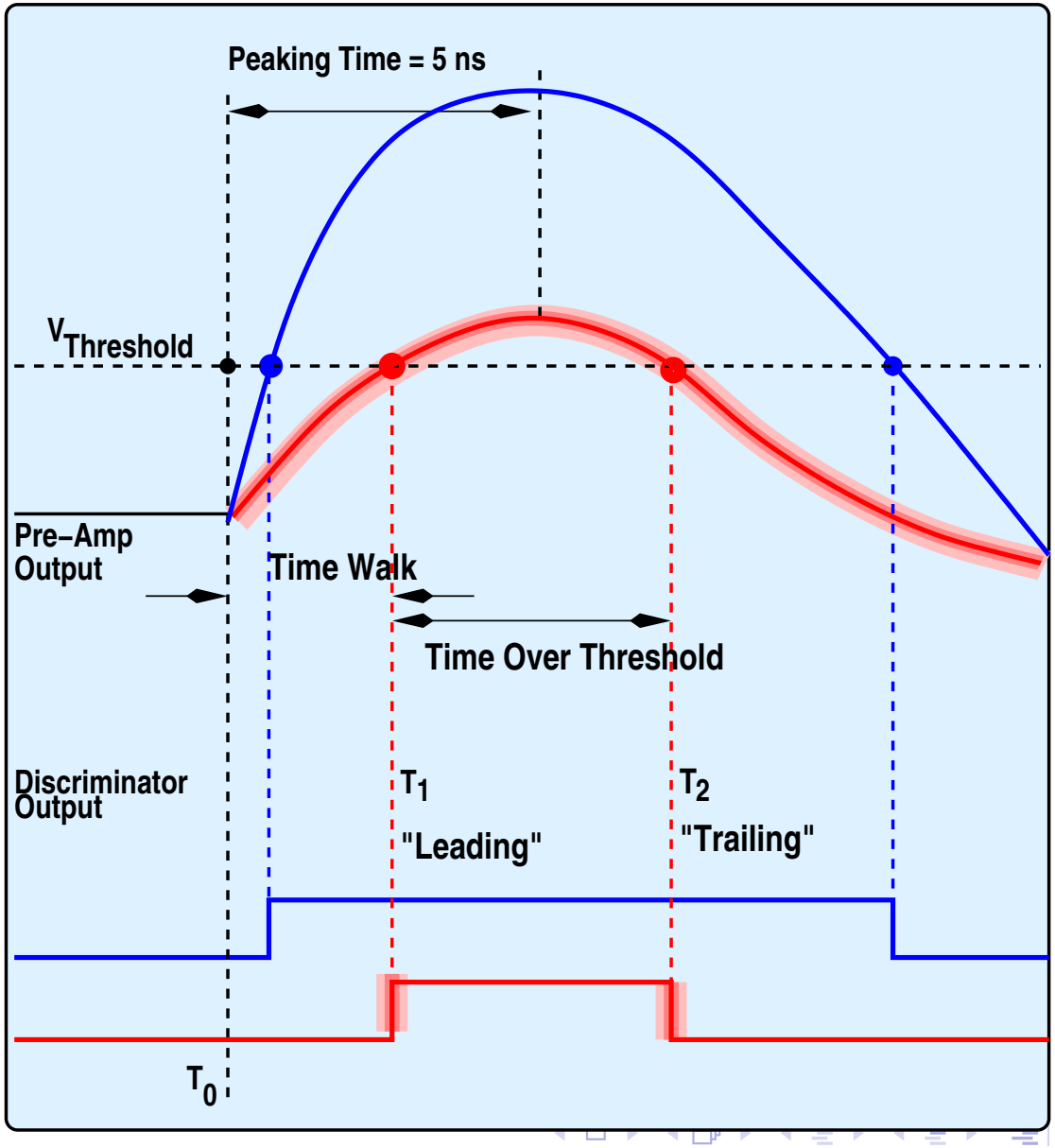
Simplified Pixel Architecture



- Gain $\sim 65\,mV/fC$
- peaking time $\sim 5\,ns$
- ENC $< 250\,e^-$
- Polarity control
- Pixel mask
- TX with pre-emphasis

Pre-Amplifier & Discriminator Signals





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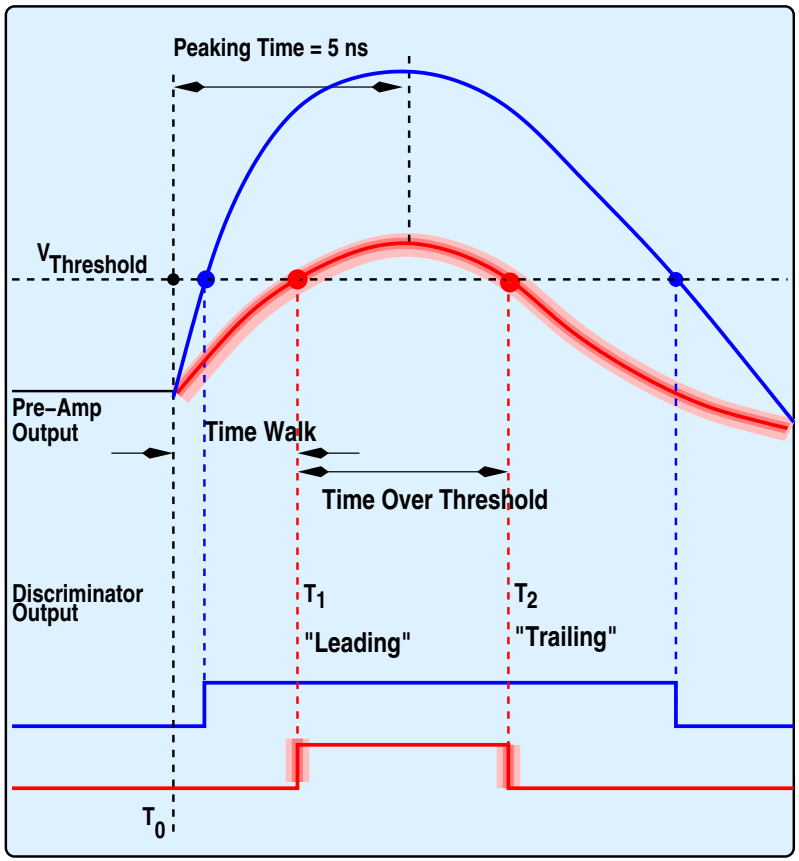
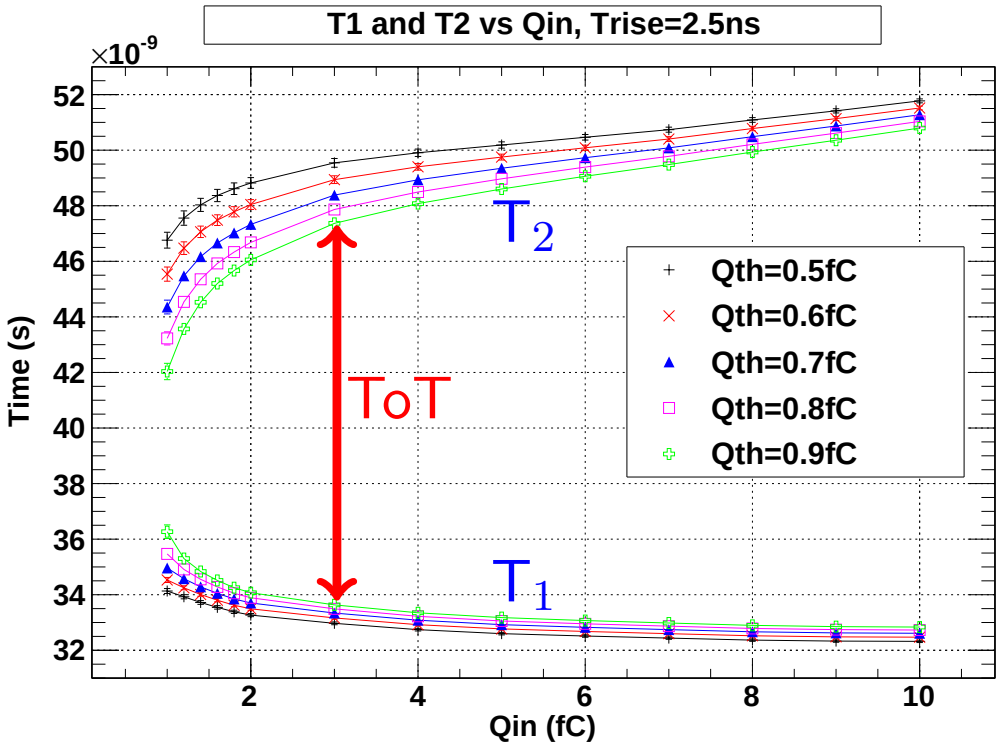
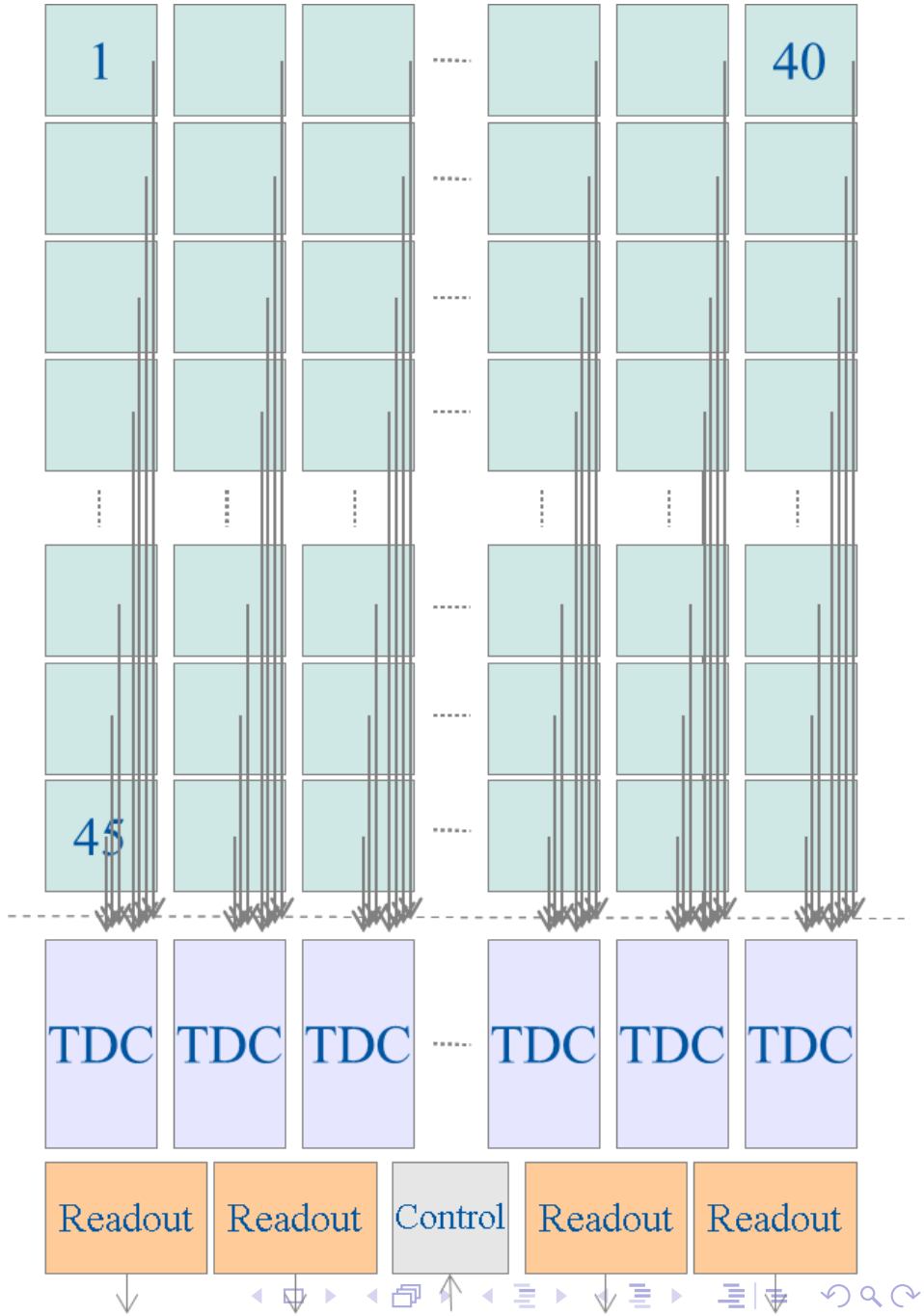




TDCPix Architectural Overview

- 40 x 45 pixels
  - 300x300 μm^2
  - asynchronous



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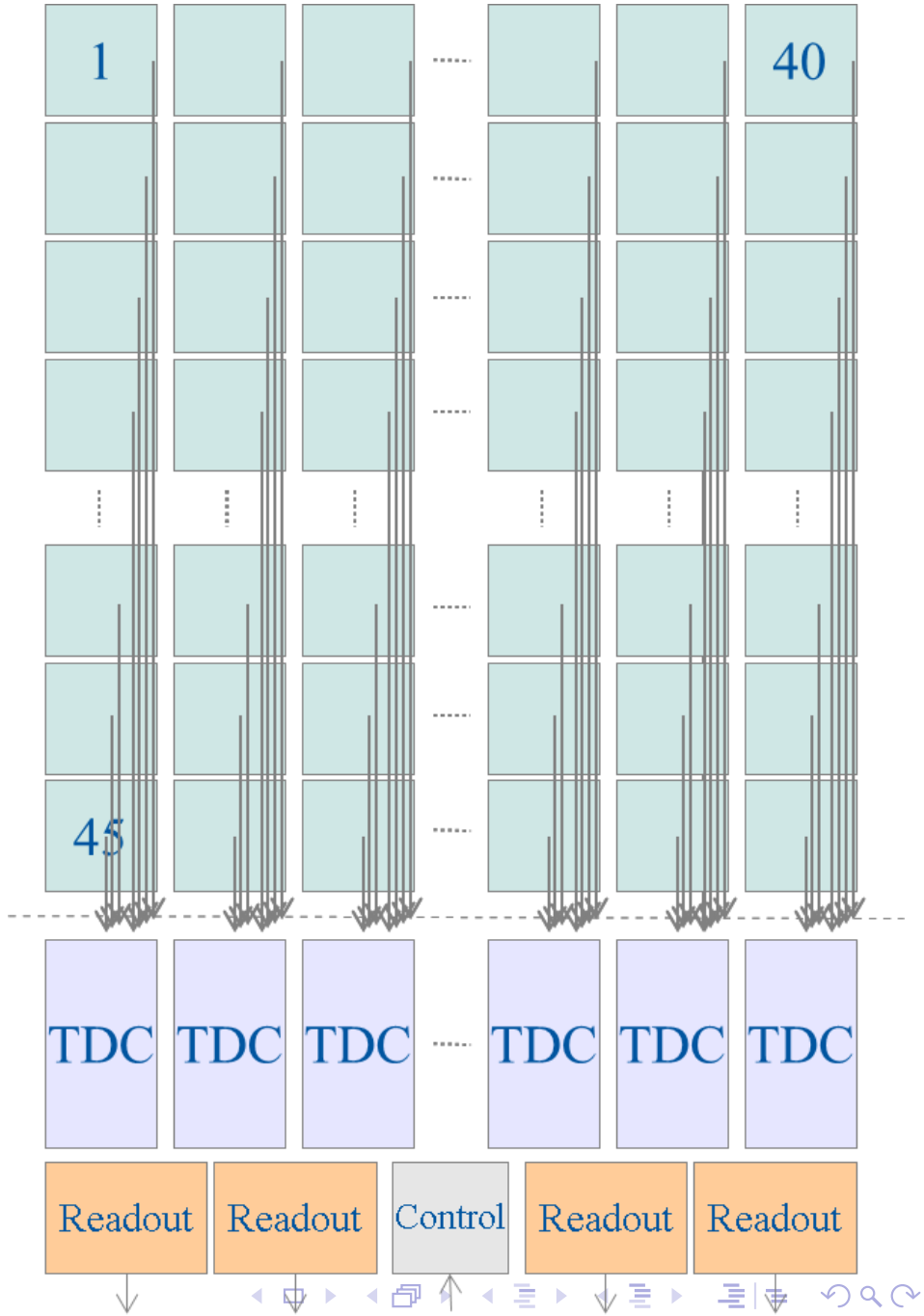
- End-Of-Column
  - per-pixel hit signal to EOC



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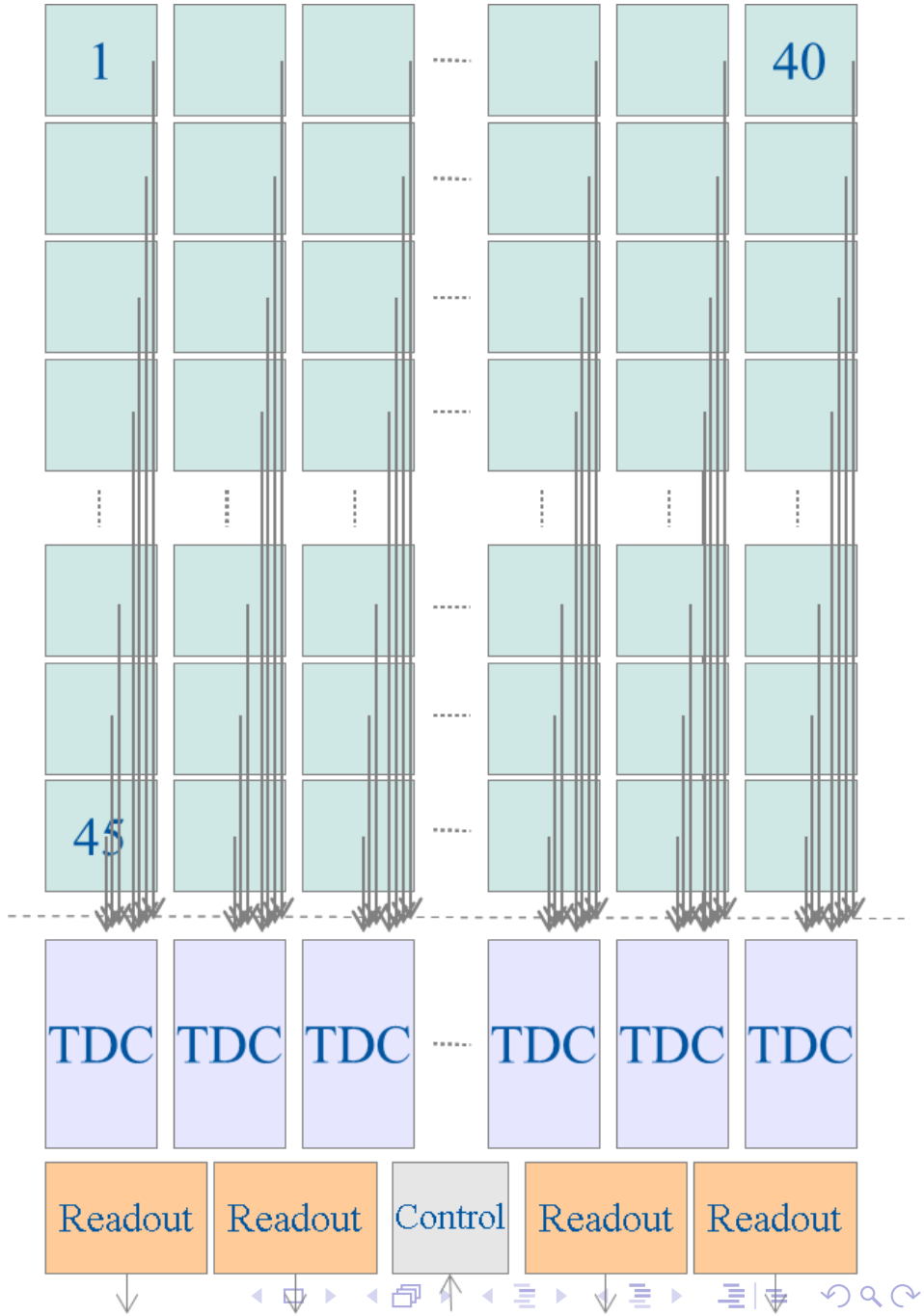
- 360 dual TDC channels
  - TDC Bin size $\sim 97\,ps$



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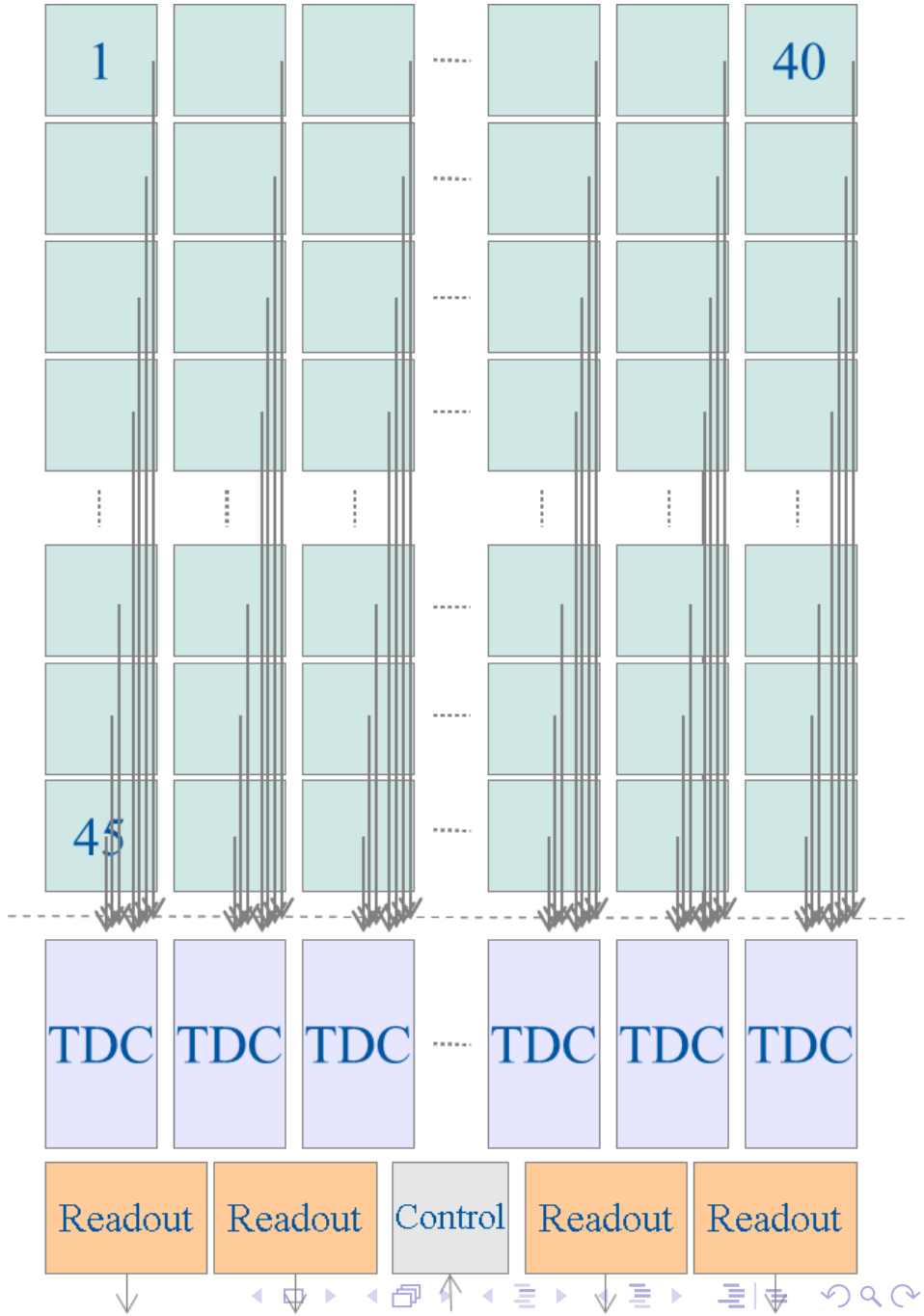
  - Rate:210MHits/s
  - 4 x $3.2\,Gb/s$ serialisers



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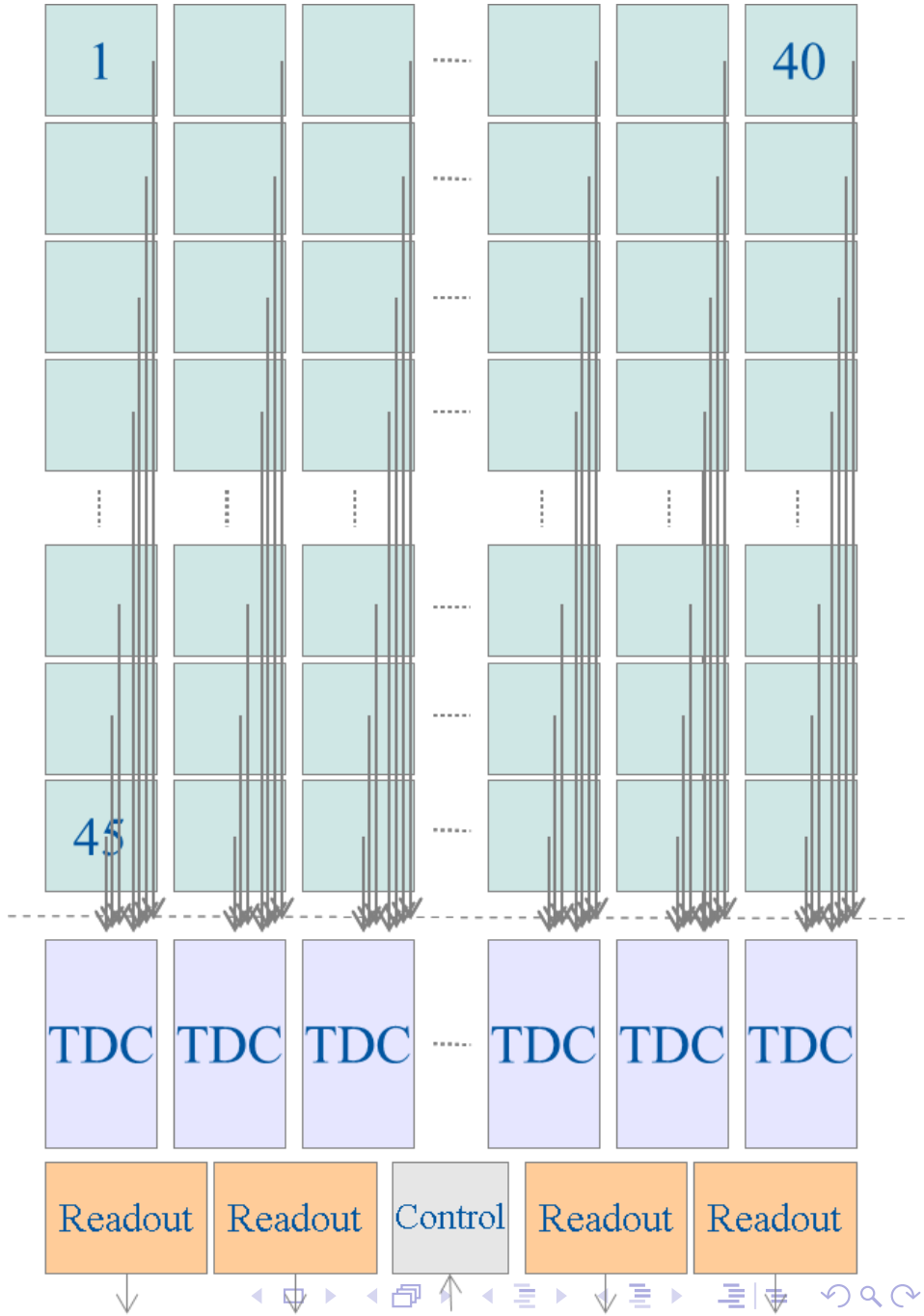
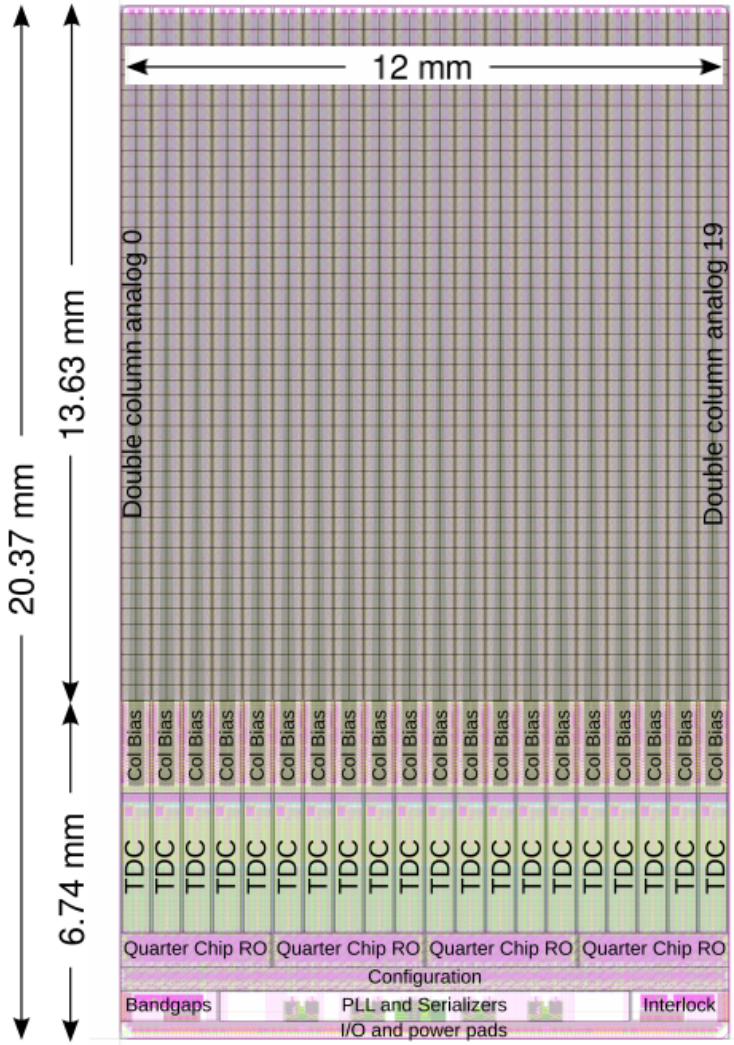
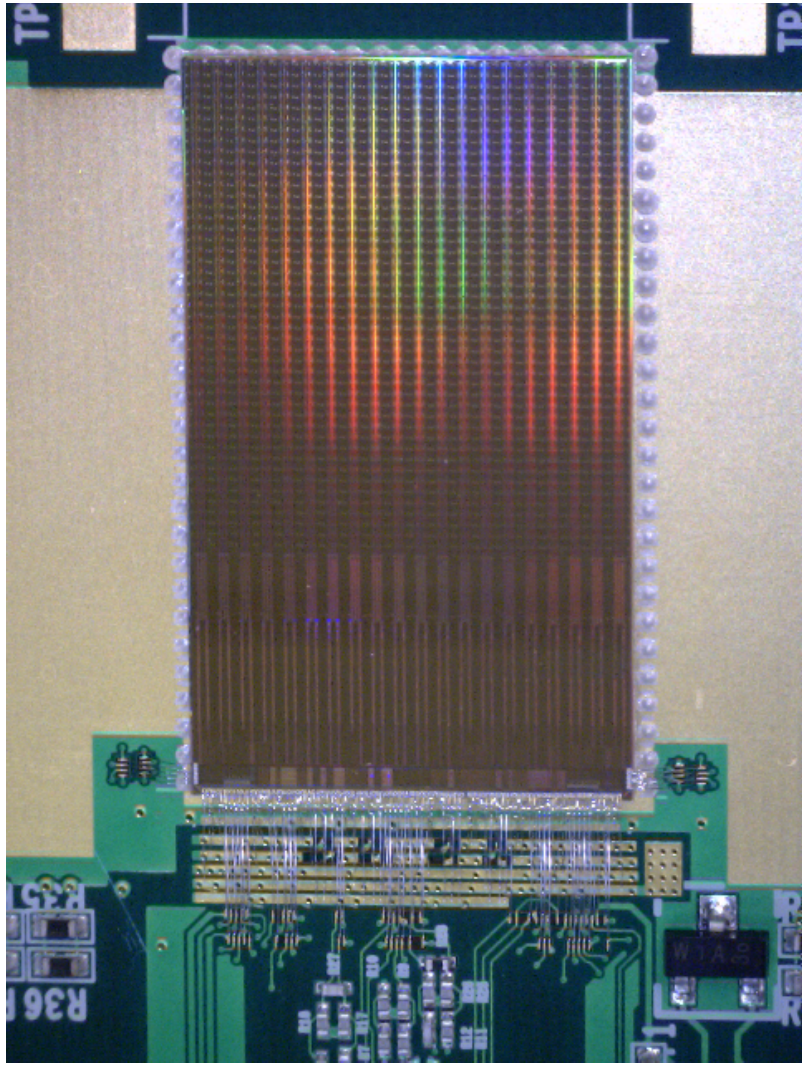
- SEE Tolerant
  - state/config.



TDCPix Top Level





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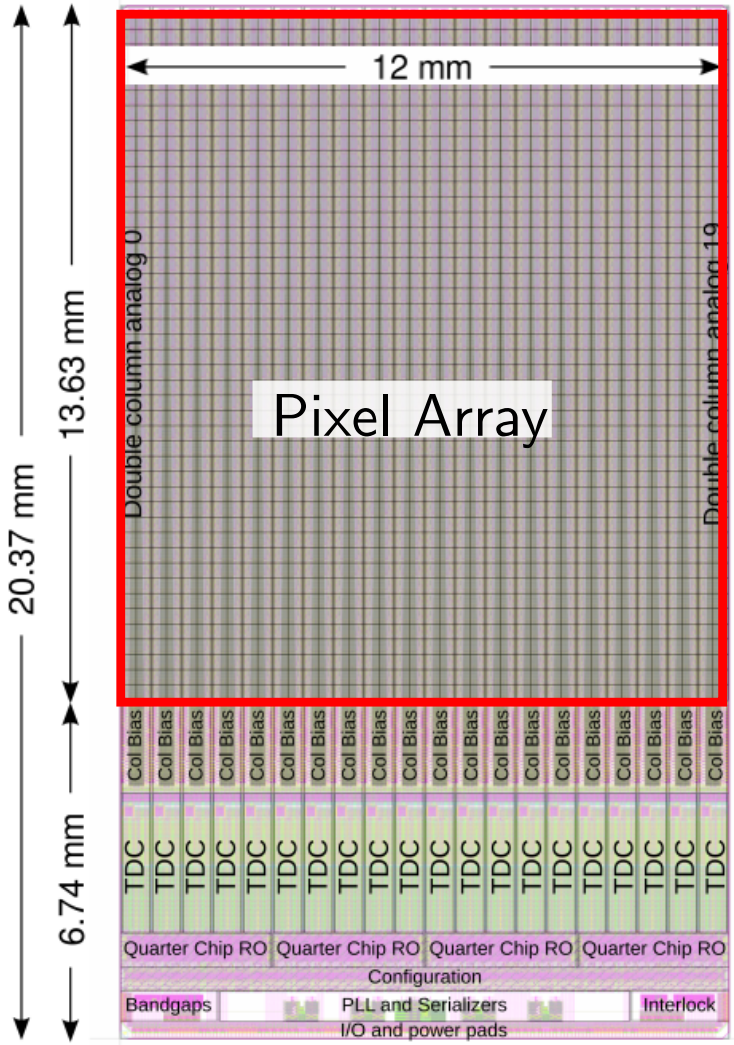

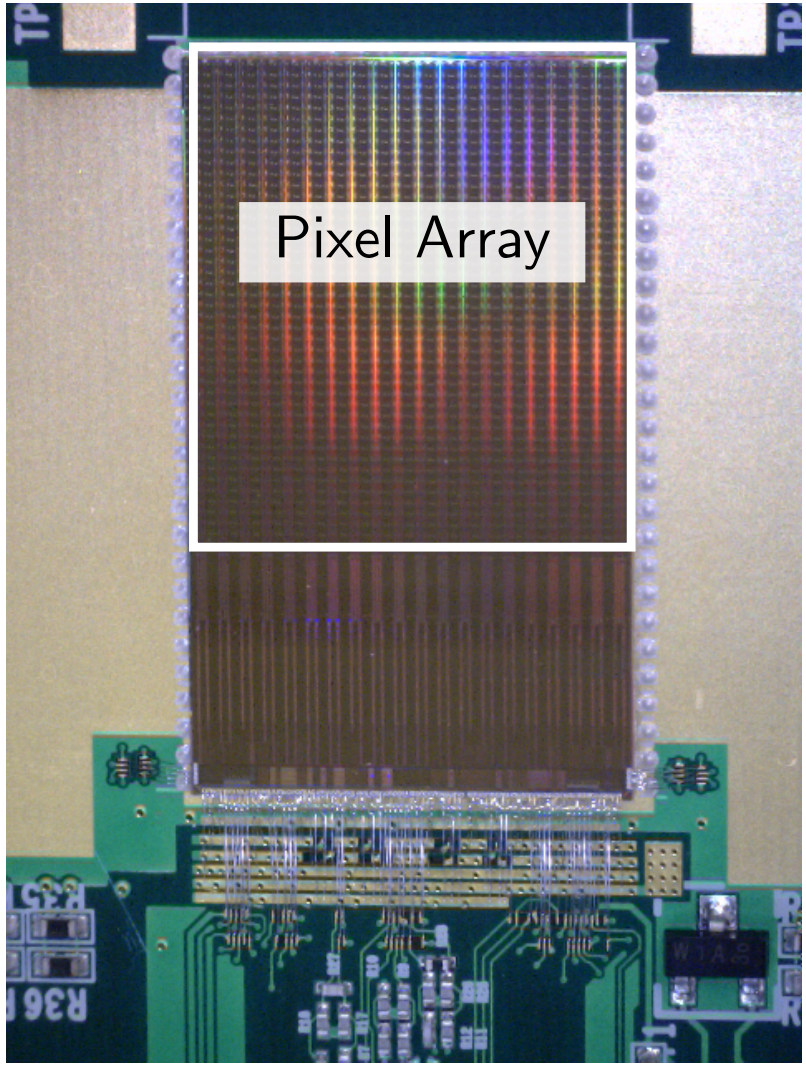

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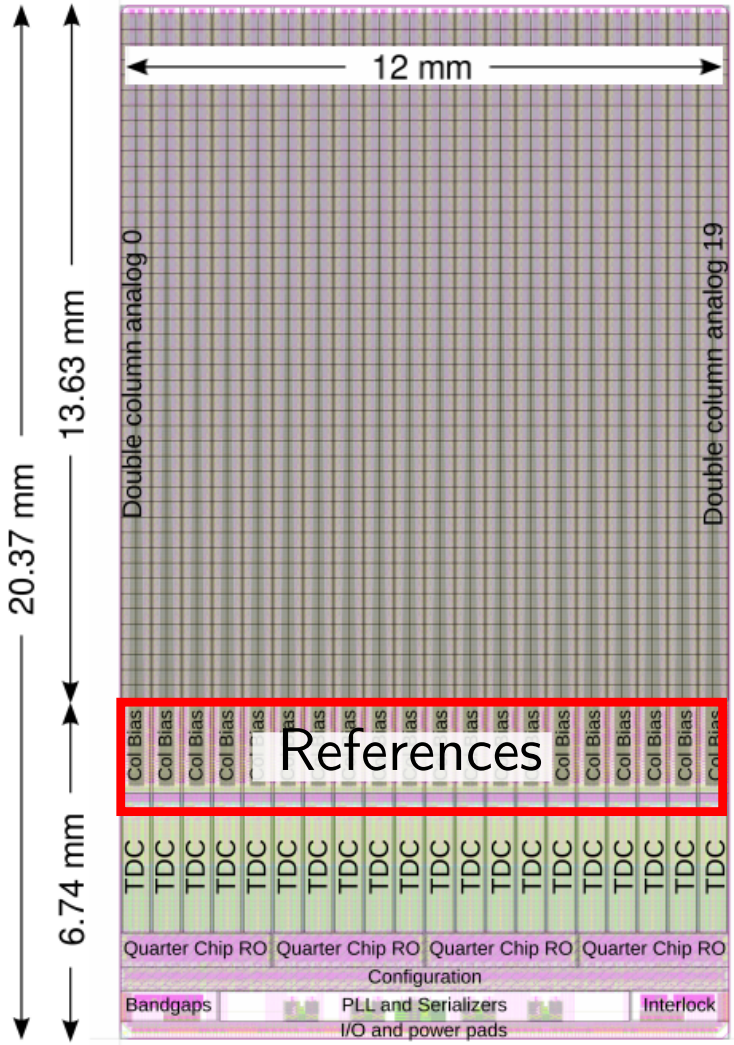
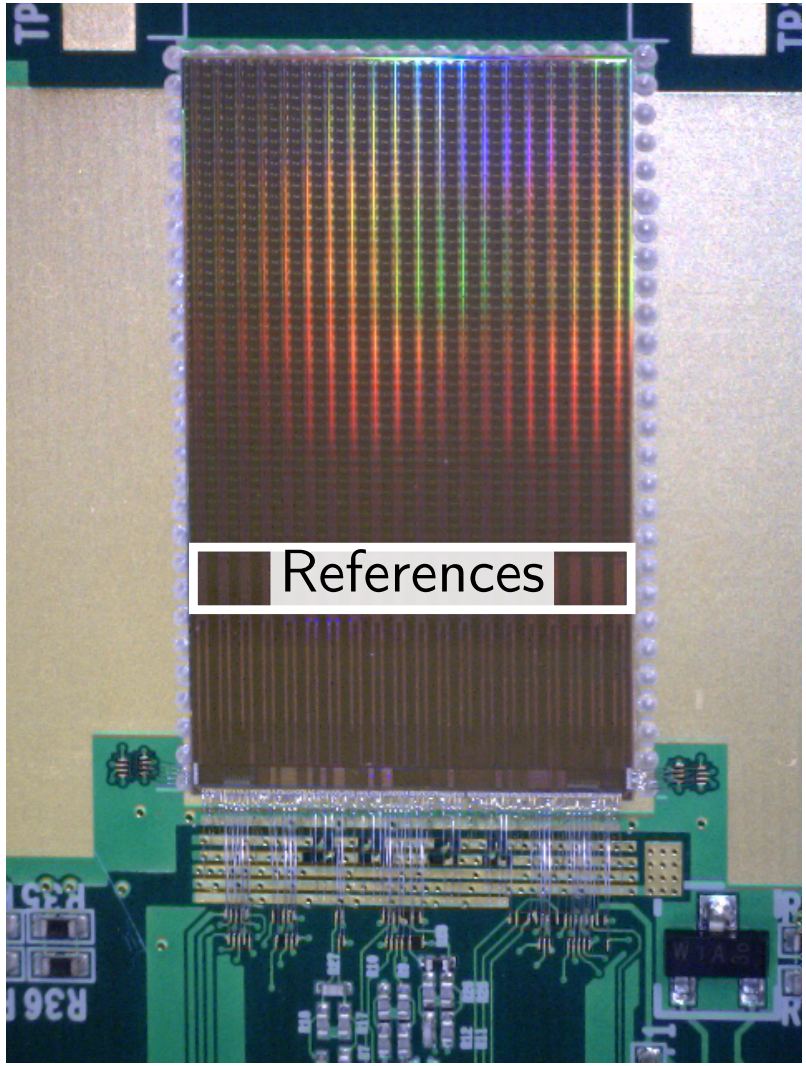
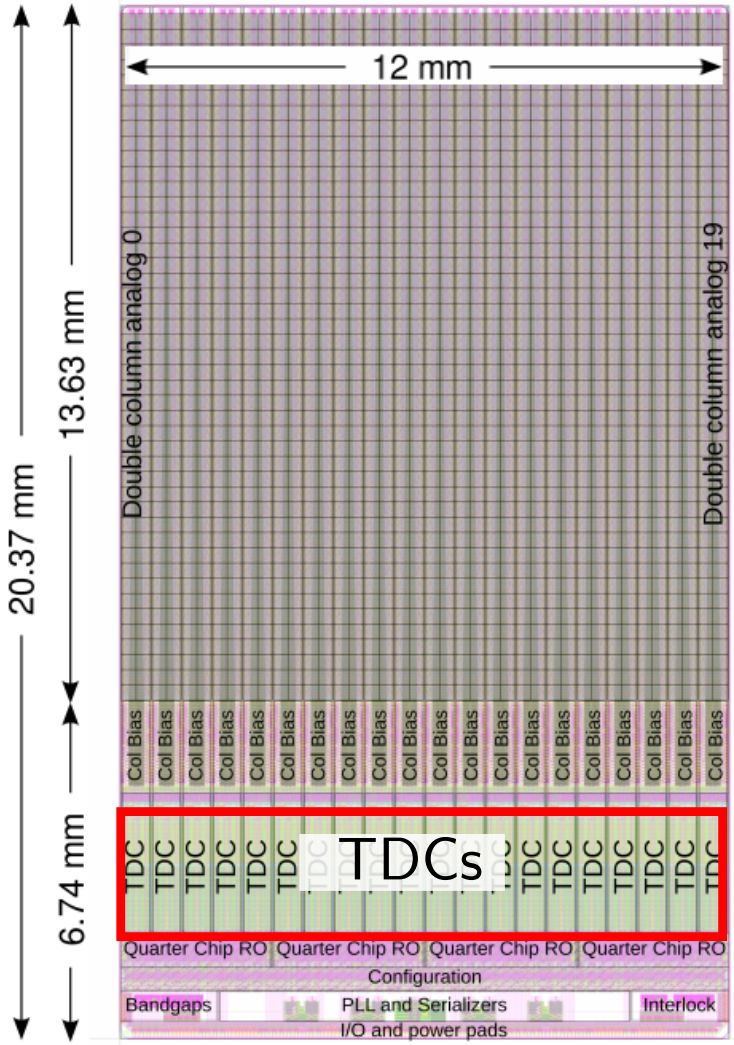
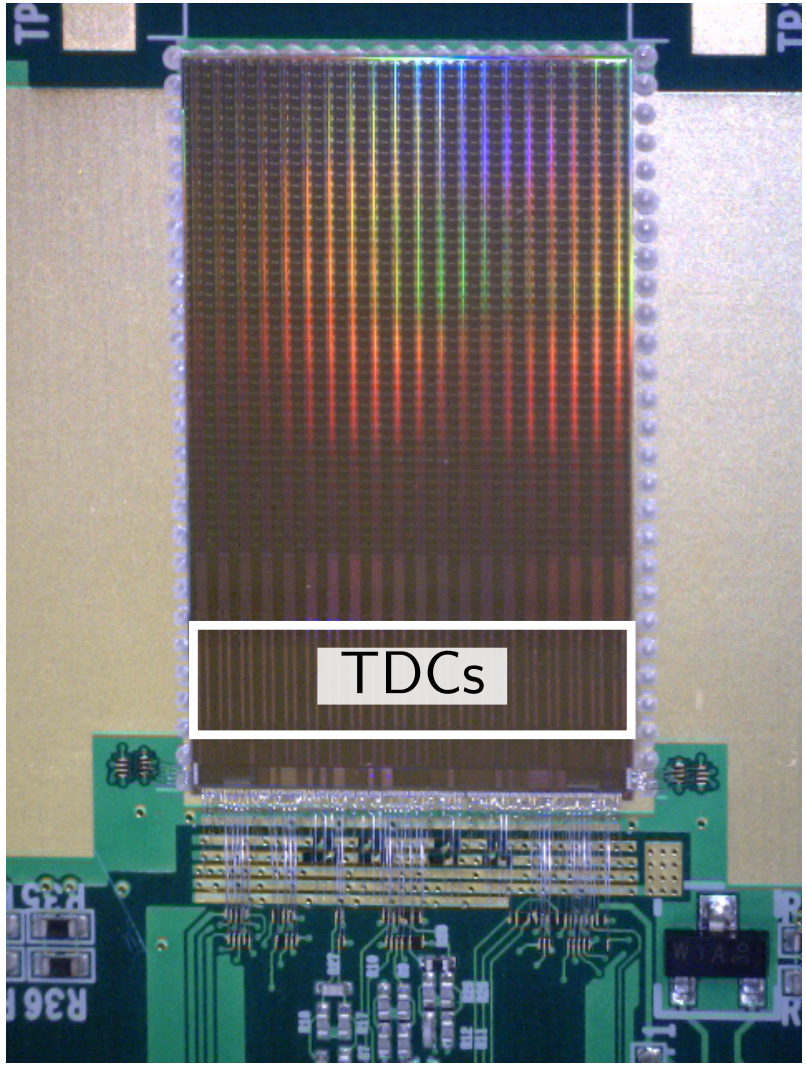




TDCPix Top Level





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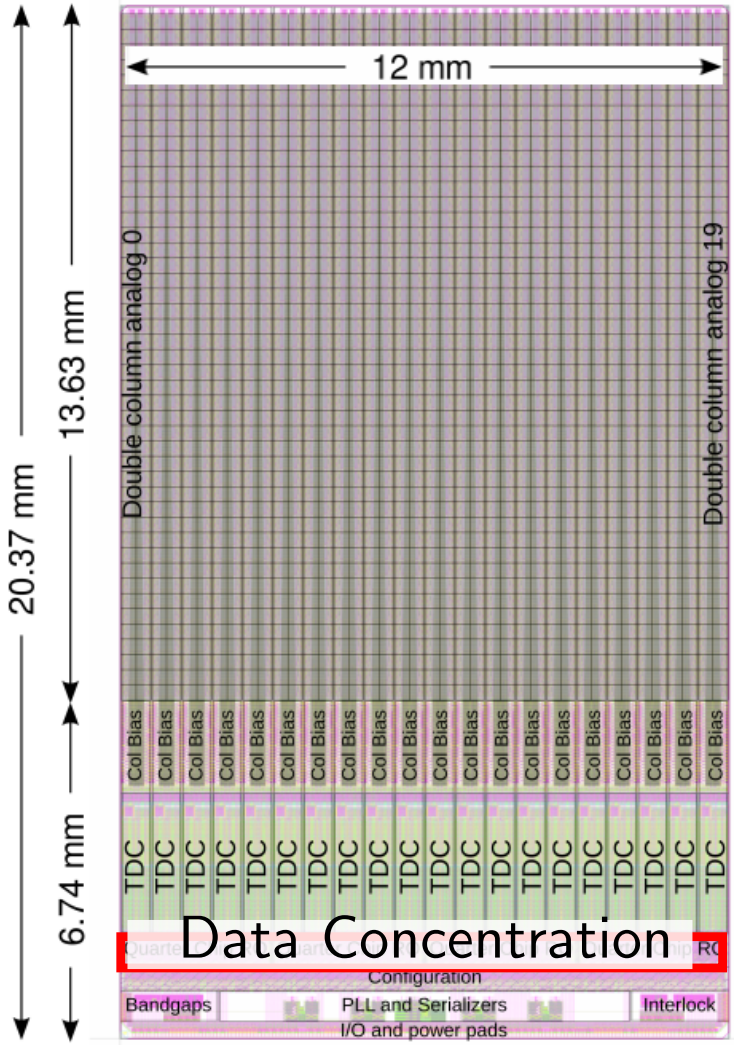

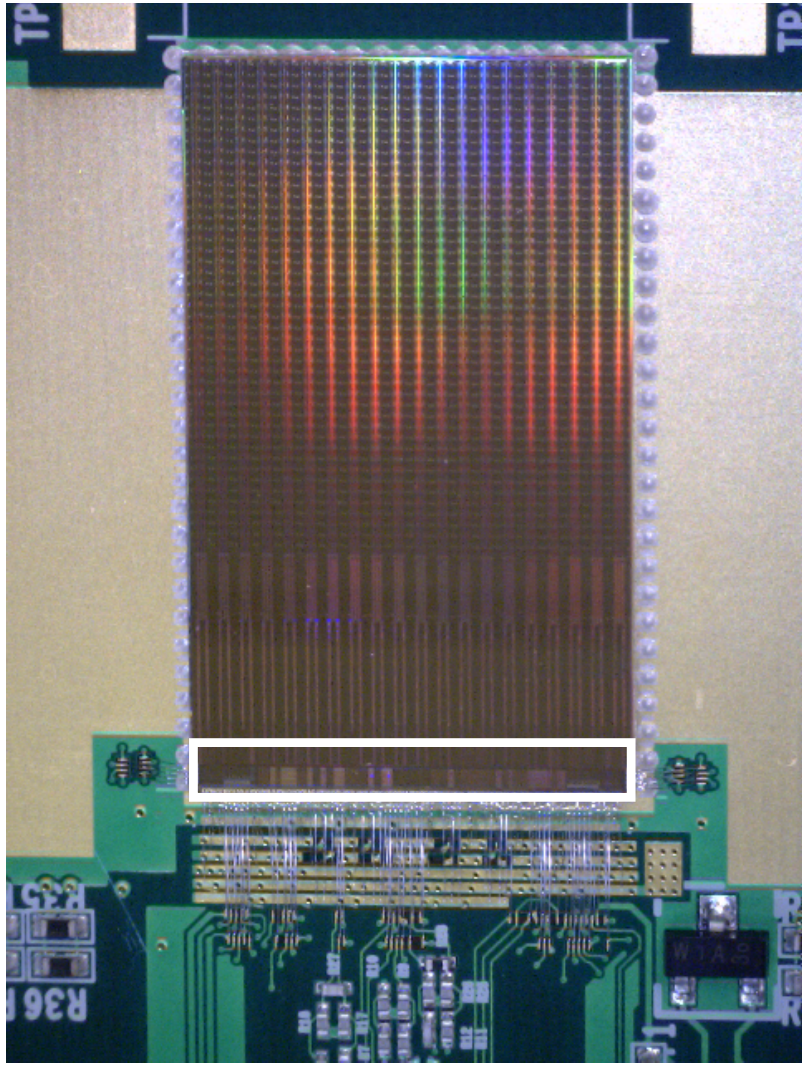

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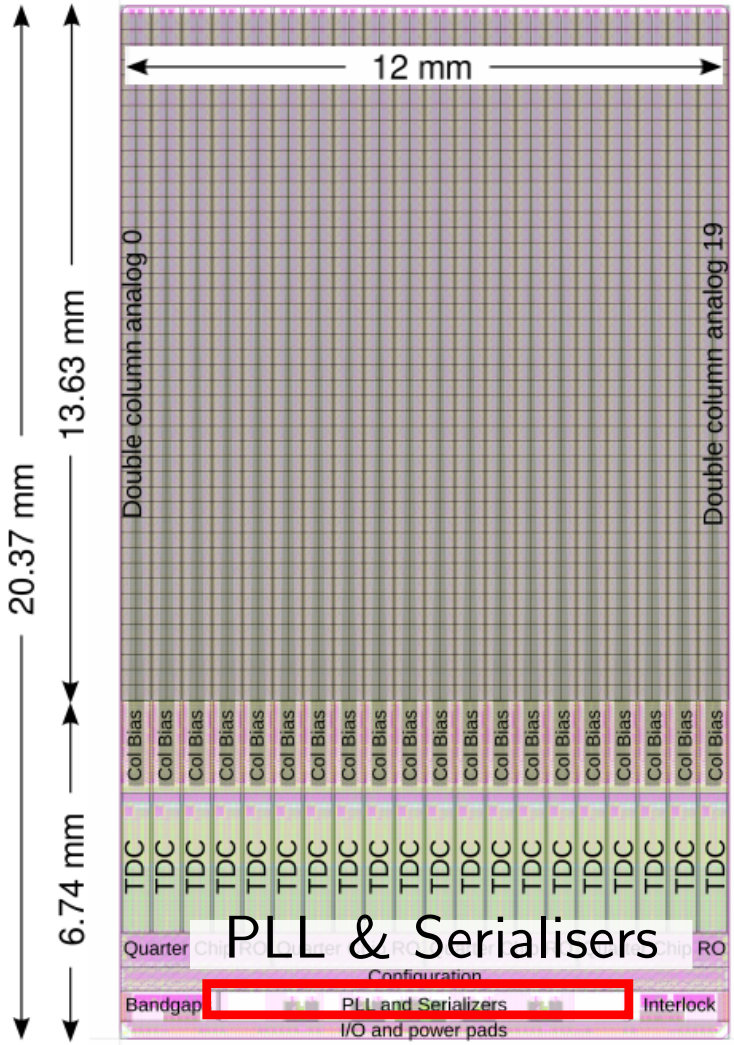

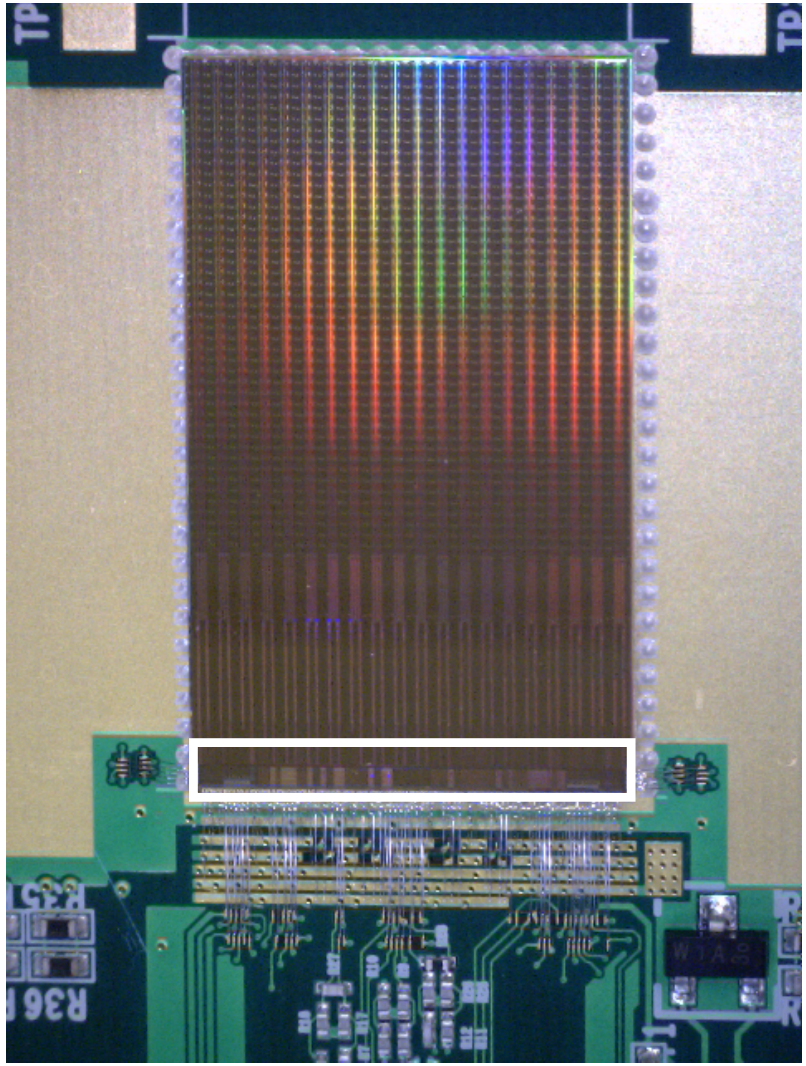

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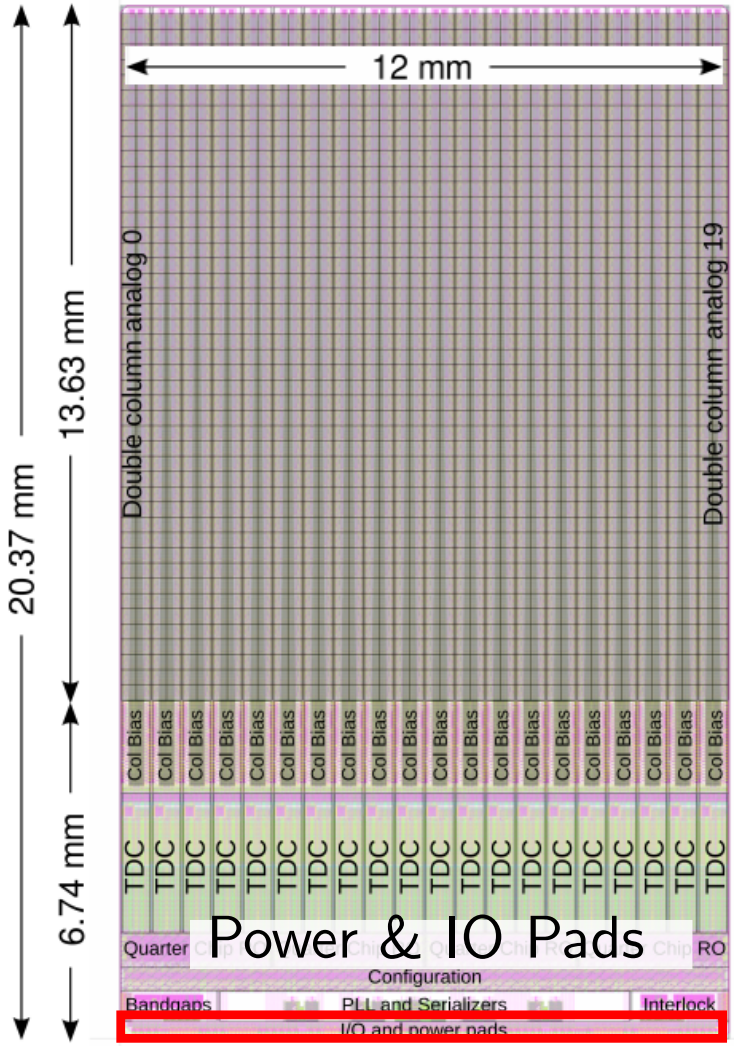
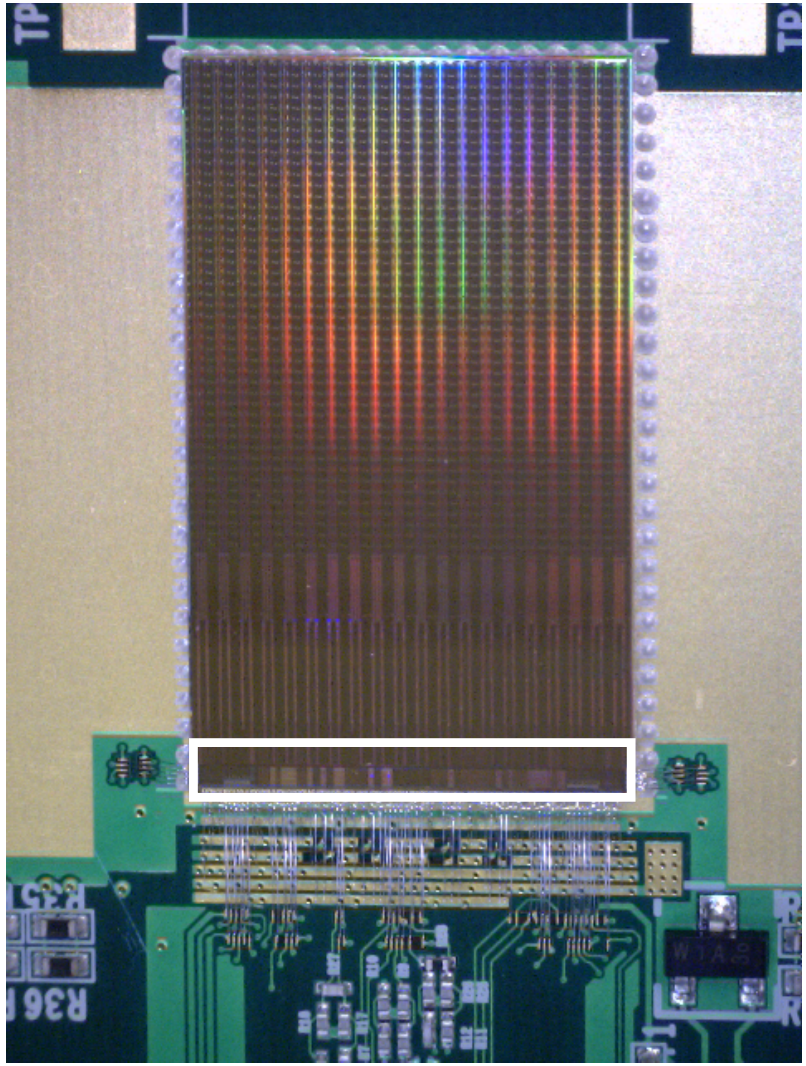
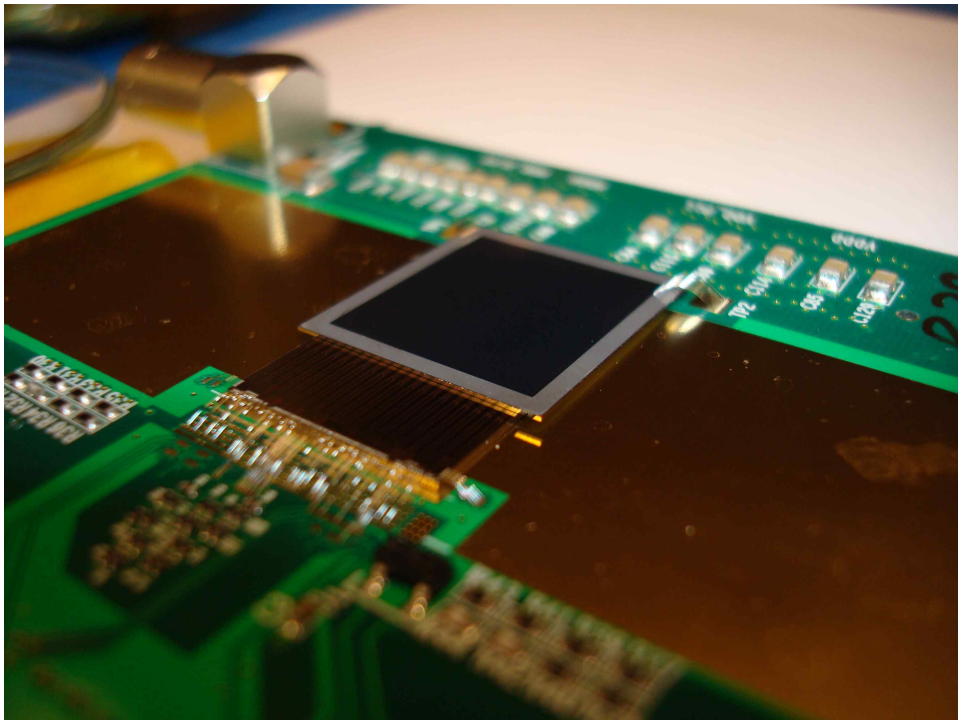
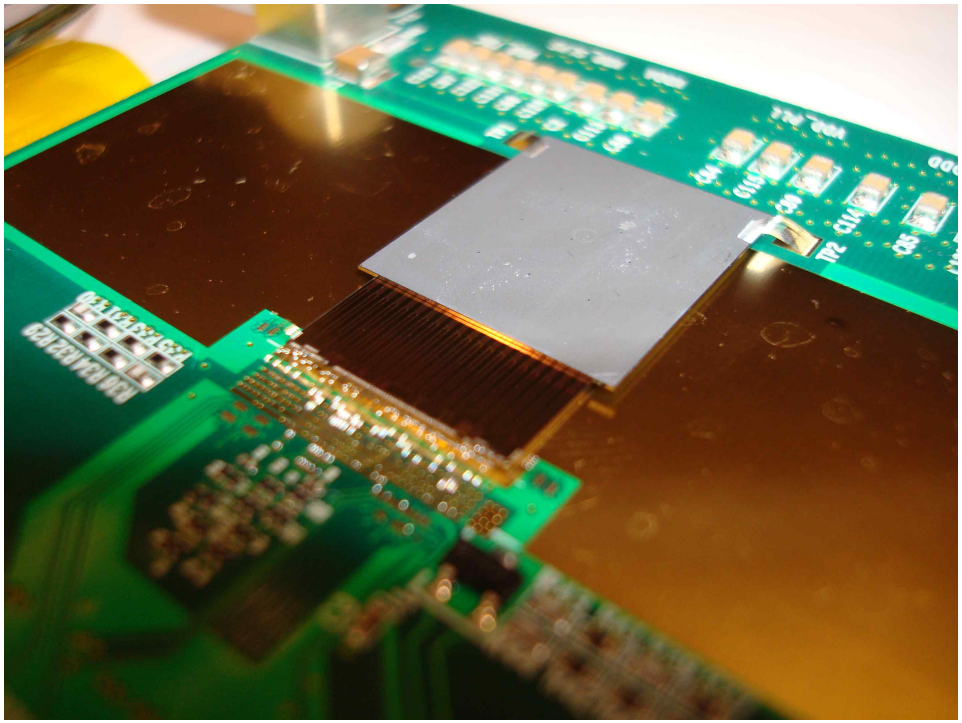




Single Chip Test Assemblies

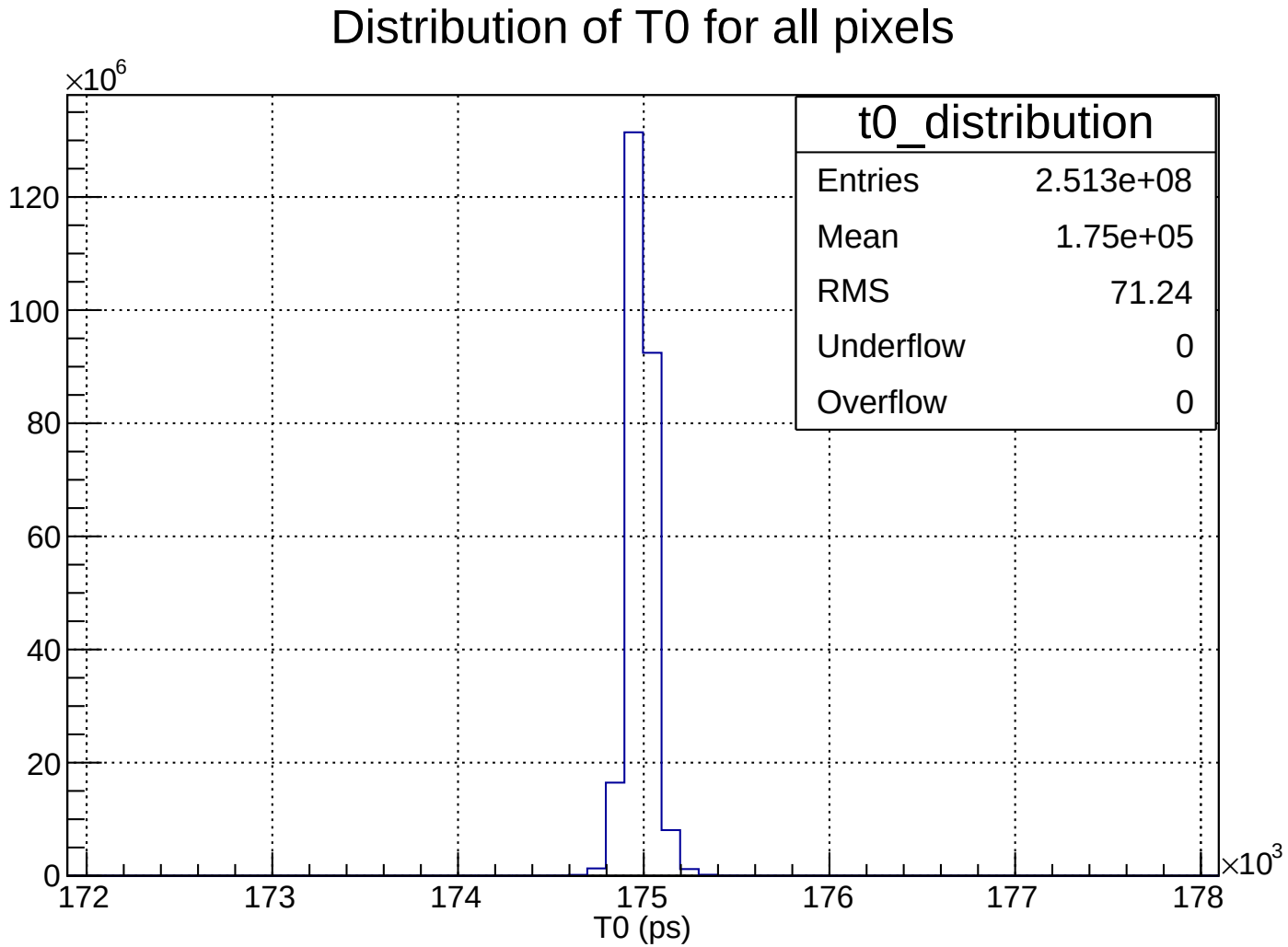


Open backside



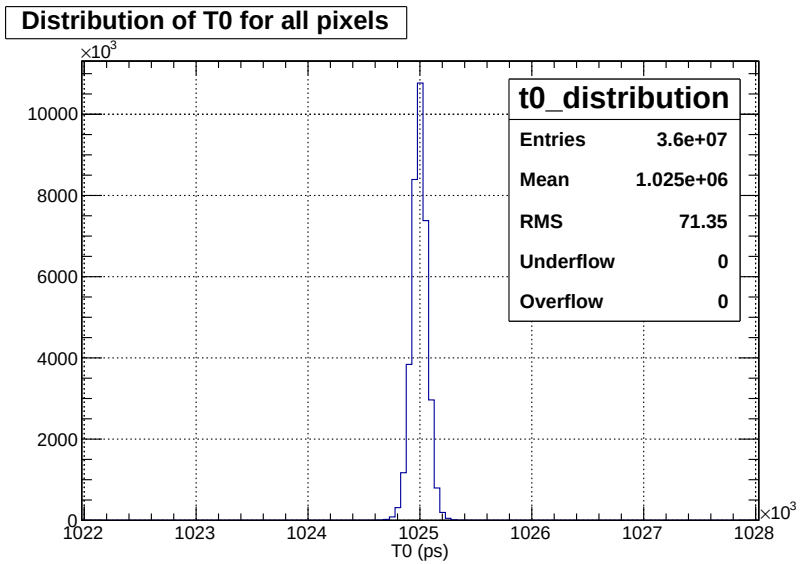
Closed backside

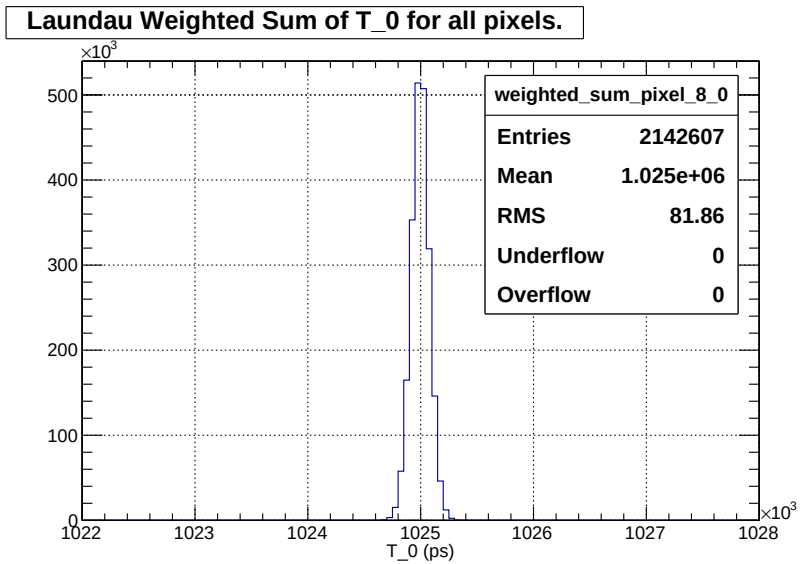
TimeWalk-Corrected (T_0) Time Resolution: Bare ASIC

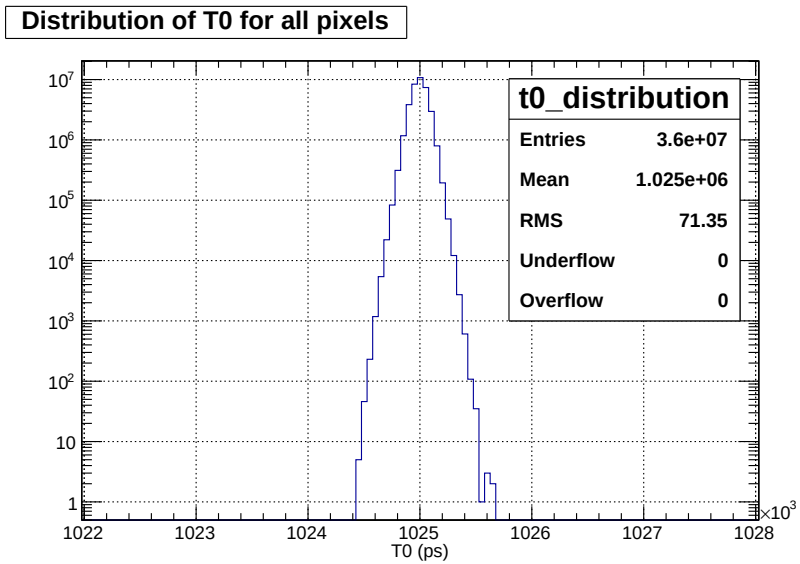


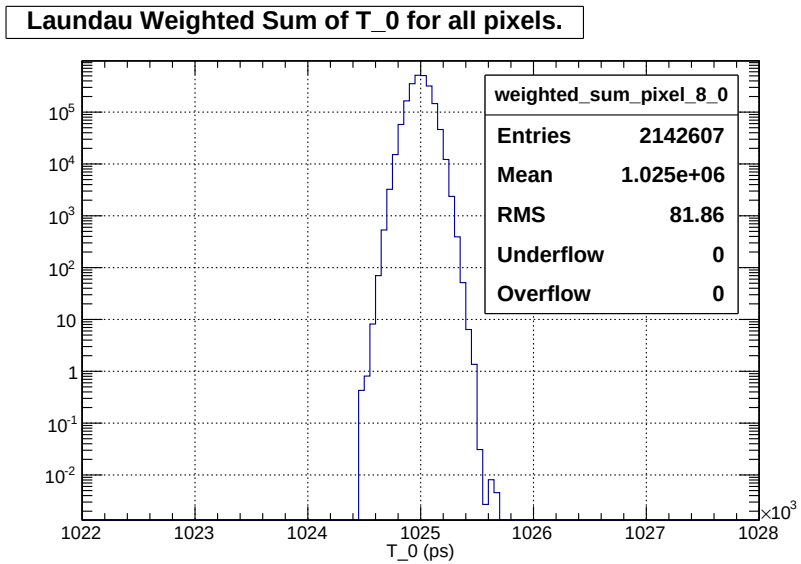
"Whole Chip" Resolution $\sim$ 72 ps RMS

Time-Walk Corrected (T_0) Resolution: Laser Light (300V)

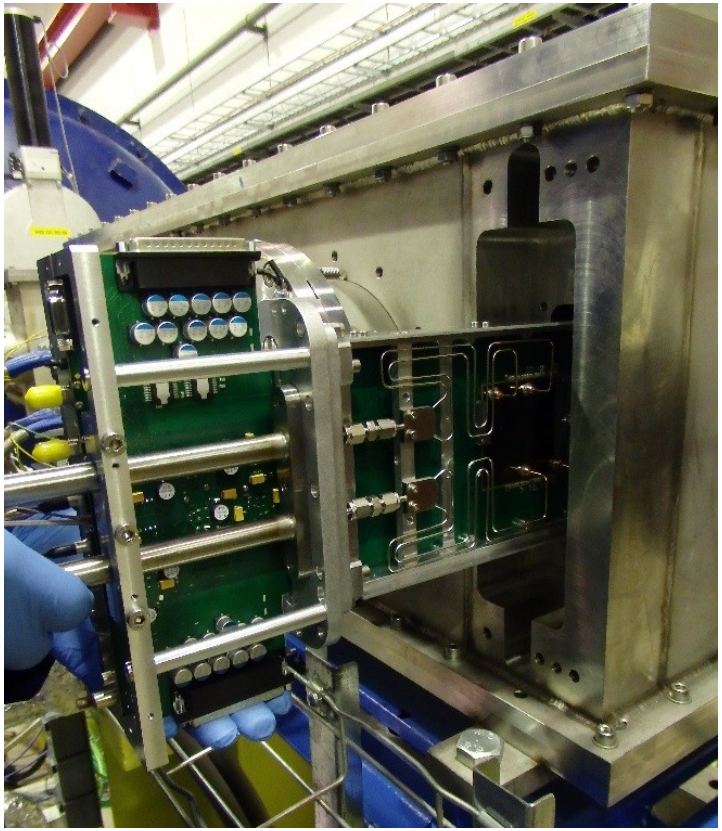


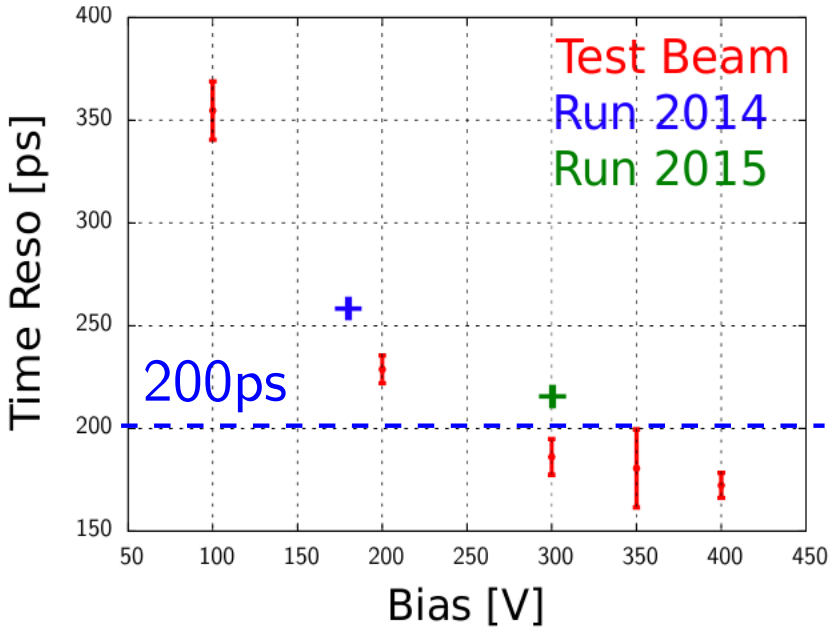


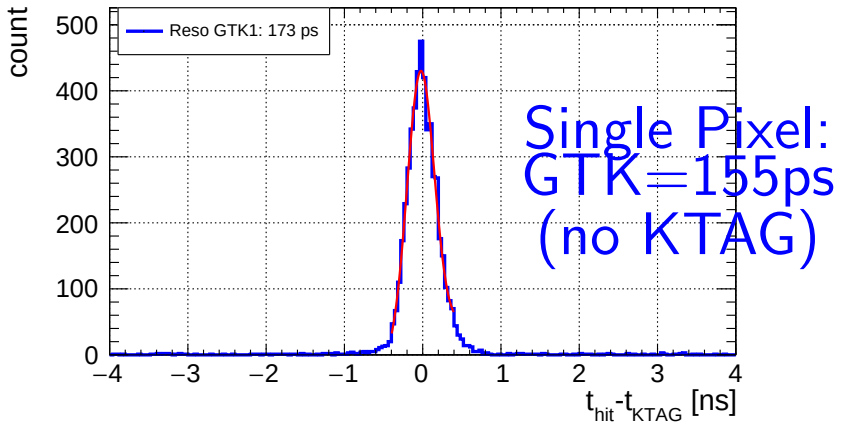




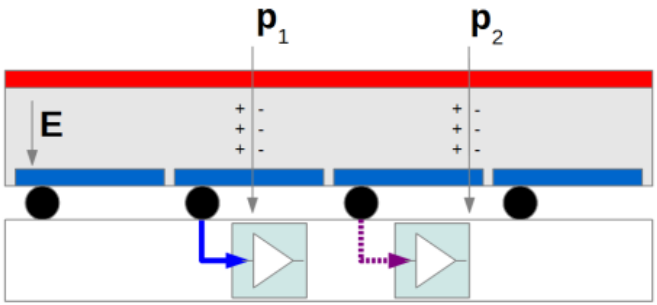
Time Resolution in the Experiment



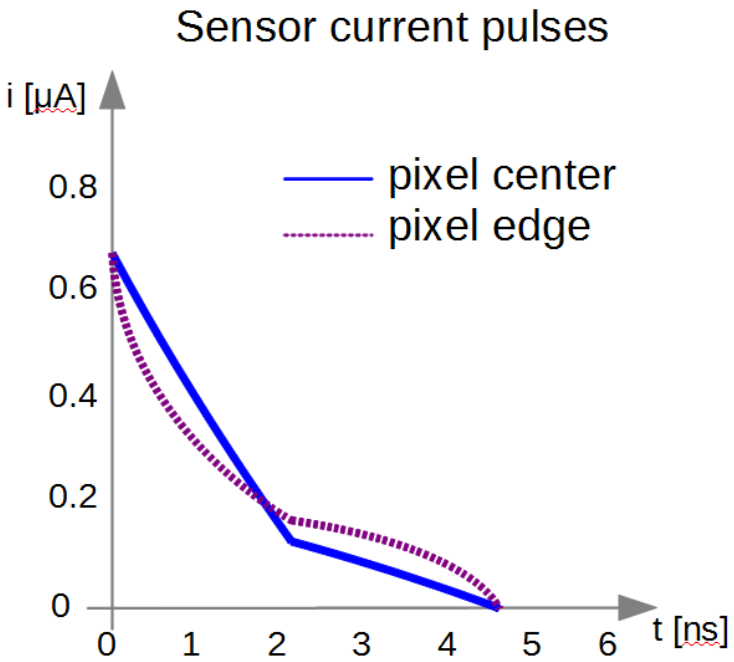


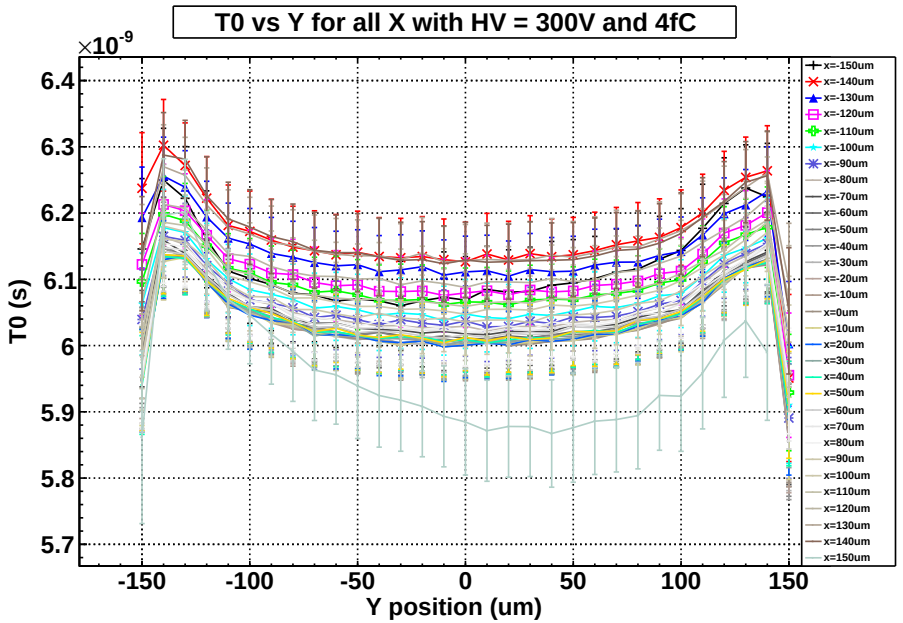


Time Resolution Limits: 1060nm Laser ($7\mu m$ spot)

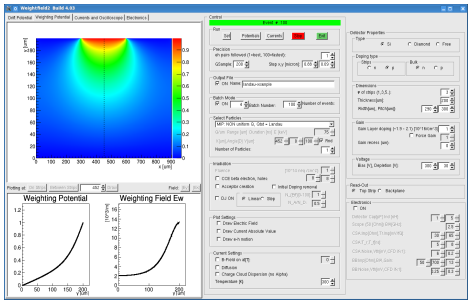


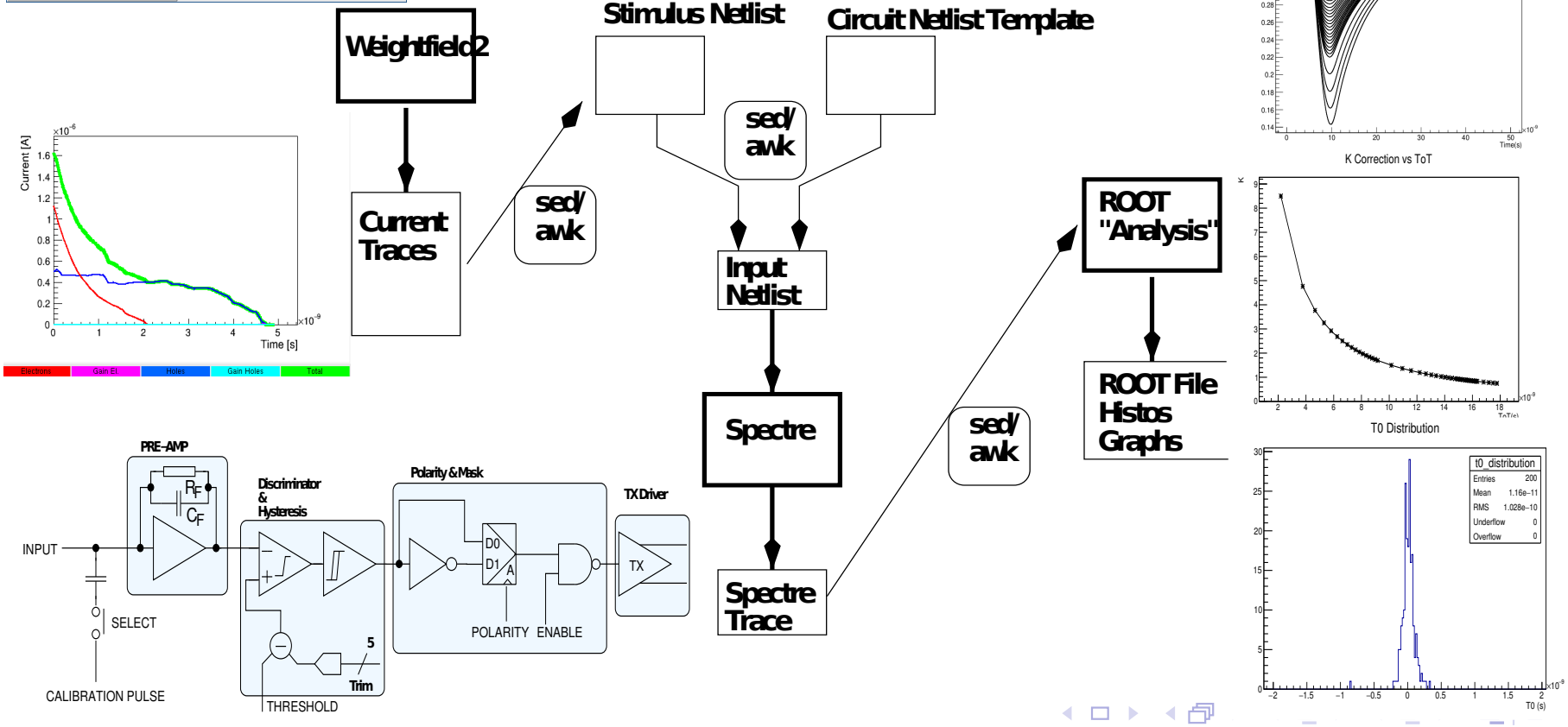
- induced current pulse on electrode changes shape
  - pre-amp output changes shape
  - adds ∼85ps
- uncorrectable contributions for current sensor



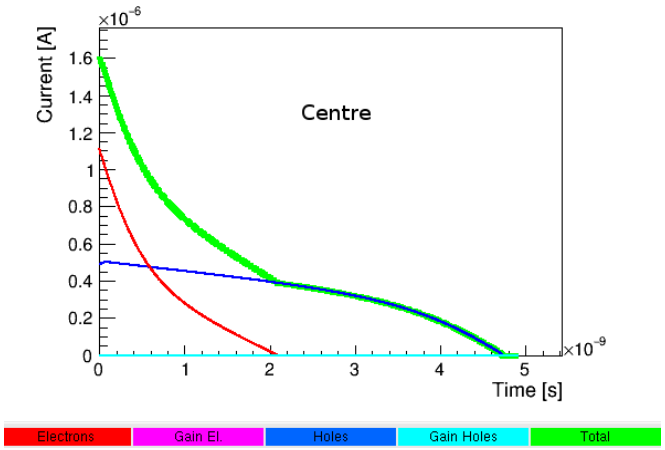


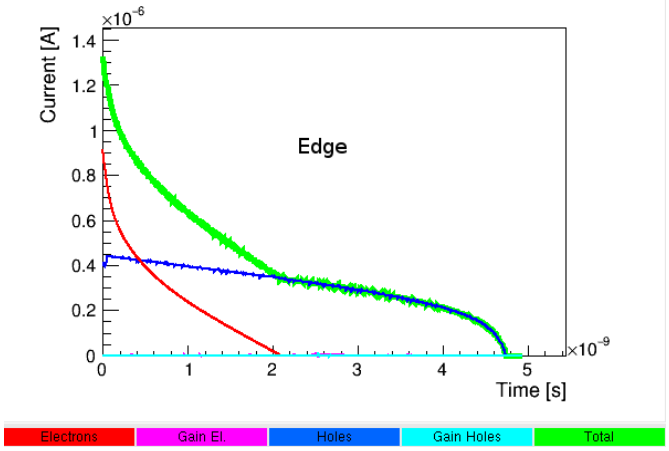
Weightfield2/Spectre Processing Flow

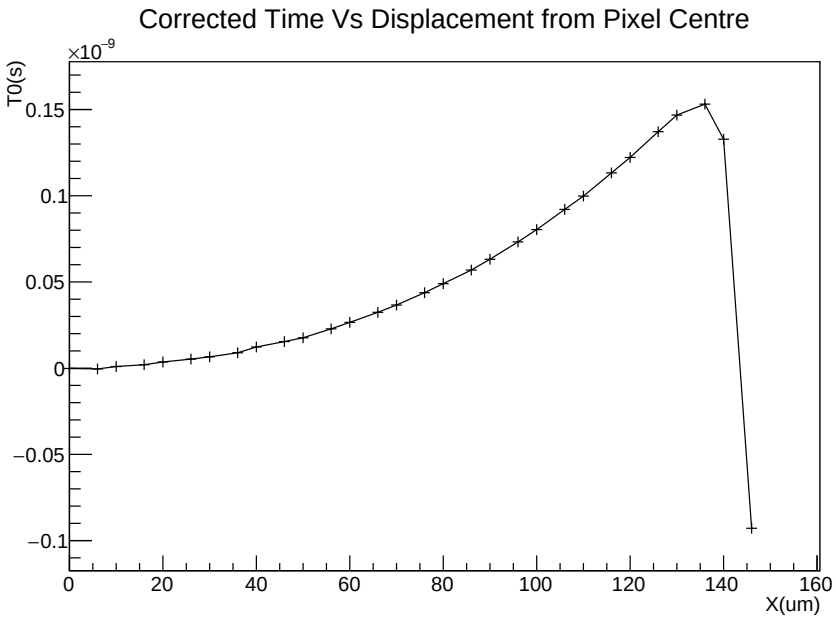




Weighting Field Simulation

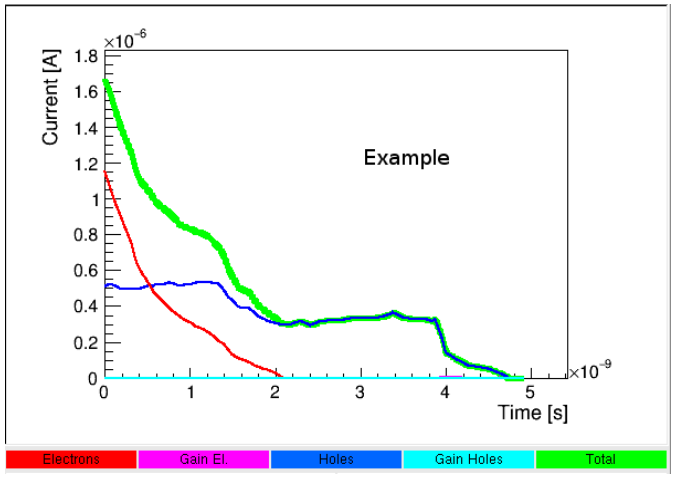


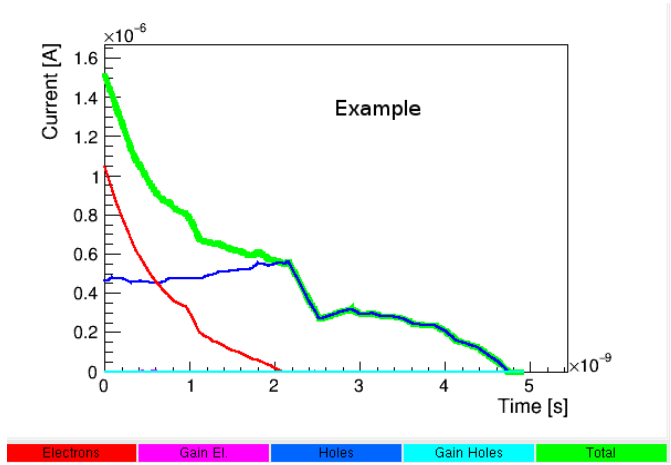


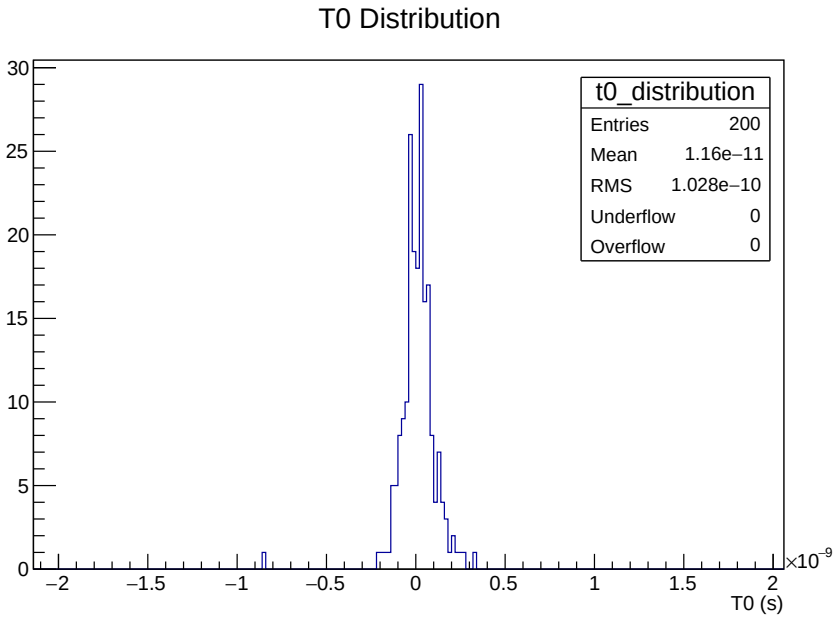


- Calibration curve at X=0μm
- 2.4 fC (uniform) stepped to edge (145μm)
- T_0 reconstructed

Charge Straggling







- Calibration curve at X=0μm
- $Q_{MP} = 2.4\, fC$, Landau fluctuation
- "pixel" centre
- $\sigma_{T0} \sim 100\, ps$

Time Resolution: Summary of Contributions

$$\text{Time Resolution} = \sqrt{\sigma^2_{electronics} + \sigma^2_{WeightingField} + \sigma^2_{straggling}}$$

$$= \sqrt{80^2 + 85^2 + 100^2} \sim 150\,ps$$

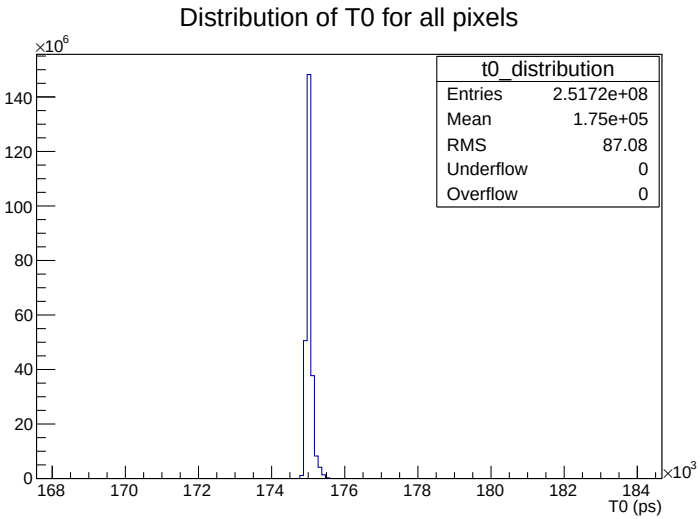
Summary

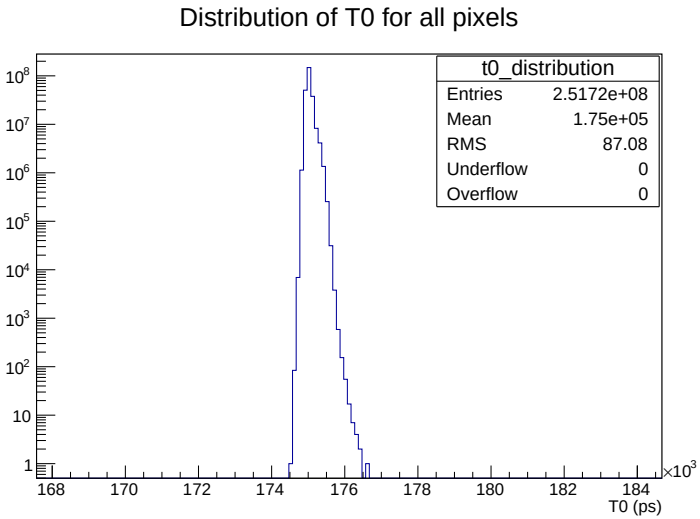
- NA62
  - Ultra rare decay: $K^+ \to \pi^+ \nu\nu$
  - Fixed target experiment at SPS, 250m long
- GTK
  - 3 plane hybrid pixel detector
  - extremely challenging design constraints
  - Material Budget: $<$0.5% X_0 per station
  - time resolution $<$ 200 ps per plane
  - TDCPix readout ASIC designed at CERN
- Performance
  - TDCPix $\sim$75 ps RMS
  - Laser light $\sim$80 ps RMS (@300V)
  - Beam Particles $\sim$155 ps RMS for single pixel (@300V)
  - Time resolution differences partially (mostly?) understood
  - Weightfield2 (1-D)/Spectre simulation: $\sim$150 ps RMS
  - Beam test with high spatial resolution telescope

Thanks for your attention !!

Backup Slides.

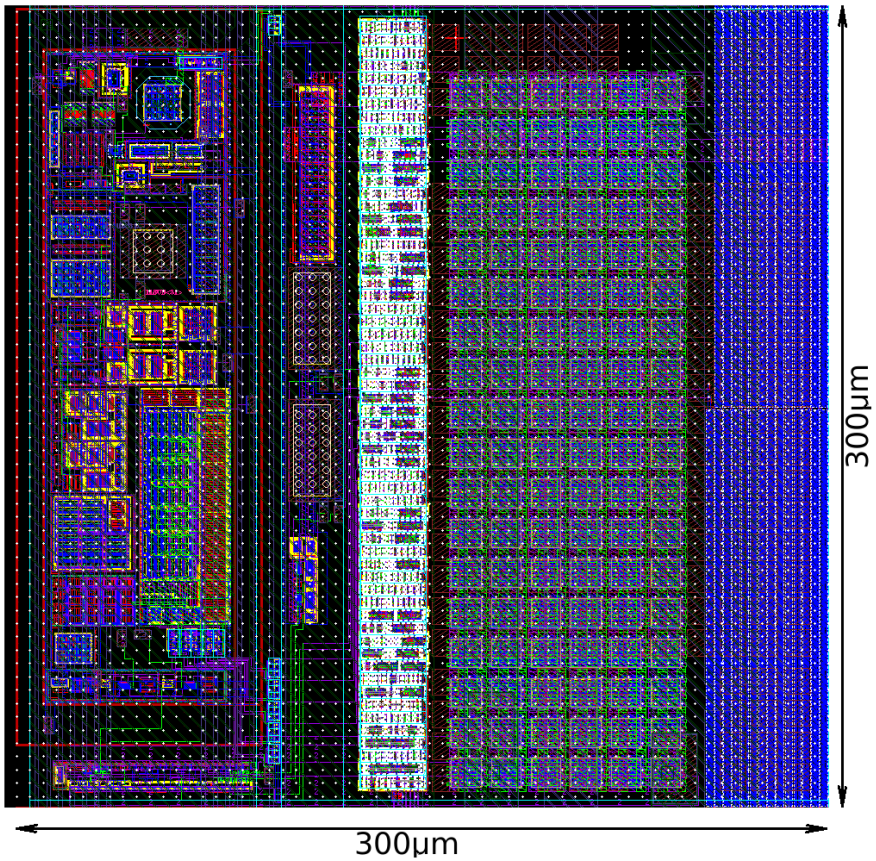
Post TID Time Resolution: bare chip





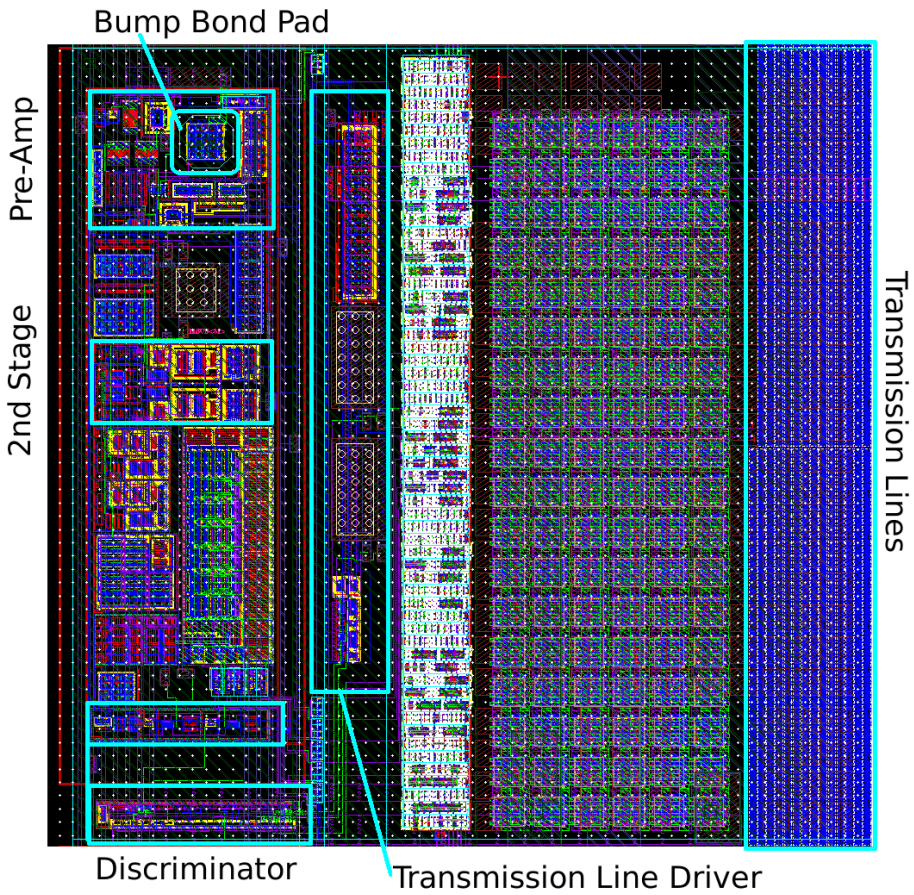
- Pixel Matrix: up to 6 Mrad
- EOC: up to 900 krad
- Calibration:
  - 0.9-7.5 fC (fine grained to $\sim$3 fC
  - 10^4 hits/point
  - spline used for "continuous" correction
- Measurement:
  - 1.0-7.5 fC
  - ana doesn't "know" which charge it's correcting
- T_0 contains all pixels and all measurement charges
- no Landau weighting
- C.f. $\sim$75 ps for un-irradiated case

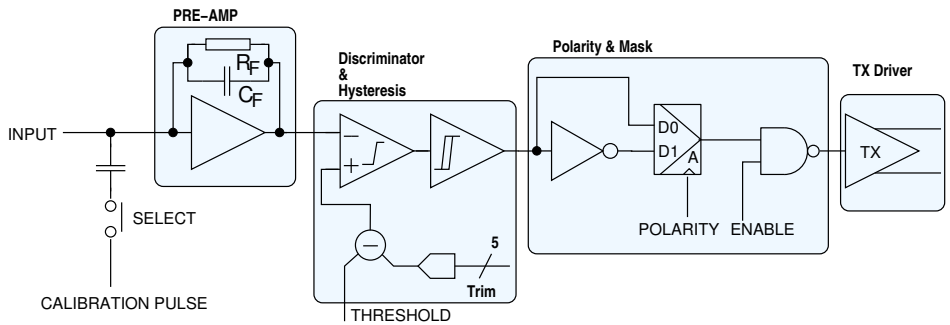
Pixel Layout:



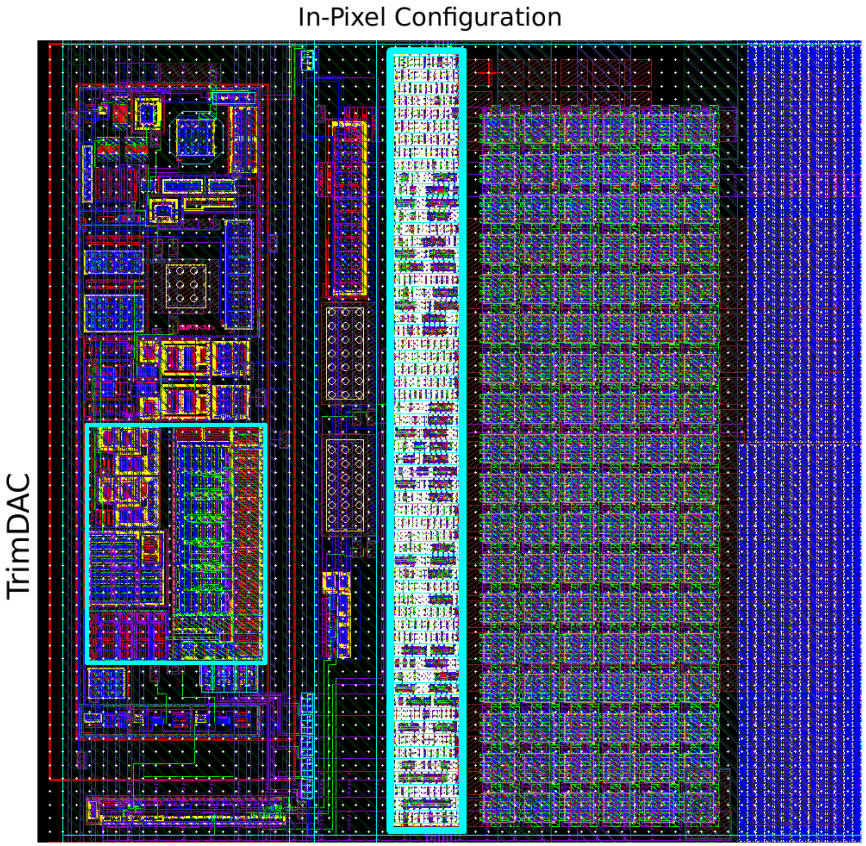
300x300μm^2 cell

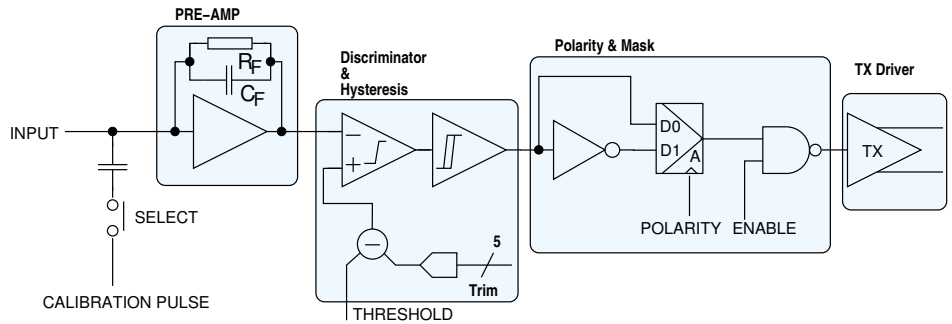
Pixel Layout: Signal Path



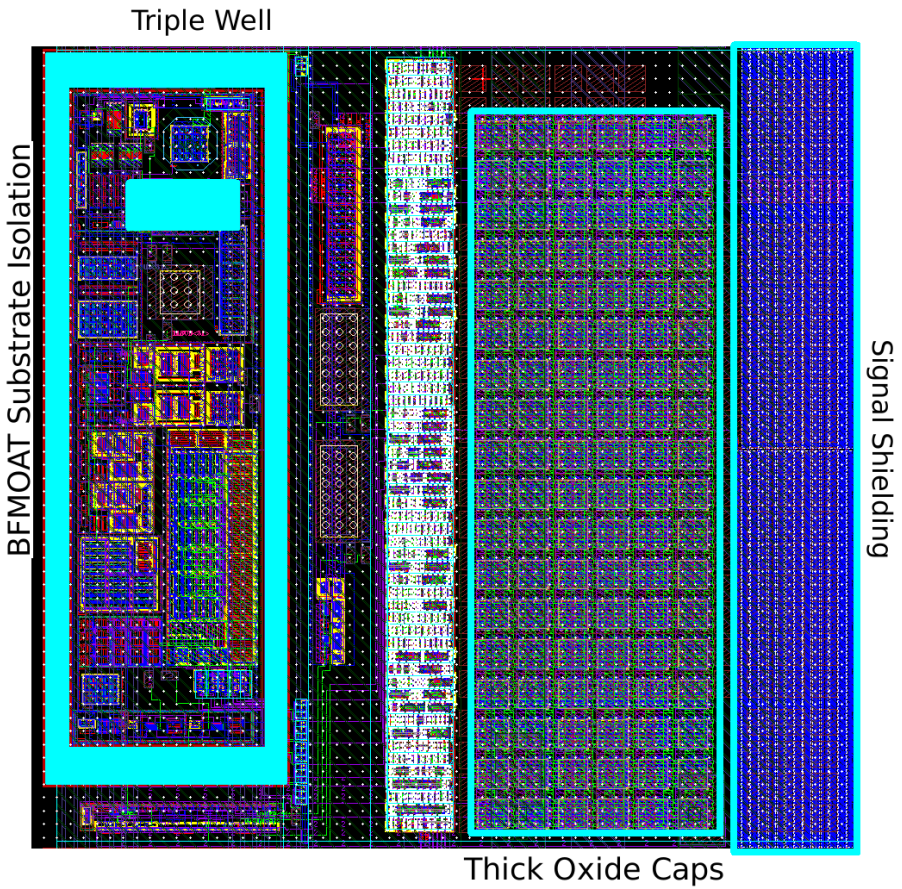


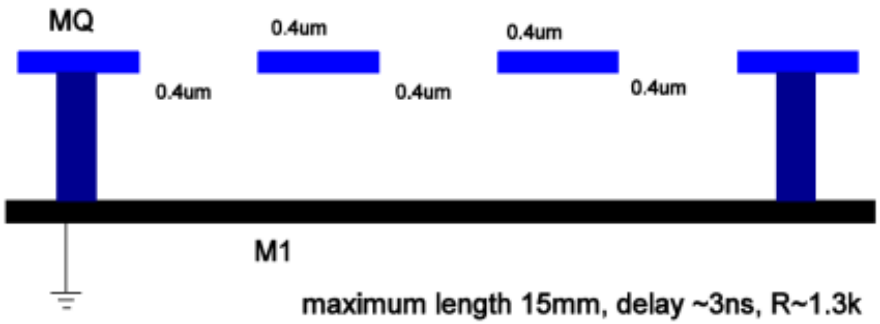
Pixel Layout: Trimming & Configuration





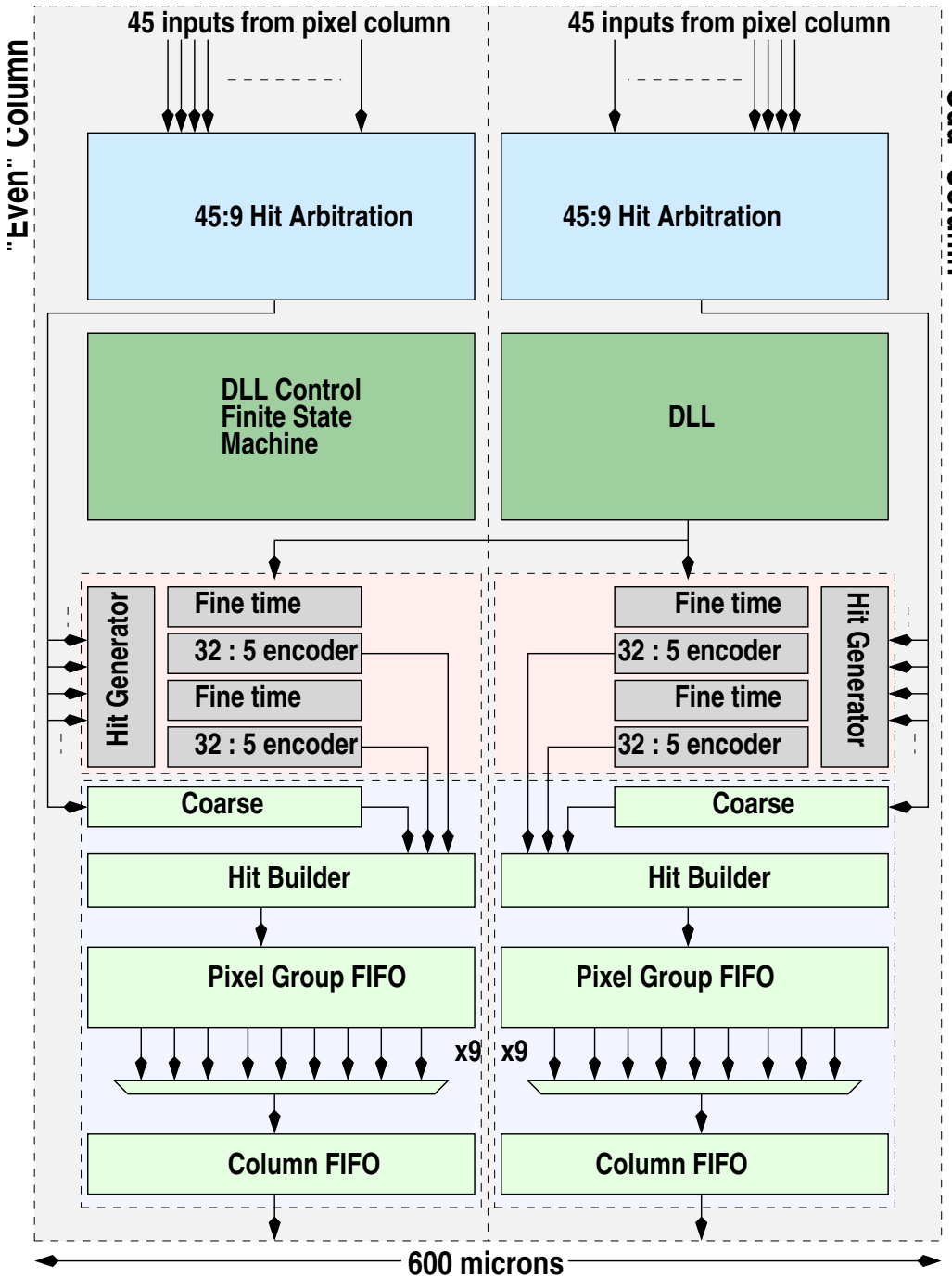
Pixel Layout: Noise Mitigation

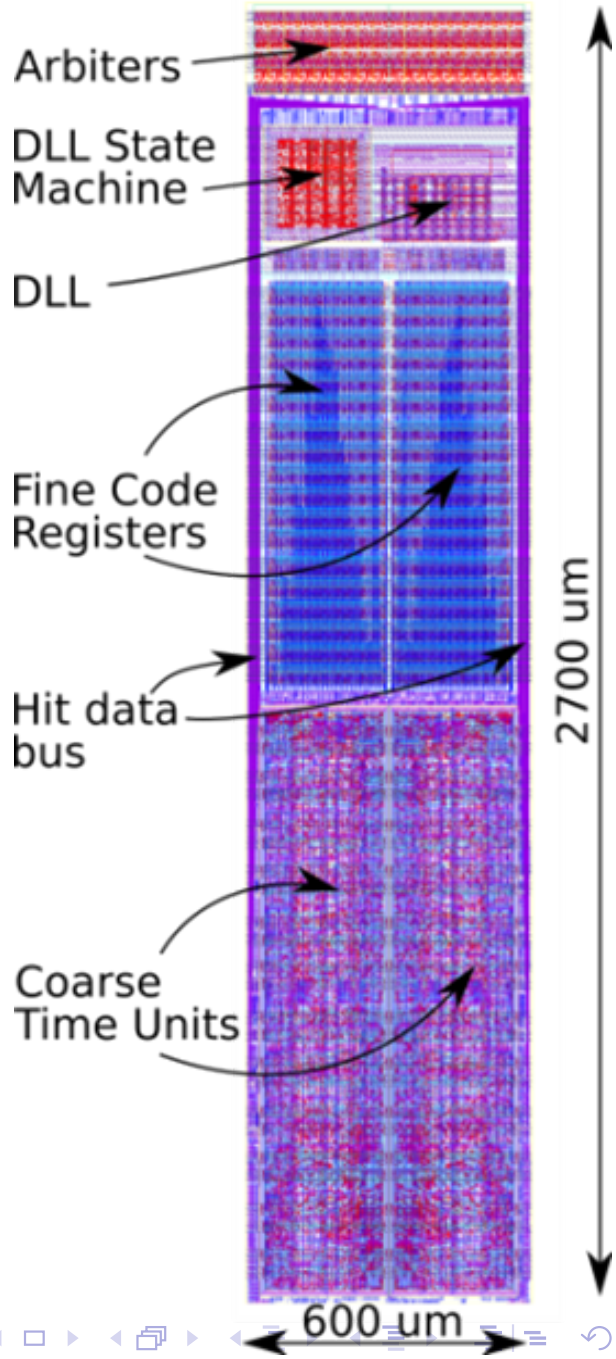




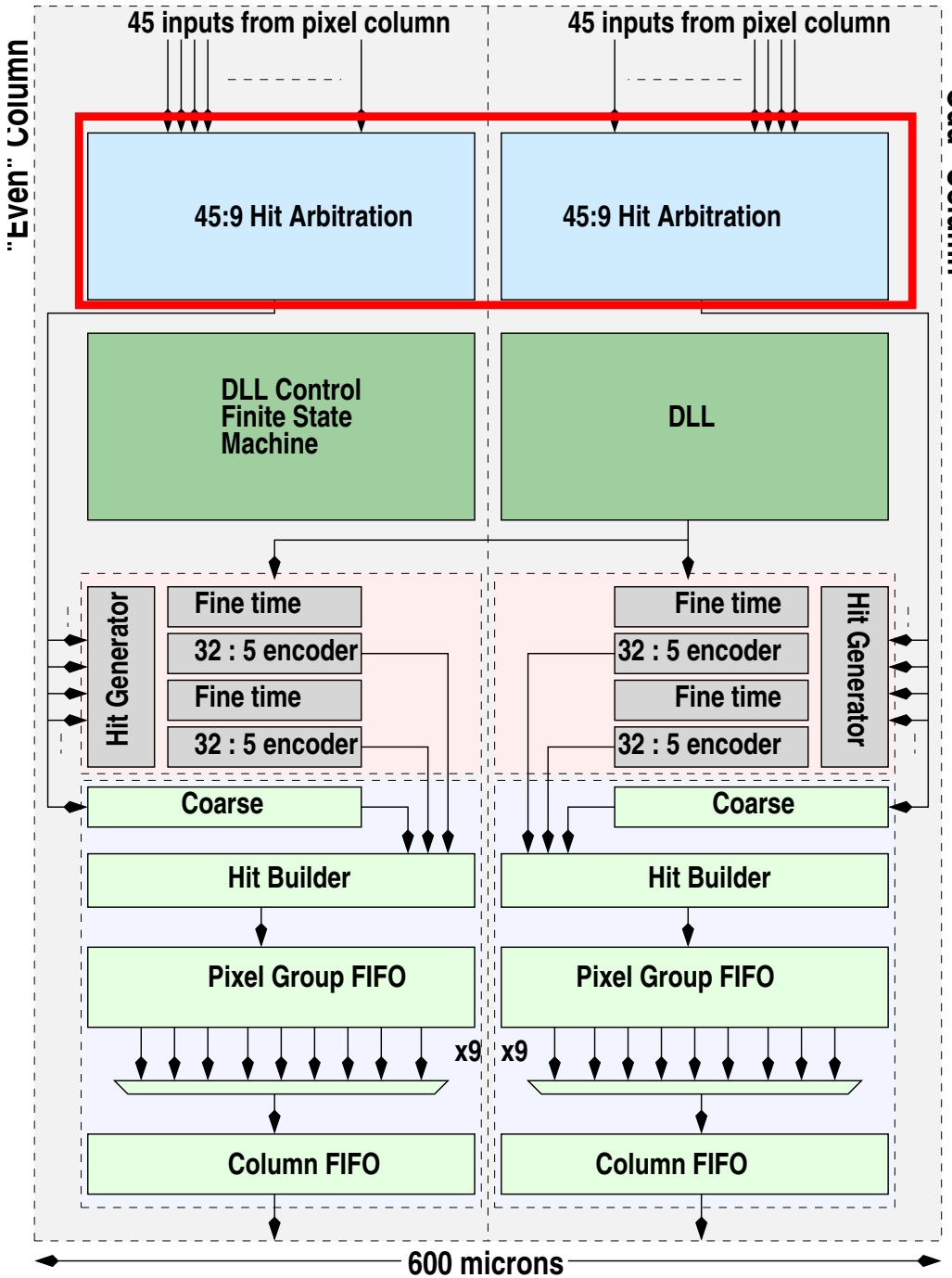
- Triple well (input transistor)
- BFMOAT substrate isolation
- signal shielding
- Power supply decoupling

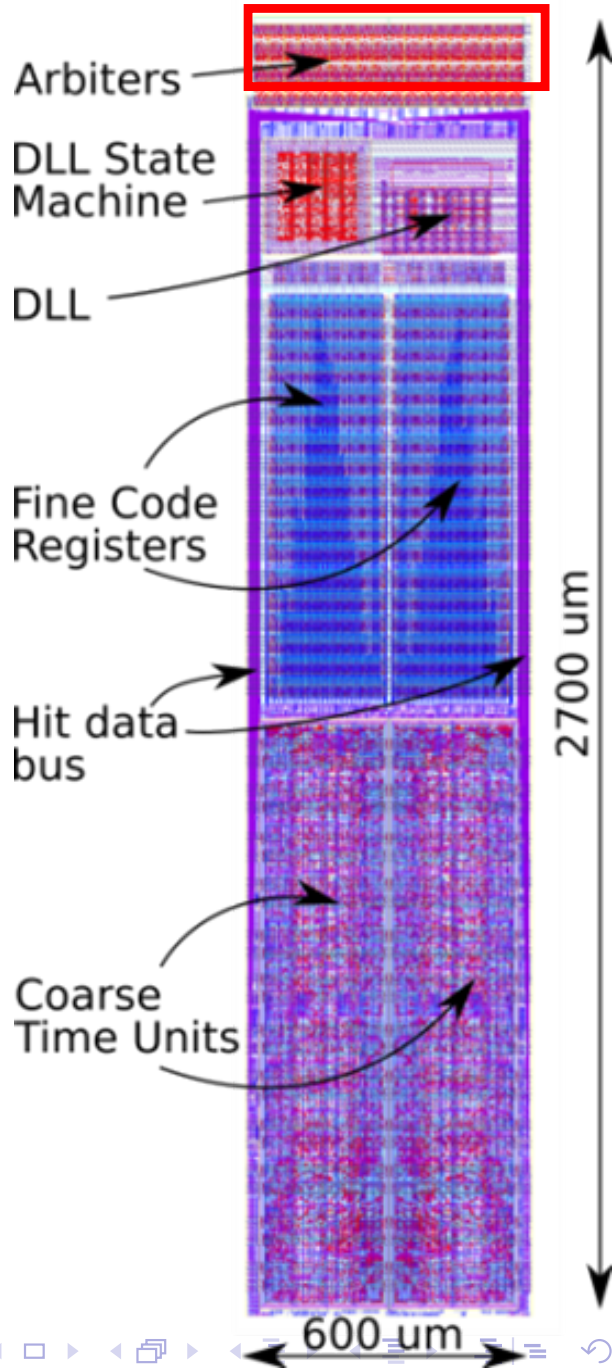
TDC: Schematic and Layout



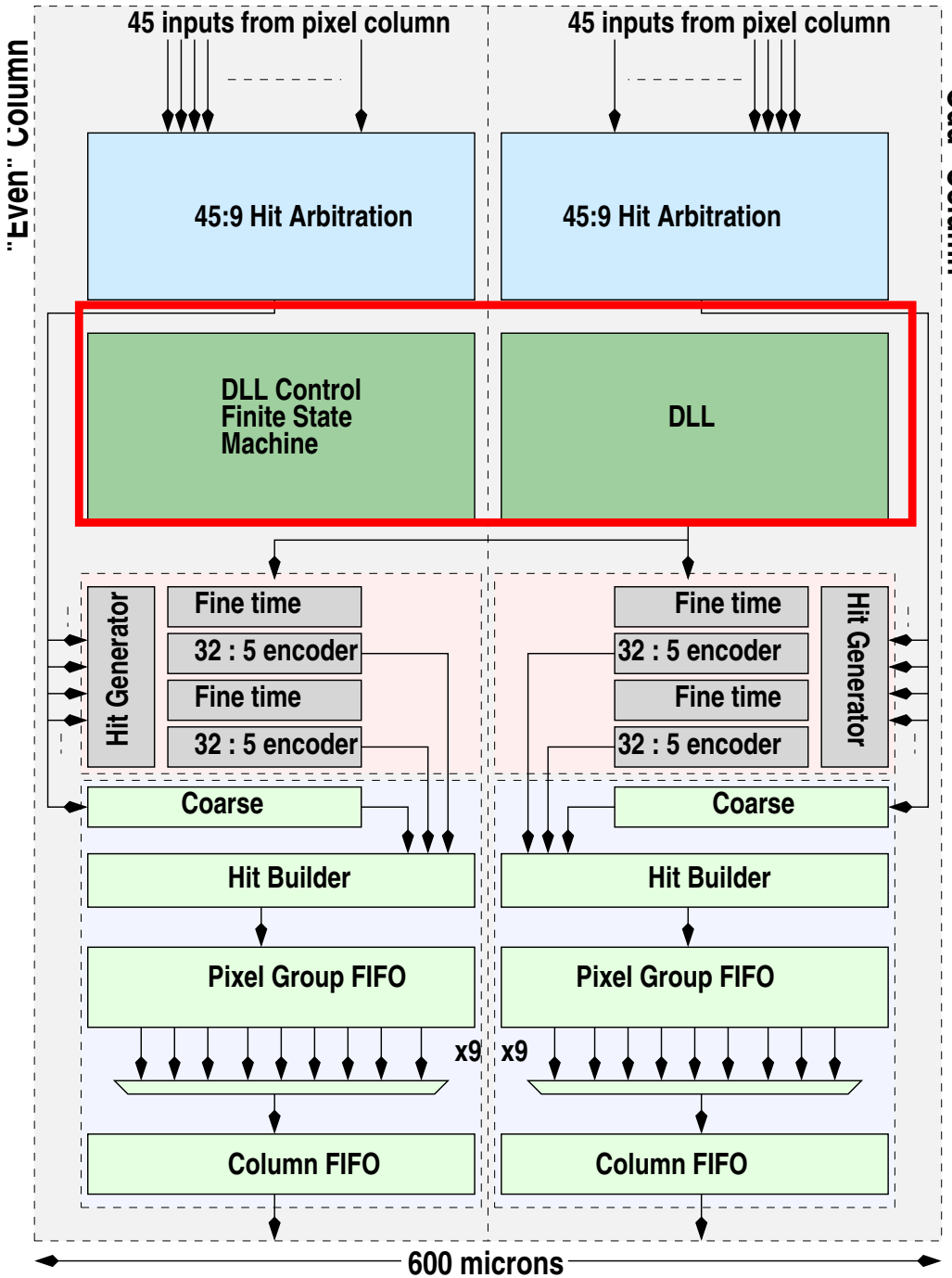


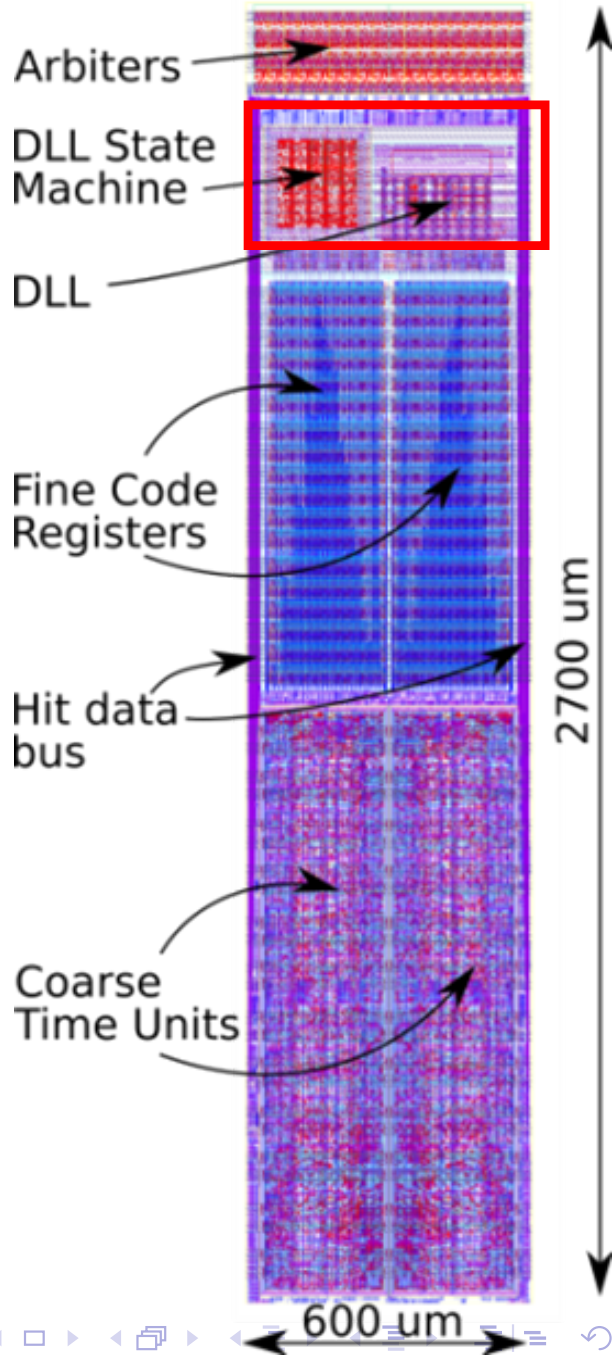
TDC: Schematic and Layout



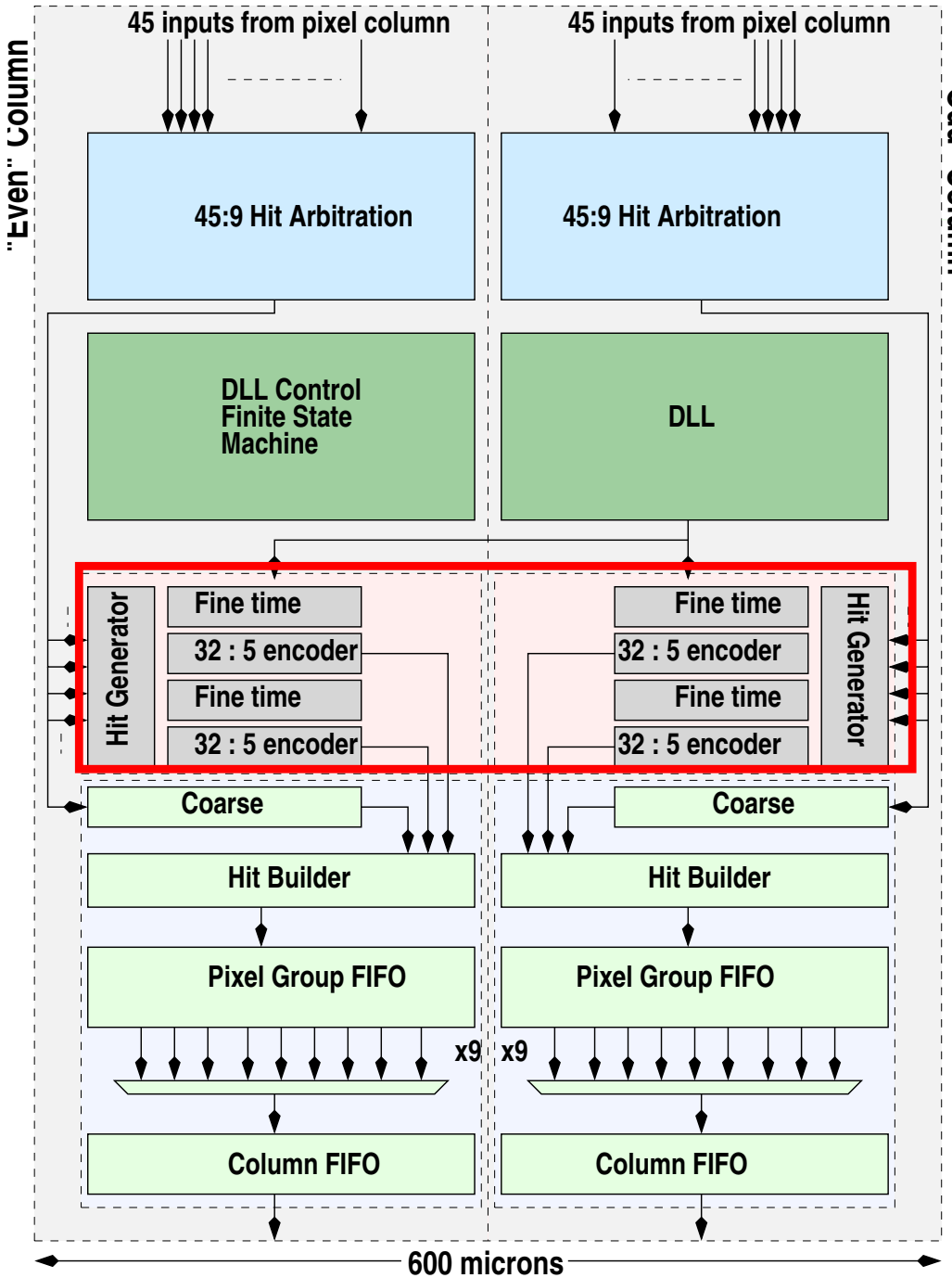


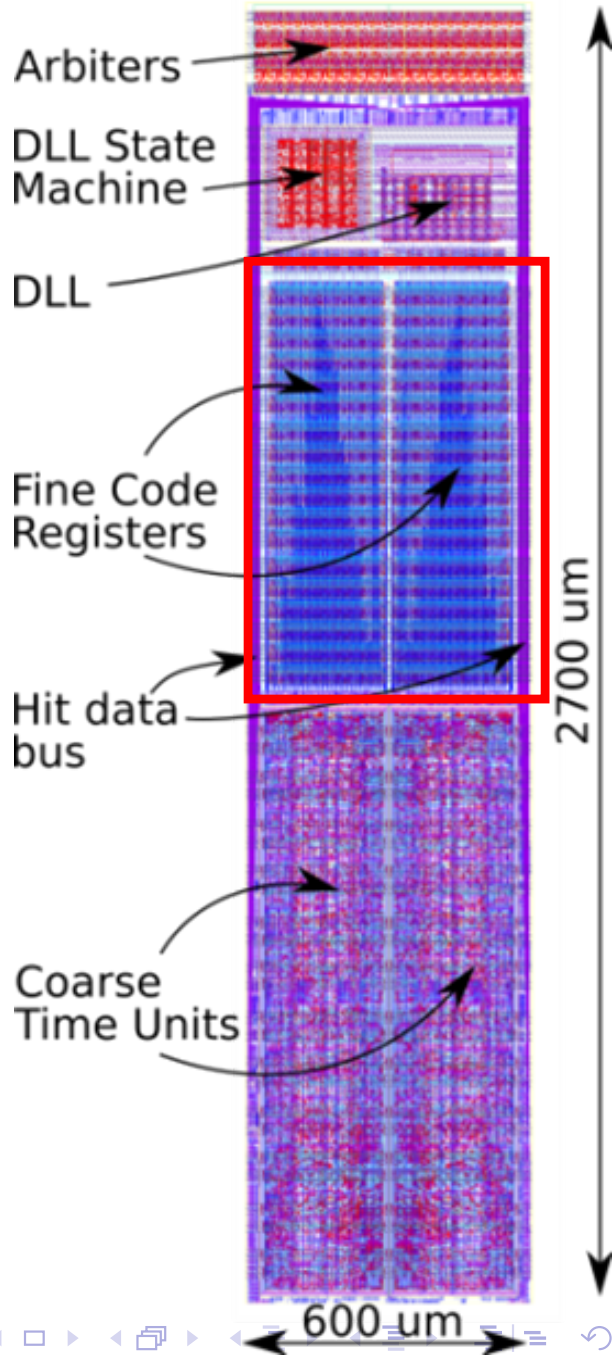
TDC: Schematic and Layout



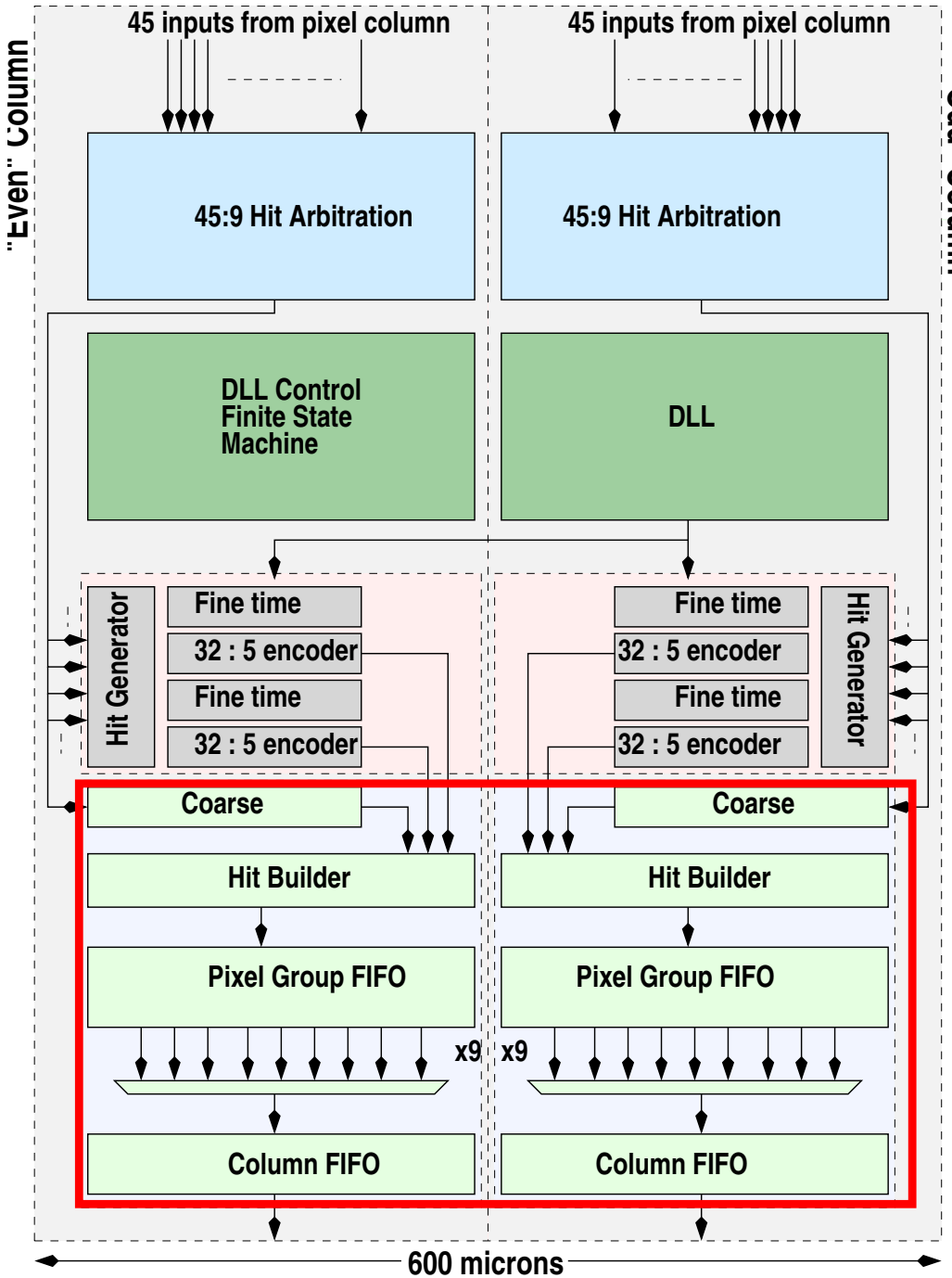


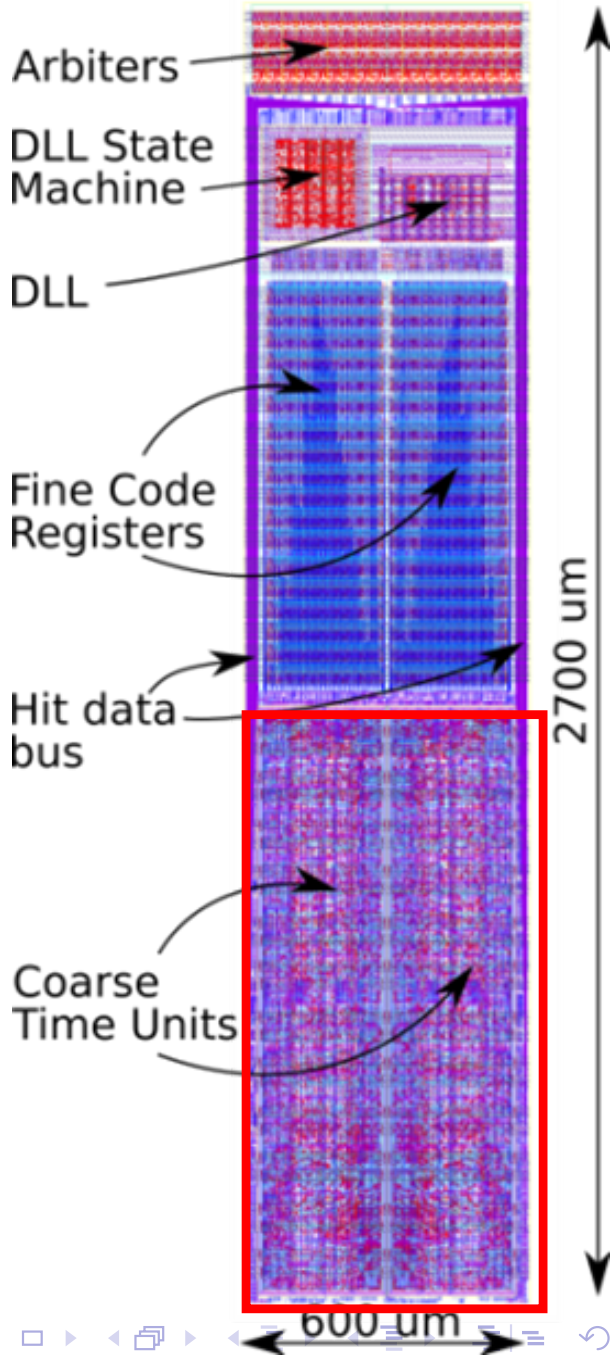
TDC: Schematic and Layout



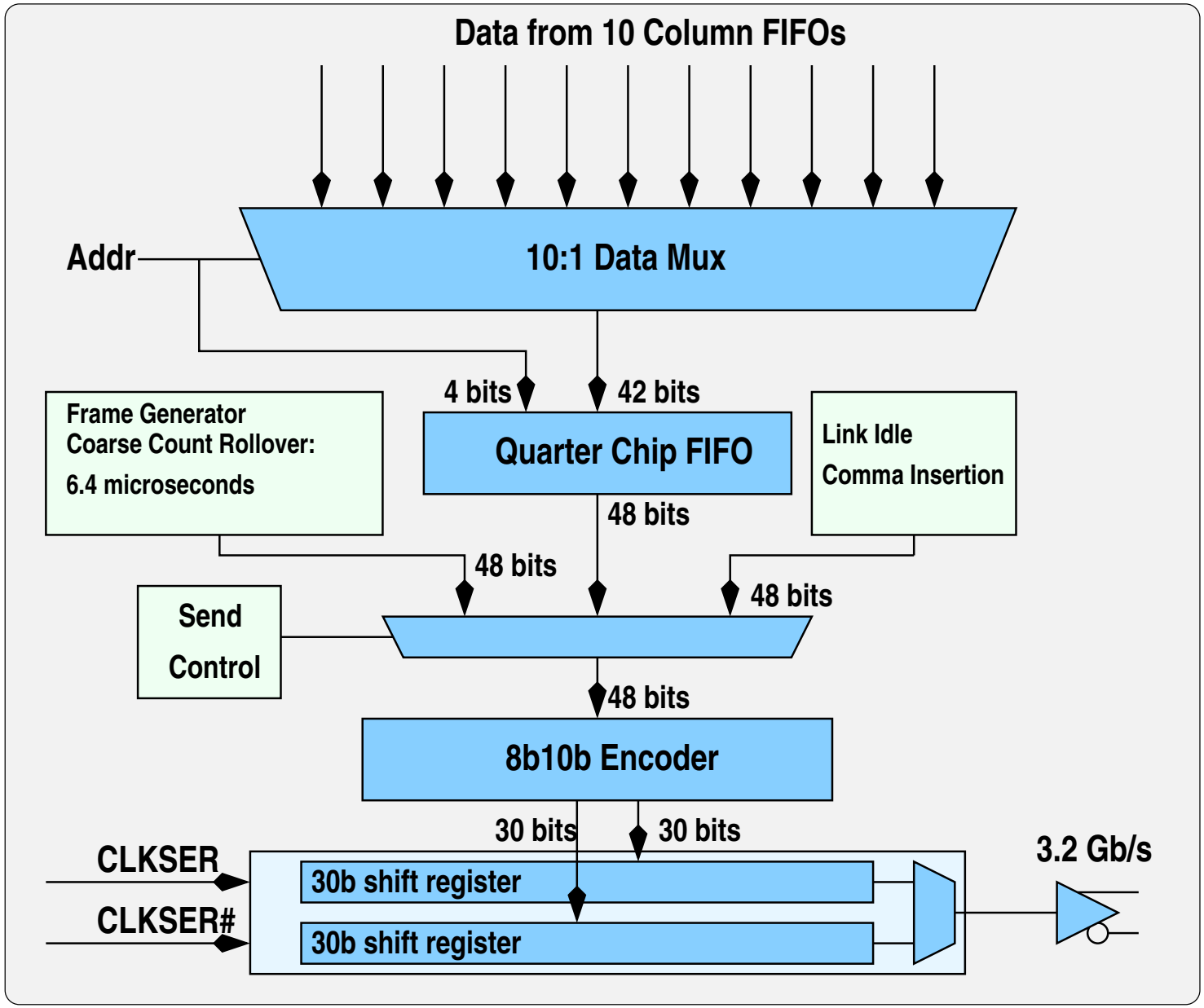


TDC: Schematic and Layout



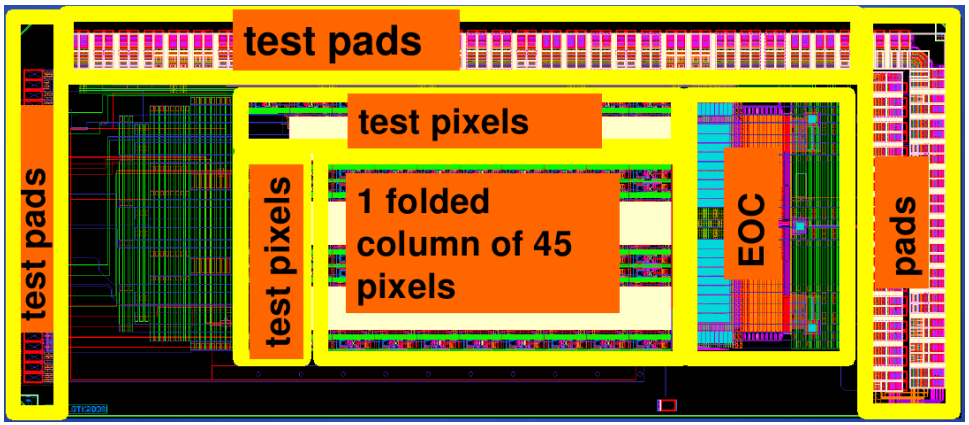


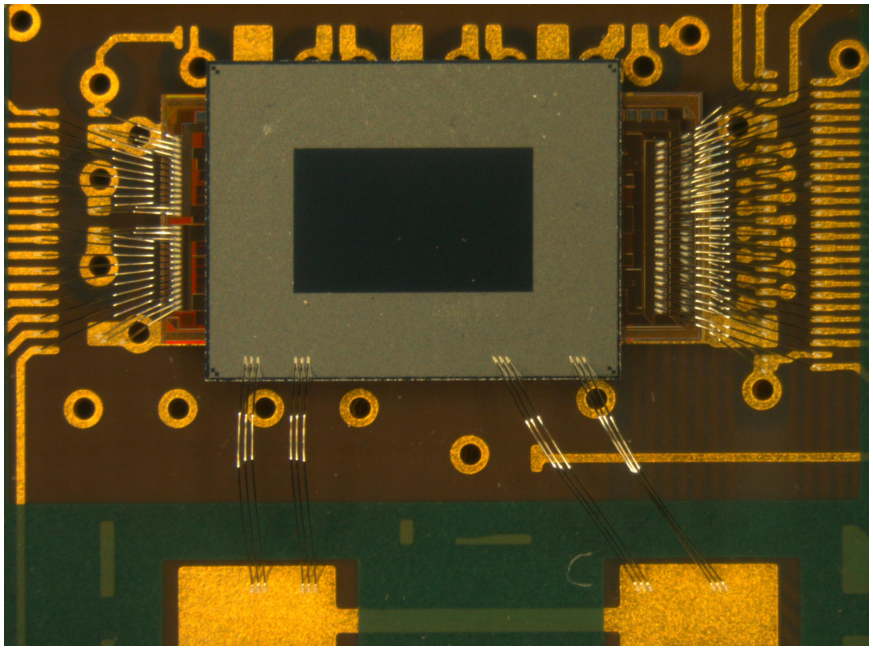
The Quarter Chip & Serialiser



Backup Slides

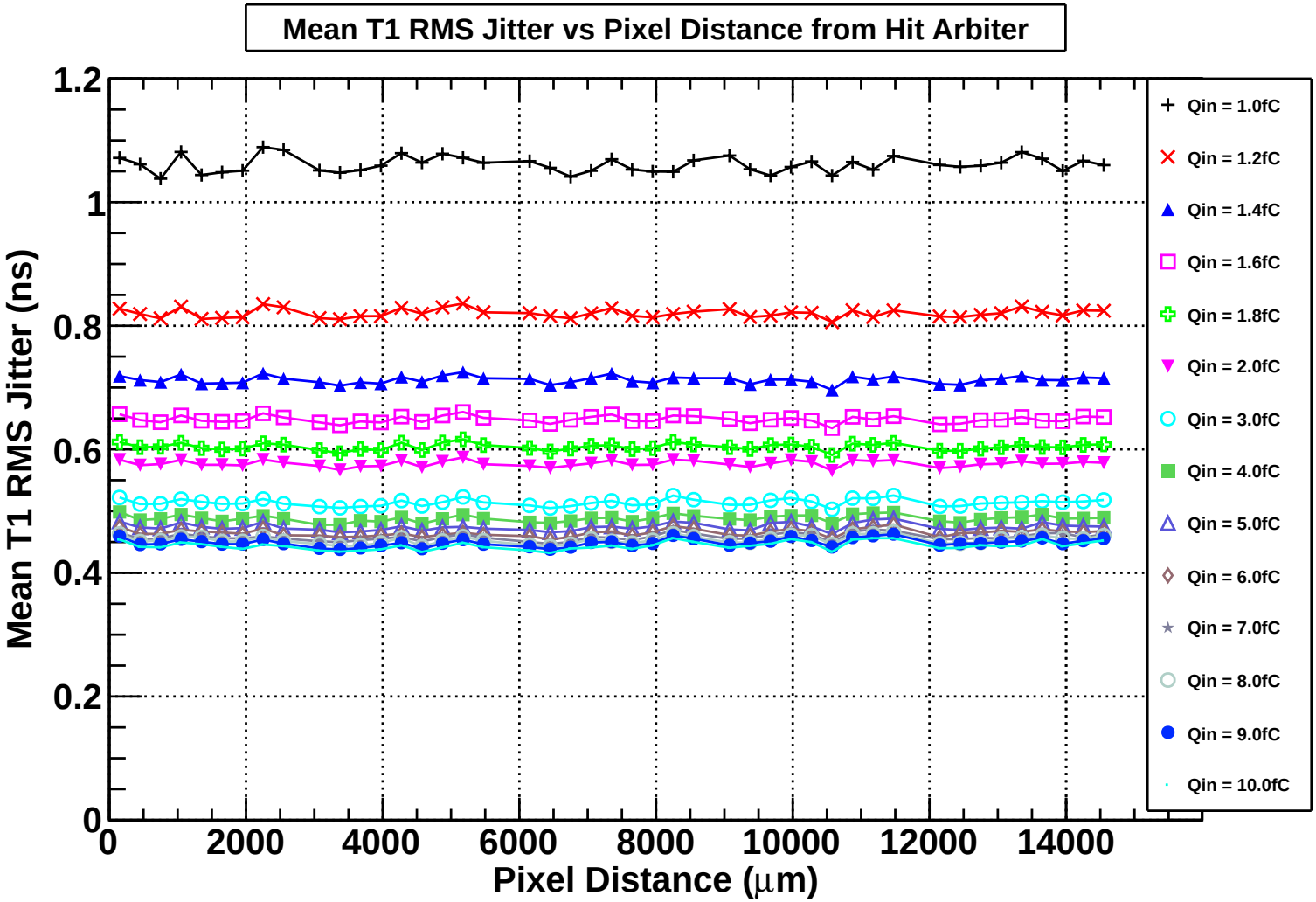
EoC Chip & Assembly





- What is the limit of the timing resolution attainable?
- Where does this limit come from?

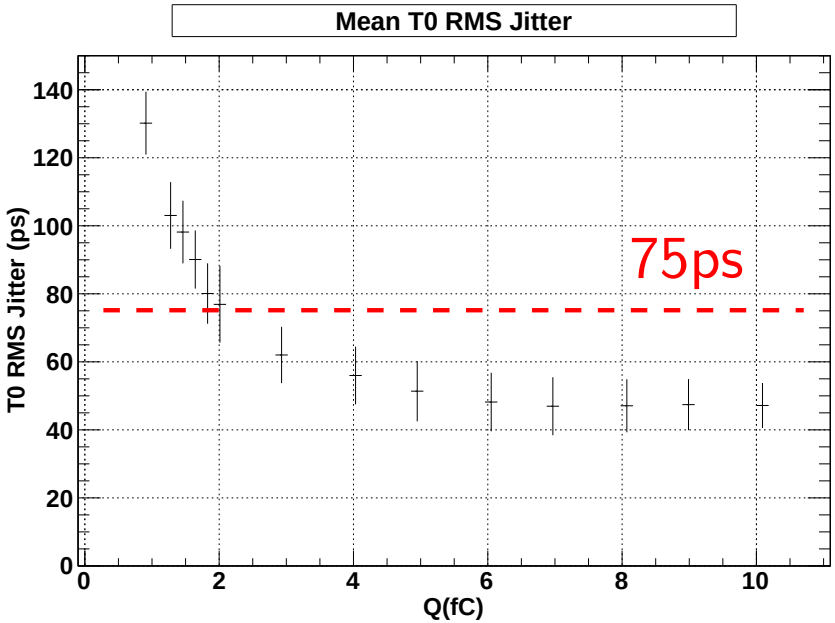
Transmission Line Uniformity T_1 RMS Jitter: ASIC



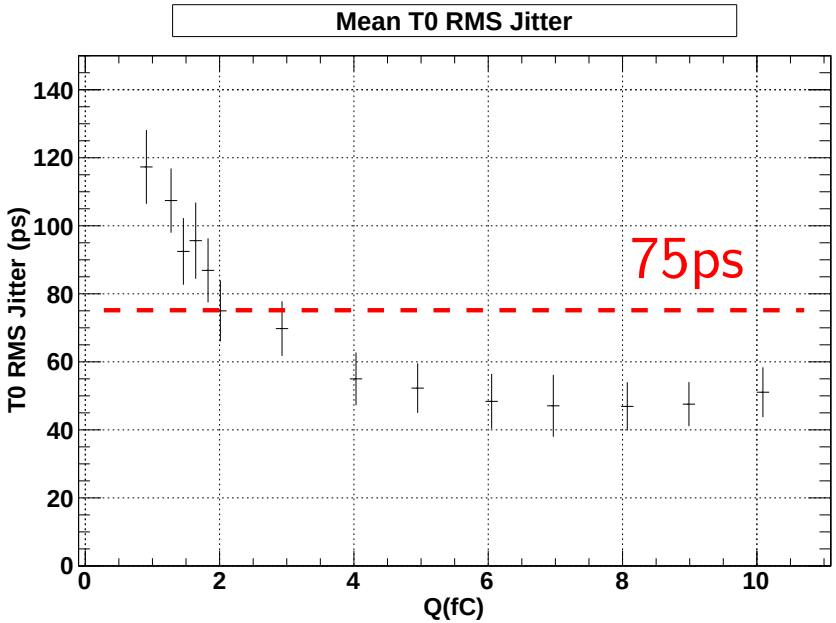
No systematic deterioration of signal quality with distance.

RMS T_0 Jitter Vs Q: Assembly (@ 300V) + Laser

Pixel 0: Far from EoC



Pixel 44: Close to EoC

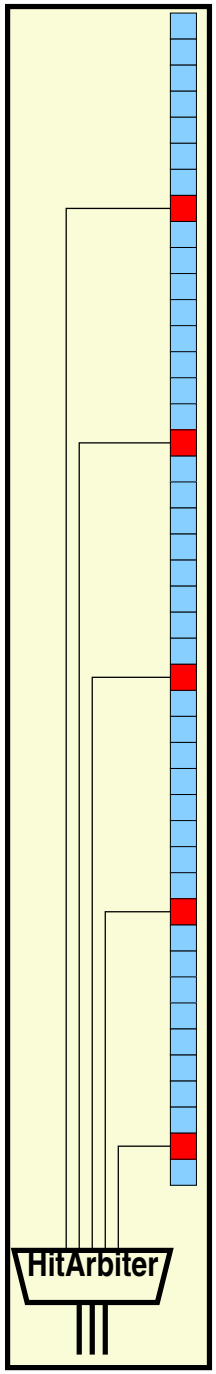


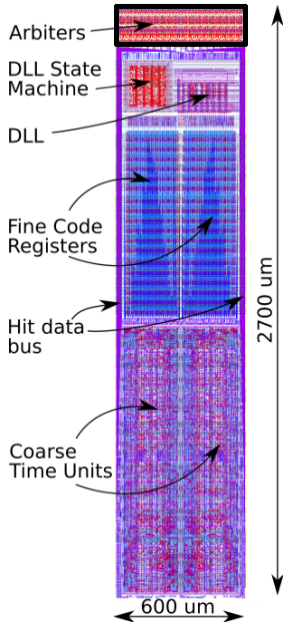
- Full event time reconstruction done
- EoC activity doesn't feed through to the pixels

- detector bias $= 300\,V$
- average case $\sim 75\,ps$ at $2.4\,fC$

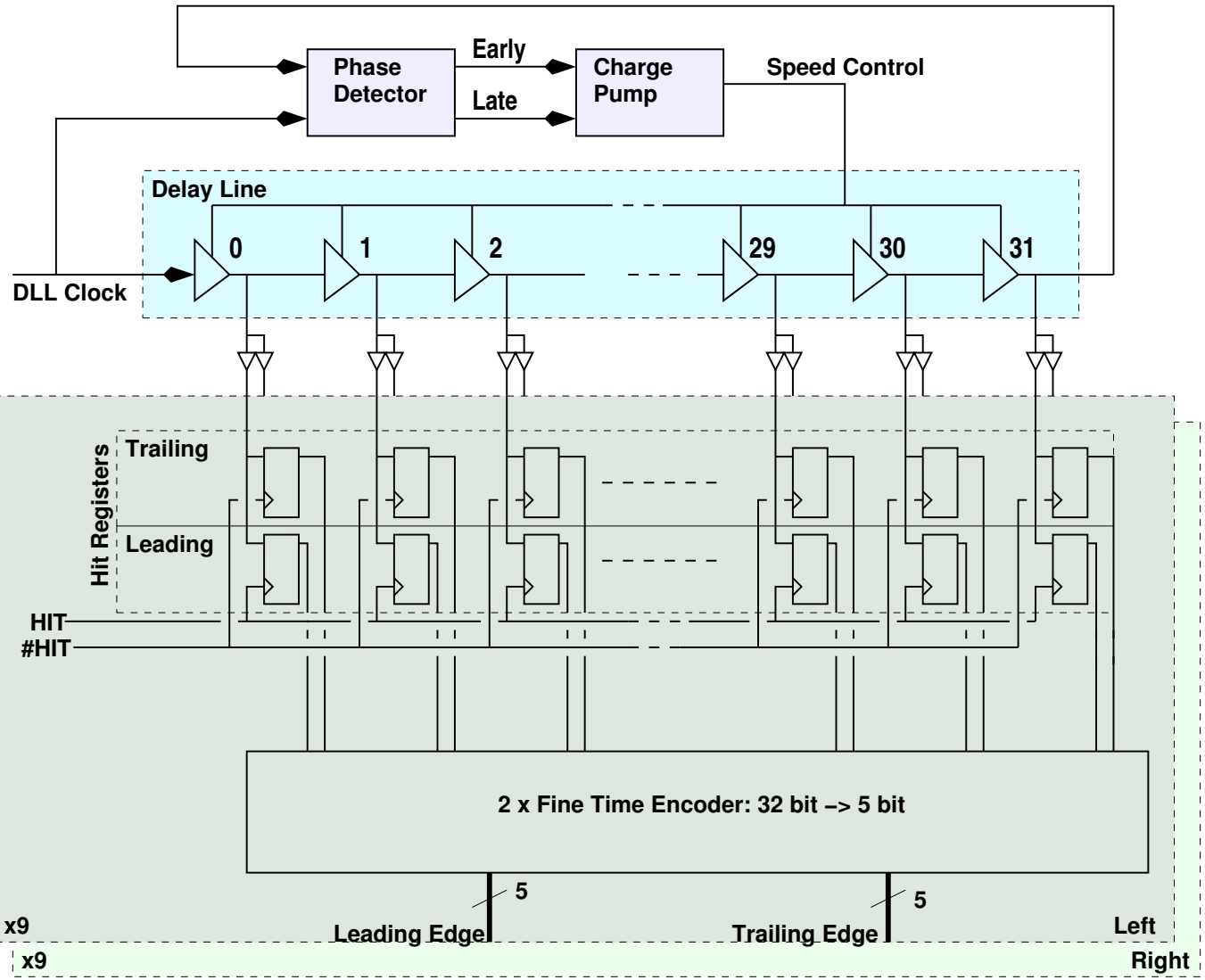
TDC: Hit Arbiter

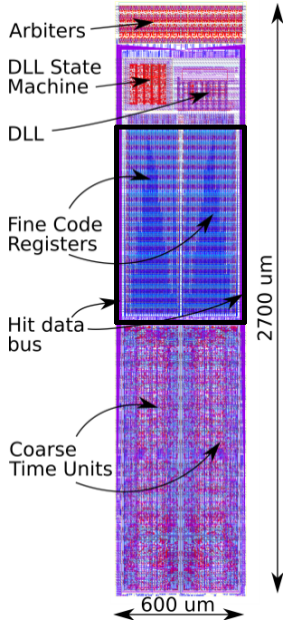
- fully asynchronous
  - timing information preserved
- 5 pixel + 1 test inputs
- hit signal
- 5 bit hit address + 5 bit pileup
- non-adjacent pixels connected to adjacent channels



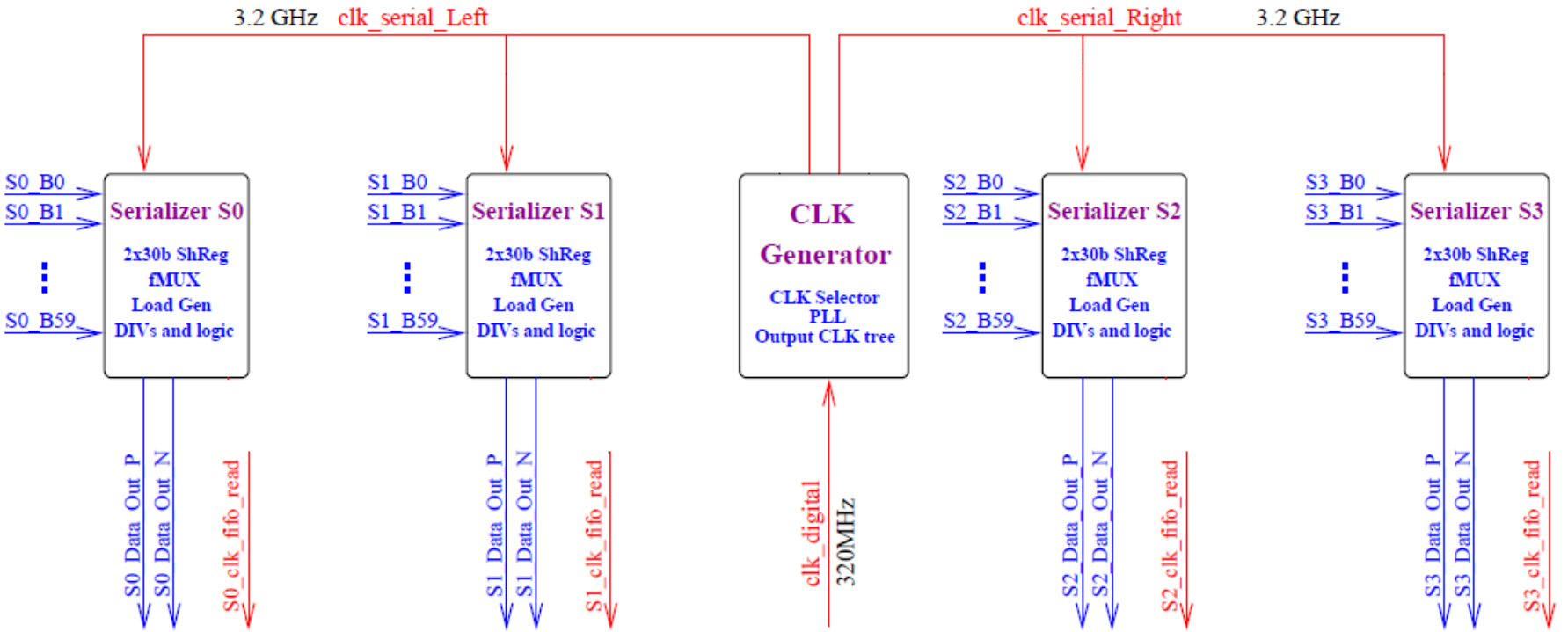


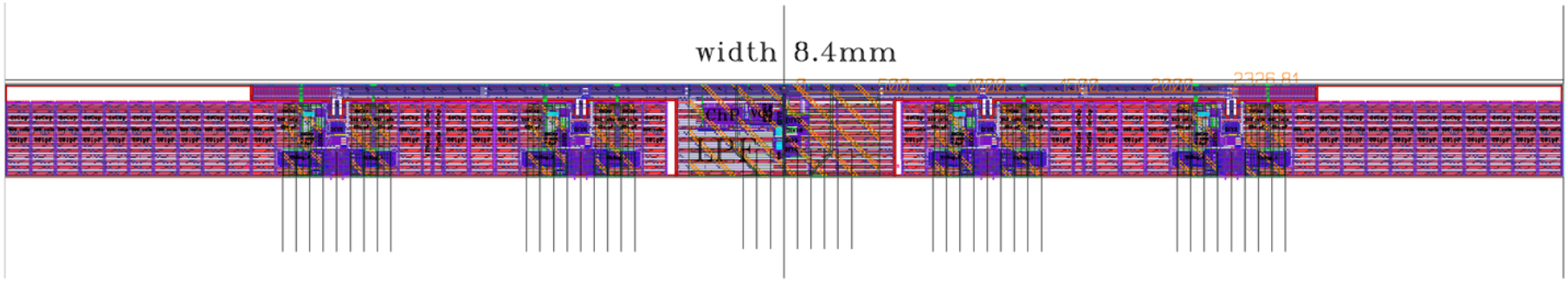
TDC: DLL & Fine Registers



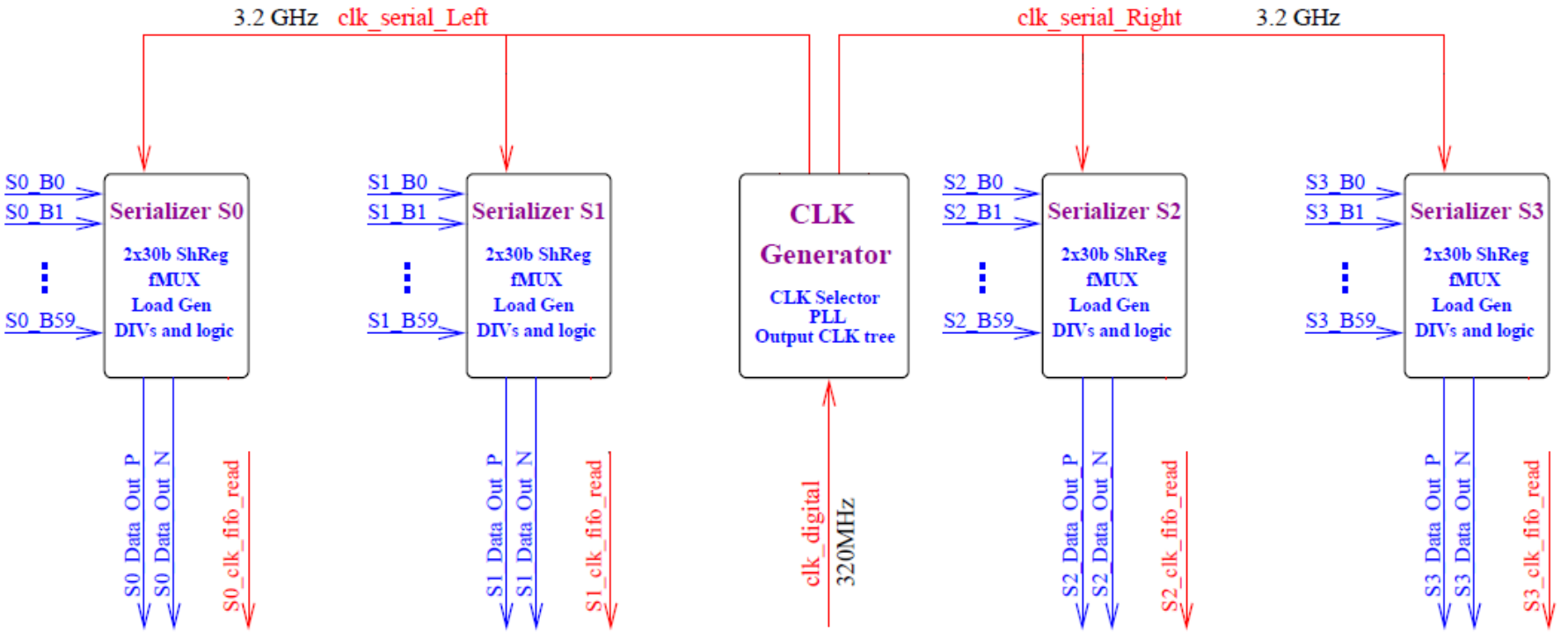


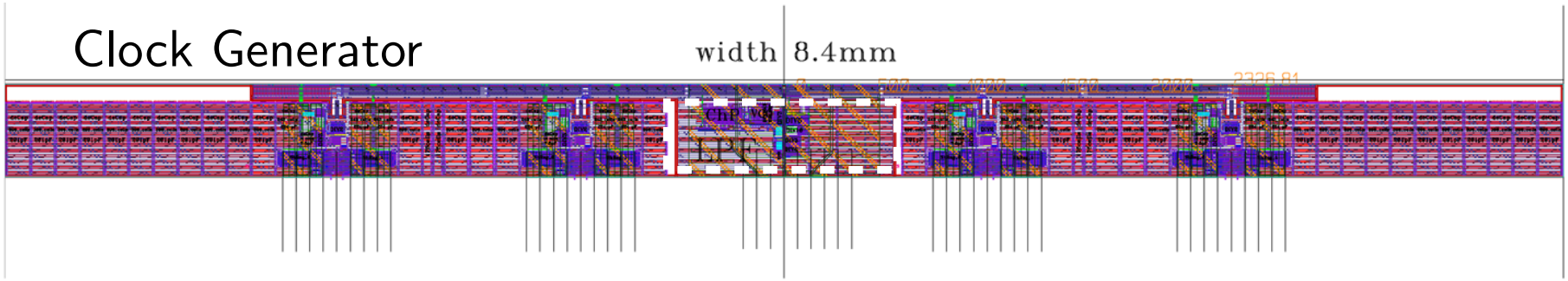
PLL and Serialisers



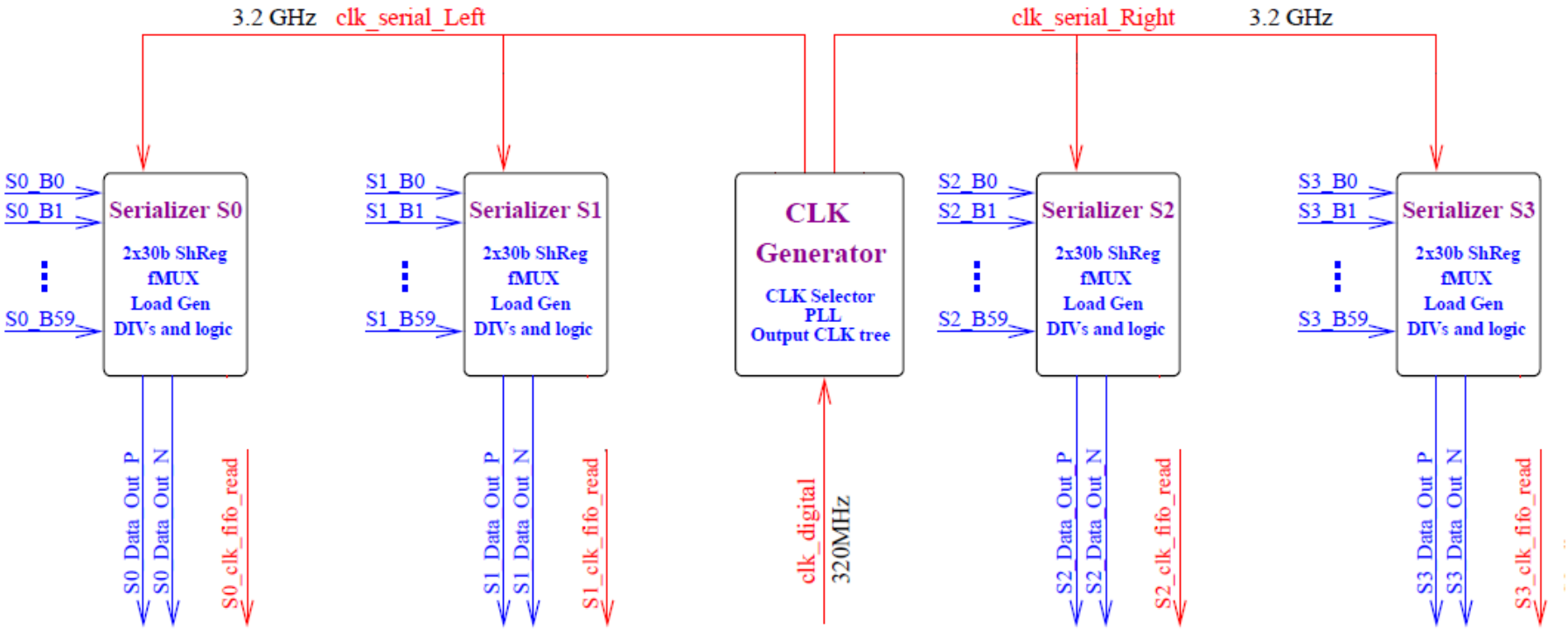


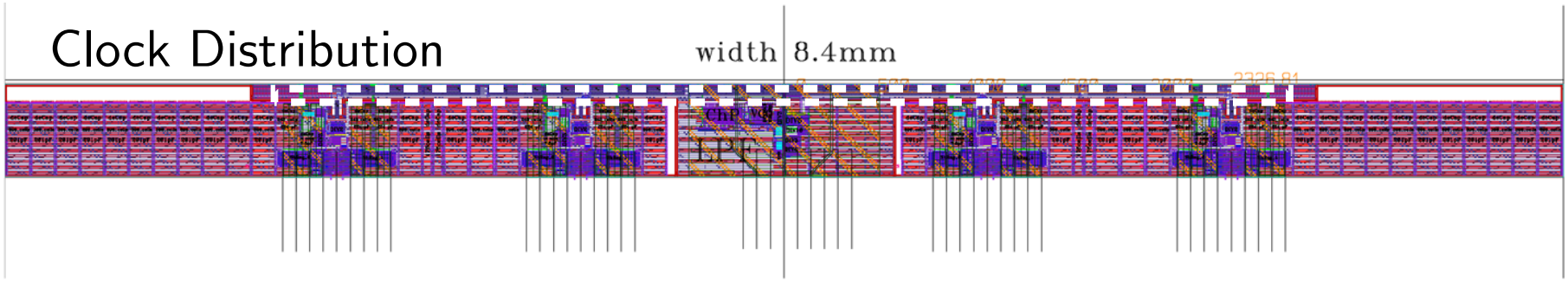
PLL and Serialisers



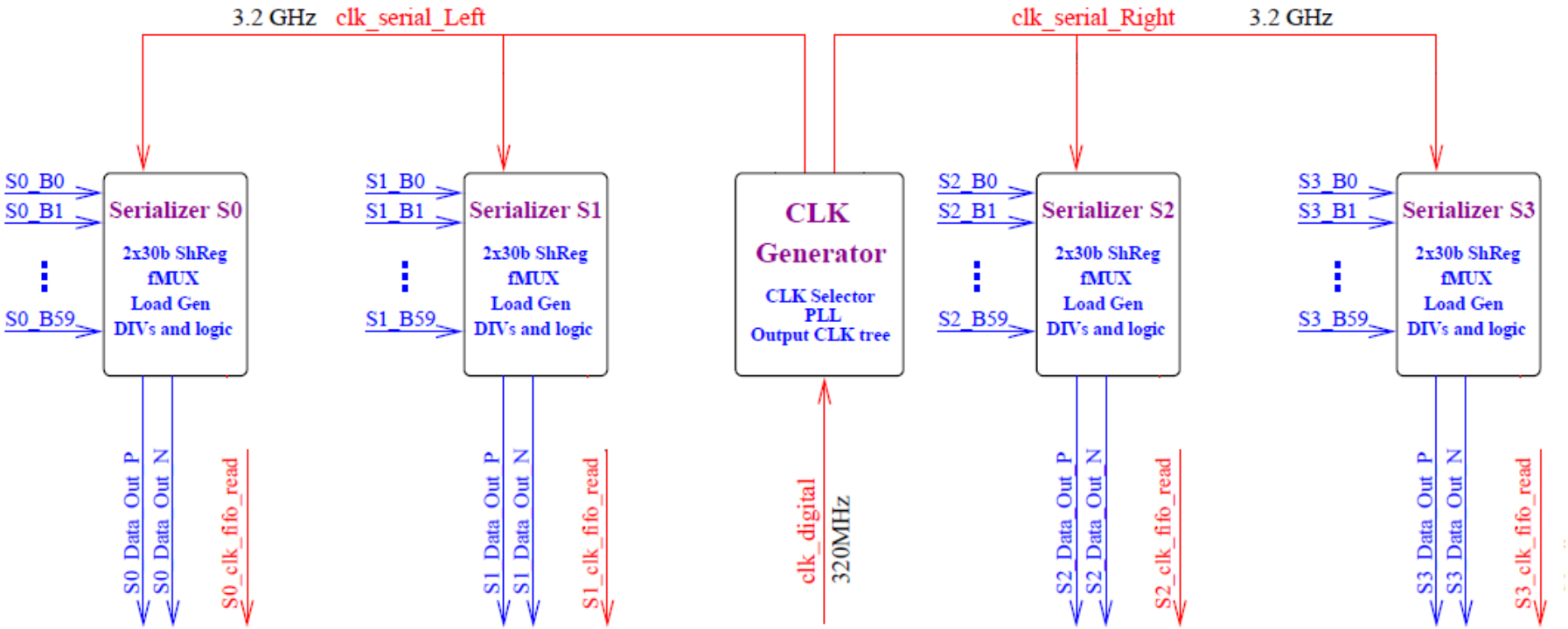


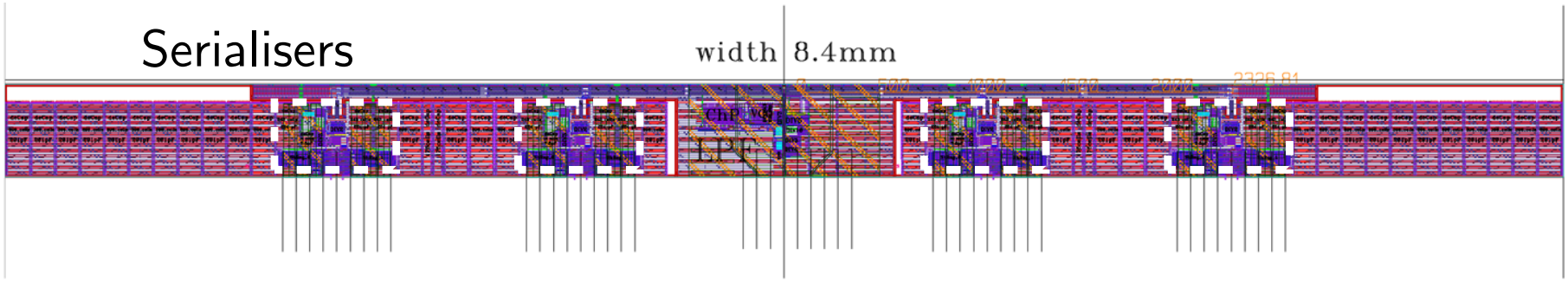
PLL and Serialisers



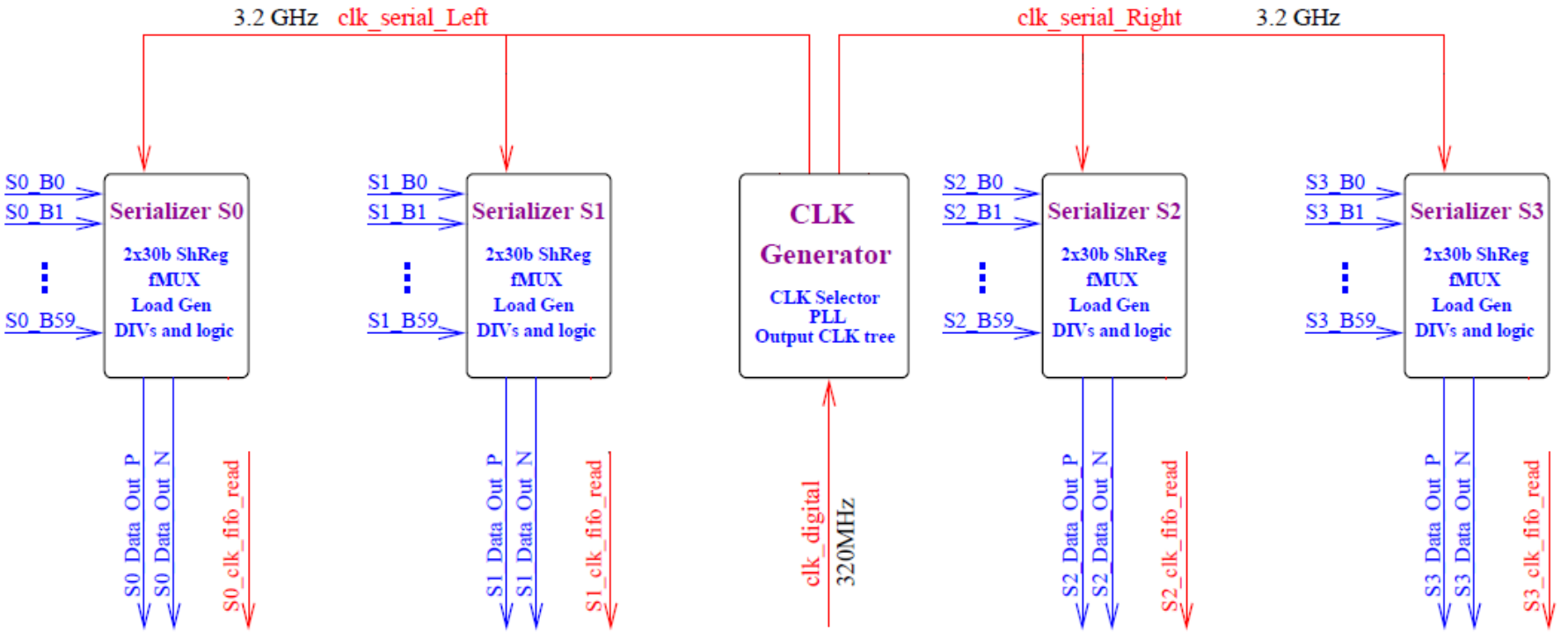


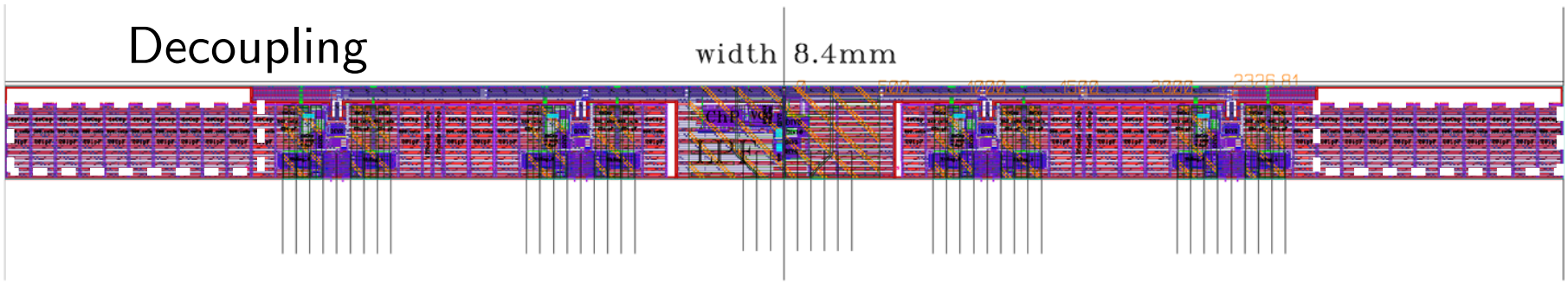
PLL and Serialisers



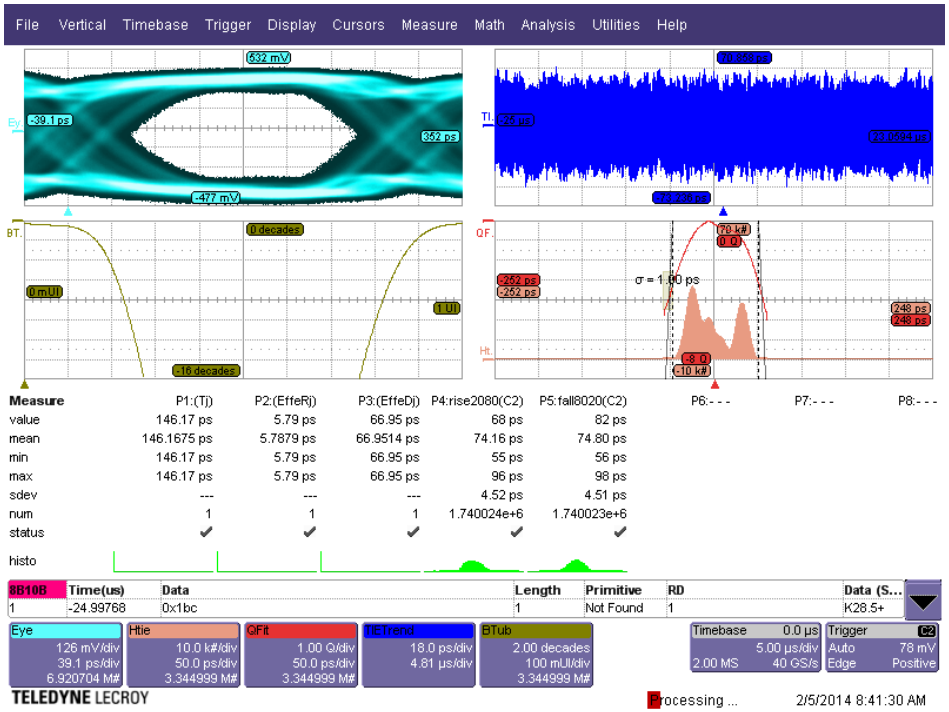


PLL and Serialisers





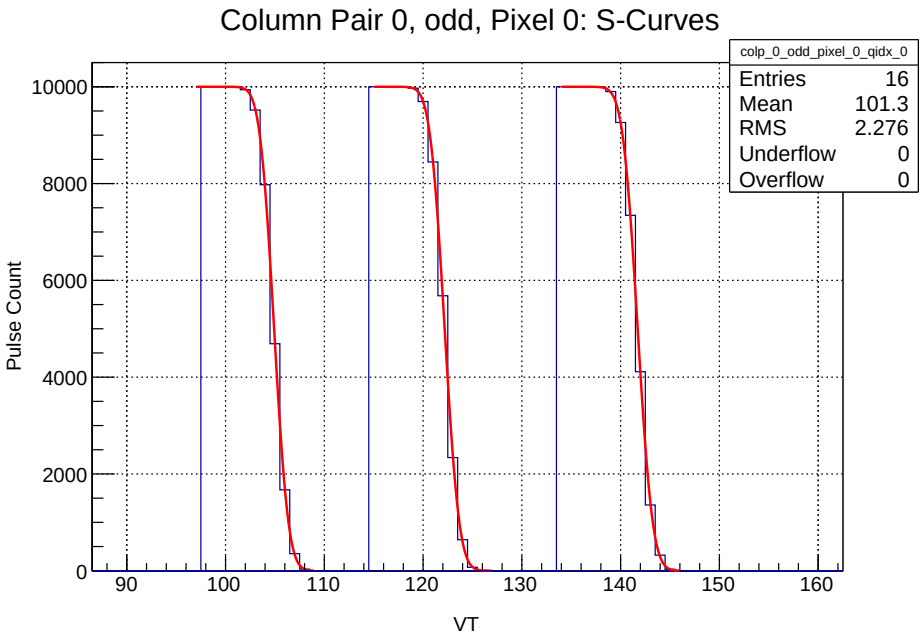
Serial Outputs at 3.2Gb/s

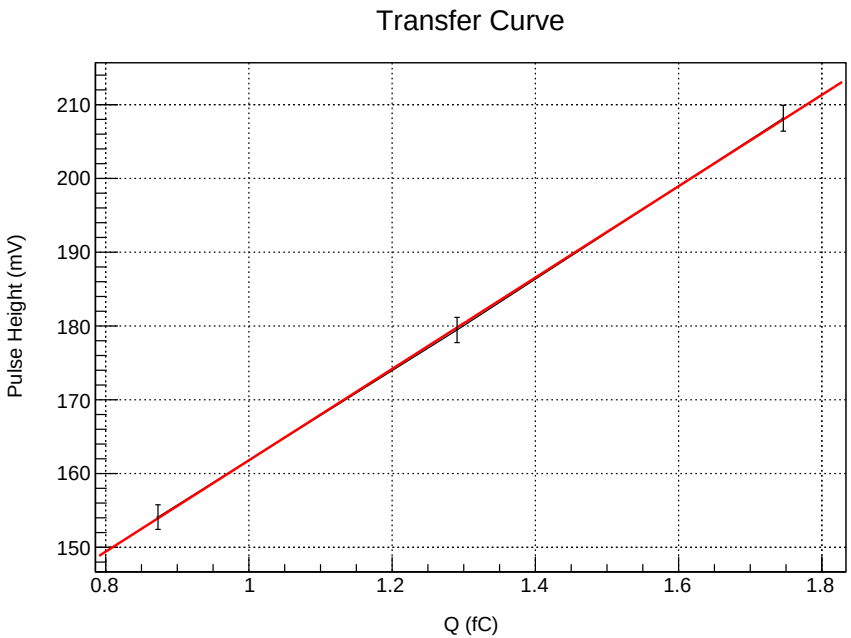


- Idle words correct
  - synchronisation works

- Total Jitter < 150 ps
- FPGA GTX recv. lock reliably
- DAQ works reliably

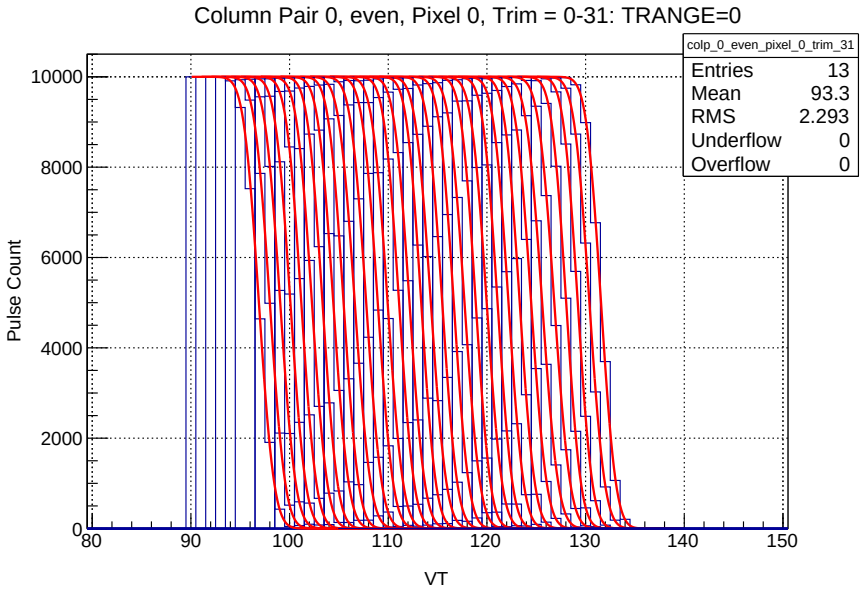
S-Curves → Pre-Amp Transfer Function

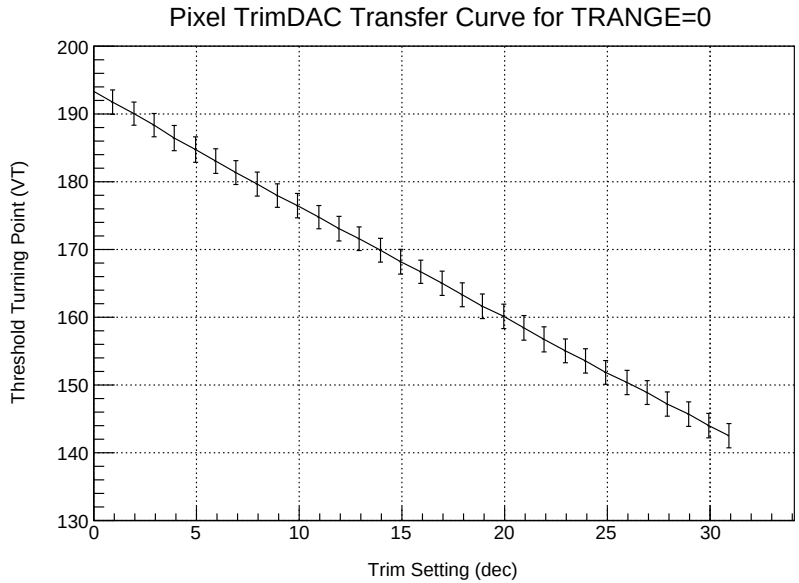


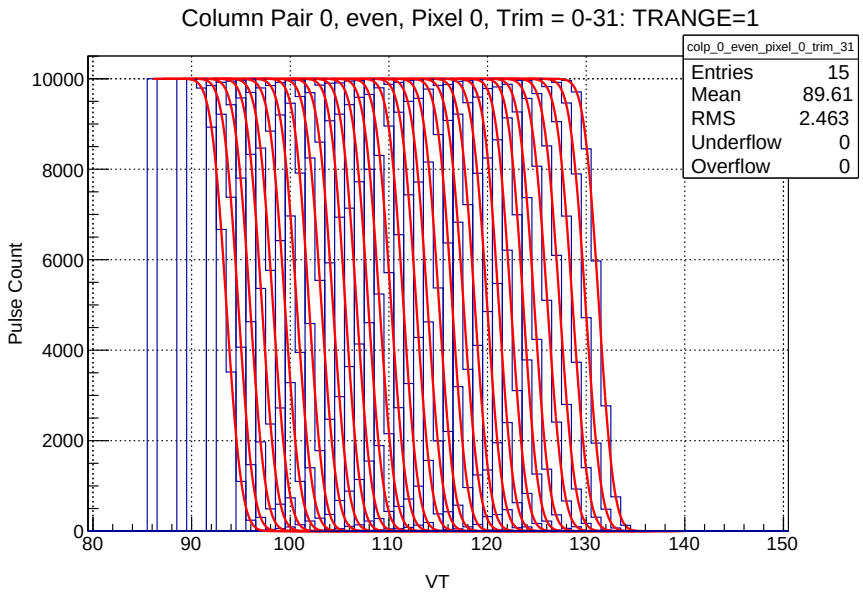


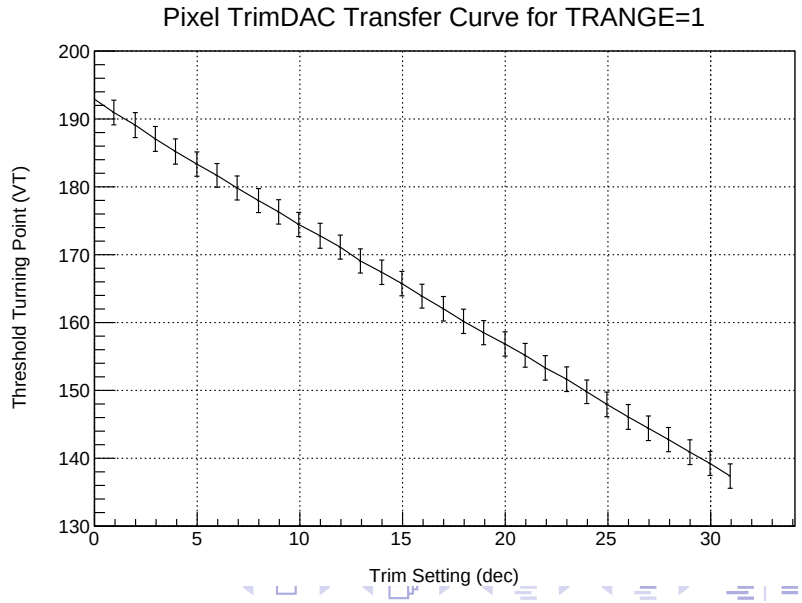
- $Q_{injected}$ adjusted for CAL DAC gain
- Transfer fit → discriminator offset and front end gain
- Polarity setup for a hole signal
  - P-on-N sensor (baseline)
  - "electron" polarity works too

Trim and TRANGE Functionality

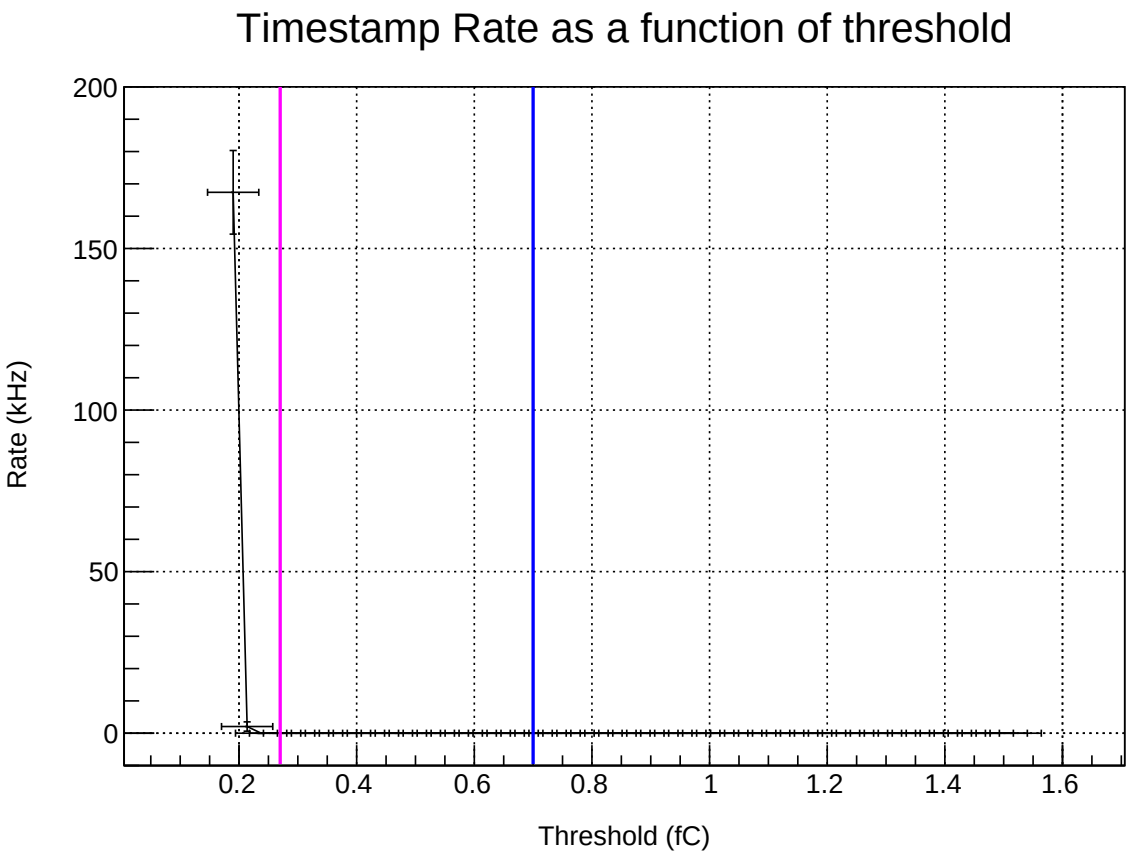








How low will the threshold go?



- All pixels enabled (& trimmed)
- Pink: minimum threshold $\sim 0.26\, fC$ ($1600e^-$)
- Blue: nomimal threshold $0.7\, fC$

Top Level Test Bench