The GigaTracKer: a silicon hybrid pixel detector with good timing resolution.

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EP-ESE-FE Group, CERN

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Introduction to NA62 and the GigaTracker

TDCPix Readout ASIC

Performance Studies

Summary
Introduction to NA62 and the GigaTracker

TDCPix Readout ASIC

Performance Studies

Summary
The NA62 Experiment

- Trajectory
  - momentum
  - angle

- Time
  - correlate hits with RICH
  - $\leq 200\text{ ps (RMS)}$ per station
The NA62 Experiment
GTK Station in the Beam Line

- in vacuum
- centred on the beam
- 0.8 → 1 GHz beam rate
The GTK Carrier Card
Introduction to NA62 and the GigaTracker

GigaTracker: Hybrid Pixel Detector

- non-uniform beam
- 6Mrad/year
- 0.5% $X_0$ per station
Sensor Parameters

- $V_{bias} \sim 300-600V$
- Charge release mechanism is stochastic
- Landau distribution
  - $Q_{MP} = 2.4 fC$
- 200 $\mu$m thick
  - (signal size vs $T_{collection}$)

![Diagram of sensor parameters]

![Graph showing sensor current pulse]
Simplified Pixel Architecture

- Gain $\sim 65 \text{mV}/fC$
- Peaking time $\sim 5 \text{ns}$
- ENC $< 250 \text{e}^-$
- Polarity control
- Pixel mask
- TX with pre-emphasis
Pre-Amplifier & Discriminator Signals

Threshold

Pre-Amp Output

Discriminator Output

Time Over Threshold

Peaking Time = 5 ns

Time Walk

"Leading" 

"Trailing"

T0

T1

T2

INPUT

OUTPUT

PRE-AMP

RF

CF

V_{\text{Threshold}}
Pre-Amplifier & Discriminator Signals

![Diagram showing pre-amplifier and discriminator signals with time over threshold, peaking time, and time walk indicated.]

- **Time Over Threshold (ToT)**
  - $T_0$
  - $T_1$ ("Leading")
  - $T_2$ ("Trailing")

- **Pre-Amp Output**
- **Discriminator Output**
- **Peaking Time = 5 ns**
- **Time Walk**
  - "Trailing"
  - "Leading"

- **Qin (fC)**
  - 2
  - 4
  - 6
  - 8
  - 10

- **Time (s)**
  - 32
  - 34
  - 36
  - 38
  - 40
  - 42
  - 44
  - 46
  - 48
  - 50
  - 52

- **$\times 10^{-9}$**

- **Graph showing $T_1$ and $T_2$ vs Qin, Trise=2.5ns**
  - $Q_{th}=0.5fC$
  - $Q_{th}=0.6fC$
  - $Q_{th}=0.7fC$
  - $Q_{th}=0.8fC$
  - $Q_{th}=0.9fC$
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TDCPix Readout ASIC

Performance Studies

Summary
TDCPix Architectural Overview

- 40 x 45 pixels
- 300x300 \( \mu m^2 \)
- asynchronous

- End-Of-Column per-pixel hit signal to EOC

- 360 dual TDC channels
- TDC Bin size \( \sim 97 \) ps
- self-triggered operation
- Rate: 210 MHzits/s
- 4 x 3.2 Gb/s serialisers

SEE Tolerant state/config.

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- 40 x 45 pixels
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TDCPix Readout ASIC

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- SEE Tolerant
  - state/config.
TDCPix Top Level

References

TDCPix Readout ASIC

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TDCPix Readout ASIC

TDCPix Top Level

PLL & Serialisers

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Single Chip Test Assemblies

Open backside

Closed backside
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Performance Studies

Summary
TimeWalk-Corrected ($T_0$) Time Resolution: Bare ASIC

Distribution of $T_0$ for all pixels

<table>
<thead>
<tr>
<th>t0_distribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Entries</td>
</tr>
<tr>
<td>Mean</td>
</tr>
<tr>
<td>RMS</td>
</tr>
<tr>
<td>Underflow</td>
</tr>
<tr>
<td>Overflow</td>
</tr>
</tbody>
</table>

“Whole Chip” Resolution $\sim$ 72 ps RMS
Time-Walk Corrected ($T_0$) Resolution: Laser Light (300V)

**Distribution of $T_0$ for all pixels**

- **$t_0$ distribution**
  - Entries: $3.6e+07$
  - Mean: $1.025e+06$
  - RMS: 71.35
  - Underflow: 0
  - Overflow: 0

**Laundau Weighted Sum of $T_0$ for all pixels.**

- **weighted_sum_pixel_8_0**
  - Entries: 2142607
  - Mean: $1.025e+06$
  - RMS: 81.86
  - Underflow: 0
  - Overflow: 0
Performance Studies

Time Resolution in the Experiment

- Test Beam
- Run 2014
- Run 2015

200ps

Bias [V]

- Single Pixel: GTK = 155ps (no KTAG)

 residuals GTK1: 173 ps

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Time Resolution Limits: 1060nm Laser ($7 \mu m$ spot)

- induced current pulse on electrode changes shape
  - pre-amp output changes shape
  - adds $\sim 85$ps
- uncorrectable contributions for current sensor

Sensor current pulses

- pixel center
- pixel edge

T0 vs Y for all X with HV = 300V and 4fC
Weightfield2/Spectre Processing Flow

Performance Studies

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6th June 2016 18 / 23
Weighting Field Simulation

- Calibration curve at $X=0\mu m$
- $2.4 \, fC$ (uniform) stepped to edge (145\,\mu m)
- $T_0$ reconstructed
Charge Straggling

- Calibration curve at $X=0\mu m$
- $Q_{MP} = 2.4 fC$, Landau fluctuation
- “pixel” centre
- $\sigma_{T0} \sim 100\,ps$
Time Resolution: Summary of Contributions

\[ \text{Time Resolution} = \sqrt{\sigma_{\text{electronics}}^2 + \sigma_{\text{WeightingField}}^2 + \sigma_{\text{straggling}}^2} \]

\[ = \sqrt{80^2 + 85^2 + 100^2} \sim 150 \text{ ps} \]
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Performance Studies

Summary
Summary

- **NA62**
  - Ultra rare decay: $K^+ \rightarrow \pi^+ \nu \nu$
  - Fixed target experiment at SPS, 250m long

- **GTK**
  - 3 plane hybrid pixel detector
  - extremely challenging design constraints
  - Material Budget: <0.5% $X_0$ per station
  - time resolution < 200 ps per plane
  - TDCPix readout ASIC designed at CERN

- **Performance**
  - TDCPix $\sim 75$ ps RMS
  - Laser light $\sim 80$ ps RMS (@300V)
  - Beam Particles $\sim 155$ ps RMS for single pixel (@300V)
  - Time resolution differences partially (mostly?) understood
  - Weightfield2 (1-D)/Spectre simulation: $\sim 150$ ps RMS
  - Beam test with high spatial resolution telescope
Thanks for your attention!!
Backup Slides.
Post TID Time Resolution: bare chip

- **Pixel Matrix**: up to 6 Mrad
- **EOC**: up to 900 krad
- **Calibration**:
  - 0.9-7.5 fC (fine grained to $\sim$3 fC)
  - $10^4$ hits/point
  - spline used for “continuous” correction
- **Measurement**:
  - 1.0-7.5 fC
  - ana doesn’t “know” which charge it’s correcting
- **$T_0$** contains all pixels and all measurement charges
- no Landau weighting
- C.f. $\sim$75 ps for un-irradiated case
Pixel Layout:

300x300\mu m^2 cell
Pixel Layout: Signal Path
Pixel Layout: Trimming & Configuration
Pixel Layout: Noise Mitigation

- Triple well (input transistor)
- BFMOAT substrate isolation
- Signal shielding
- Power supply decoupling
Backup Slides
TDC: Schematic and Layout

Even Column

45 inputs from pixel column

DLL Control
Finite State Machine

Hit Generator

Fine time
32 : 5 encoder

Coarse

Hit Builder

Pixel Group FIFO

Column FIFO

Odd Column

45 inputs from pixel column

45:9 Hit Arbitration

DLL

Hit Generator

Fine time
32 : 5 encoder

Coarse

Hit Builder

Pixel Group FIFO

Column FIFO

Arbiters
DLL State Machine

Fine Code Registers

Hit data bus

Coarse Time Units

600 microns

600 microns

2700 um

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TDC: Schematic and Layout

- Backup Slides

- Even Column
  - 45:9 Hit Arbitration
  - DLL Control
    - Finite State Machine
  - Hit Generator
    - Fine time
    - 32:5 encoder
  - Coarse
  - Hit Builder
  - Pixel Group FIFO
  - Column FIFO

- Odd Column
  - 45 inputs from pixel column
  - 45:9 Hit Arbitration
  - DLL State Machine
  - DLL
  - Fine Code Registers
  - Hit data bus
  - Coarse Time Units

- 600 microns
- 2700 um

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Backup Slides

The Quarter Chip & Serialiser

Data from 10 Column FIFOs

10:1 Data Mux

Quarter Chip FIFO

Data from 10 Column FIFOs

4 bits 42 bits

8b10b Encoder

30b shift register

Frame Generator
Coarse Count Rollover:
6.4 microseconds

Link Idle
Comma Insertion

Send Control

Send Control

CLKSER
CLKSER#

3.2 Gb/s

30b shift register
30b shift register

Address

Addr

48 bits

48 bits

48 bits

48 bits

48 bits

48 bits

48 bits

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Backup Slides
EoC Chip & Assembly

- What is the limit of the timing resolution attainable?
- Where does this limit come from?
Transmission Line Uniformity $T_1$ RMS Jitter: ASIC

Mean T1 RMS Jitter vs Pixel Distance from Hit Arbiter

No systematic deterioration of signal quality with distance.
RMS $T_0$ Jitter Vs Q: Assembly (@ 300V) + Laser

Pixel 0: Far from EoC

- Full event time reconstruction done
- EoC activity doesn’t feed through to the pixels

Pixel 44: Close to EoC

- detector bias = 300 V
- average case $\sim 75$ ps at 2.4 $fC$
TDC: Hit Arbiter

- fully asynchronous
  - timing information preserved
- 5 pixel + 1 test inputs
- hit signal
- 5 bit hit address + 5 bit pileup
- non-adjacent pixels connected to adjacent channels
TDC: DLL & Fine Registers

- Phase Detector
- Charge Pump
- Speed Control
- DLL Clock
- Delay Line
- Early
- Late
- DLL & Hit Registers
- 0 1 2 29 30 31
- Early
- Late
- Leading
- Trailing
- Hit Registers
- Leading
- Trailing
- HIT
- #HIT
- 2 x Fine Time Encoder: 32 bit -> 5 bit
- 5
- Leading Edge
- Trailing Edge
- Left
- Right

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PLL and Serialisers

3.2 GHz clk_serial_Left

S0_B0
S0_B1

Serializer S0
2x30b ShReg MUX
Load Gen DIVs and logic

S0_B59

S1_B0
S1_B1

Serializer S1
2x30b ShReg MUX
Load Gen DIVs and logic

S1_B59

CLK Generator
CLK Selector PLL
Output CLK tree

clk_digital
320MHz

S2_B0
S2_B1

Serializer S2
2x30b ShReg MUX
Load Gen DIVs and logic

S2_B59

S3_B0
S3_B1

Serializer S3
2x30b ShReg MUX
Load Gen DIVs and logic

S3_B59

clk_serial_Right
3.2 GHz

S0 Data Out, P
S0 Data Out, N

S1 Data Out, P
S1 Data Out, N

S1 clk, fifo_read

S2 Data Out, P
S2 Data Out, N

S2 clk, fifo_read

S3 Data Out, P
S3 Data Out, N

S3 clk, fifo_read

width 8.4mm
PLL and Serialisers

Clock Generator width 8.4mm
PLL and Serialisers

Clock Distribution

width 8.4mm
PLL and Serialisers

Serialiser S0
- 2x30b ShReg MUX
- Load Gen DIVs and logic
- S0 B0, S0 B1, S0 B59
- S0 Data Out P, S0 Data Out N
- S0clkfifo_read

Serialiser S1
- 2x30b ShReg MUX
- Load Gen DIVs and logic
- S1 B0, S1 B1, S1 B59
- S1 Data Out P, S1 Data Out N
- S1 clk_fifo_read

CLK Generator
- CLK Selector PLL
- Output CLK tree
- S2 B0, S2 B1, S2 B59
- S2 Data Out P, S2 Data Out N
- S2 clk_fifo_read

Serialiser S2
- 2x30b ShReg MUX
- Load Gen DIVs and logic
- S3 B0, S3 B1, S3 B59
- S3 Data Out P, S3 Data Out N
- S3 clk_fifo_read

Serialiser S3
- 2x30b ShReg MUX
- Load Gen DIVs and logic
- S3 B0, S3 B1, S3 B59
- S3 Data Out P, S3 Data Out N
- S3 clk_fifo_read

Serialisers width 8.4mm
PLL and Serialisers

Decoupling width 8.4mm
Serial Outputs at 3.2Gb/s

- Idle words correct
- Synchronisation works
- Total Jitter < 150 ps
- FPGA GTX recv. lock reliably
- DAQ works reliably
S-Curves → Pre-Amp Transfer Function

- $Q_{injected}$ adjusted for CAL DAC gain
- Transfer fit → discriminator offset and front end gain
- Polarity setup for a hole signal
  - P-on-N sensor (baseline)
  - “electron” polarity works too
Trim and TRANGE Functionality

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How low will the threshold go?

- All pixels enabled (& trimmed)
- Pink: minimum threshold $\sim 0.26\ fC\ (1600e^-)$
- Blue: nominal threshold $0.7\ fC$
Top Level Test Bench

Test Sequences
- TestA
- TestB
- TestC
- TestB
- TestB

Test Library

Log

Test Library

Within ncsim executable

"Within" the simulator

RSTGEN
CLKGEN

DAQ Proc.

CMD Server

Readout Bus Functional Model

Bus Functional Model

"Back Door" Access

TDCPix Top Level

8b10b SERDES

Server

CMD

IPC

FIFO UP

FIFO DOWN