28th RD50 Workshop (Torino)



Contribution ID: 26 Type: not specified

TCT studies on AMS H35 CMOS devices for application in the ATLAS tracker upgrade

Monday, 6 June 2016 12:30 (20 minutes)

H35Demo chips are High-Voltage CMOS (HV-CMOS) devices produced in the 350nm AMS technology (H35) on wafers with four different substrate resistivity, the standard one of 20 Ω ·cm and 80, 200 and 1000 Ω ·cm. The aim of this HV-CMOS production is to study the radiation hardness of such detectors and investigate the possibility to introduce this technology in the next ATLAS tracker upgrade for the high luminosity LHC.

Having the same sensor production on several resistivities will show whether resistivity higher than the standard one for HV-CMOS would bring a beneficial effect in terms of depletion depth and charge collection efficiency.

Each chip includes four different pixel matrices. Two of them are designed to be interconnected to readout chips only, whilst the other two are completely monolithic.

In addition to the pixel matrices the chips include three test structures to characterize the sensor properties. The characterisation of test structures with different substrate resistivity has been carried out at IFAE using the Transient Current Technique (TCT). The test structure taken under examination consists of a single diode with eight neighbours that do not include additional electronics allowing to directly sample the signal waveform. The results of TCT and edge-TCT studies on samples from all the available substrate resistivities will be shown.

Summary

TCT and edge-TCT on H35Demo chip test structure

Primary author: Mr CAVALLARO, Emanuele (IFAE)

Presenter: Mr CAVALLARO, Emanuele (IFAE)

Session Classification: Simulation and HV CMOS