



The status and the perspectives of the silicon 3D and 4D pixel detectors

Part 2

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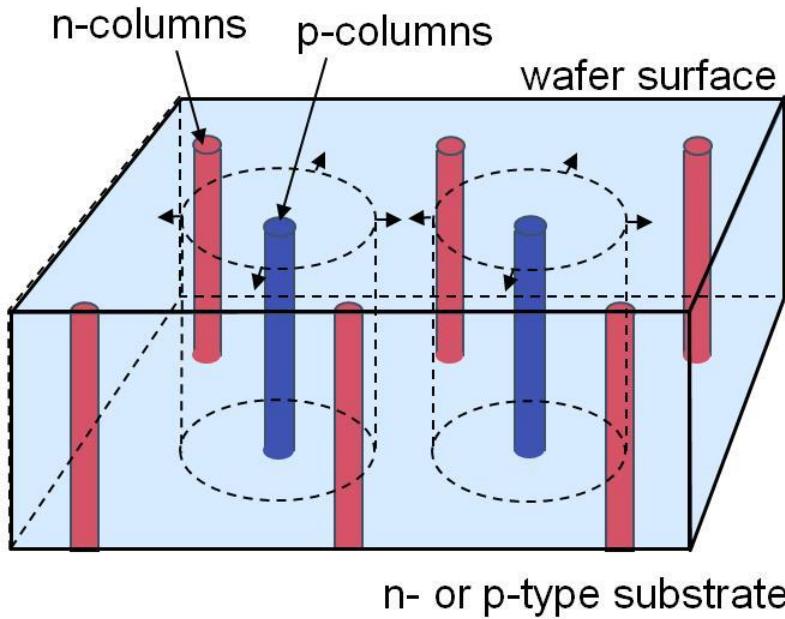
V Seminario Nazionale Sensori Innovativi (SNRI2016)
Padova, 24-28 ottobre 2016



Outline

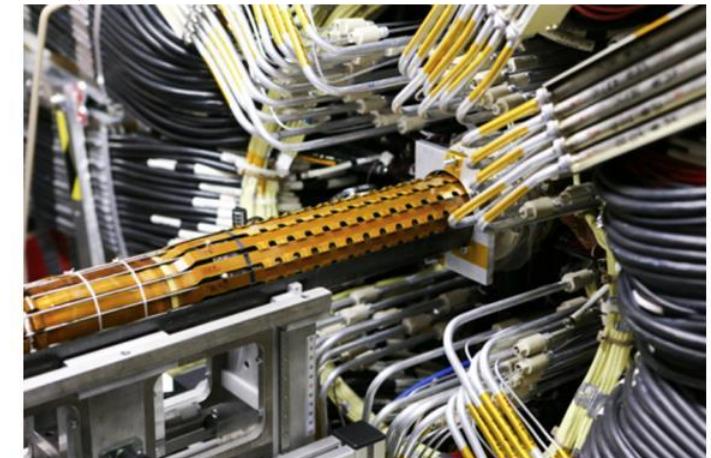
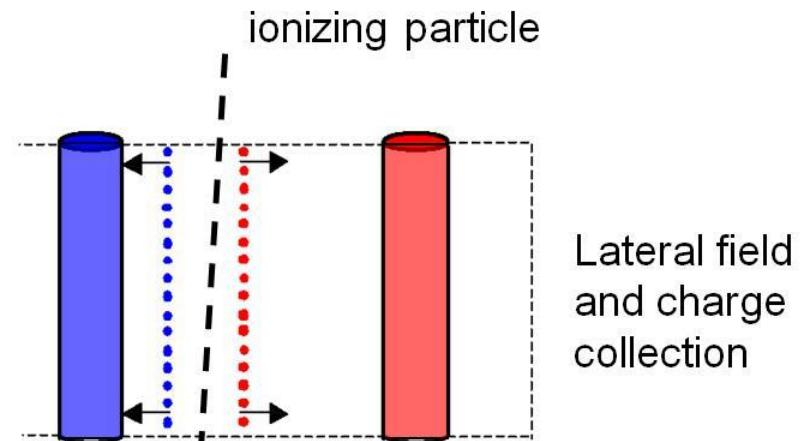
- Introduction
- APiX: Geiger-mode avalanche pixel detectors
for ionizing particles
- Low Gain Avalanche Detectors
- 3D detectors
- PixFEL: a pixelated detector for application at
future XFEL facilities

3D sensors



n- or p-type substrate

S. Parker et al. NIMA395 (1997)



- Distance between *n* and *p* electrodes can be made short ($\sim 50 \mu\text{m}$)
 **extremely radiation hard detector**
- First HEP application:
the ATLAS Insertable B-Layer (IBL)

C. Da Via et. al. NIMA 694 (2012), 321

Signal efficiency and inter-electrode spacing

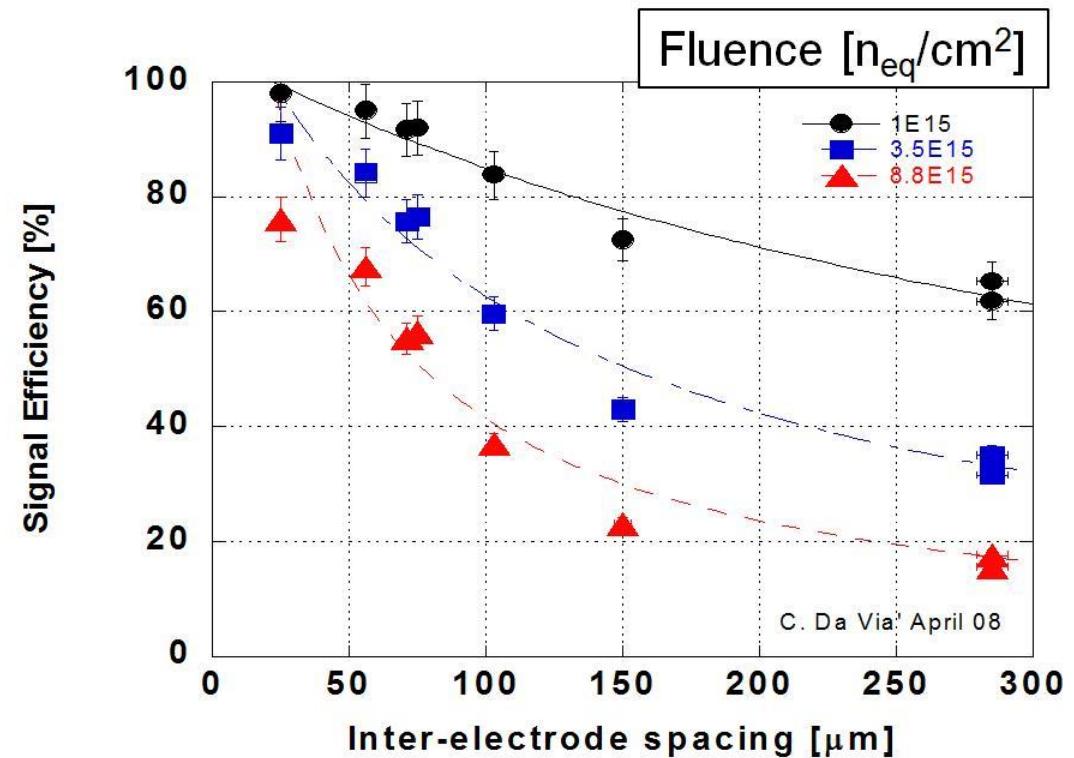
Radiation damage:
Trap states are generated

Electrons and holes
captured by trap states
are not collected

Low inter-electrode
spacing:



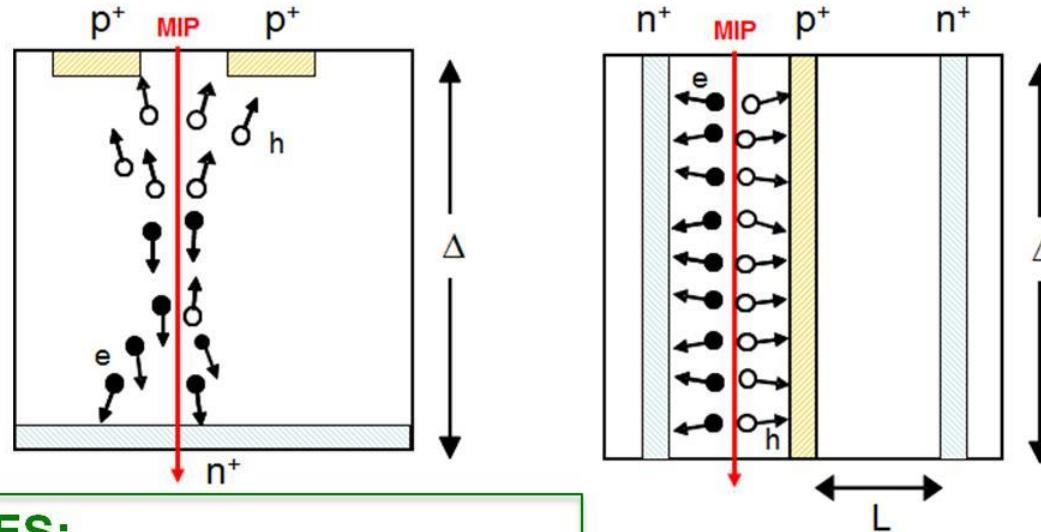
Higher collection efficiency



C. Da Via, NIMA 603 (2009) 319

3D vs planar

Electrode distance (L) and active substrate thickness (Δ) are decoupled $\rightarrow L \ll \Delta$ by layout



3D ADVANTAGES:

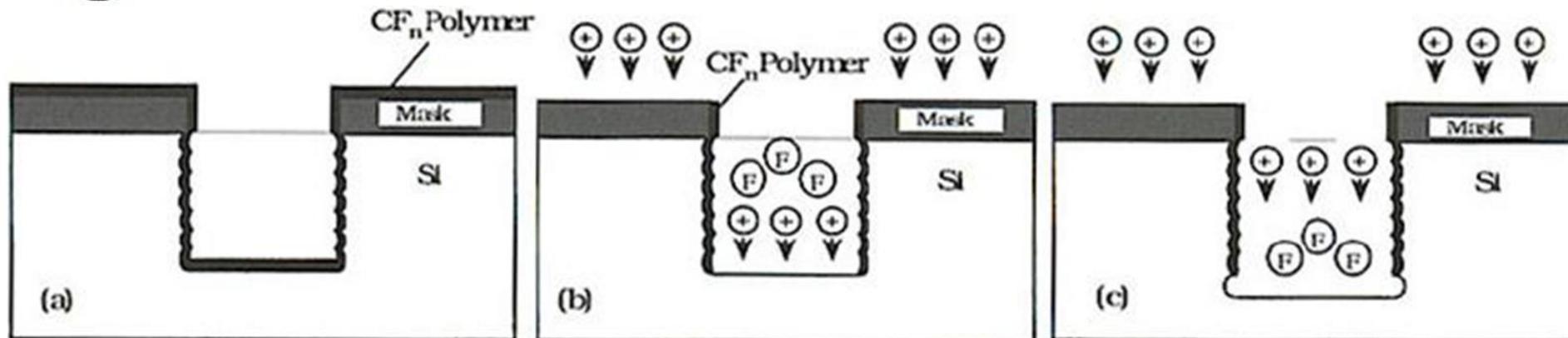
- Low depletion voltage (low power diss.)
- Short charge collection distance:
 - Fast response time
 - Less trapping probability after irr.
- Lateral drift \rightarrow cell “shielding” effect:
 - Lower charge sharing
 - Low sensitivity to magnetic field
- **Active edges**

→ **HIGH RADIATION HARDNESS**

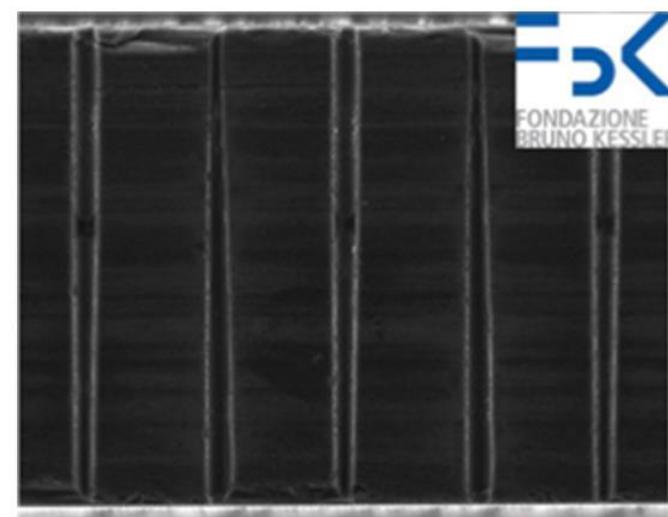
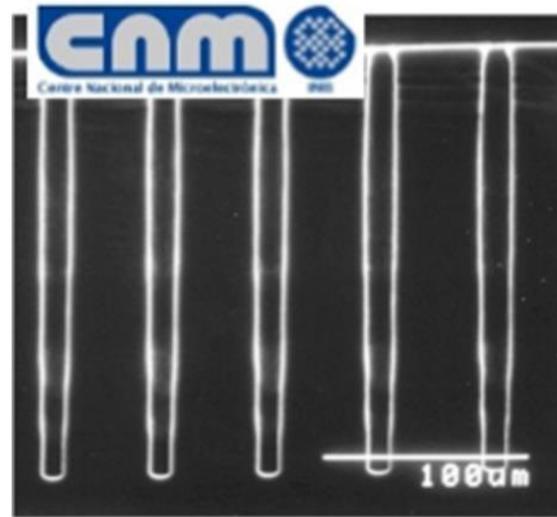
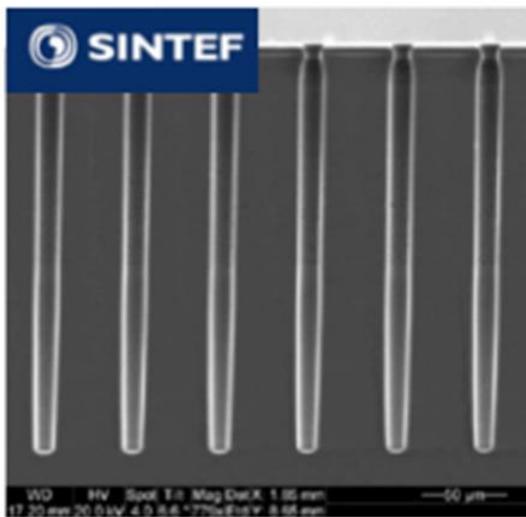
DISADVANTAGES:

- Non uniform spatial response (electrodes and low field regions)
- Higher capacitance with respect to planar ($\sim 3\text{-}5x$ for $\sim 200\text{ }\mu\text{m}$ thickness)
- **Complicated technology (cost, yield)**

Key technology: DRIE by the Bosch process

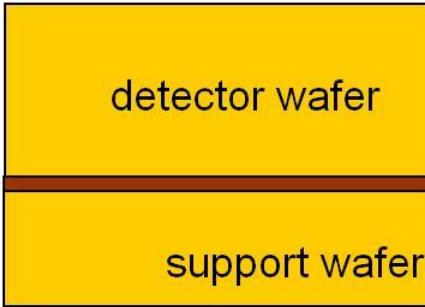


- Alternating etch cycles (SF_6) and passivation cycles (C_4F_8)
- High aspect ratio (~20:1 or better for trenches) and good uniformity

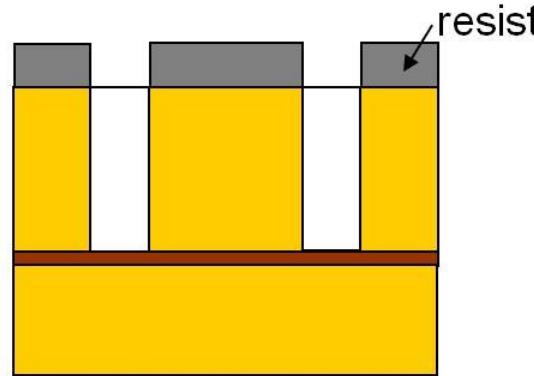


Full 3D with active edge

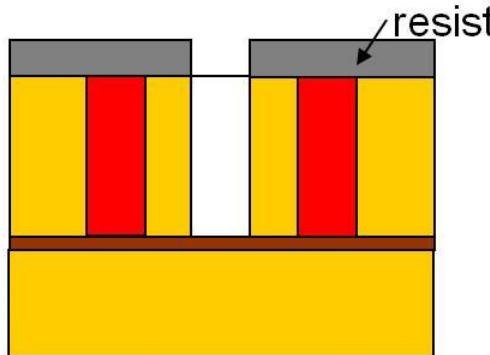
C. Kenney et al., IEEE TNS, vol. 46, n. 4 (1999) 1224
 T.E. Hansen et al., JINST 4 (2009) P03010



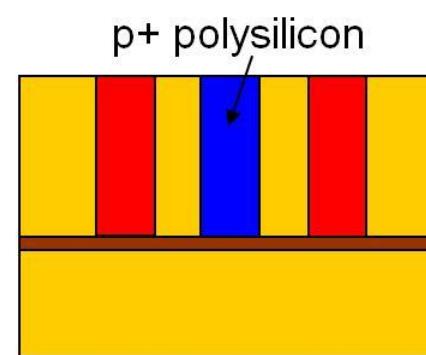
1) wafer bonding



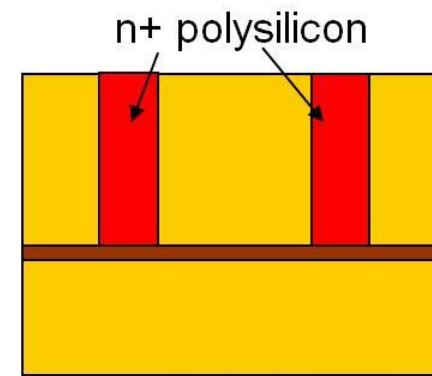
2) n+ hole definition and etching



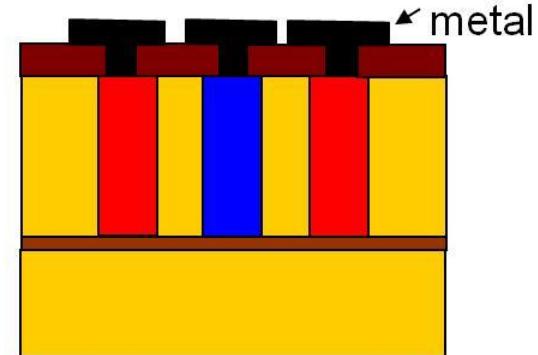
4) p+ hole definition and etching



5) hole doping and filling



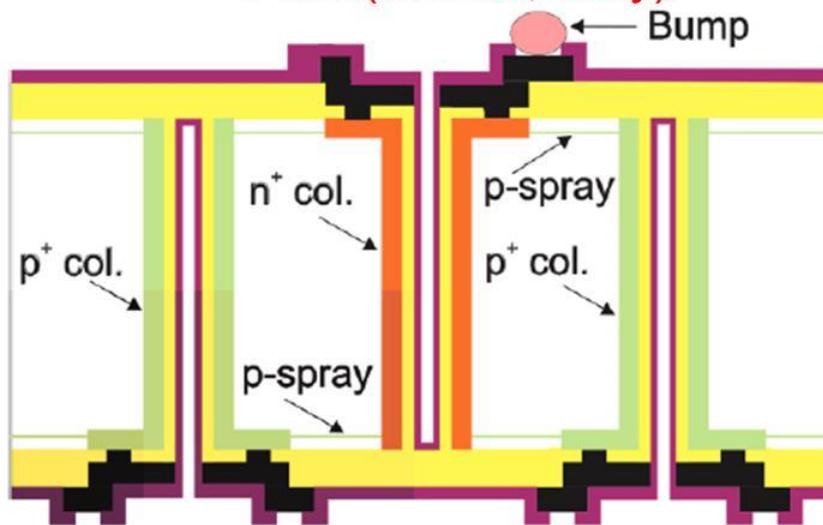
3) hole doping and filling



6) Metal deposition and definition

Double-sided 3D sensors

FBK (Trento, Italy)

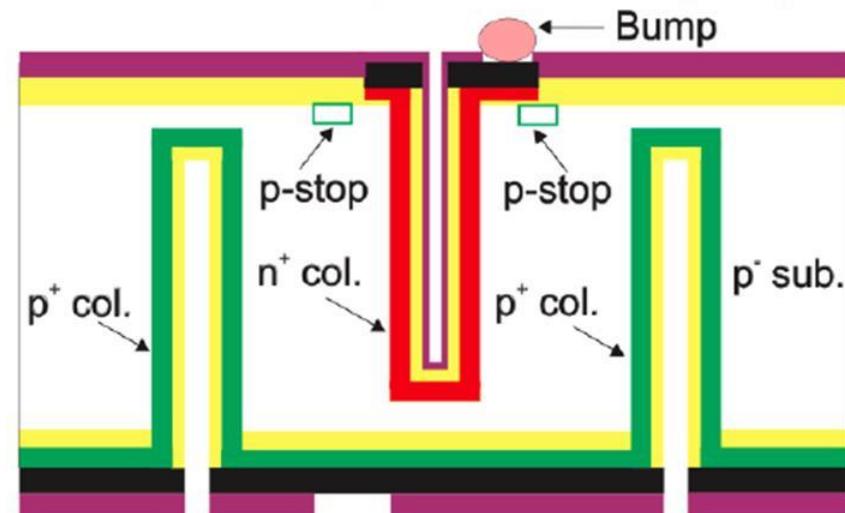


oxide	metal	passivation
p- Si	p+ Si	n+ Si

A. Zoboli et. al., IEEE TNS 55(5) (2008), 2775

G. Giacomini, et al., IEEE TNS 60(3) (2013) 2357

CNM (Barcelona, Spain)



oxide	metal	passivation	
p- Si	p+ poly-Si	n+ poly-Si	p+ Si

G. Pellegrini et. al. NIMA 592(2008), 38

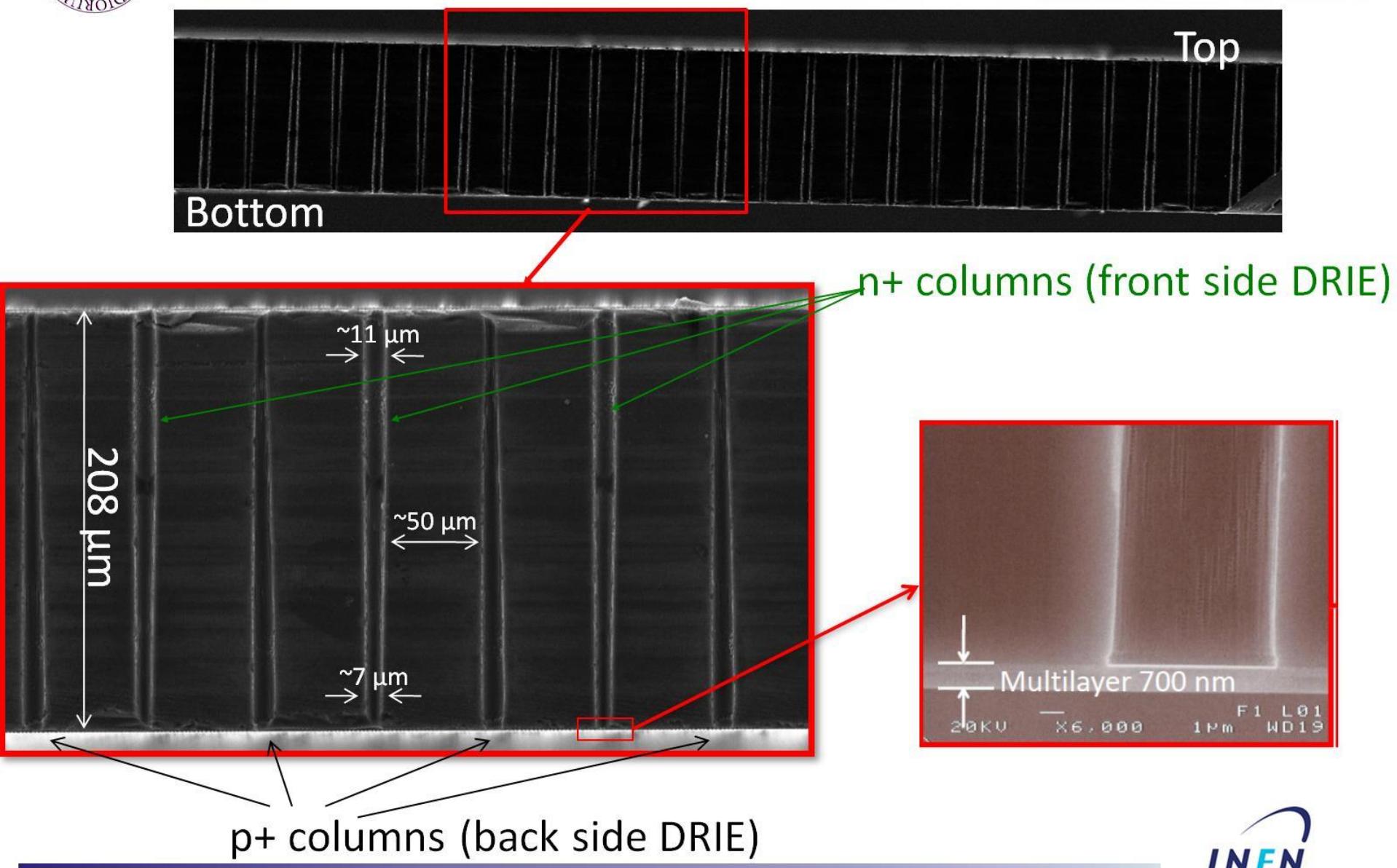
G. Pellegrini et. al. NIMA 699(2013), 27

- Do not use support wafer → reduced process complexity
- Back-side accessible → Easier assembly within systems
- Active edge not feasible → **Slim edge ...**

} **Technology
of choice
for the IBL**

INFN
 Istituto Nazionale
 di Fisica Nucleare

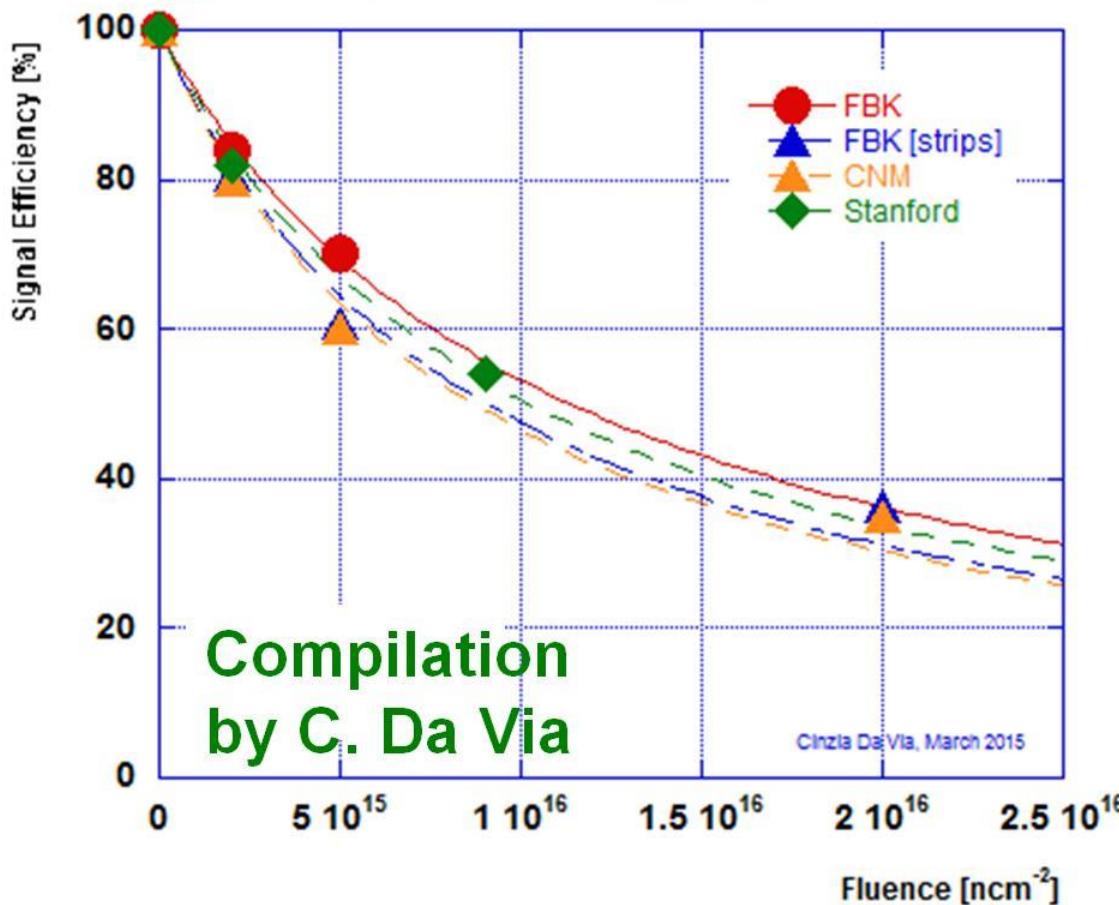
Passing through columns



Signal Efficiency

Data from:

- [1] ATLAS IBL Collaboration, JINST 7 (2012) P11010
- [2] G.-F. Dalla Betta, et al., NIMA 765 (2014) 155
- [3] M. Koehler et al. NIMA 659 (2011) 272
- [4] C. Da Via, et al., NIMA 604 (2009) 505



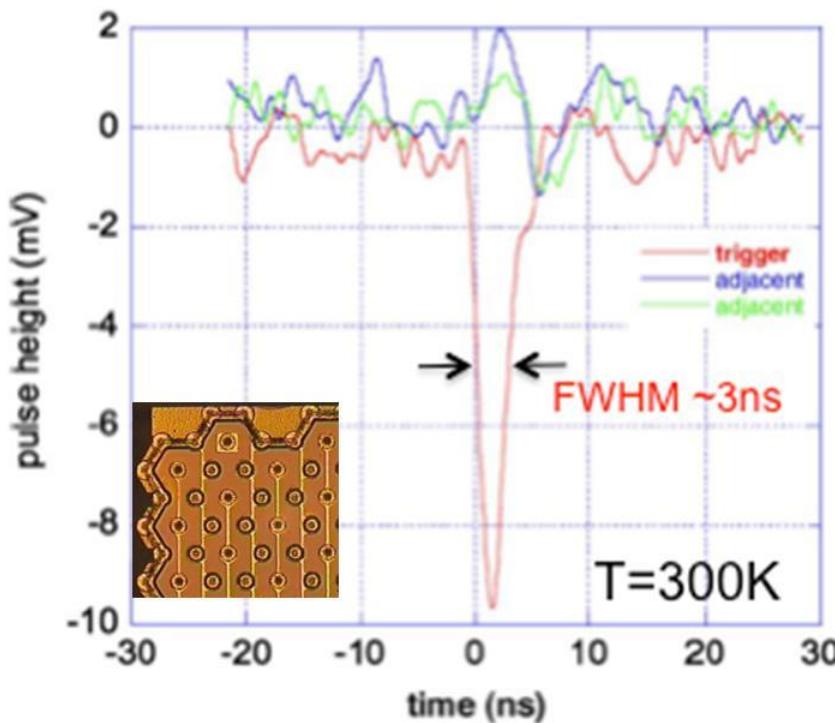
Signal Efficiency =
Ratio of max. signal
after irradiation
and before irradiation

$$SE = \frac{1}{1 + 0.6L \frac{K_\tau}{\nu_D} \Phi}$$

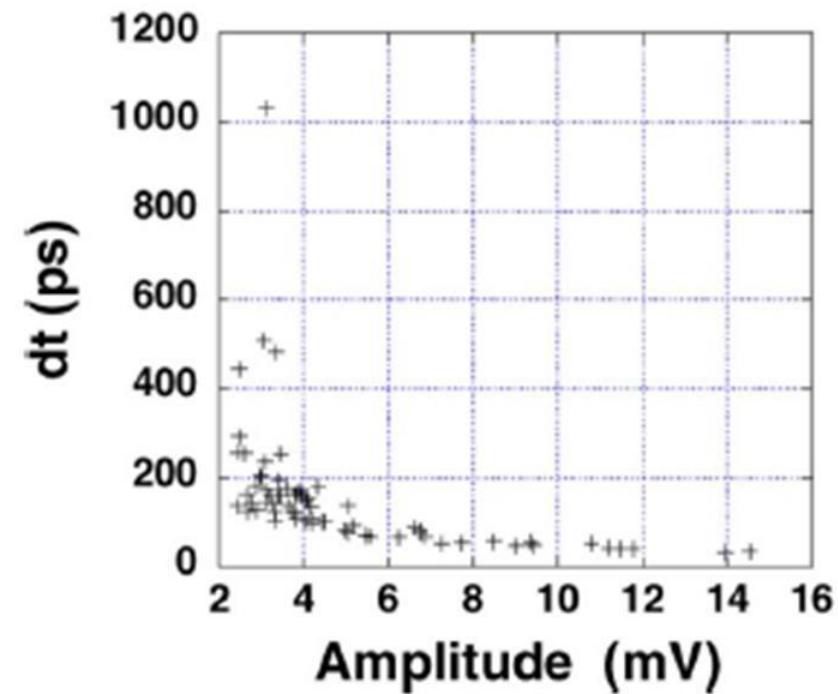
C. Da Via, S. Watts,
NIMA 603 (2009) 319

Signal speed

So far tested with hex-cell 3D's
($L=50\mu\text{m}$) & fast current amplifier



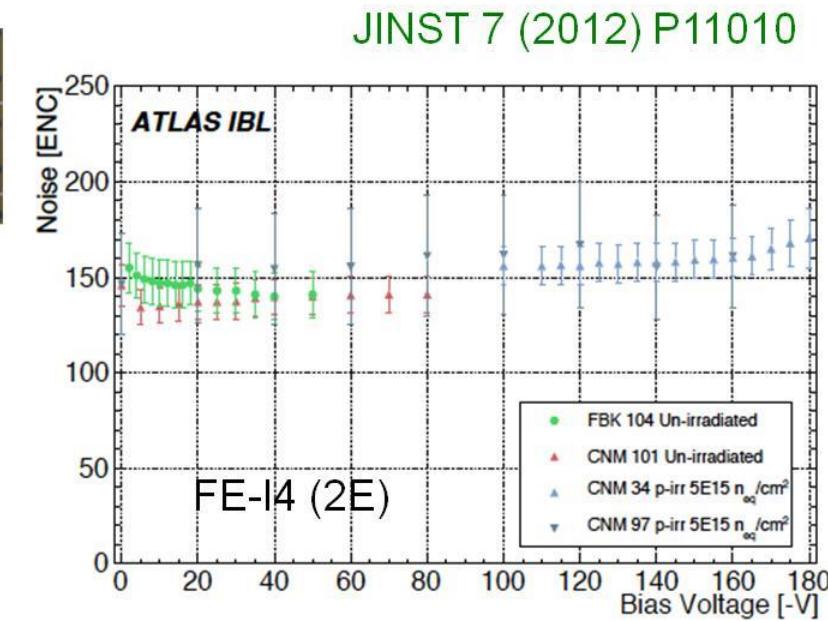
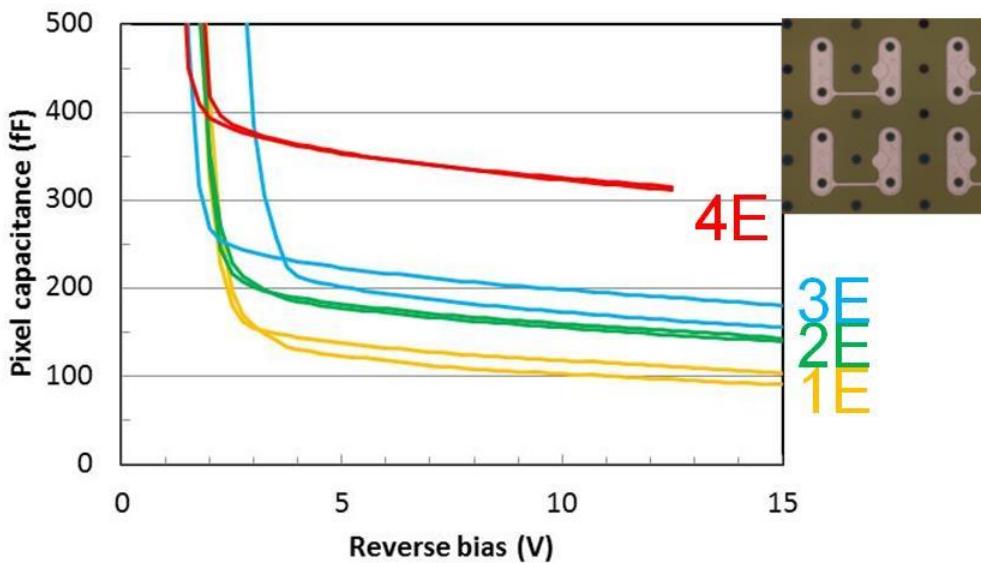
Timing resolution **from 177 ps to 31ps**, limited by front-end noise



S. Parker et al. IEEE TNS 58(2) (2011) 404

Capacitance and noise

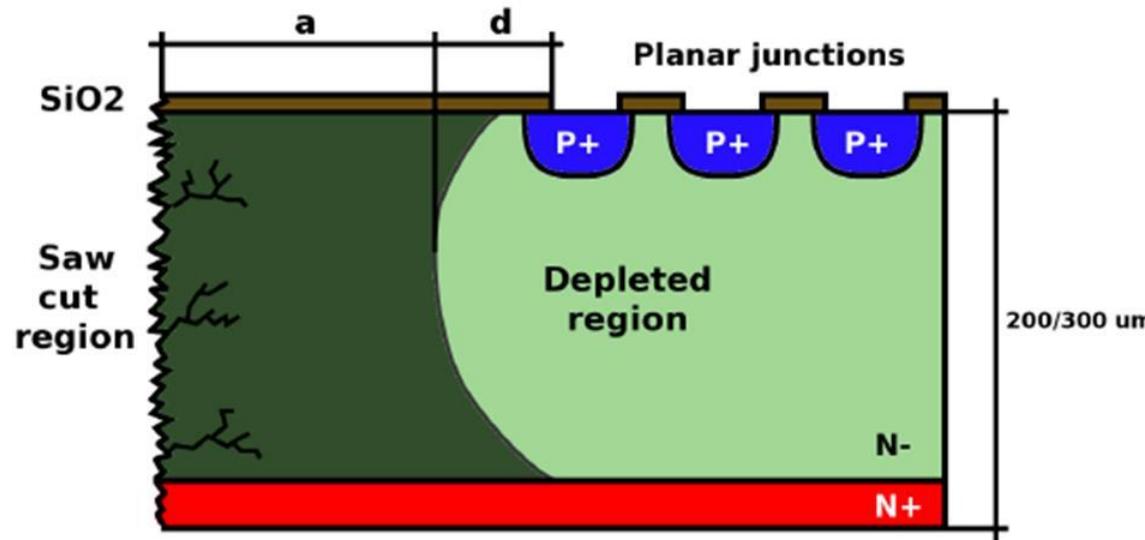
3D sensors have a larger capacitance than planar sensors:
possible noise penalty



Full depletion is reached at
Very low voltage

Low noise obtained with FE-I4

The edge termination problem



- In standard designs with saw-cut dicing, there's risk of high leakage current injection from the damaged cut region.
- Need to account for:
 - Lateral depletion region (d)
 - Additional safety margin (a), also used to host multiple guard rings in most designs for higher V_{bd} and better stability

→ Wide dead area at the edge: $a+d \sim 0.5 - 1 \text{ mm}$

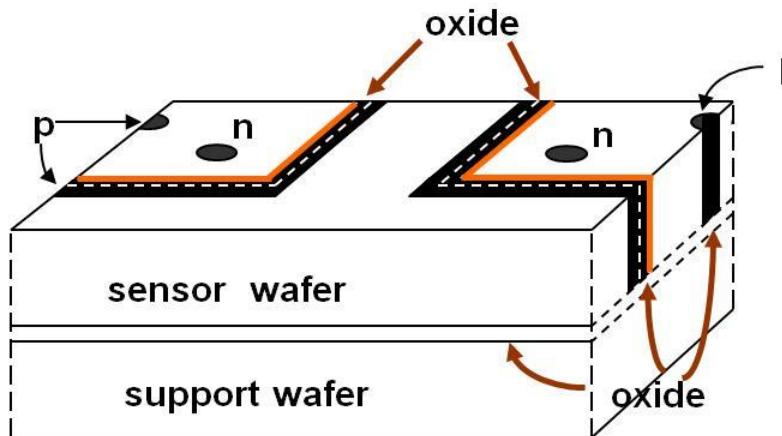


Going edgeless

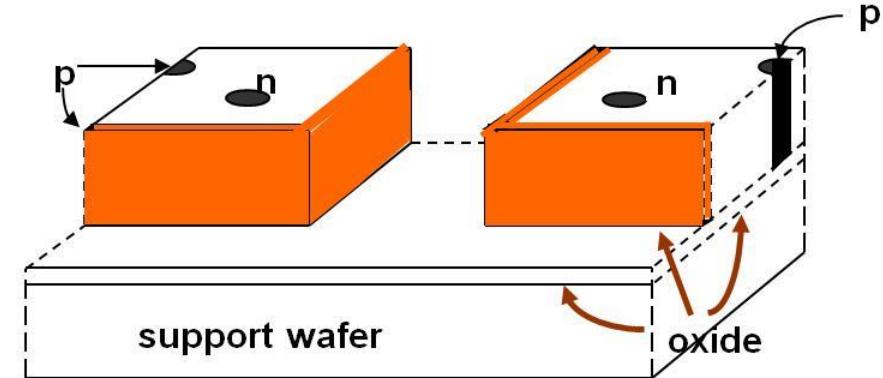
- Future HEP experiments (e.g. HL-LHC) require new sensors for the inner layers (pixels) with reduced geometrical inefficiency
- TOTEM experiment uses 1-side edgeless strip sensors
- Other forward physics experiments (AFP,HPS) will use 1-side edgeless pixels
- X-ray imaging: 4-side edgeless sensors used to obtain seamless large area images by detector tiling

Active edges

- First introduced at Stanford as an extension of 3D sensor technology, later applied also to planar sensors
- Cut lines are not sawed but etched with DRIE & doped to act as electrodes, **arbitrary shapes possible**
- Process is more complicated:
 - Need of support wafer → wafer bonding and final removal
 - Several DRIE steps (3-4 for 3D, 2 for planar)



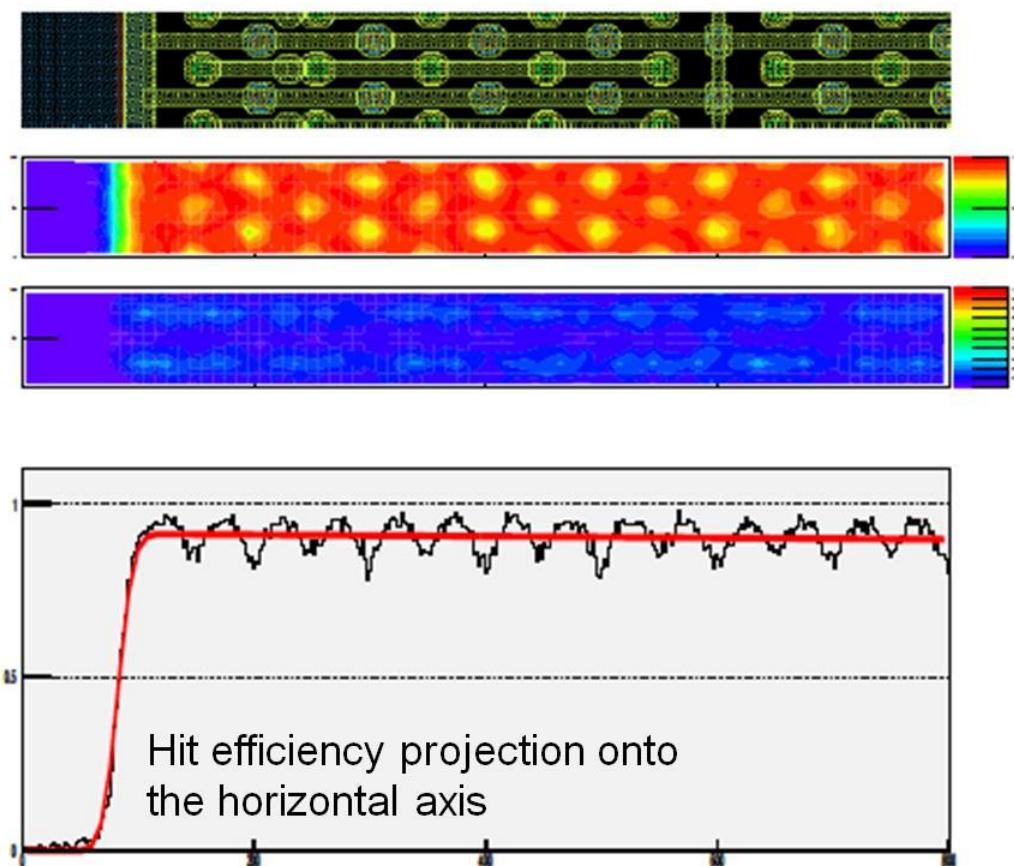
C. Kenney et al., IEEE TNS 48 (2001) 2405



C. Kenney et al., NIMA 565 (2006) 272

Active edge: sensitivity

3D active-edge pixel sensors coupled to FEI3 and tested with a 180 GeV/c pion beam at CERN



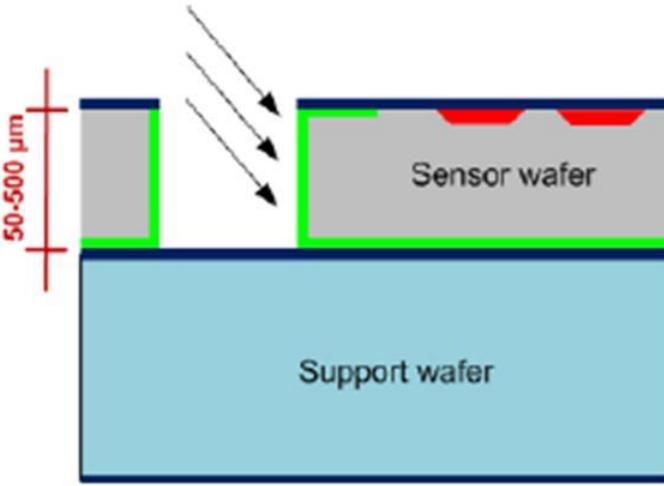
O. Røhne, IEEE NSS 2008, N27-8
C. Da Via, et al. IEEE TNS 56(2) (2009) 505

Active edge: recent highlights

Active edge technology now available also at other processing facilities (e.g., VTT, SINTEF, FBK).

VTT sensor with 4-quadrant edge implant

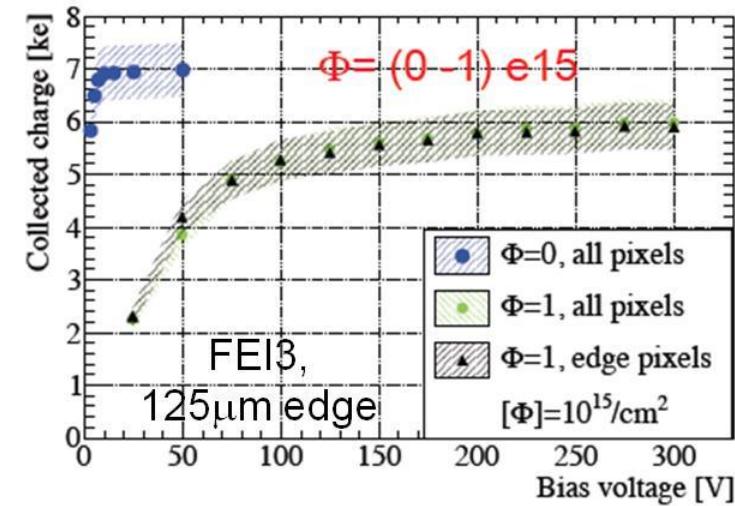
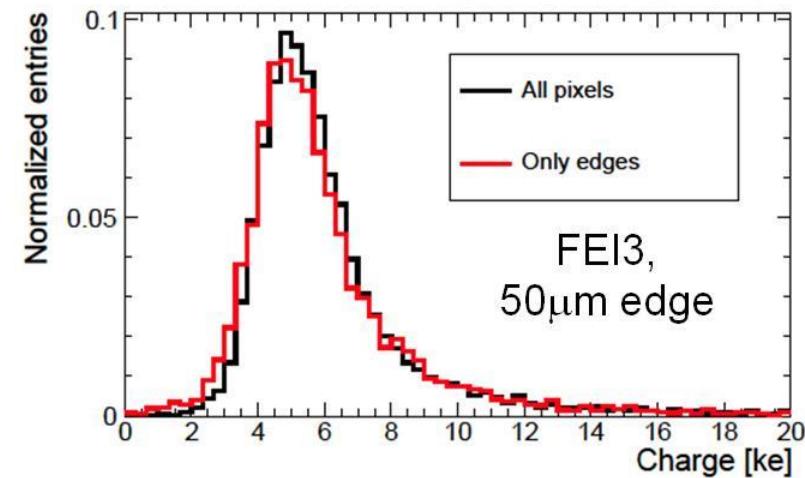
X. Wu et al., JINST 7 (2012) P02001



WIDEPIX 10x10 (<http://www.widepix.cz>)



A. Macchiolo et al., HSTD9 (2013)





The ATLAS 3D Sensor Collaboration

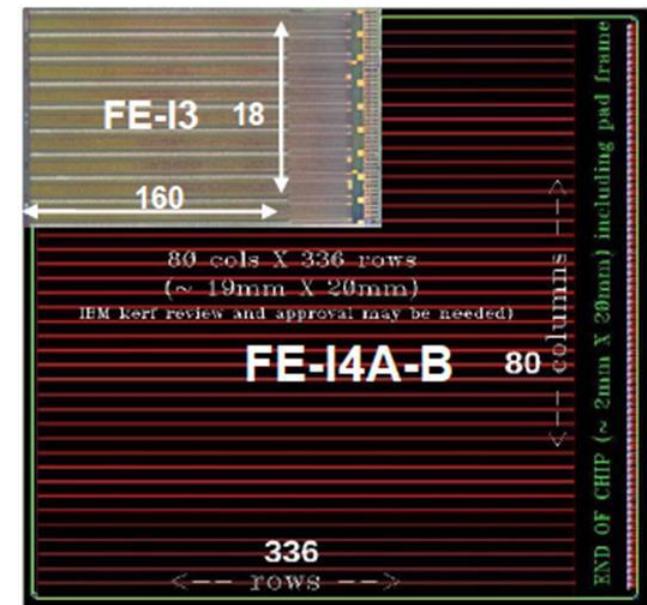
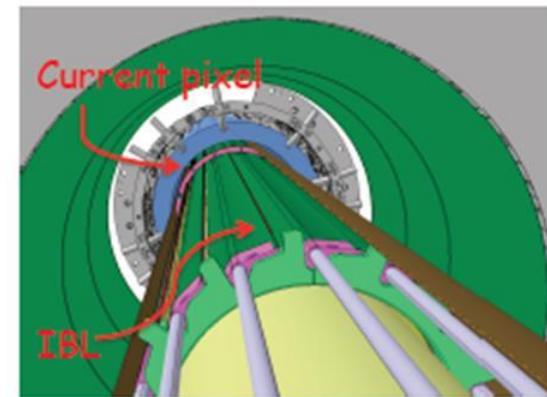
- Approved in 2007 with the **goal** of “Development, Testing and Industrialization of Full-3D Active-Edge and Modified-3D Silicon Radiation Pixel Sensors with Extreme Radiation Hardness”.
- The Collaboration includes **18 Institutions and 4(+1) processing facilities**: SNF, SINTEF, CNM, and FBK (VTT joined later).
- **Systematic studies** on existing 3D samples from different foundries proved comparable performance
- Focus on the **ATLAS IBL** (2009-2012)



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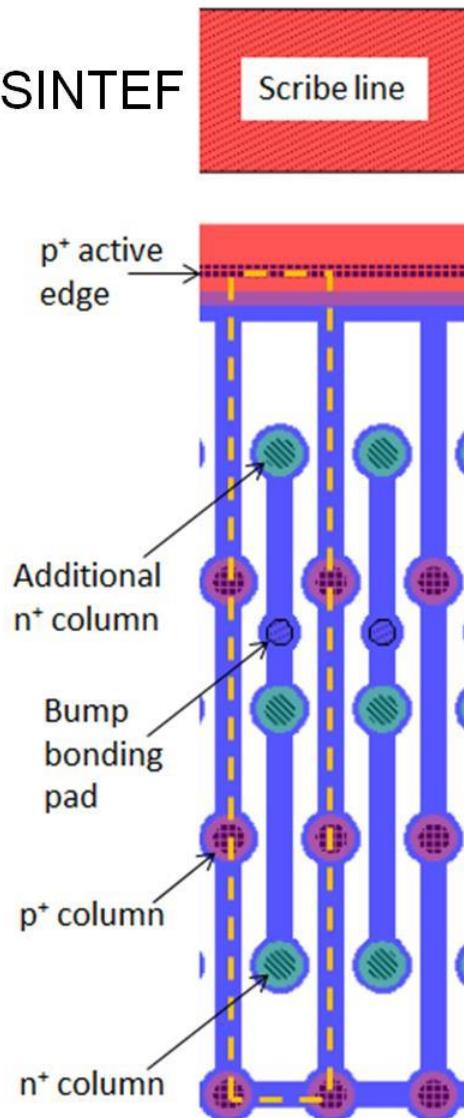
The ATLAS pixel Insertable B-Layer (IBL)

- Planar pixels originally installed at LHC have been designed for a fluence of $\sim 1\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$
- A new (**4th**) pixel layer at 3.4 cm from the beam installed inside the existing pixel layers of ATLAS
- New radiation hard technologies needed for both the sensors ($6\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$) and the front-end electronics (250 Mrad)

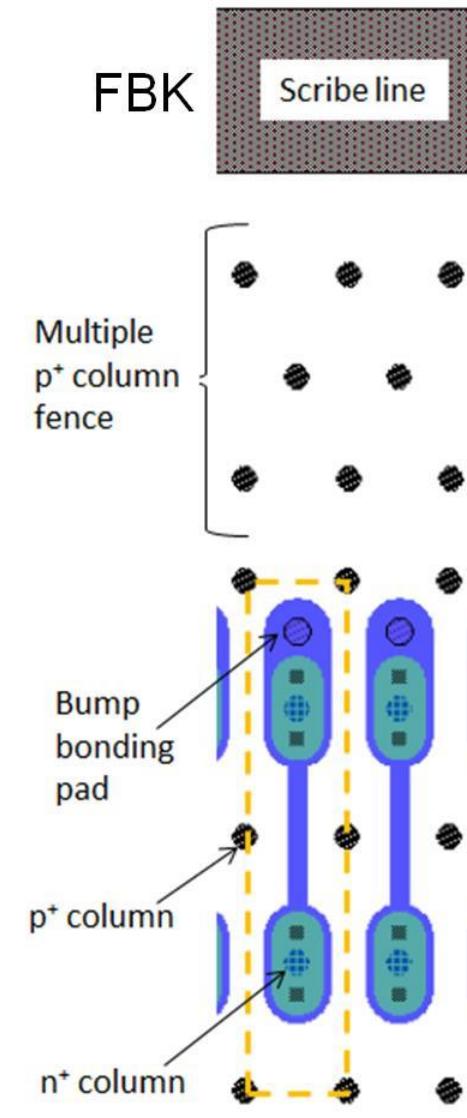


Edge Design (active vs slim)

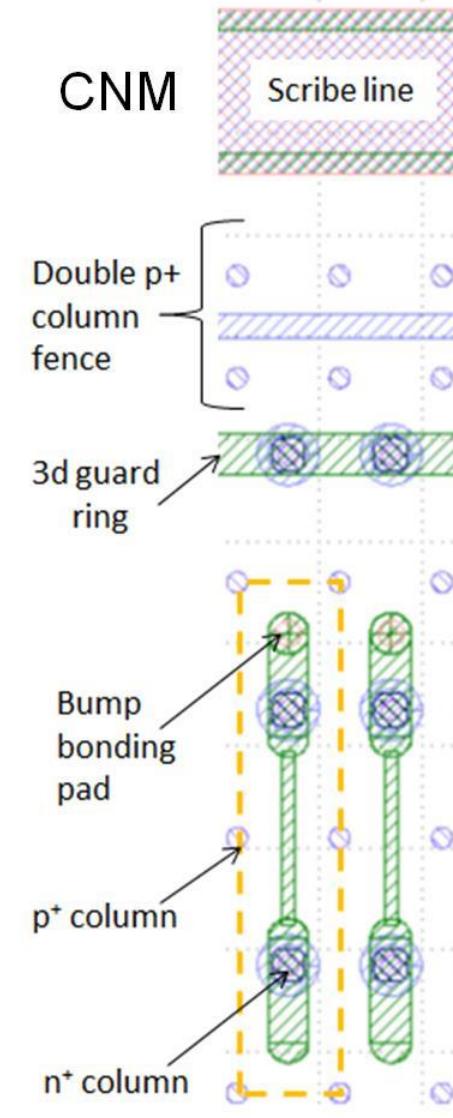
SNF/SINTEF



FBK



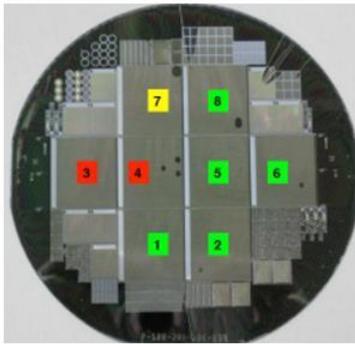
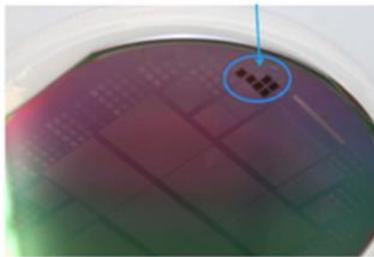
CNM



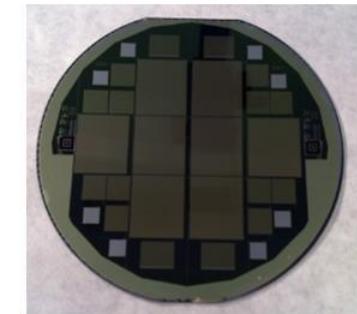
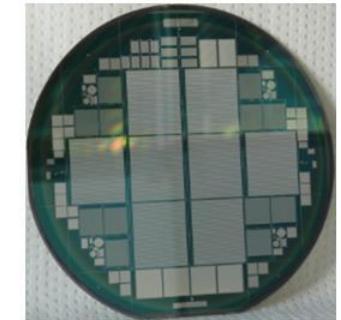
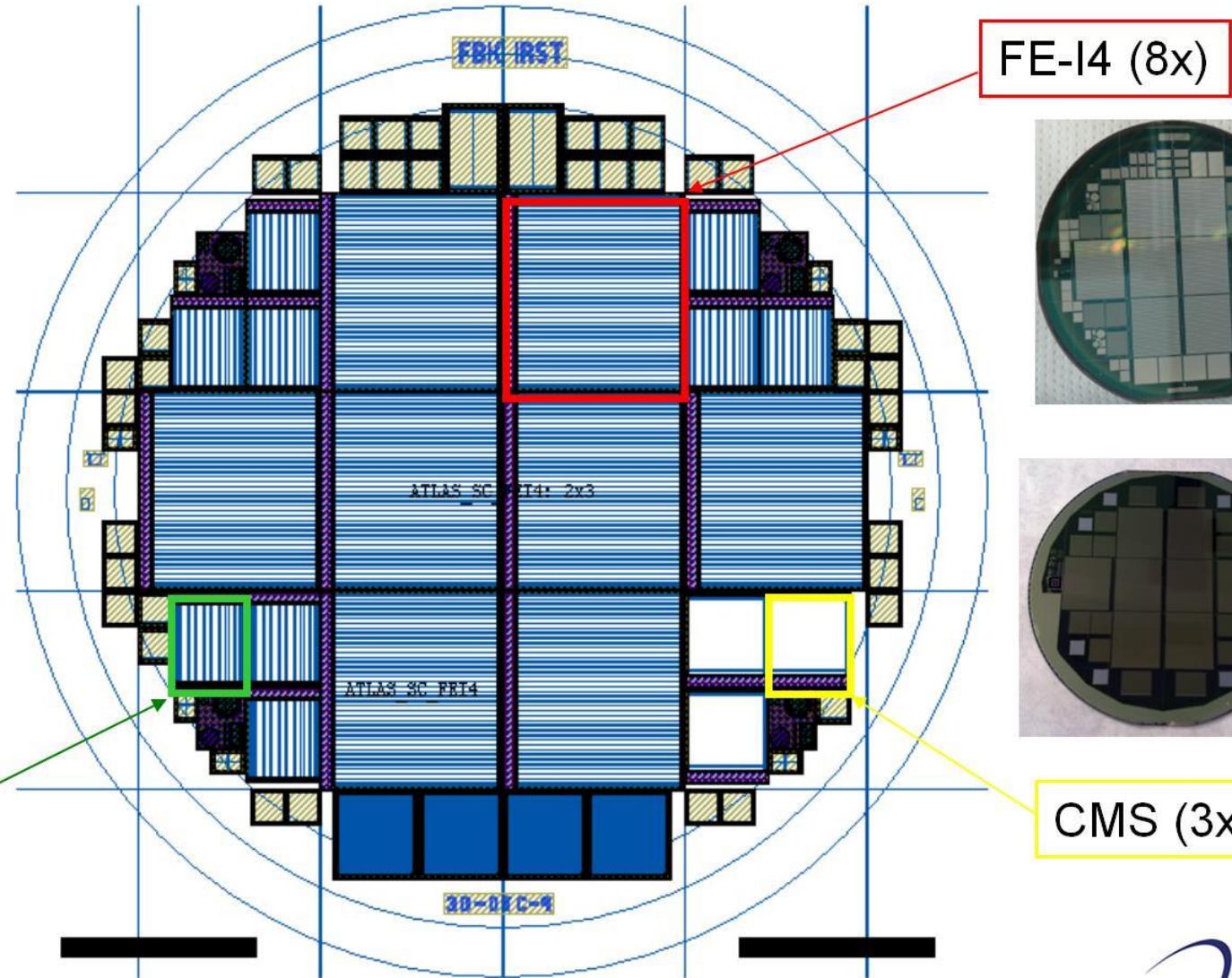


ATLAS 3D common floor-plan

Test
structures at
the periphery



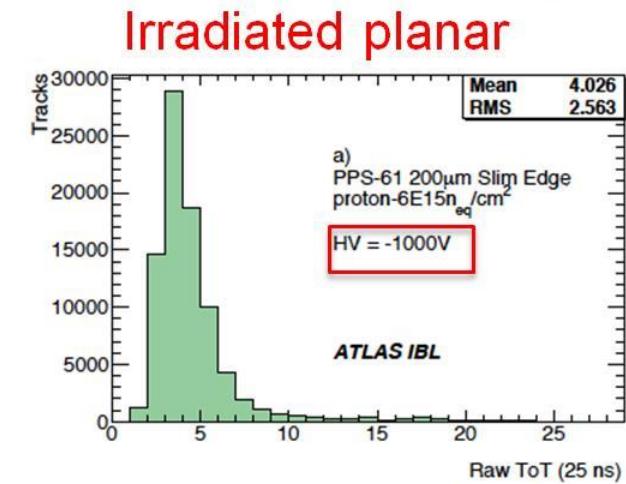
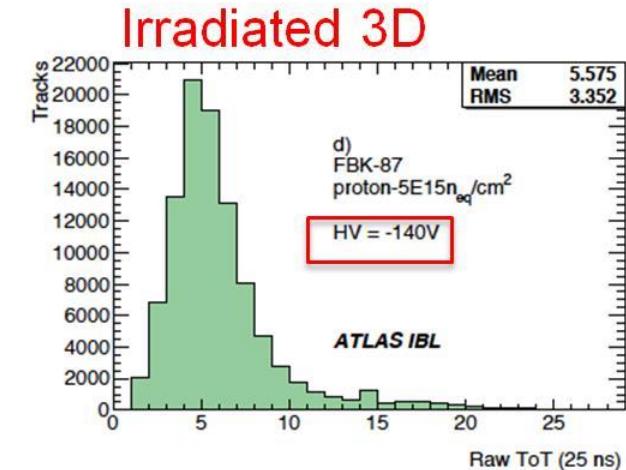
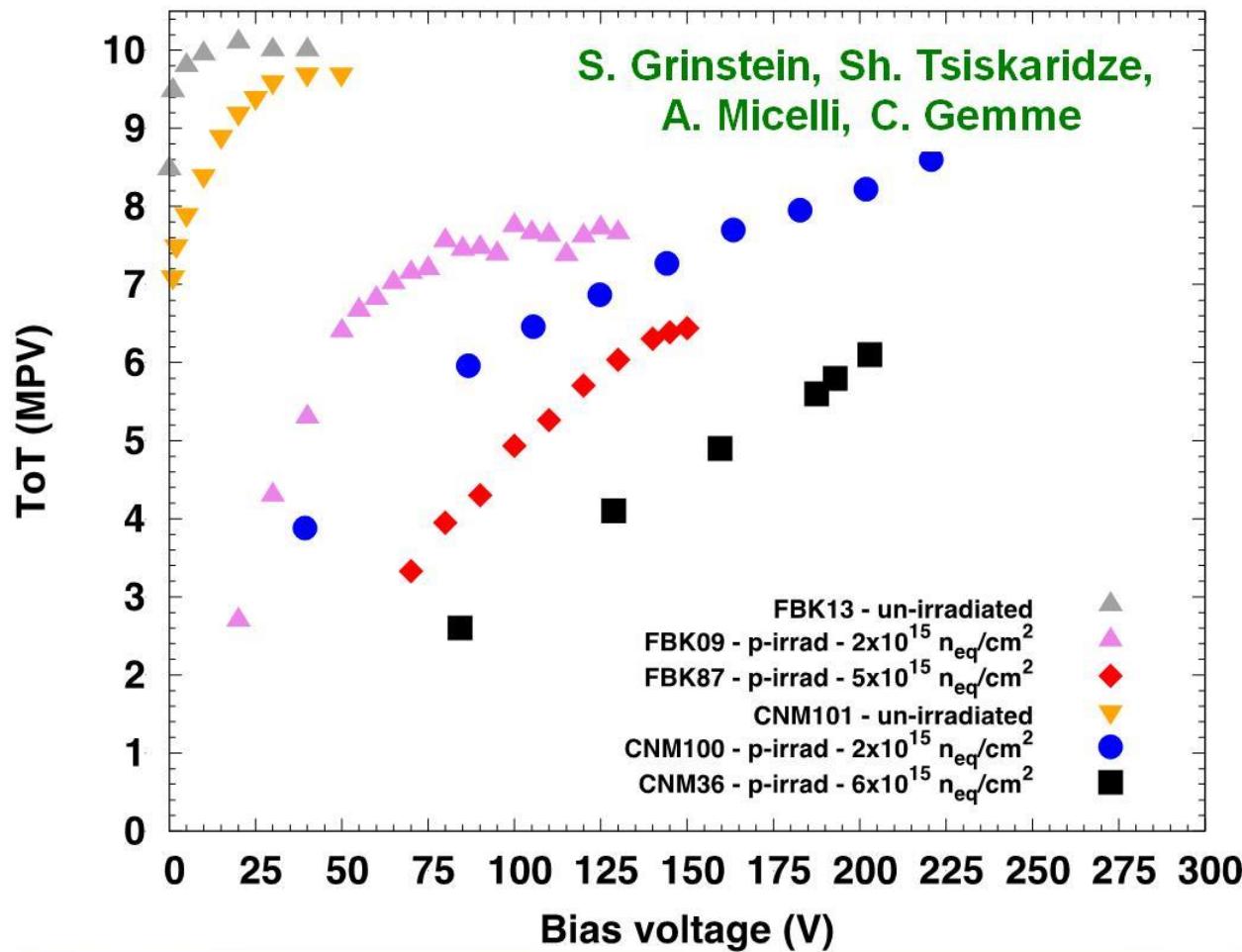
FE-I3 (9x)



CMS (3x)

Charge collection properties

Data from: ATLAS IBL Collaboration, JINST 7 (2012) P1101
+ S. Grinstein, unpublished results (FBK09)





Summary of CERN beam tests results

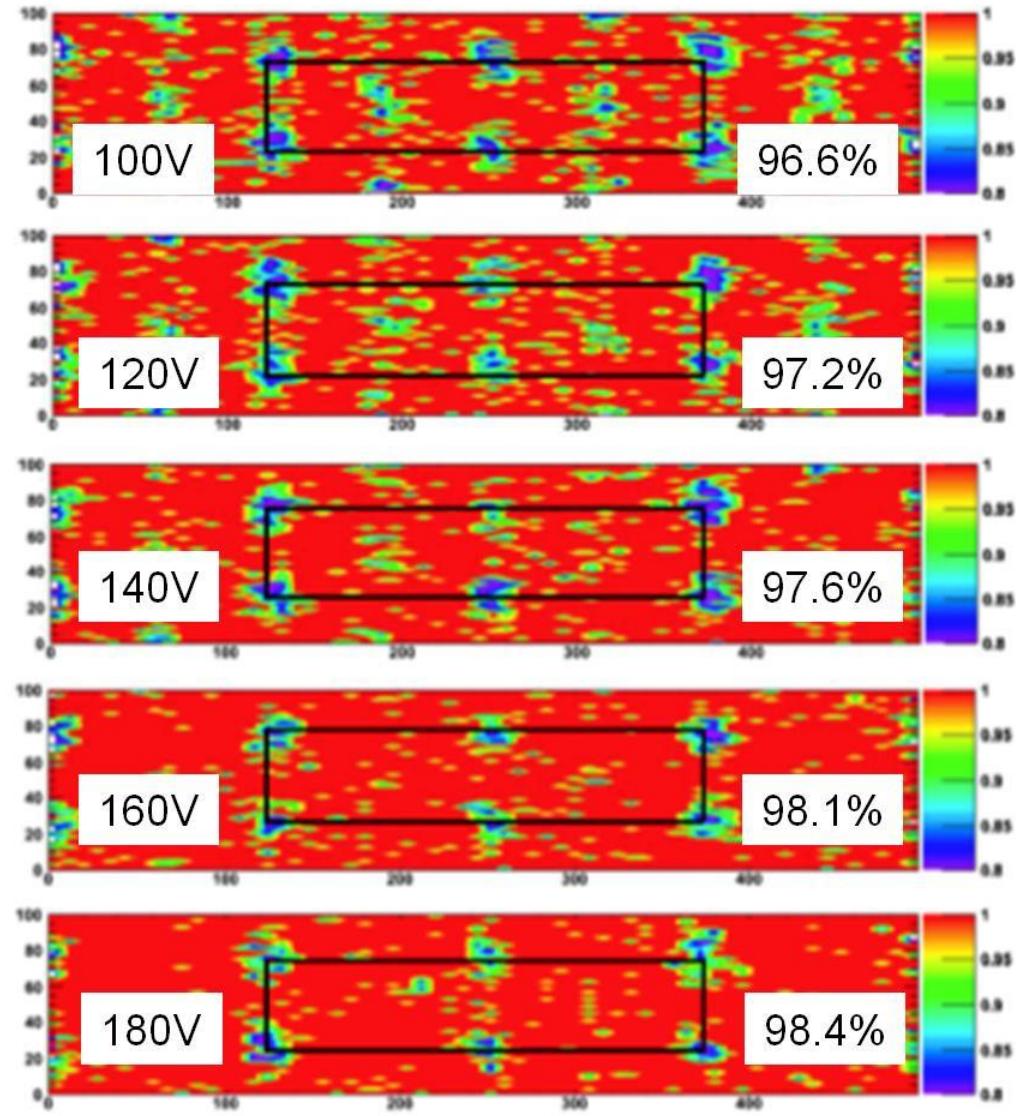
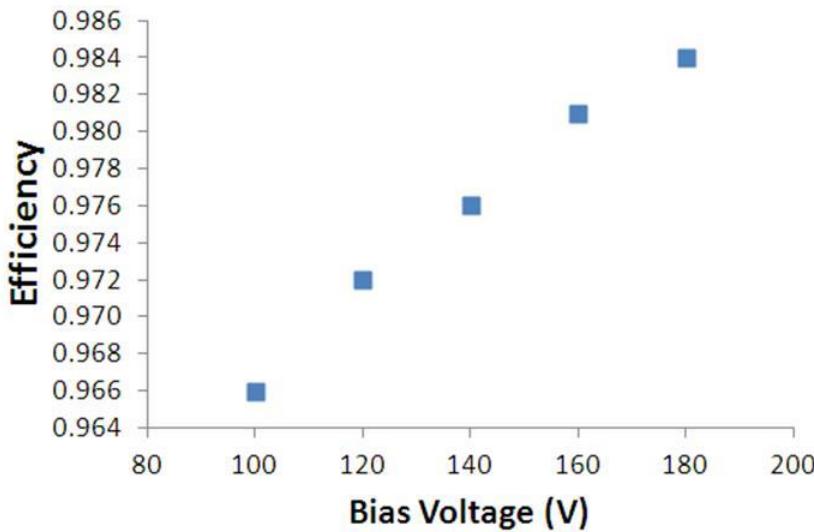
The ATLAS IBL Collaboration, "Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip", JINST 7 (2012) P11010.

Sensor ID	Bias (V)	Tilt Angle °	Irrad.	Fluence (n_{eq}/cm^2)	Threshold (e-)	Hit Eff. (%)
CNM55	20	0	no	-	1600	99.6
FBK13	20	0	no	-	1500	98.8
CNM34	160	0	25 MeV protons	5×10^{15}	1500	98.1
CNM97	140	15	25 MeV protons	5×10^{15}	1800	96.6
CNM34	160	15	25 MeV protons	5×10^{15}	1500	99.0
CNM81	160	0	Reactor Neutrons	5×10^{15}	1500	97.5
FBK90	60	15	25 MeV protons	2×10^{15}	3200	99.2
FBK11	140	15	25 MeV protons	5×10^{15}	2000	95.6
FBK87	160	15	25 MeV protons	5×10^{15}	1500	98.2

Hit efficiency vs bias voltage

S. Grinstein, Sh. Tsiskaridze

- CNM34, p-irrad $5e15$ n_{eq} cm⁻²
- Threshold at 1500 e-
- Efficiency and charge collection increase with voltage
- At 160V inefficiency regions due to n⁺ columns disappear
- Noise occupancy becomes a problem beyond 170V

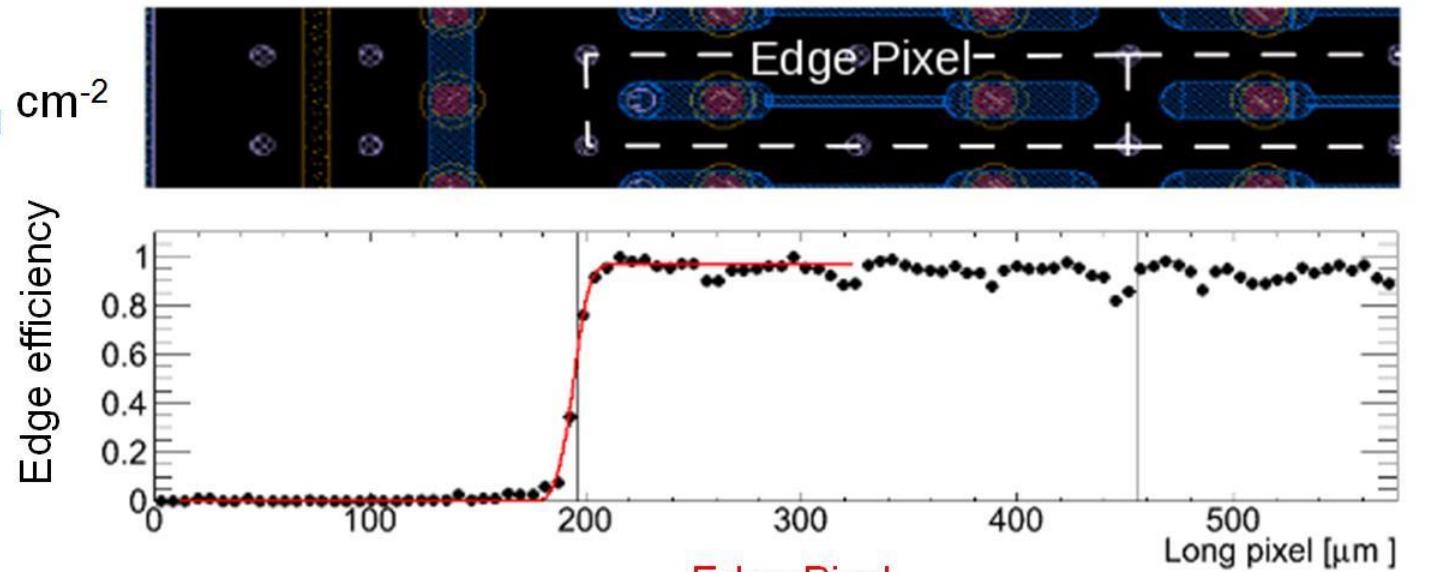




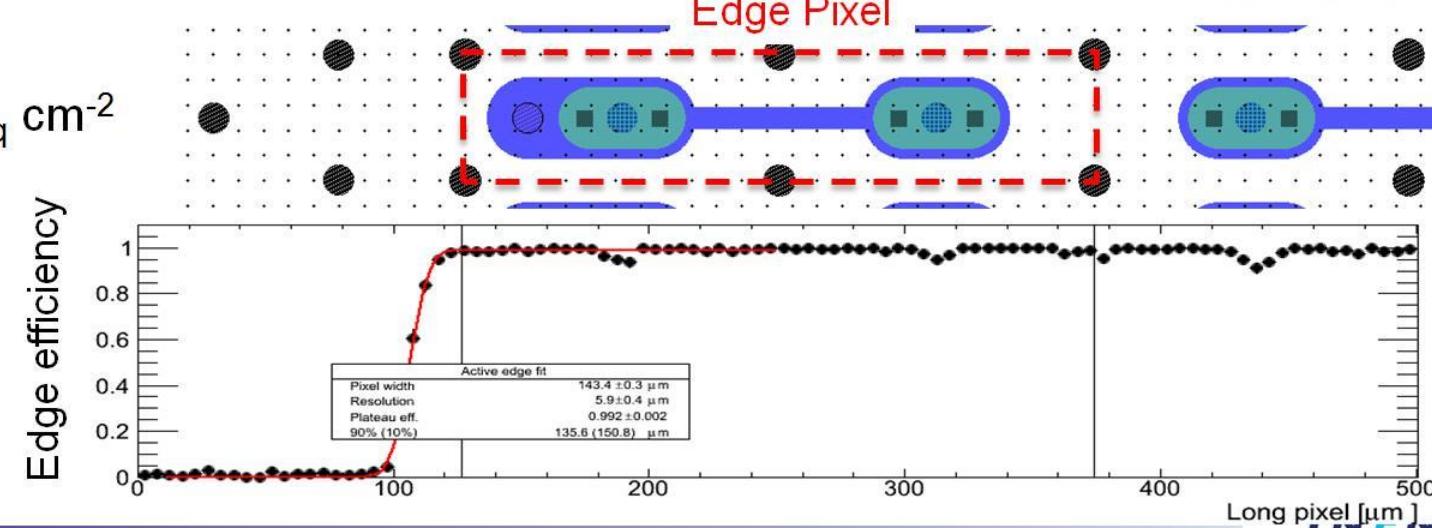
Edge efficiency

P. Grenier, S. Grinstein, Sh. Tsiskaridze

CNM34
p-irrad $5 \times 10^{15} n_{eq} cm^{-2}$
Tilt 15°, 140V

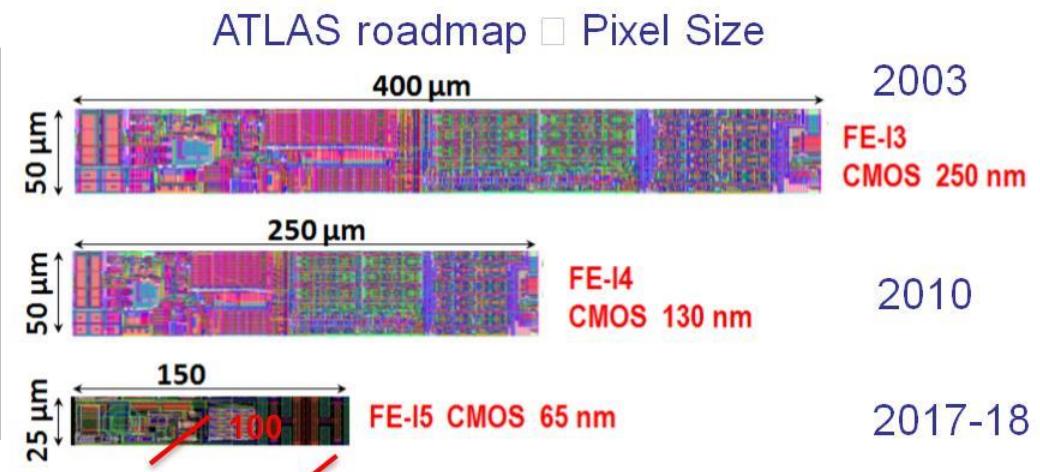
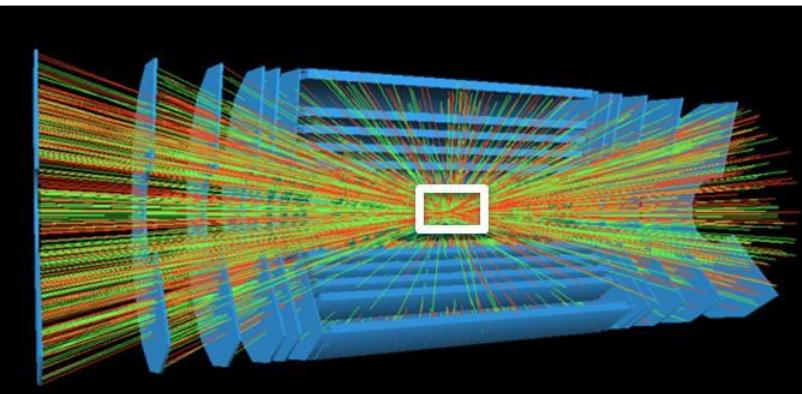


FBK90,
p-irrad $2 \times 10^{15} n_{eq} cm^{-2}$
Tilt 15°, 60V



Pixel Roadmap LHC → HL-LHC

N. Wermes, 9th TN Workshop (Genova, 2014)



Increased luminosity
requires

- higher hit-rate capability
- increased granularity
- higher radiation tolerance
- lighter detectors



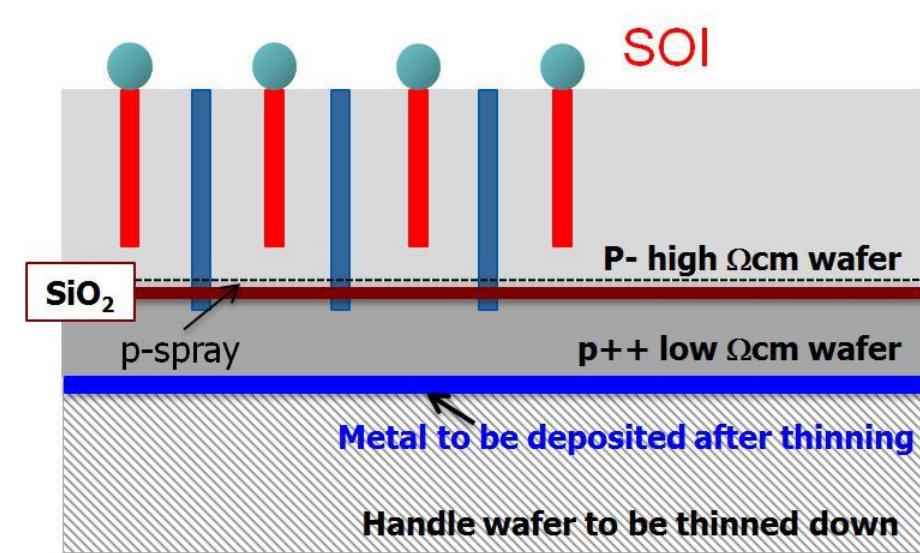
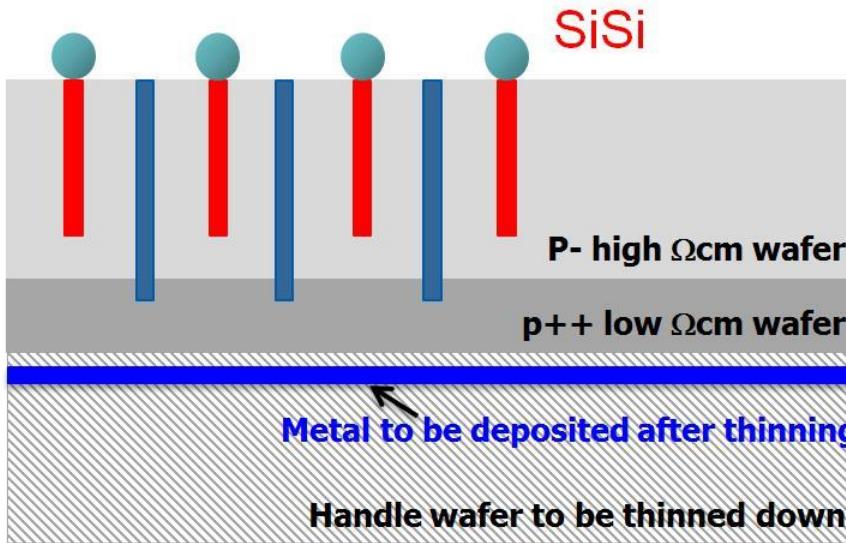
Implications for 3D sensors

- Modified technology/design for:
- thinner sensors
 - narrower electrodes
 - reduced electrode spacing
 - very slim (or active) edges

New SS-3D approach at FBK

- Proposed by INFN-FBK, also used at SINTEF and SNF

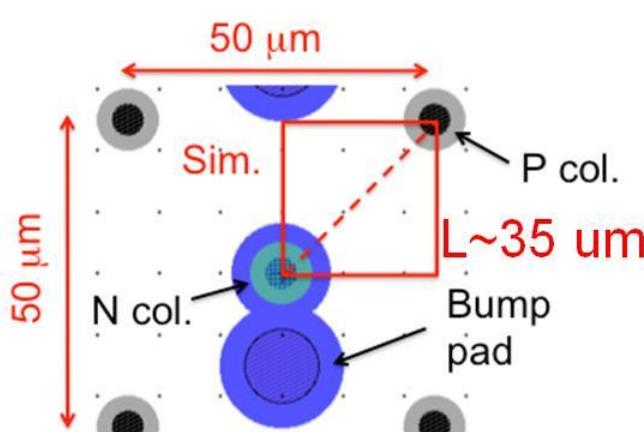
G.-F. Dalla Betta et al.,
NIMA 824 (2016) 388



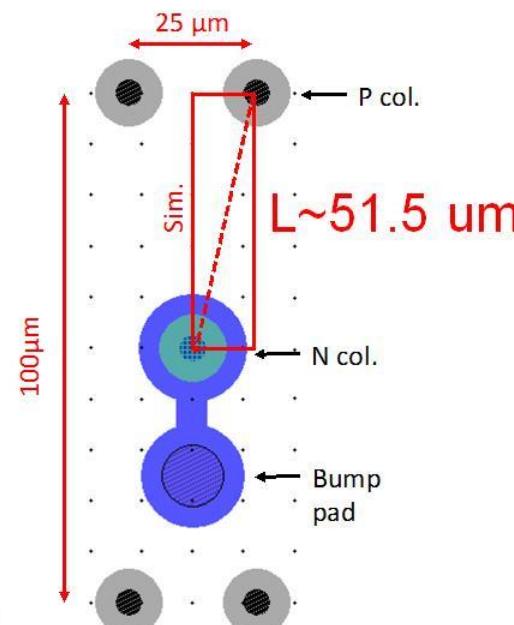
- Thin sensors on support wafer: SiSi or SOI
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~ 5 μm
- Holes (at least partially) filled with poly-Si

Small-pitch 3D pixel layouts

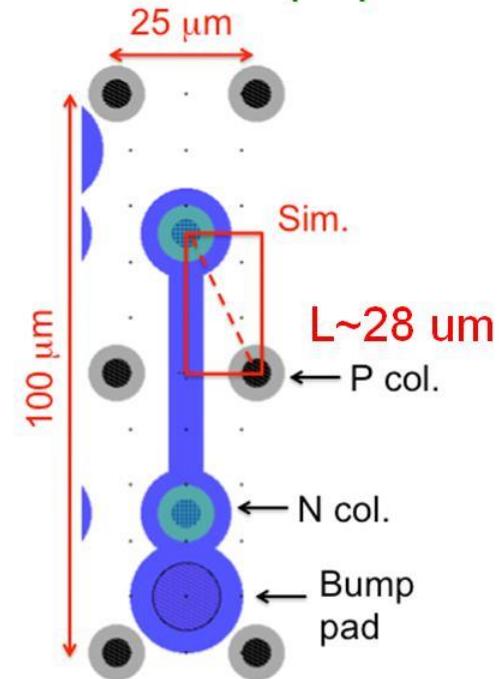
50 x 50 (1E)



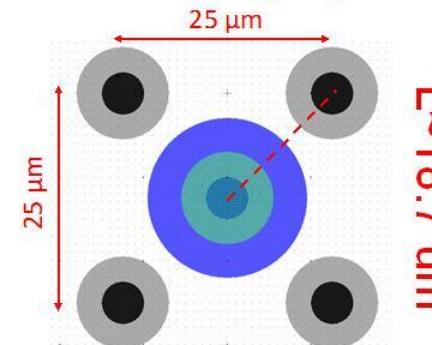
25 x 100 (1E)



25 x 100 (2E)



25 x 25 (1E)



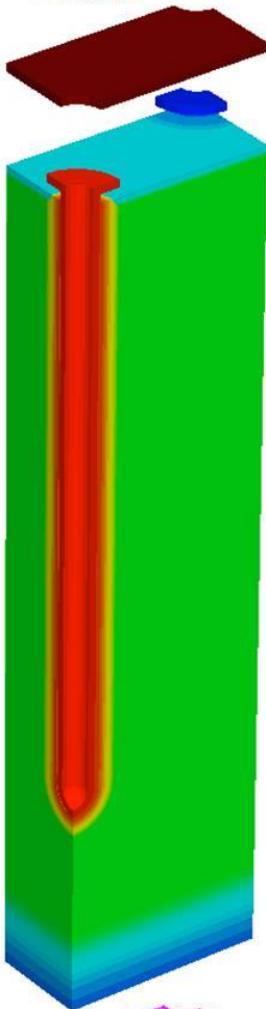
All designs refer to FBK SS-3D process, assuming $d=5 \mu\text{m}$

- No problems with 50x50 -1E (and 25x100 -1E) designs
- 25x100 -2E is difficult with SS-3D, because of the bump pad
- new ideas to be tested: bumps on columns

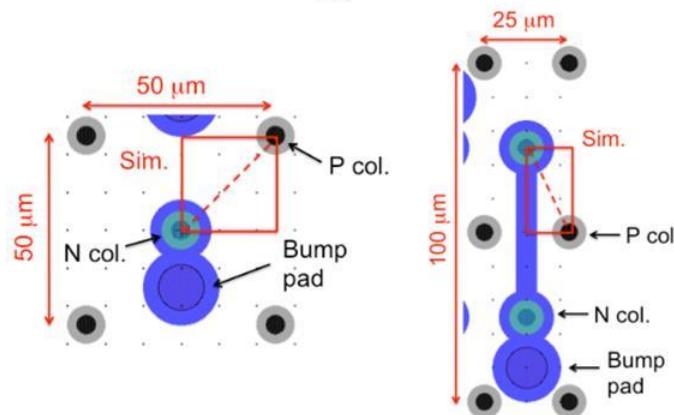
G.-F. Dalla Betta et al., NIMA 824 (2016) 386



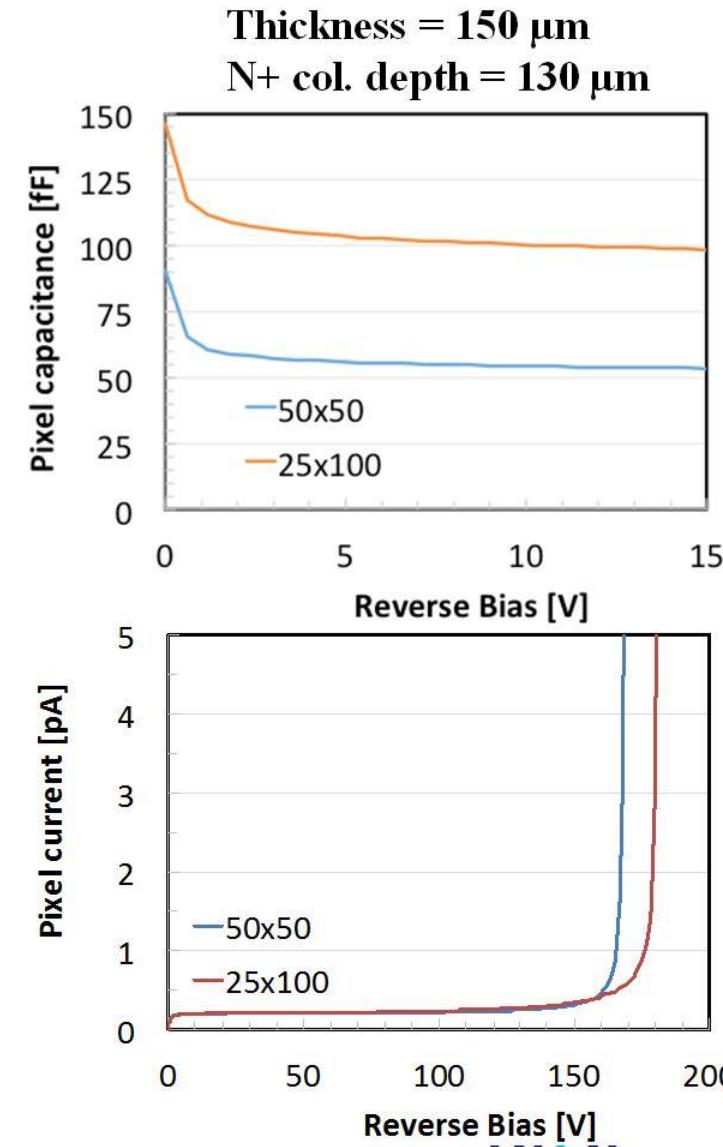
New SS-3D pixel simulations



- Full 3D simulation with parameters representative of FBK technology



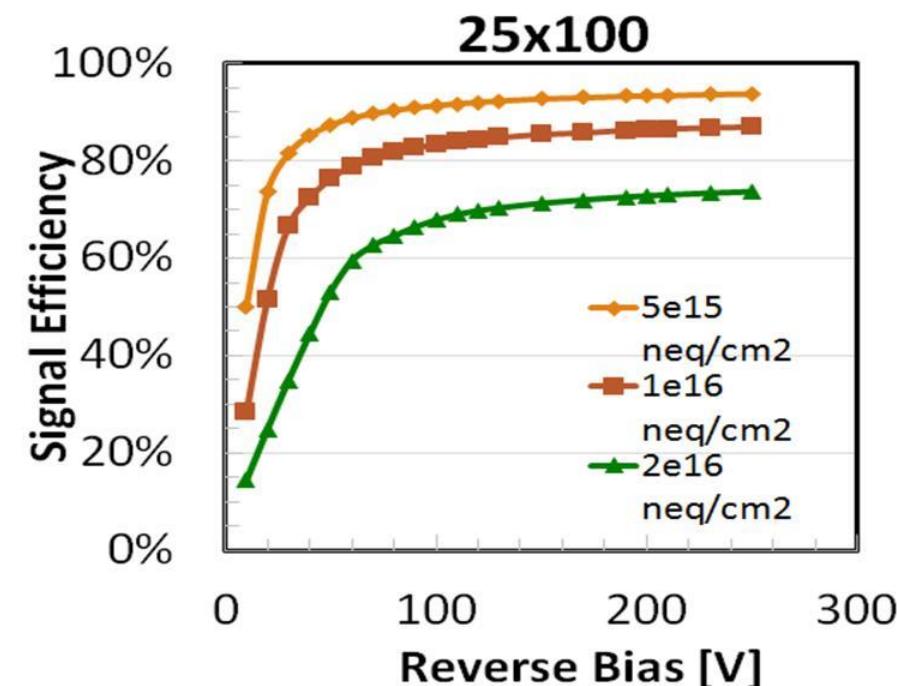
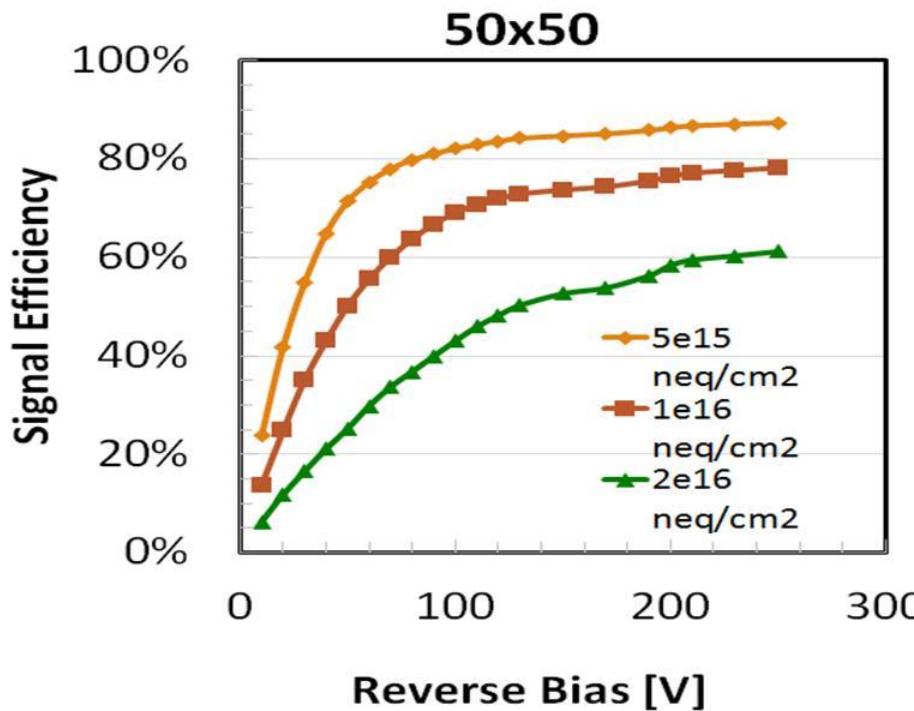
- Capacitance compatible with RD53s specifications
- Initial breakdown voltage very high



D.M.S. Sultan et al., IWORD 2016

Simulated Signal Efficiency

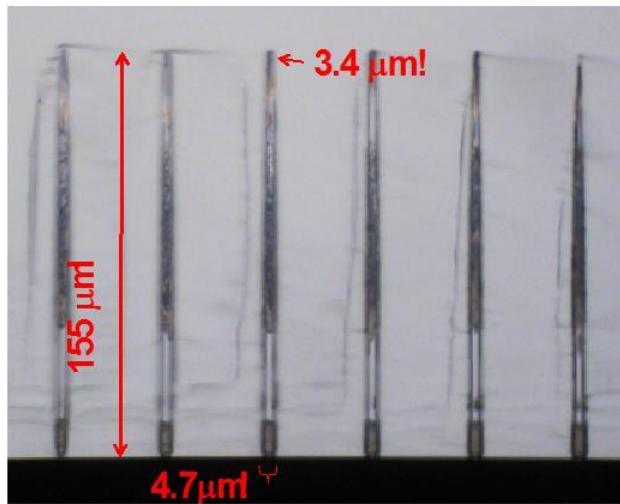
R. Mendicino, TIFPA



- Bulk damage: new Perugia radiation damage model
- Very high average signal efficiency
- Possible impact ionization effects at high field

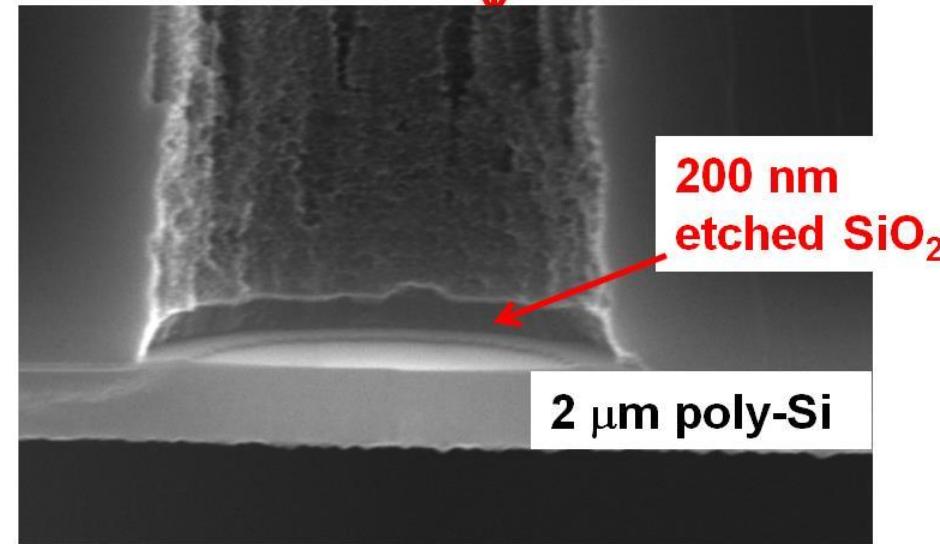
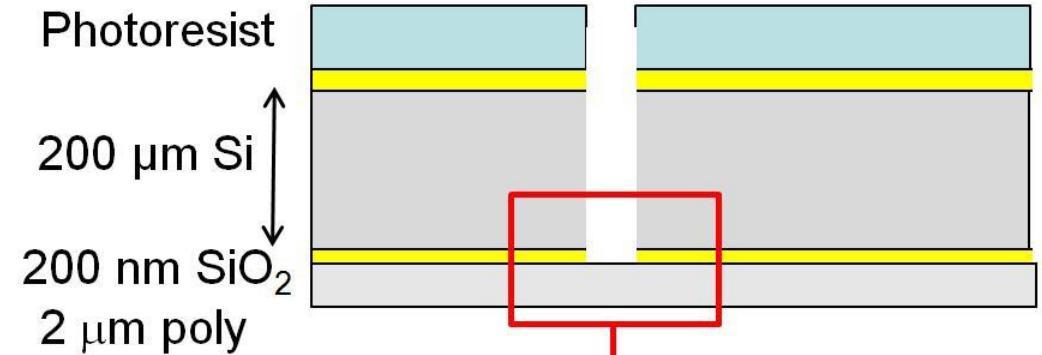
G.-F. Dalla Betta et al., IEEE NSS 2015, N3C3-5

Etching narrow columns by DRIE



Ohmic columns optimized for depth

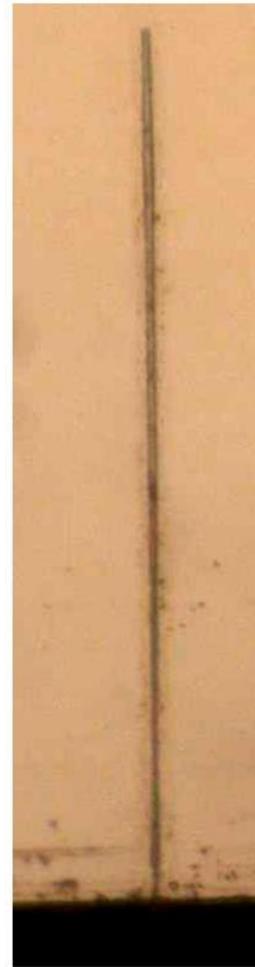
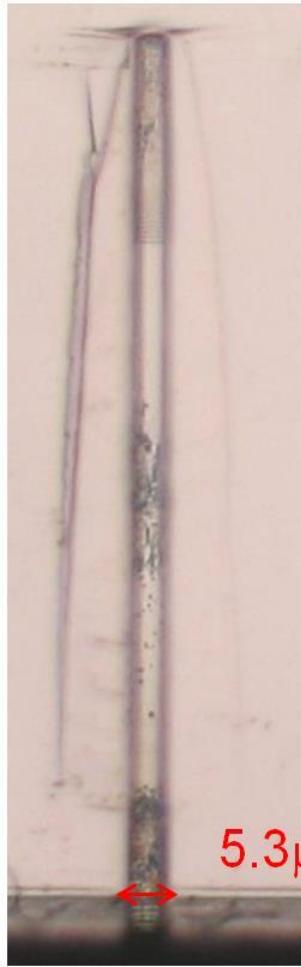
Testing different etching depth
and etching through oxide layer
for SOI approach



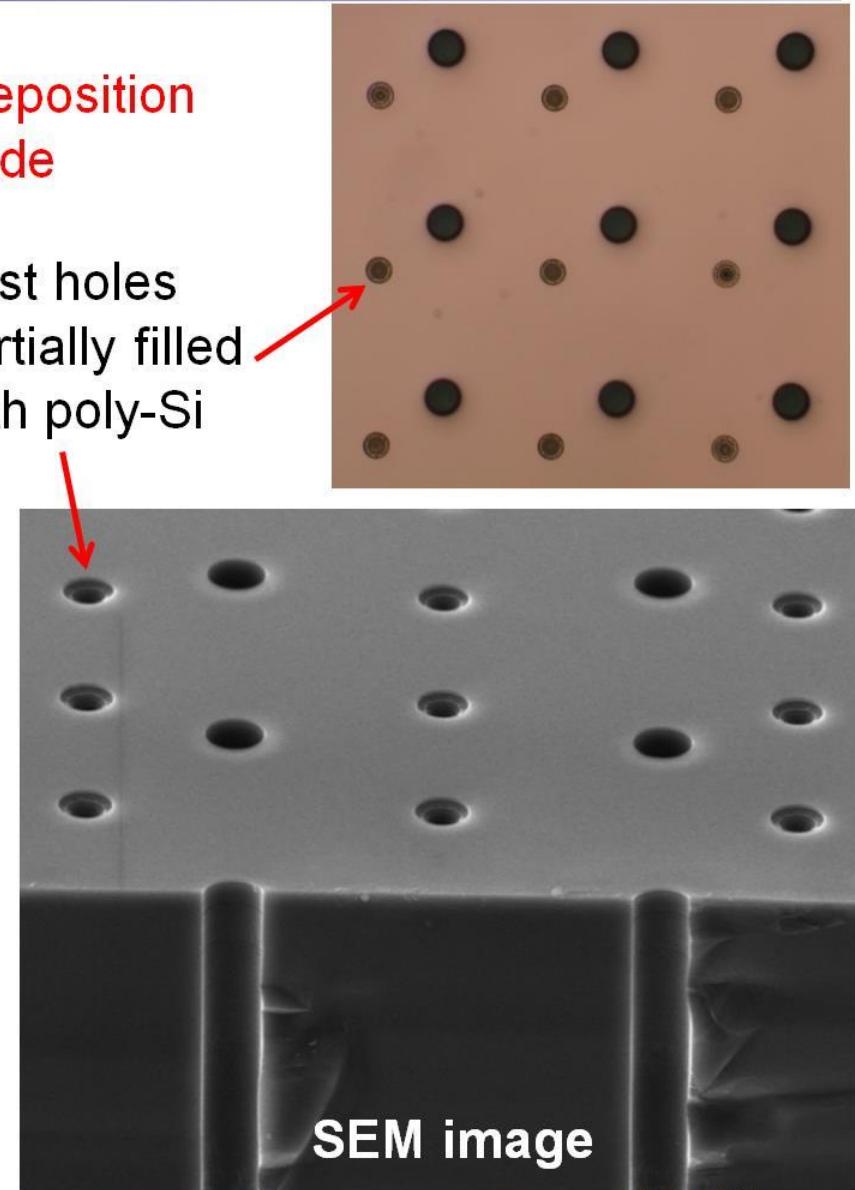
G.-F. Dalla Betta et al., NIMA 824 (2016) 386 and 388

Poly-Si filling and 2nd DRIE

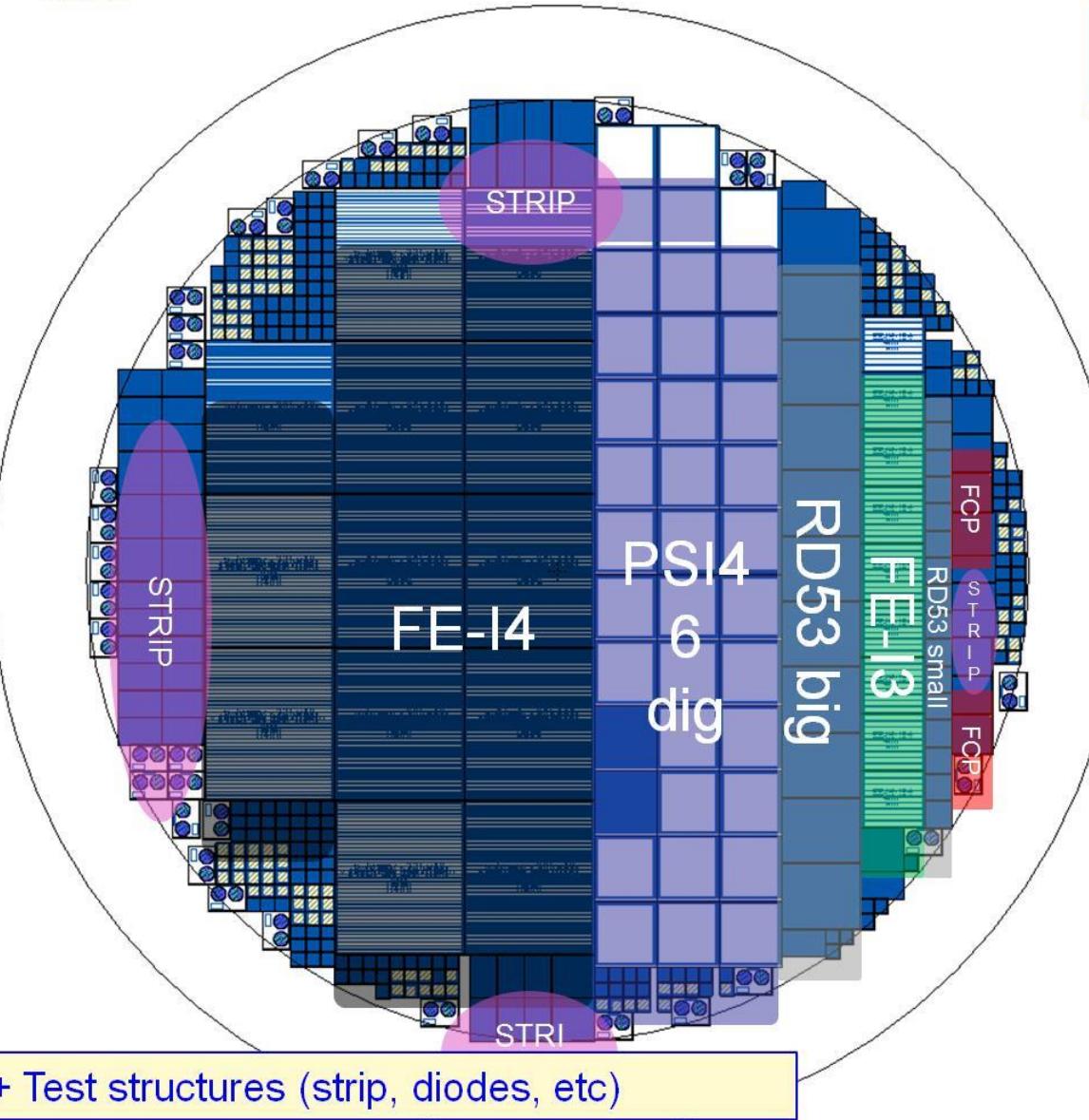
Reducing the hole diameter with poly-Si deposition
to ease the 2nd DRIE on the same wafer side



First holes
partially filled
with poly-Si



3D Pixel Wafer Layout



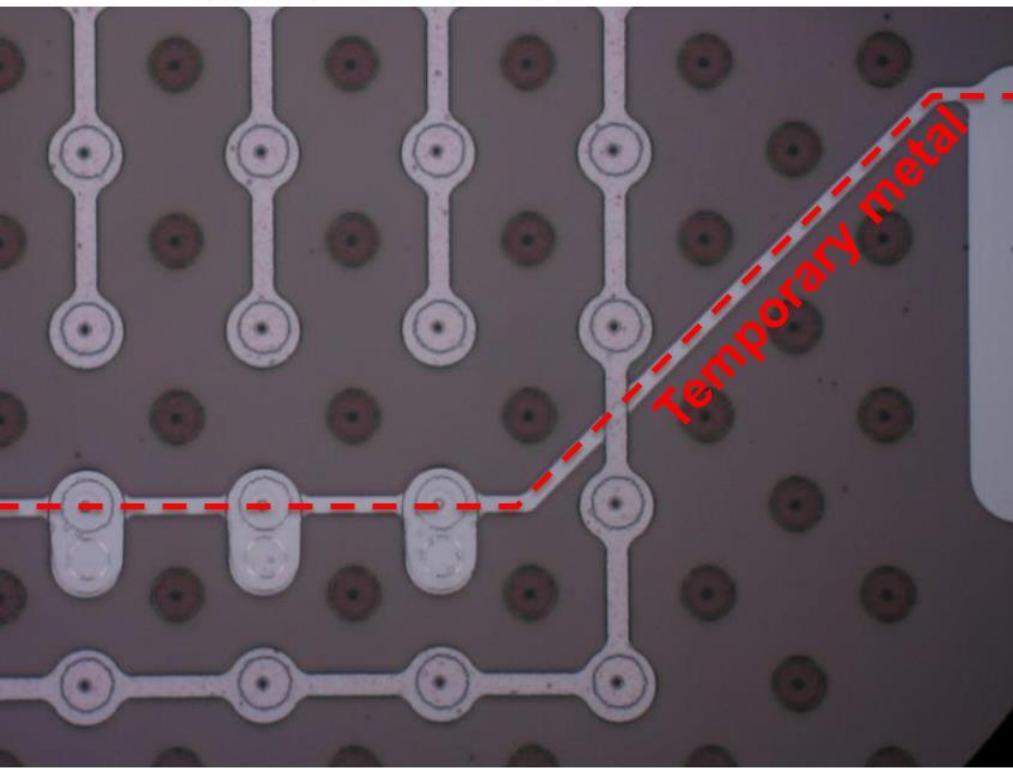
Many different pixel geometries and pitch variations:

- **FE-I4**
 - 50 x 250 (2E) std
 - 50 x 50 (1E)
 - 25 x 100 (1E and 2E)
 - 25 x 500 (1E)
- **FE-I3**
 - 50 x 50 (1E)
 - 25 x 100 (1E and 2E)
- **PSI46dig**
 - 100 x 150 (2E and 3E) std
 - 50 x 50 (1E and 2E)
 - 50 x 100, 100 x 100 (2E + 4E)
 - 50 x 100, 100 X 150 (2E + 6E)
 - 25 x 100 (1E and 2E)
- **FCP**
 - 30 x 100 (1E)
- **RD53/CHIPIX65**
 - 50 x 50 (1E)
 - 25 x 100 (1E)
 - 25 x 100 (2E)

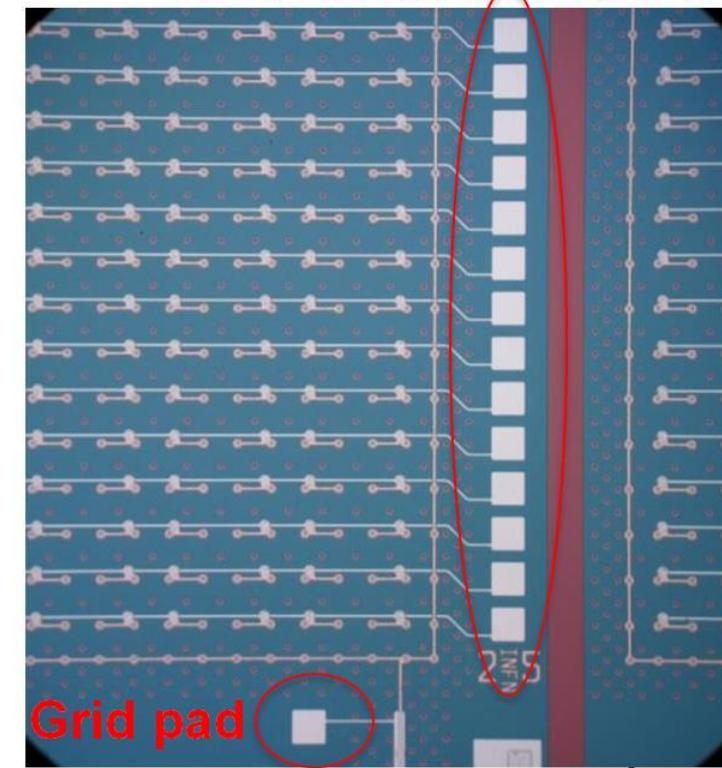
Temporary metal tests on pixels

- Rows of pixels are shorted by temporary metal for electrical tests on wafer (more effective monitoring of process defects)
- Total currents are obtained by the sum of all single-row and grid currents

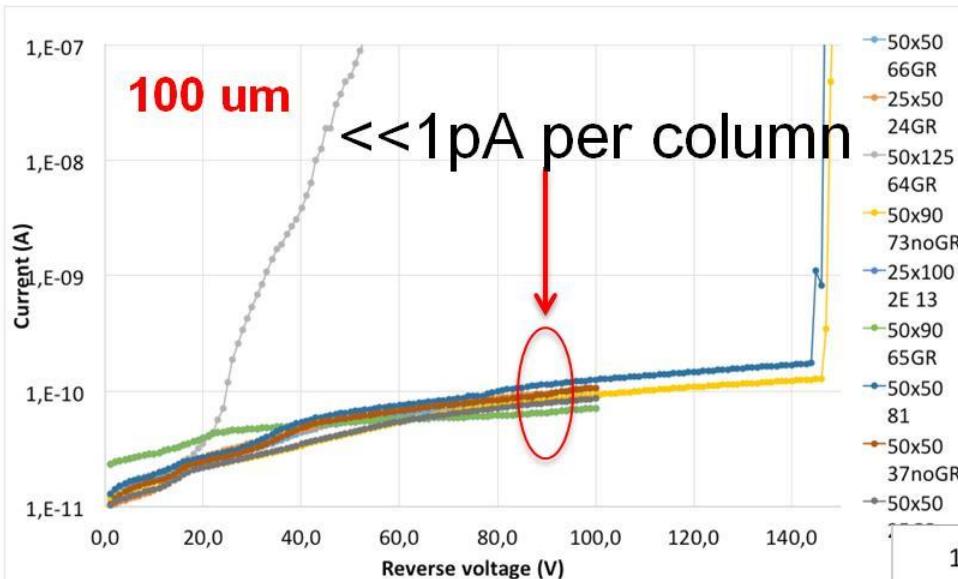
Permanent metal



Temporary metal pads



Test results: 3D diodes



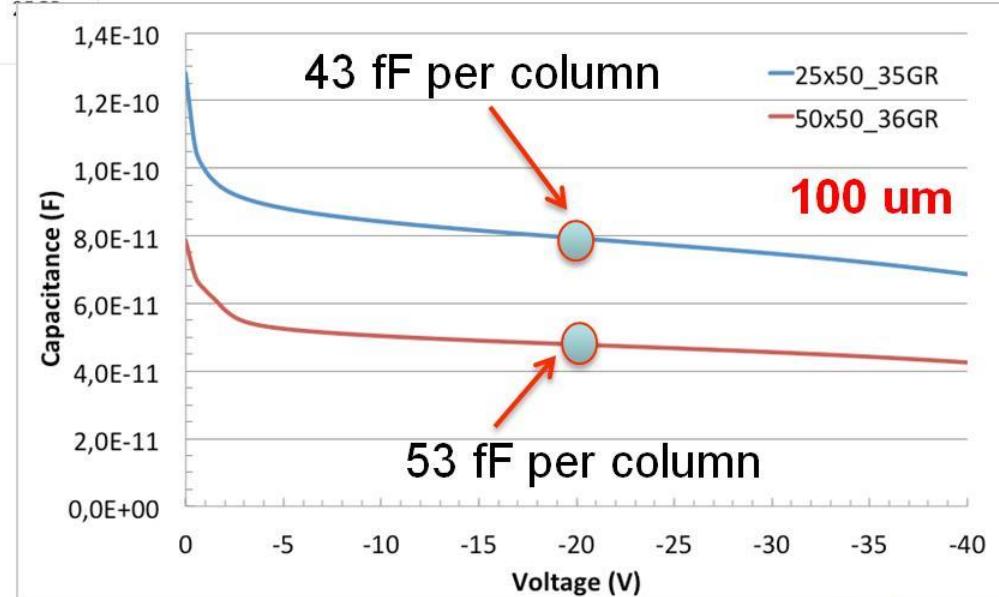
3D diodes also used for irradiation tests, devices already sent to:

- Sandia and JSI (neutrons)
 - Los Alamos (protons)

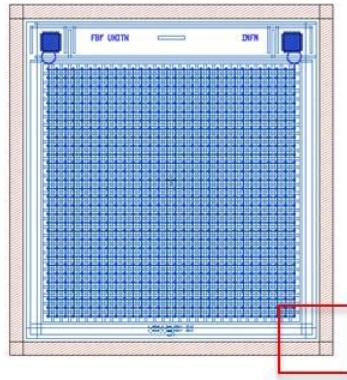
Good electrical figures:

- low depletion voltage
 - low leakage current
 - high breakdown voltage

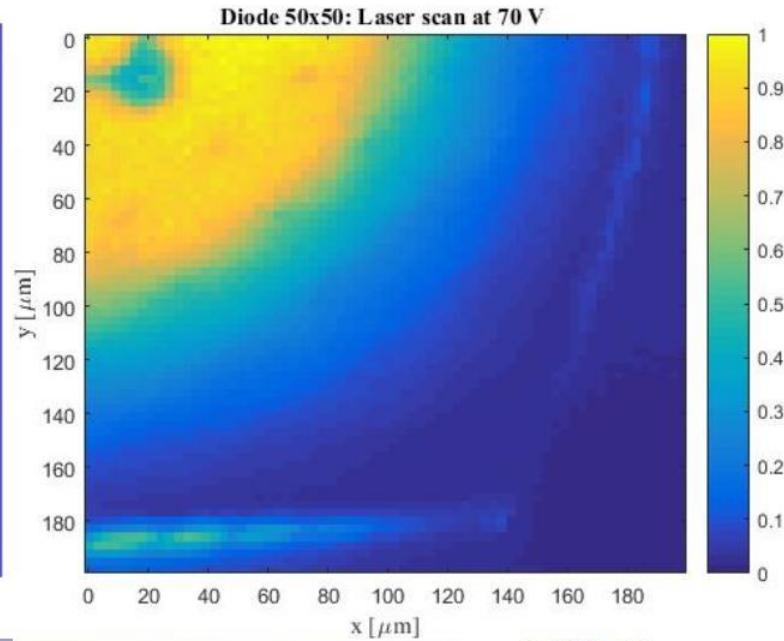
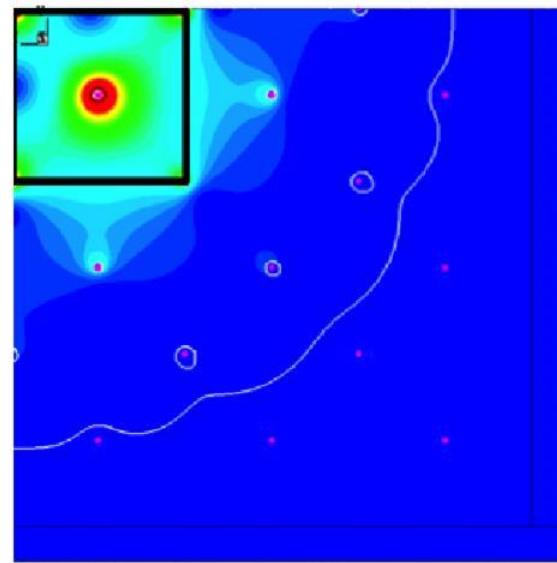
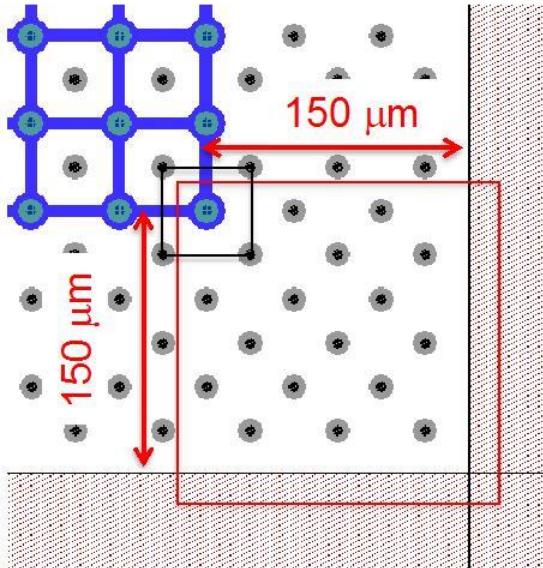
in good agreement with simulations



Slim edge laser test



- Slim edge based on multiple ohmic columns
- Safe operation of 3D diode ($50 \mu\text{m} \times 50 \mu\text{m}$ design) tested with position resolved laser system
- Extension of the depleted volume at the corner is $\sim 80 \mu\text{m}$ at 70V, in good agreement with simulations





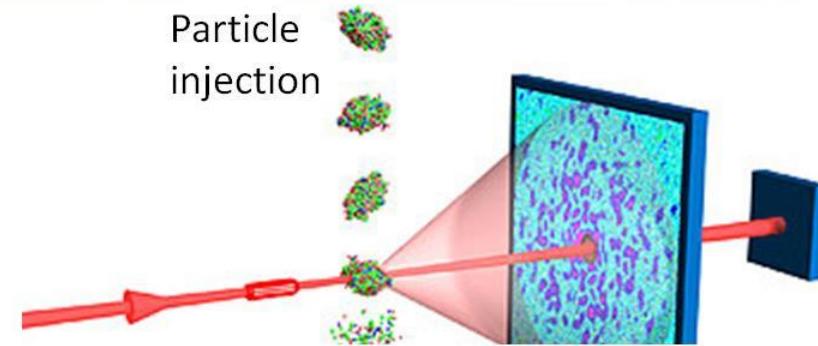
Outline

- Introduction
- APiX: Geiger-mode avalanche pixel detectors
for ionizing particles
- Low Gain Avalanche Detectors
- 3D detectors
- PixFEL: a pixelated detector for application at
future XFEL facilities

Characteristics of X-ray IS for FEL

Detection of diffraction patterns with a **large pixel camera**.

- FEL pulse repetition rate
 - Eu-XFEL: burst (2700 pulses at **4.5MHz**)
 - LCLSII: continuous (up to **1MHz**)
- Focal plane signal intensity:
 - From single photon to **10^4 ph/pixel/pulse**
- Radiation hardness:
 - 10 MGy – **1 GGy**, 3 years operation
- Pixel size: 20 - 700 μm ,
 - depending on distance and angle
- **Large area coverage:**
 - multiple tiles



Ultra-high frame rate



High dynamic range

VERY Rad-hard

High spatial resolution



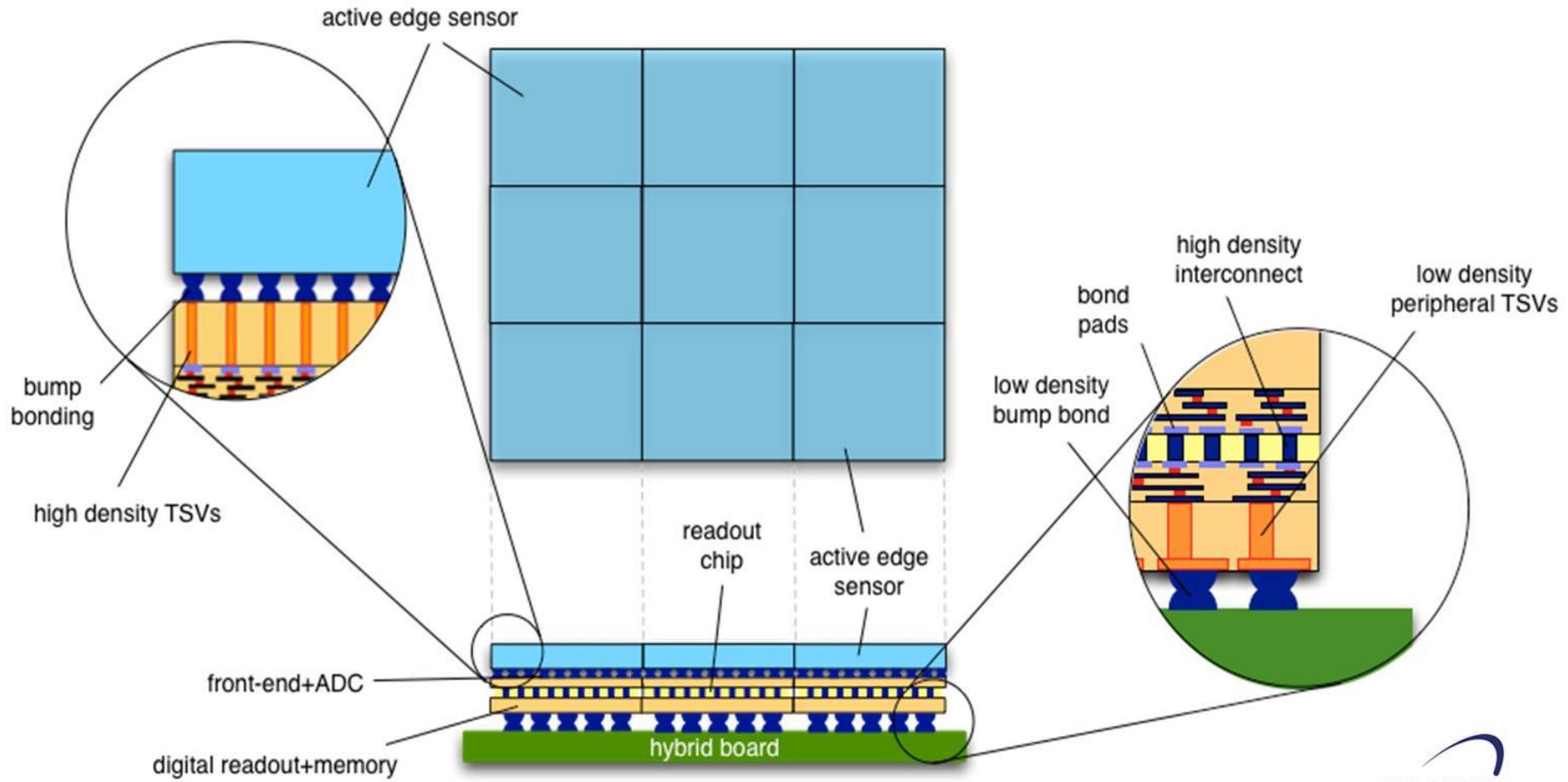
Detector specifications

- Tiling dead space < 5%
- **Pixel size:** **100μm**
- Photon energy (programmable) 1keV or 10keV
- Dynamic range **1 – 10⁴ photons**
- Frame rate: **4.5 Mfps** (burst)
- ADC in-pixel
- In-pixel digital memory 1000 frames
- Radiation hardness (3 years operation) up to **1GGy**

Detector structure

3-layer structure:

CMOS 65nm (analog + digital tiers)
custom high resistivity silicon (detectors)





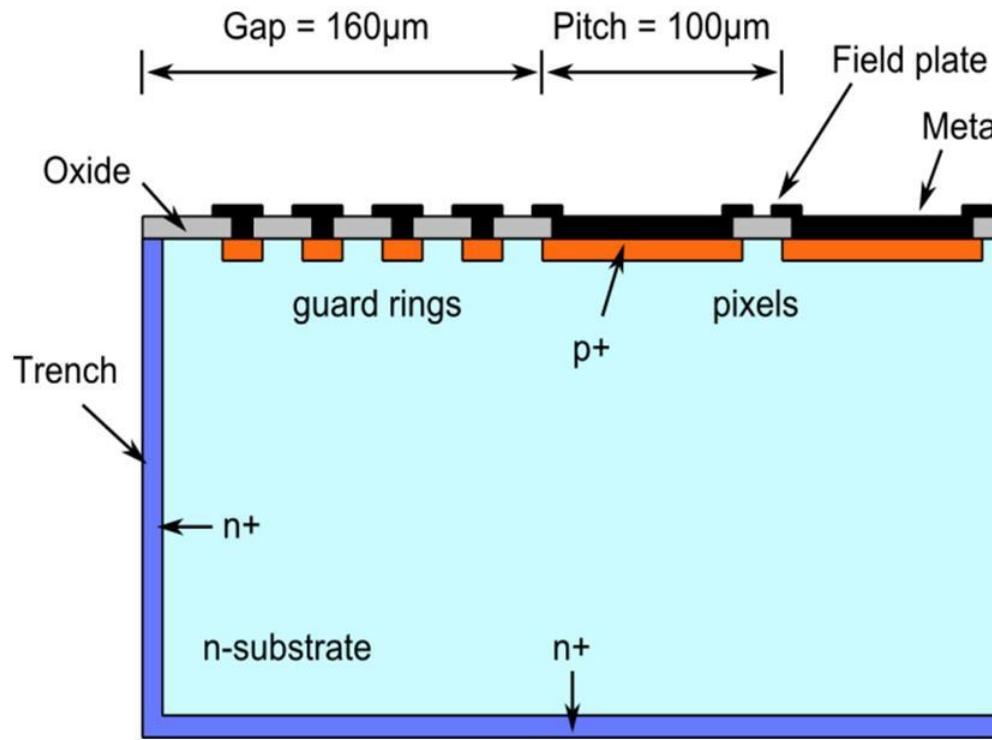
Silicon sensor - characteristics

- High **efficiency** at 10 keV: → HR Si with 450um thickness
- Charge **collection time** < 50ns
- Mitigate **space-charge effect** for good MTF at high photon counts
- Minimum **dead area** → Active edge sensor
- Resistance to ionizing radiation (minimized Nox with 1GGy) → p-on-n Si

Silicon sensor - design

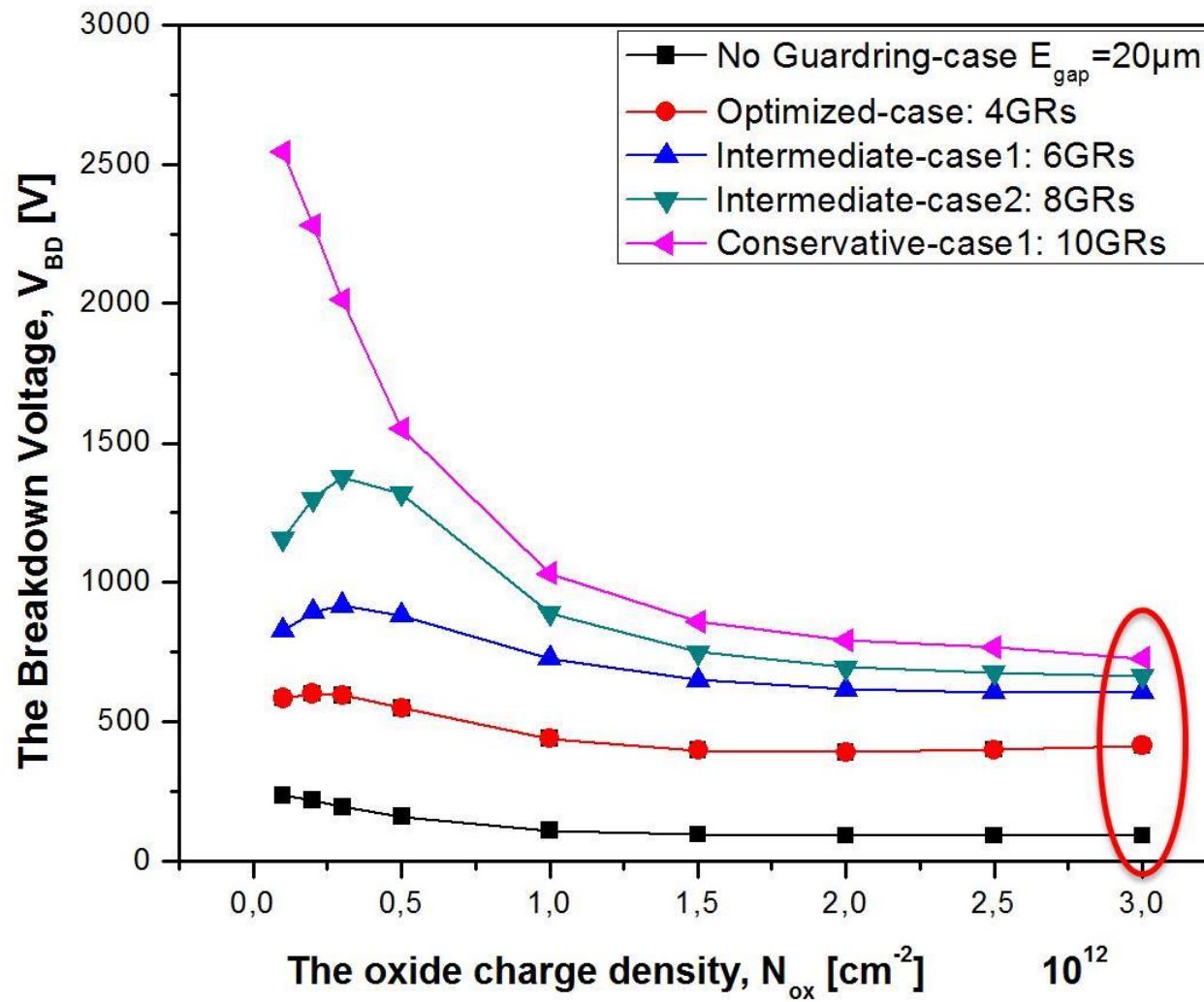
- More guard rings:
- 😊 Increased V_{BD}
 - 😢 Increases tiling dead area

Tradeoff: 4 guard rings: $V_{BD} > 400V$ at end-of-life ($N_{ox} = 3 \times 10^{12} \text{ cm}^{-2}$)



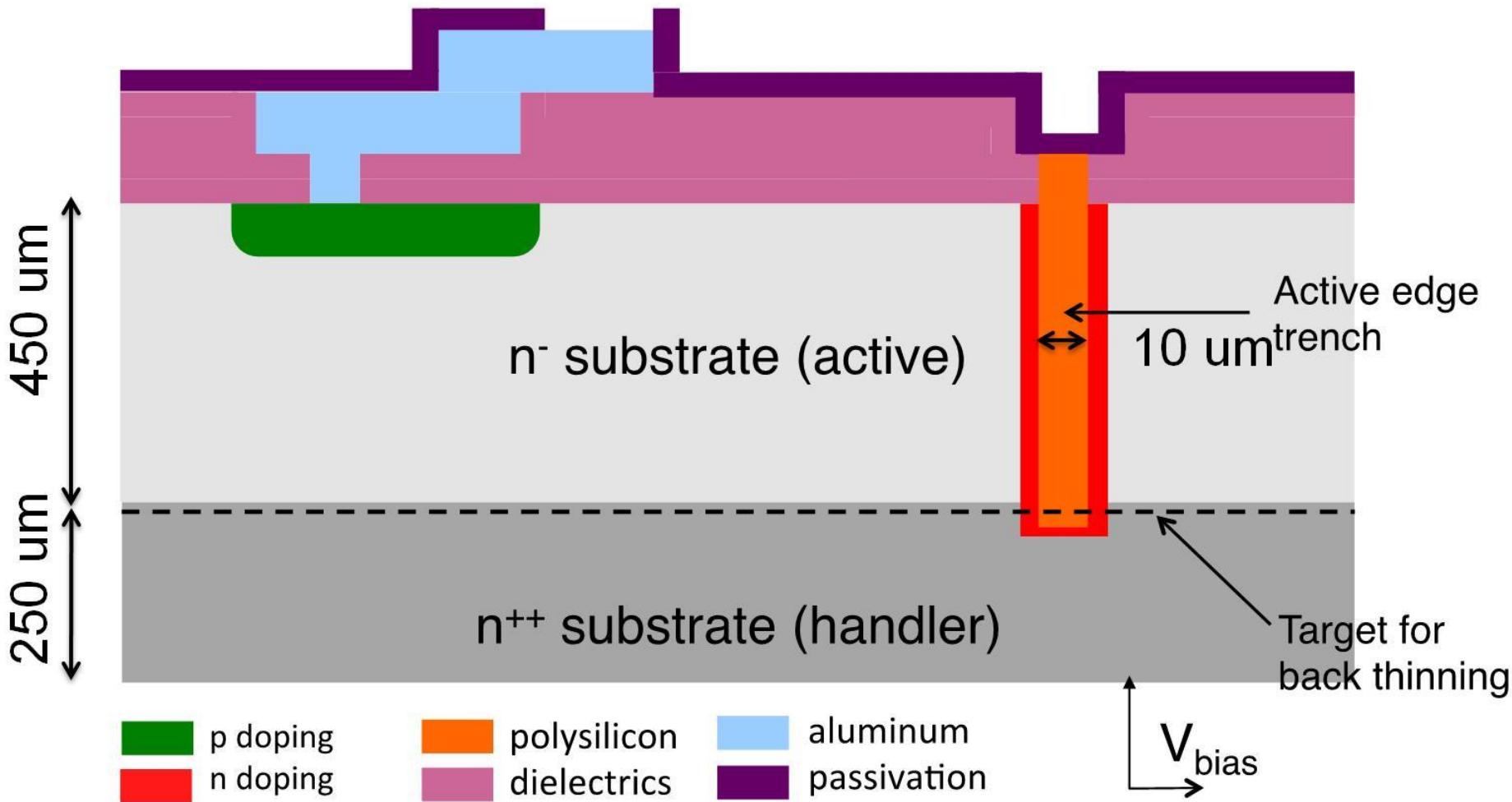
Simulated breakdown voltage

G.-F. Dalla Betta et al., PM2015(doi:10.1016/j.nima.2015.08.027)

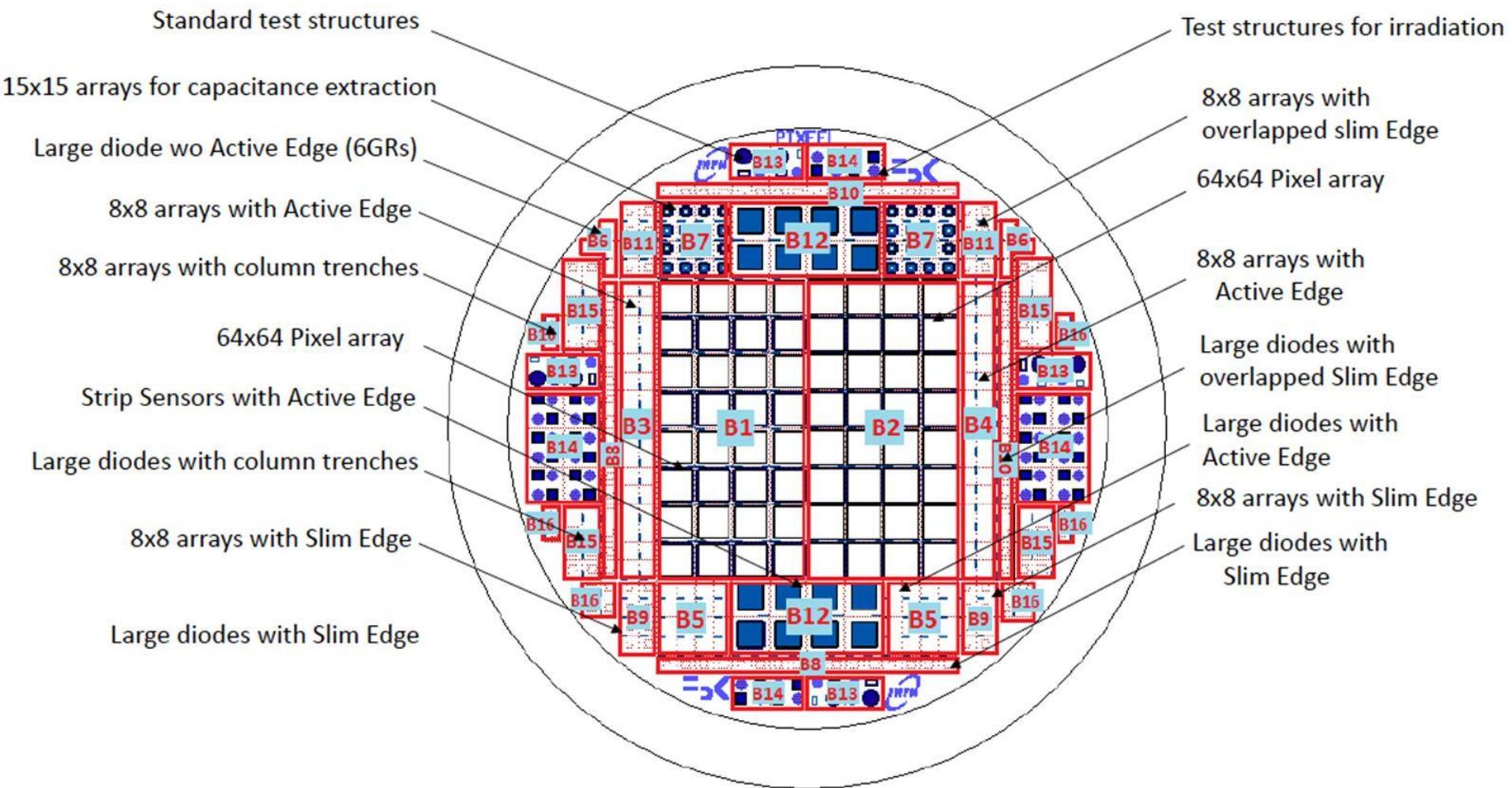


J. Zhang et al.,
JINST 7 (2012)
C12012.

Fabrication process @ FBK



Wafer layout



Etching deep trenches by DRIE

Aluminum mask

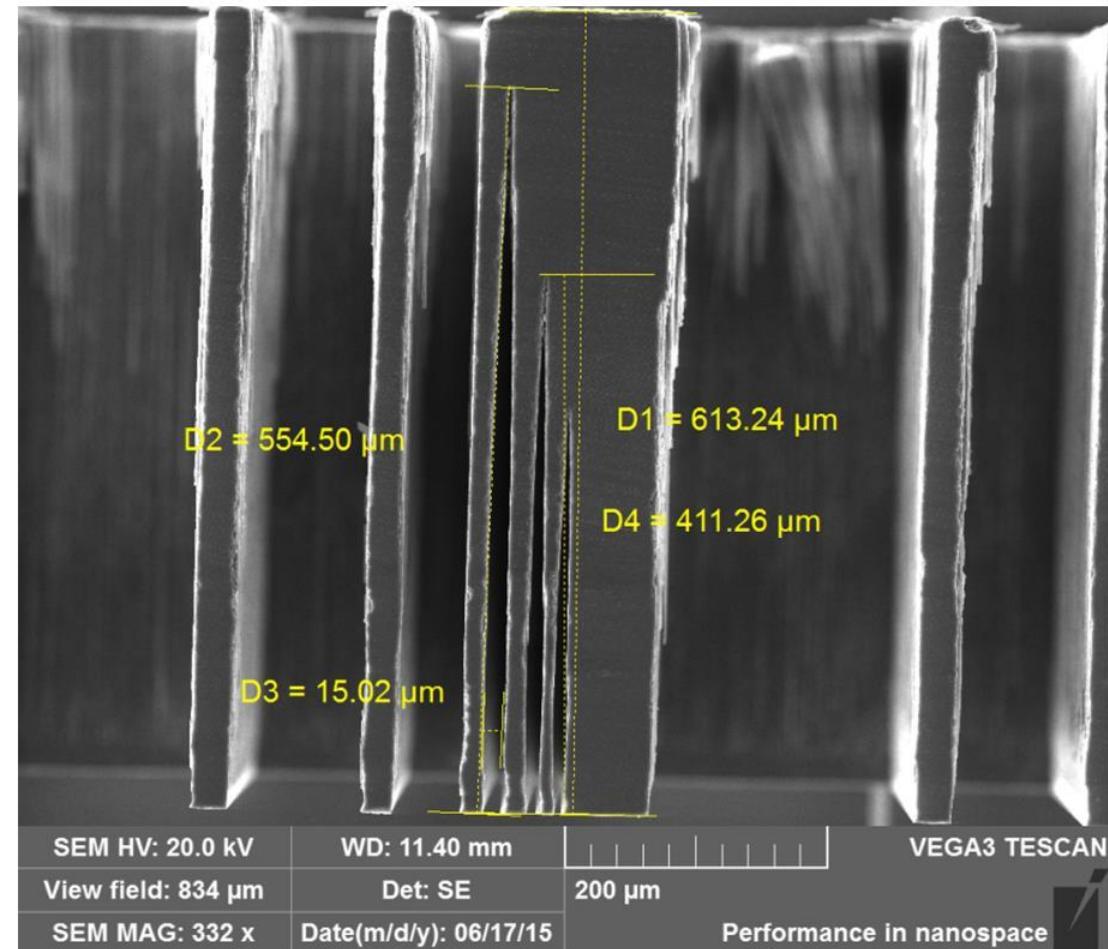
Width 6 μm (D4)

Depth >410 μm

Width 12 μm (D1)

Depth > 610 μm

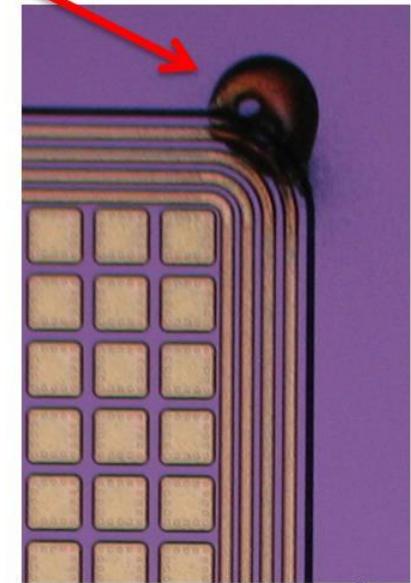
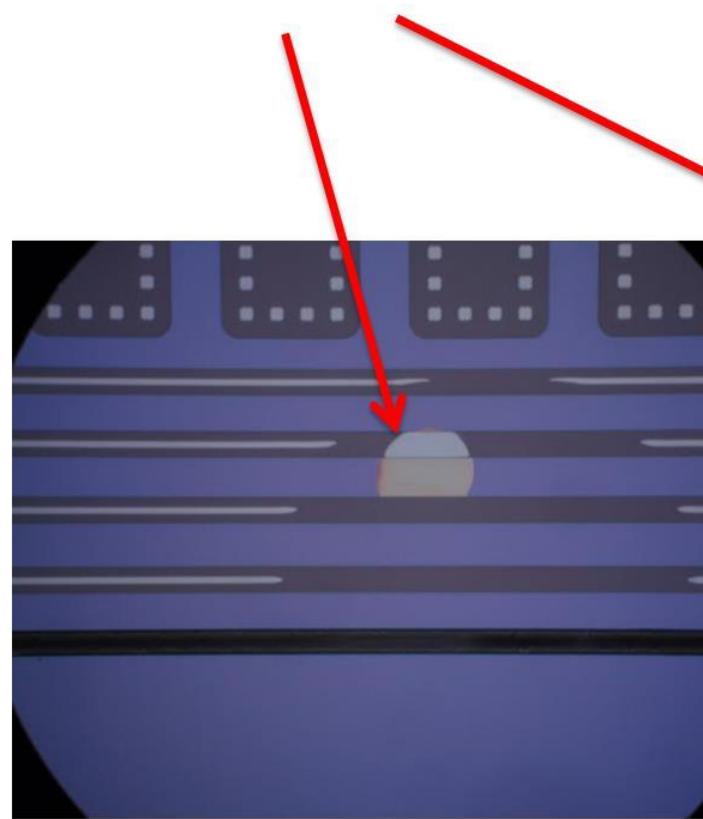
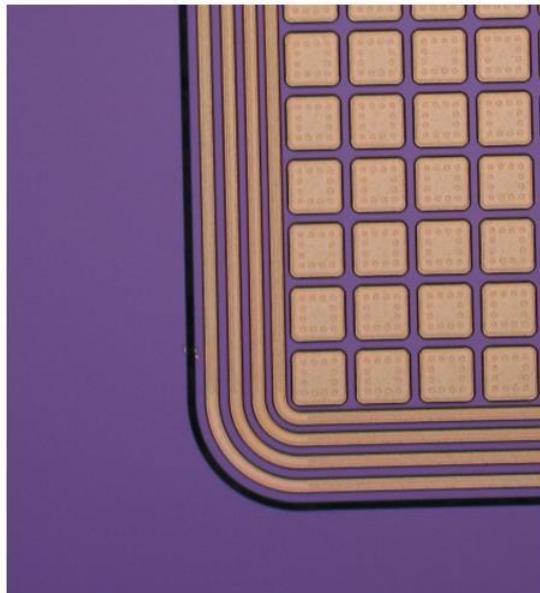
In case of larger width,
trenches are passing
through the wafer



The shape of the trench tip is a cleaving artifact

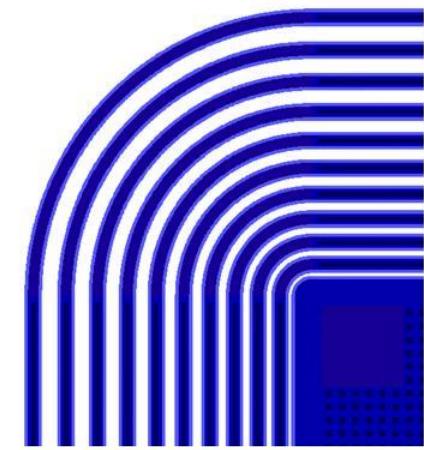
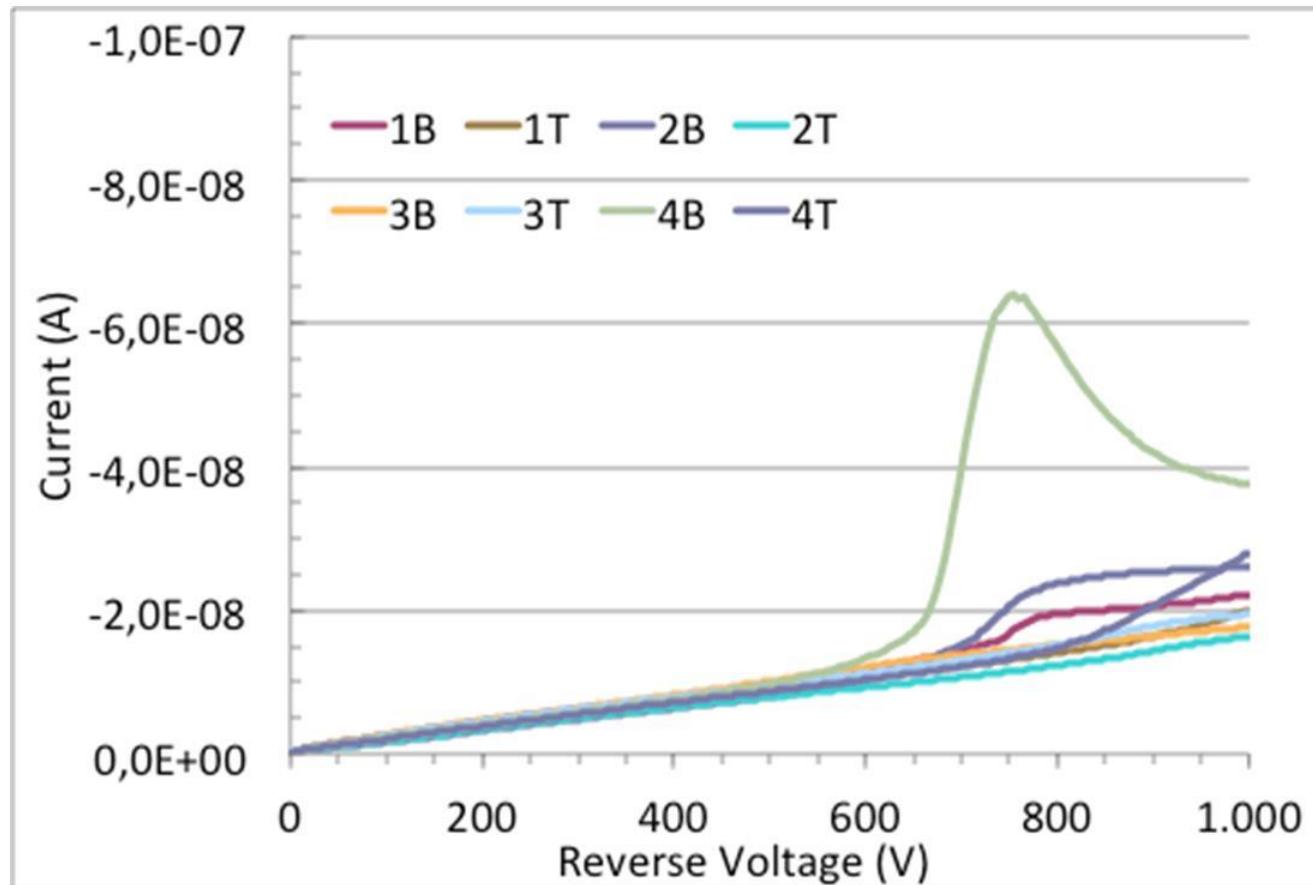
Defects at the edge

Trench size after poly-Si deposition is still too large:
difficult to obtain uniform resist coverage
defects close to the trenches



Reference device

Diode without active edge – 10 rings

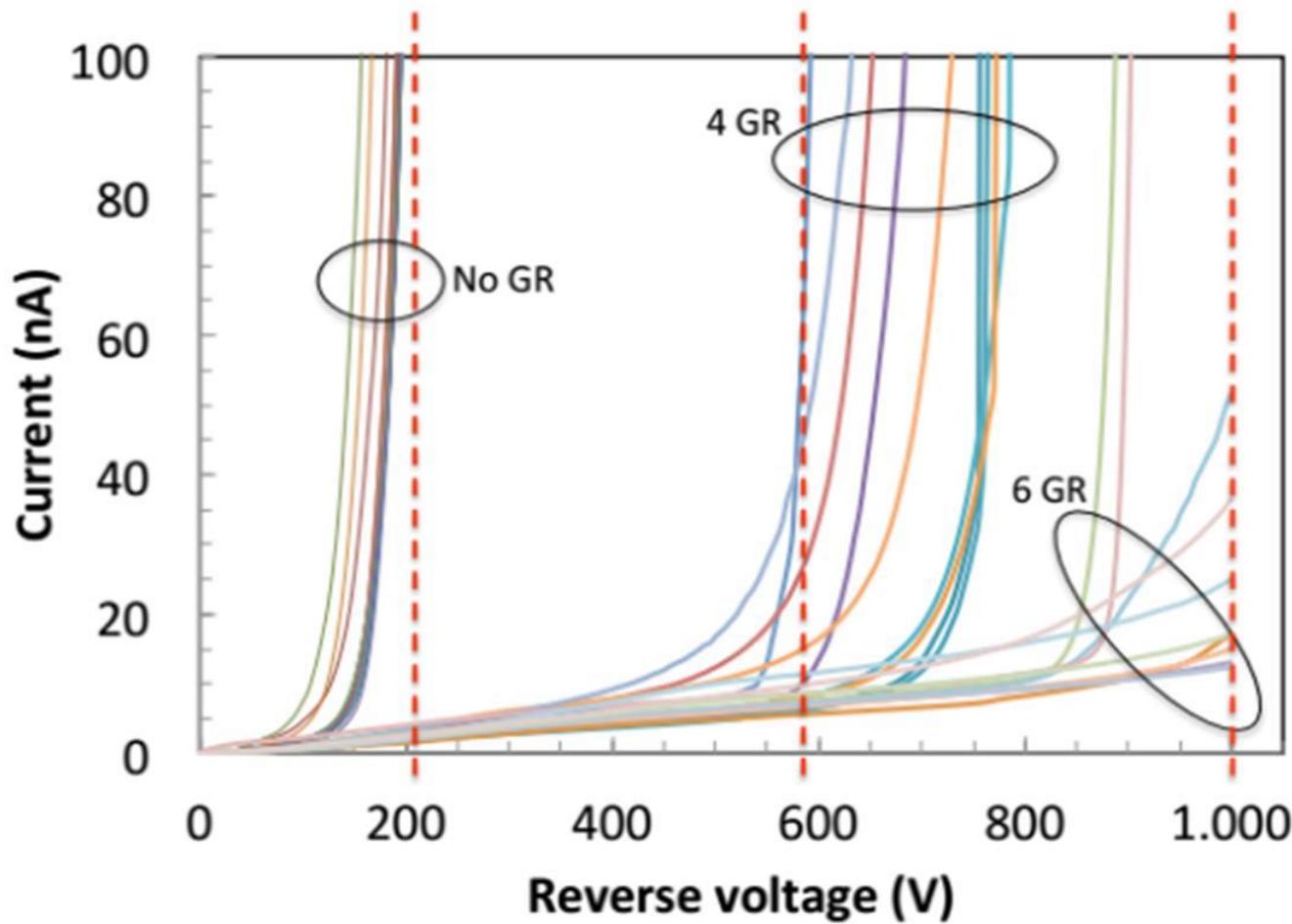


Simulated value
was ~1500V

All diodes: $V_{BD} > 1000$ V (setup limited)

Guard ring number

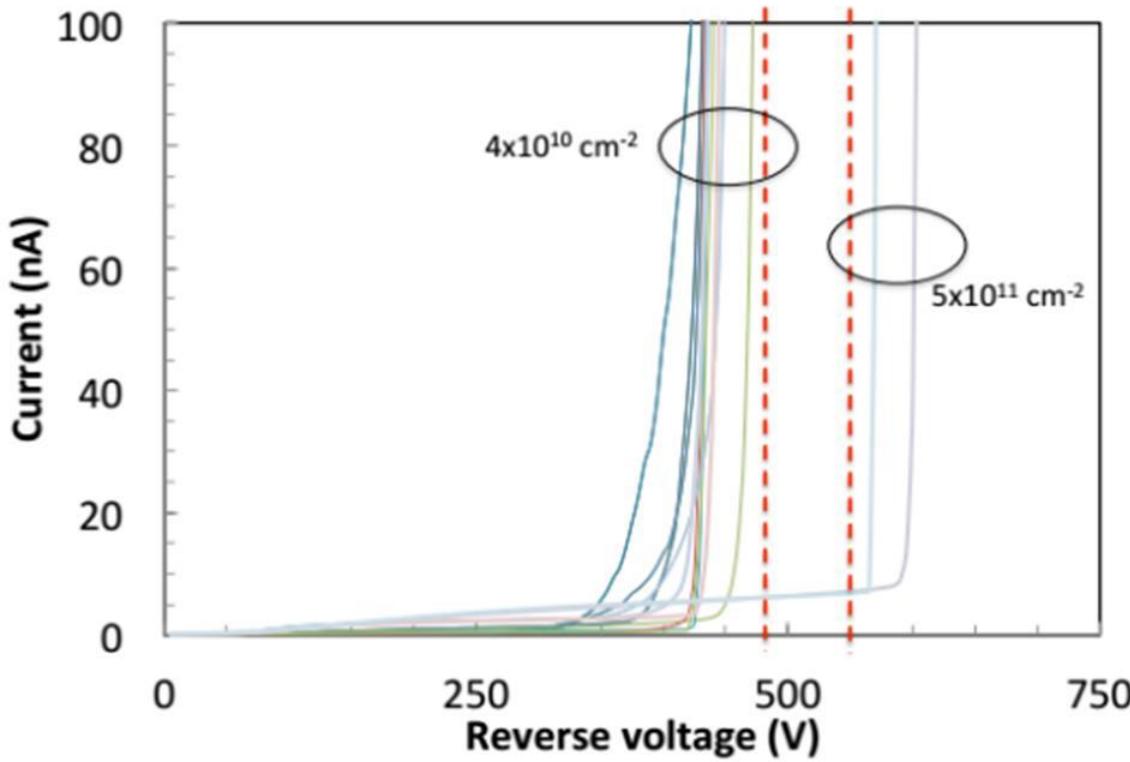
Good agreement with TCAD simulations



Active edge sensors – 4 guard rings

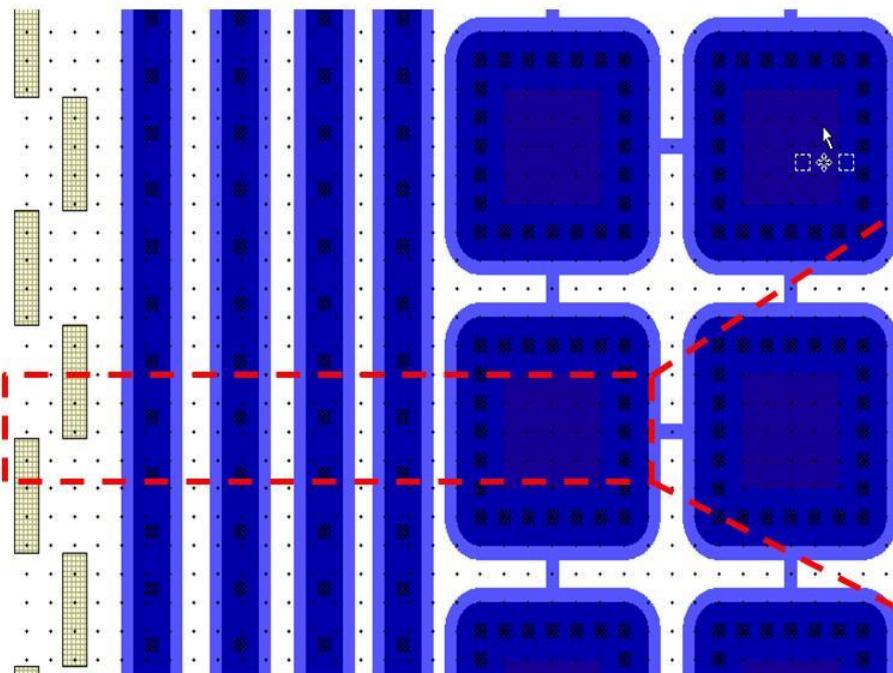
Effect of interface oxide charge:

- First wafer: $N_{ox} = 5 \times 10^{11} \text{ cm}^{-2}$
- Next wafers: additional poly-Si and reoxidation,
 $N_{ox} = 4 \times 10^{10} \text{ cm}^{-2}$



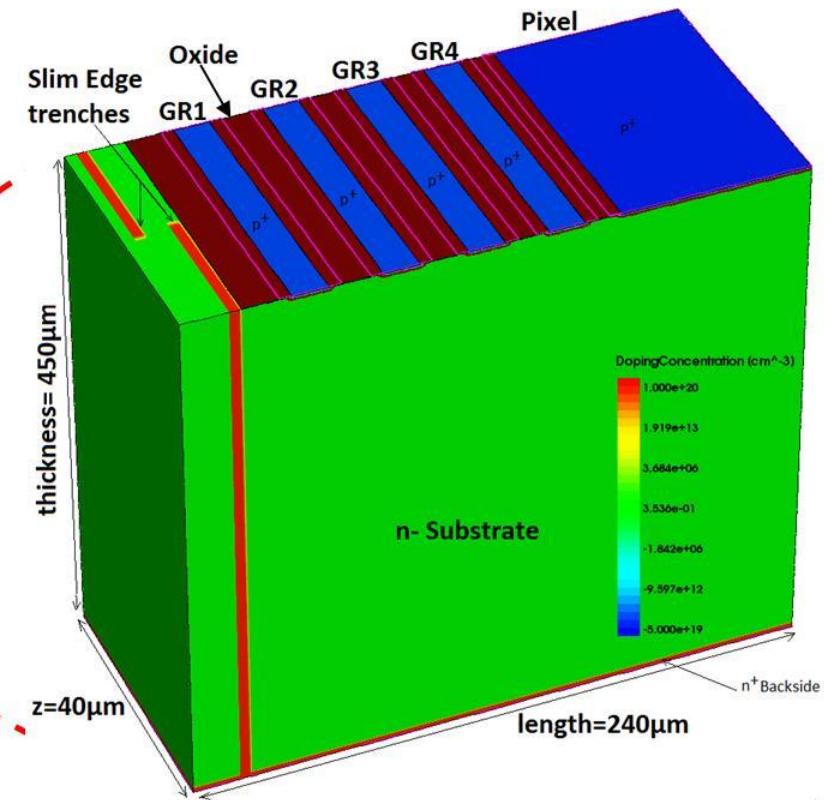
The Slim Edge approach (1)

Structure Layout



Segmented trench

TCAD 3D structure

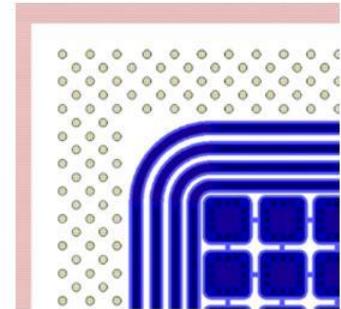


The Slim Edge approach (2)

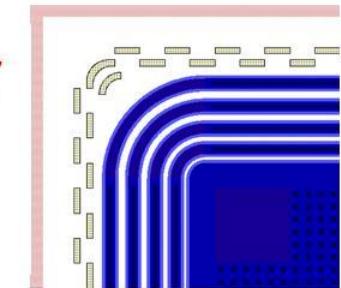
Advantages:

- Get rid of the support wafer
simplified process
- Entrance window for low energy
X-ray can be optimized
- Lower risk of defects at the edge
higher yield
- Same breakdown voltage

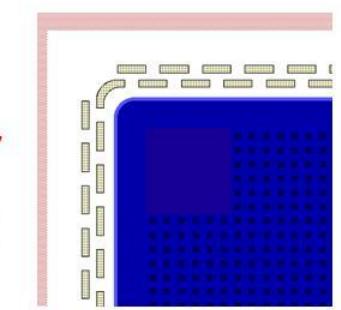
Circular



Rectangular
without
overlap



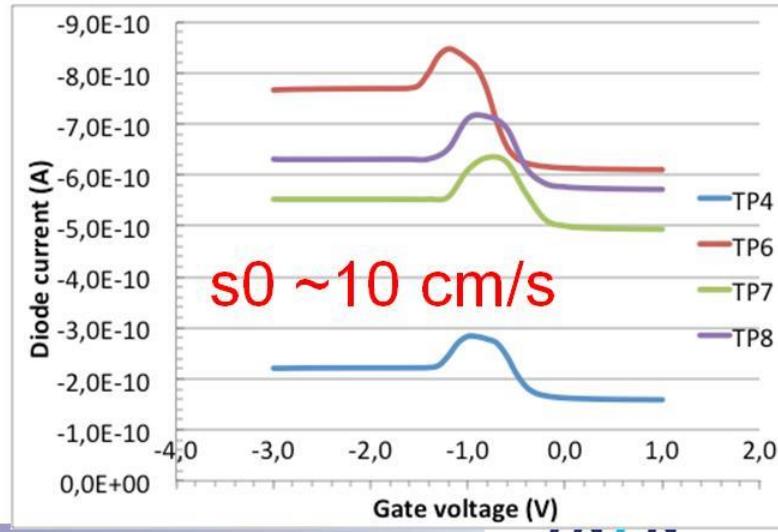
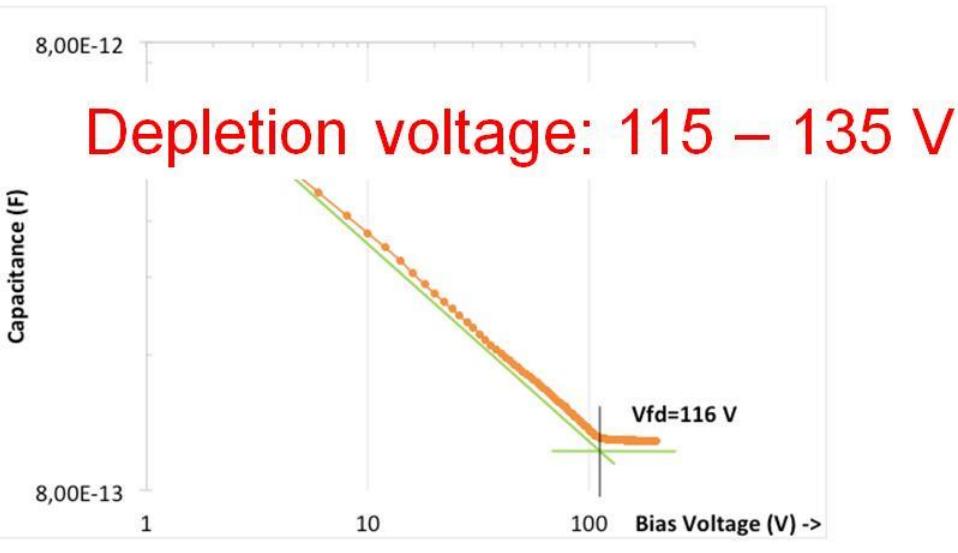
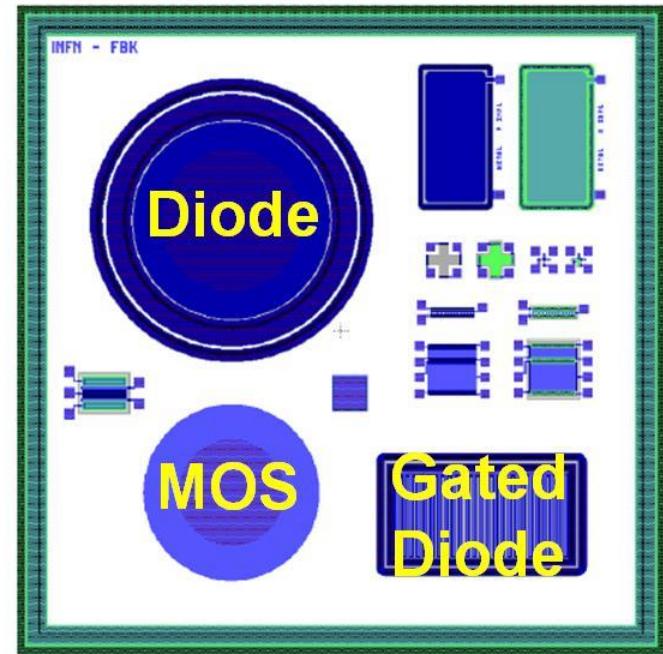
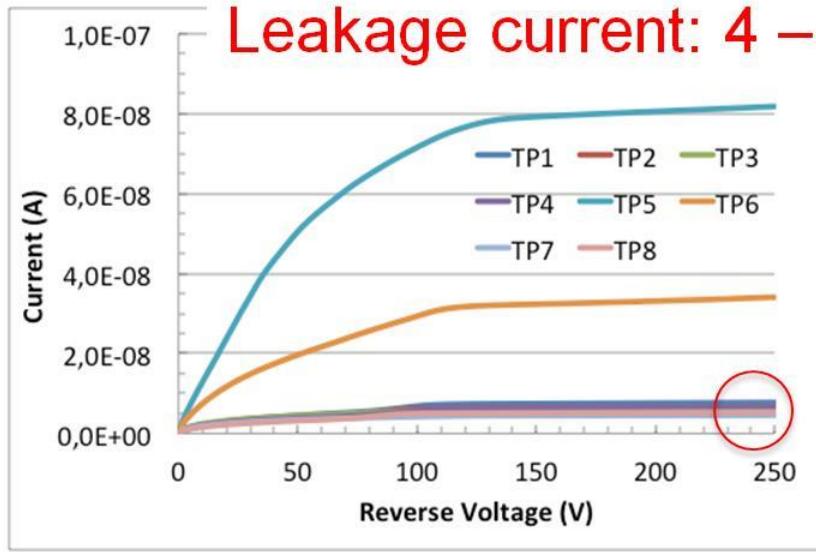
Rectangular
with overlap



Disadvantages:

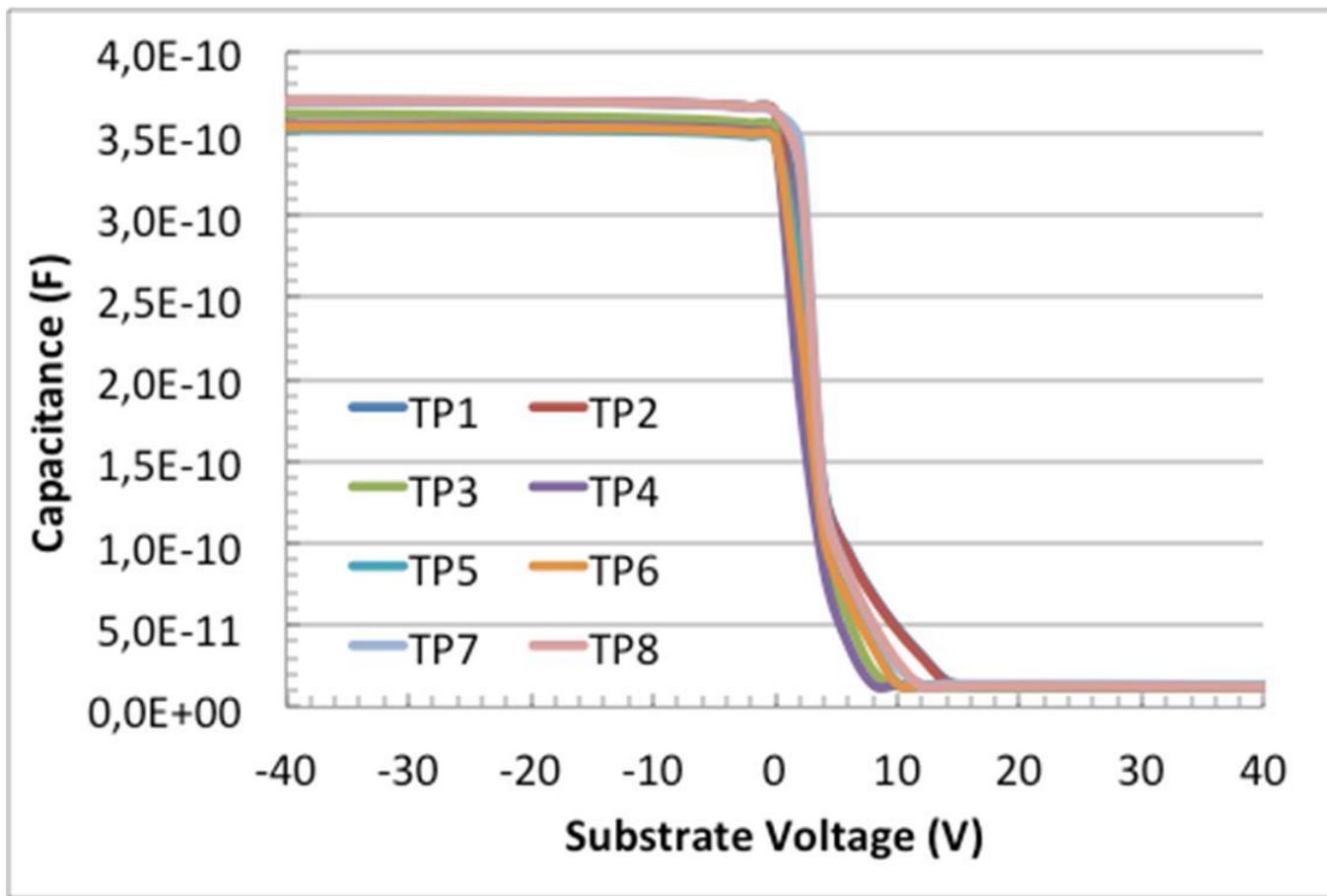
- Additional dead space at
the border

Process monitoring



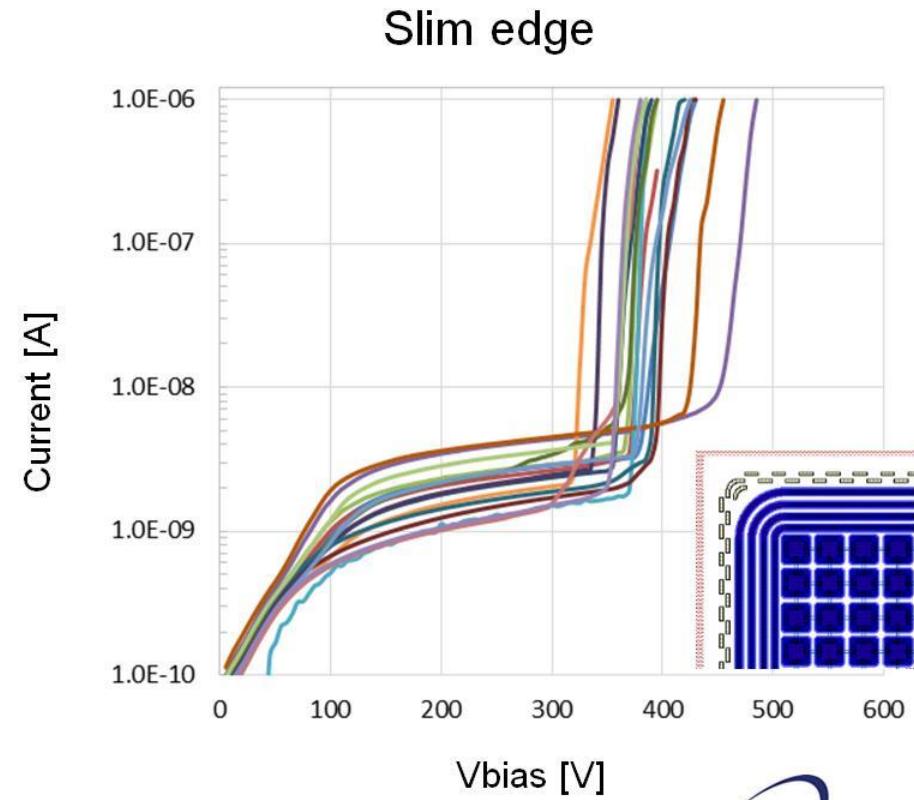
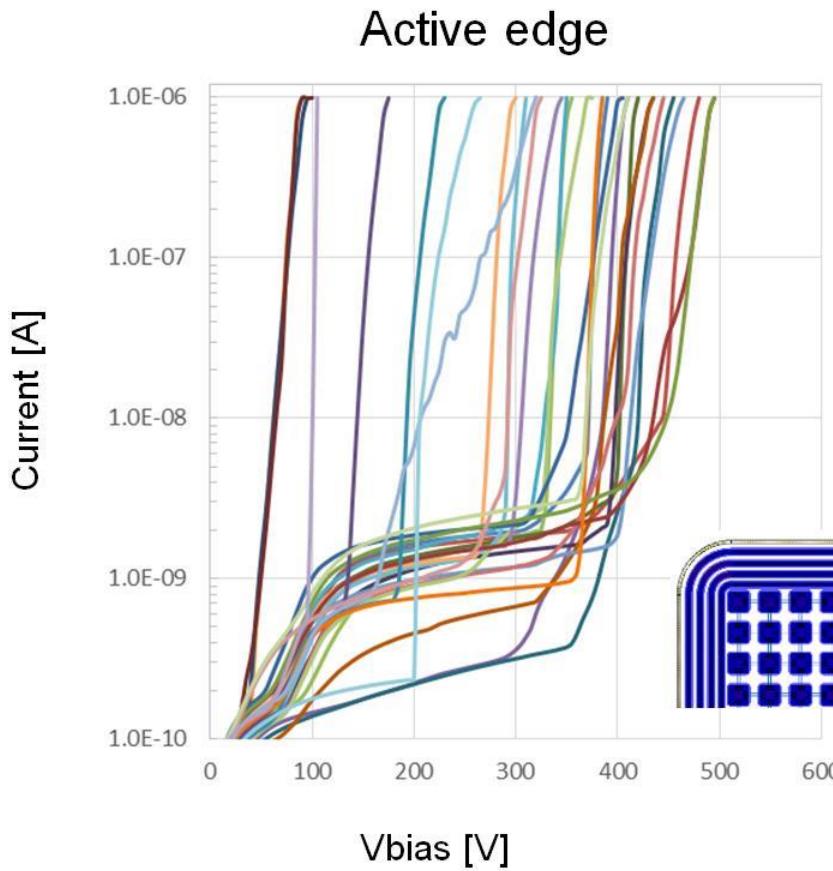
Oxide thickness and charge

- Oxide thickness: 300 ± 8 nm
- N_{OX} in the range $4 - 7 \times 10^{11} \text{ cm}^{-2}$



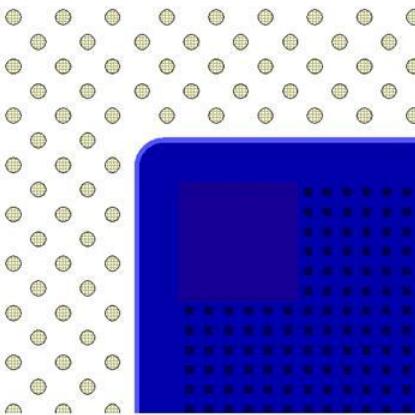
Slim-edge: breakdown voltage

Slim-edge sensors: reduced defectivity

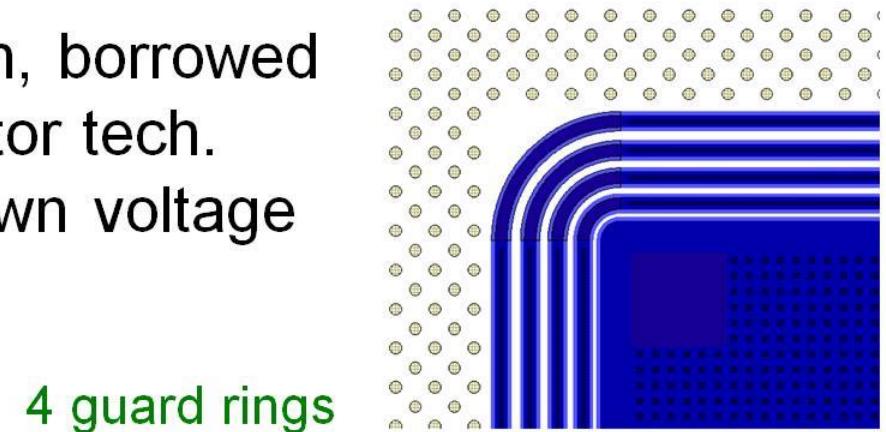
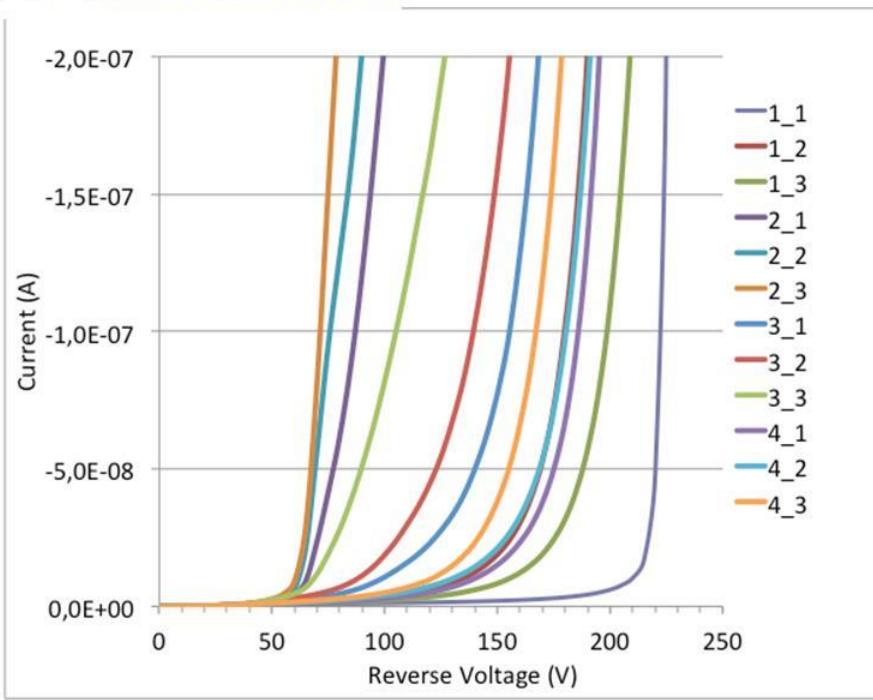


Circular columns

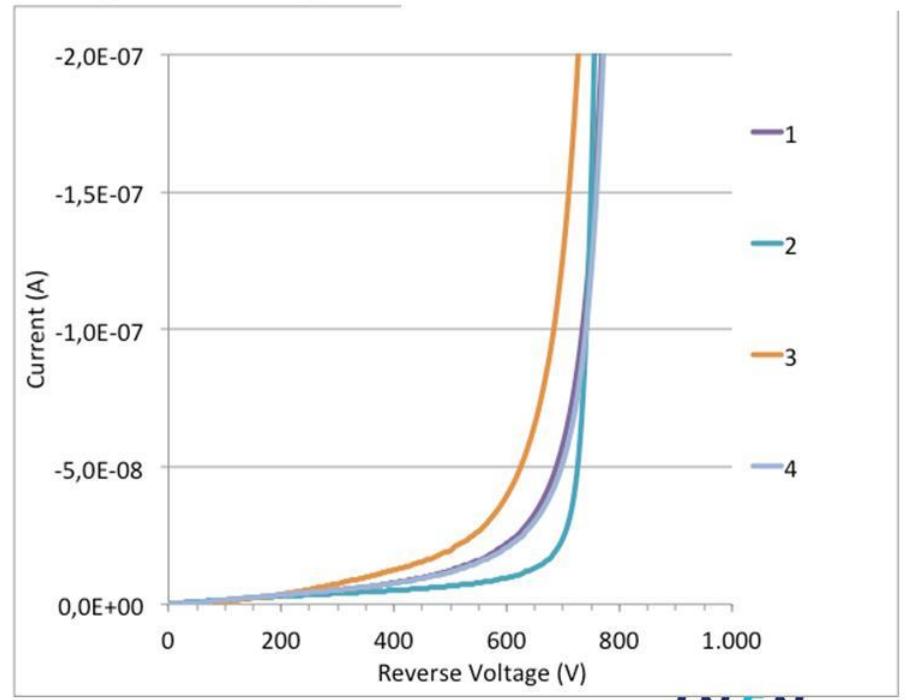
- Simple solution, borrowed from 3D detector tech.
- Good breakdown voltage



No guard rings



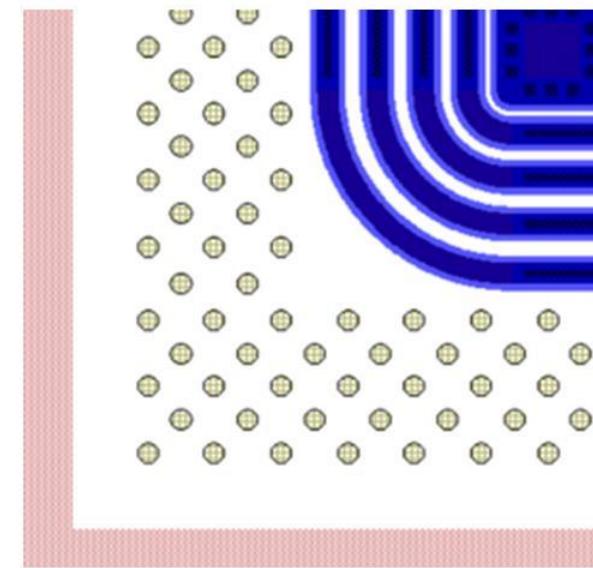
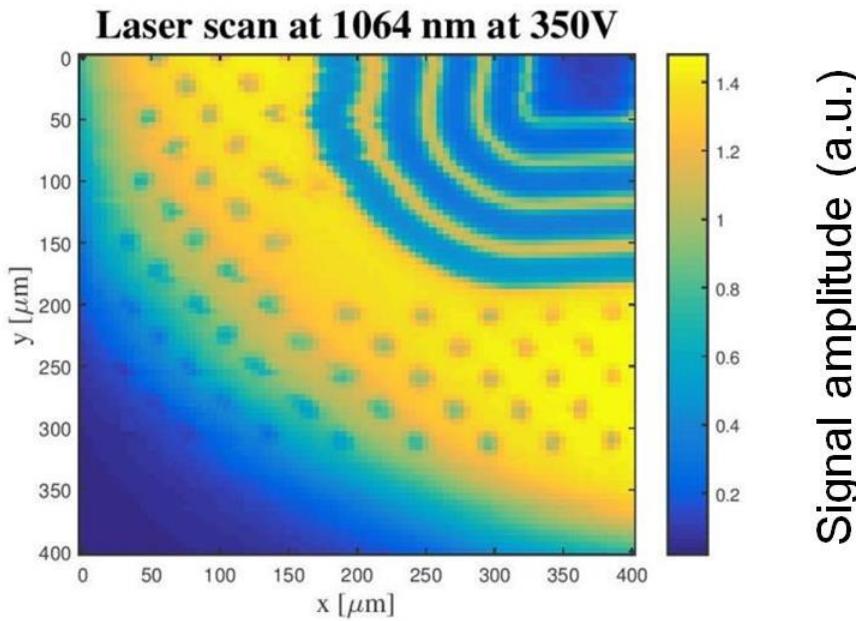
4 guard rings



Circular column: charge collection

Circular column slim edges:

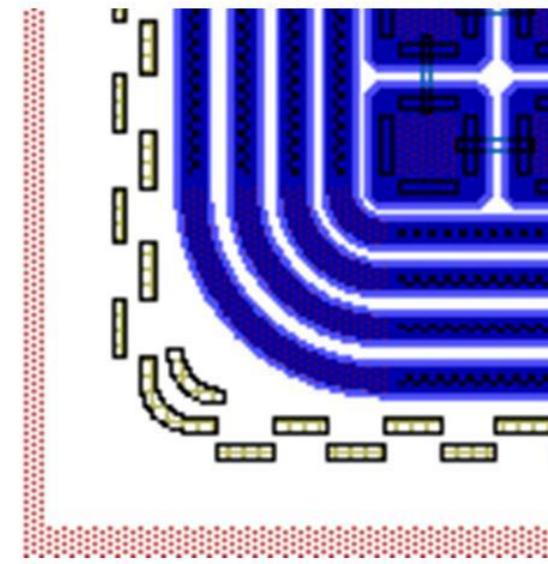
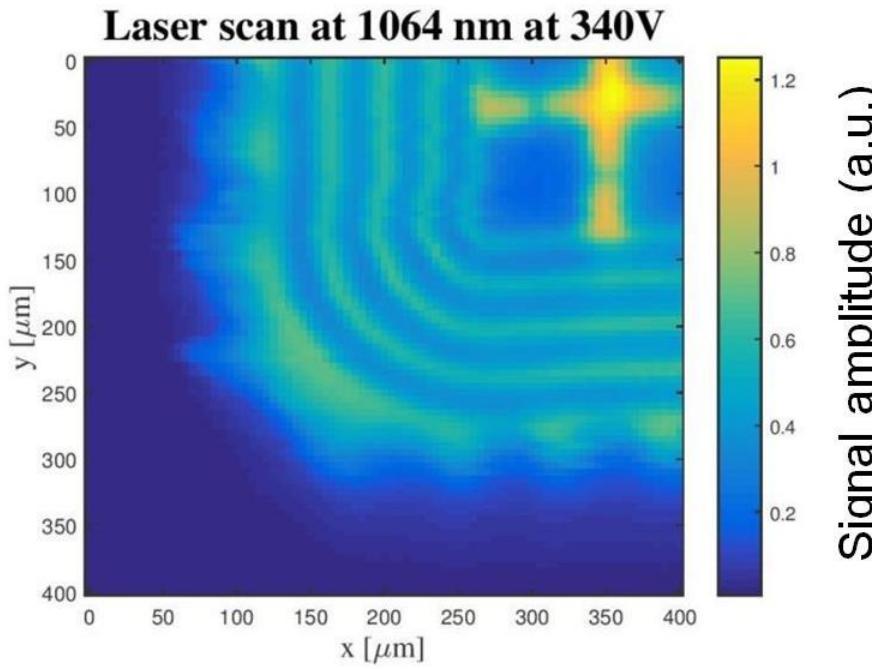
- **Signal** generated outside the trenches is collected:
- Columns do not stop completely the depletion region at high voltage



Rectangular trenches: charge coll.

Segmented-trench slim edges:

- **Signal generated outside the trenches is blocked:**
- Sensor can be cut very close to trenches: ~ 10s of micron



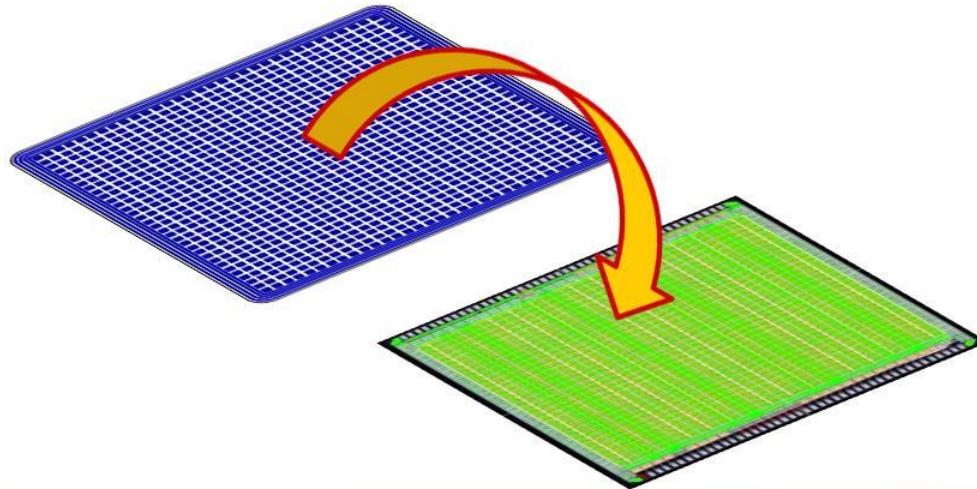


Conclusions

- The **first batch of devices** was fabricated at FBK on 450+250 um SiSi DWB, 6" wafers
- Continuous trenches: high density of **defects**
- **4-GRs**: breakdown voltage close to TCAD sim.
- **Slim edge samples** :
 - high yield
 - Same breakdown voltage as active edges
 - Very promising option for future developments
(simple process + optimized entrance window)

On-going - future work

- Functional sensor characterization with X-rays
- Characterization of radiation hardness
- Bump bonding of 32x32 pixel sensor to 32x32 ROIC
- Development of slim edge technology





Thank you