The status and the perspectives of the silicon 3D and 4D pixel detectors

Part 1

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V Seminario Nazionale Sensori Innovativi (SNRI2016)

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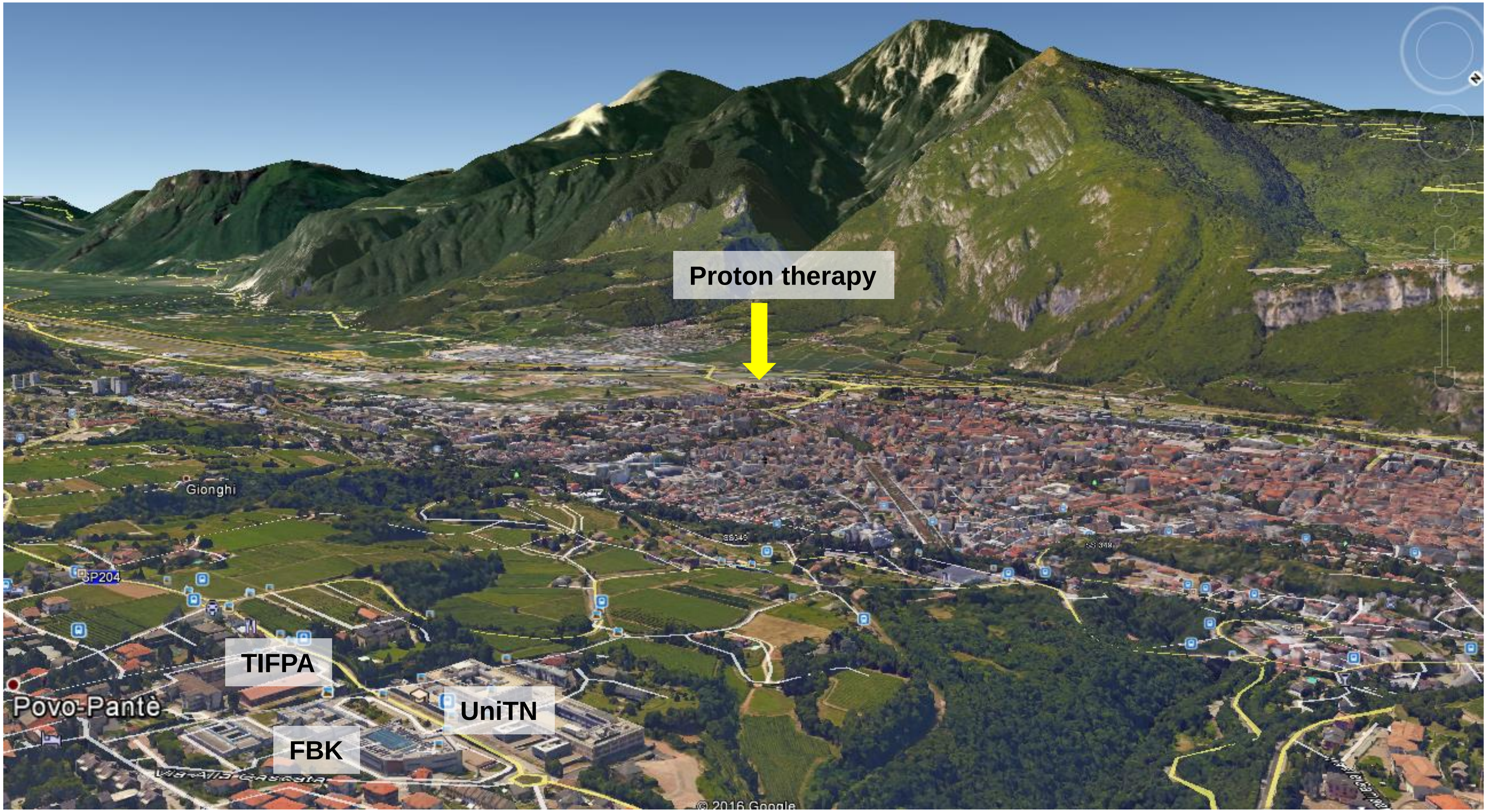
Research on silicon detectors in Trento


Proton therapy
Gionghi
SP204
TIFPA
Povo-Pantè
UniTN
FBK
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Outline

- Introduction
- APiX: Geiger-mode avalanche pixel detectors for ionizing particles
- Low Gain Avalanche Detectors
- 3D detectors
- PixFEL: pixelated active-edge detector for application at future XFEL facilities

Acknowledgements

APiX2: "Development of an Avalanche Pixel Sensor for tracking applications", funded by **INFN**
Project coordinator: Pier Simone Marrocchesi

UFSD: "Ultra Fast Silicon Detectors", funded by **INFN, ERC, RD50**
Project coordinator: Nicolò Cartiglia

3D detectors: funded by **INFN, RD50, AIDA2020**
Reference person: Gian-Franco Dalla Betta

PixFEL: "Enabling technologies, building blocks and architectures for advanced X-ray pixel cameras at FELs", funded by **INFN**
Project coordinator: Lodovico Ratti

Much of the material contained in these slides have been kindly shared by Nicolò Cartiglia, Giovanni Paternoster and Gian-Franco Dalla Betta

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Semiconductor detectors

Tighter specification for silicon sensors in future experiments (not only LHC!):

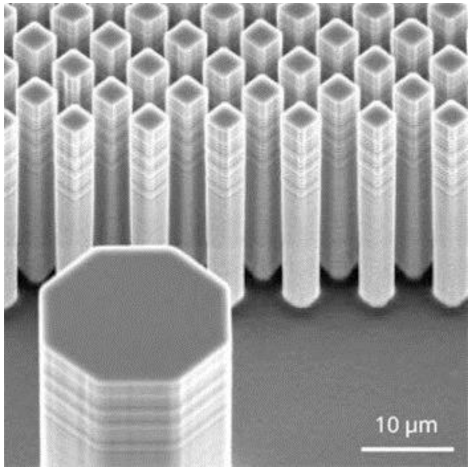
- Radiation tolerance: high dose – high fluence
- High spatial resolution
- High event rate/ frame rate
- Low power consumption
- Low material budget
- On-chip data processing
- Larger areas
- …

Istituto Nazionale di Fisica Nucleare

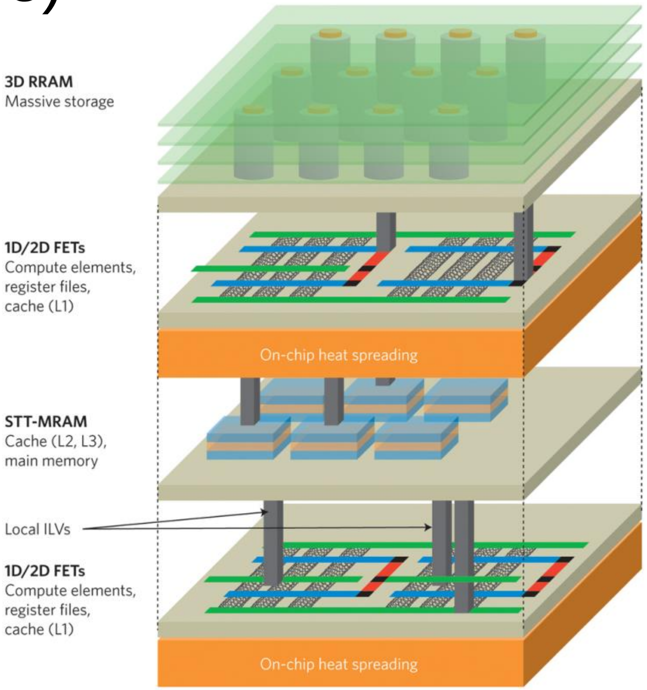
Processing technologies

Novel opportunities:

- Deep submicrometer processes (Moore's law)
- **3D integration** (more than Moore)
- MEMS technologies:
  exploit **silicon 3rd dimension**



www.samcointl.com

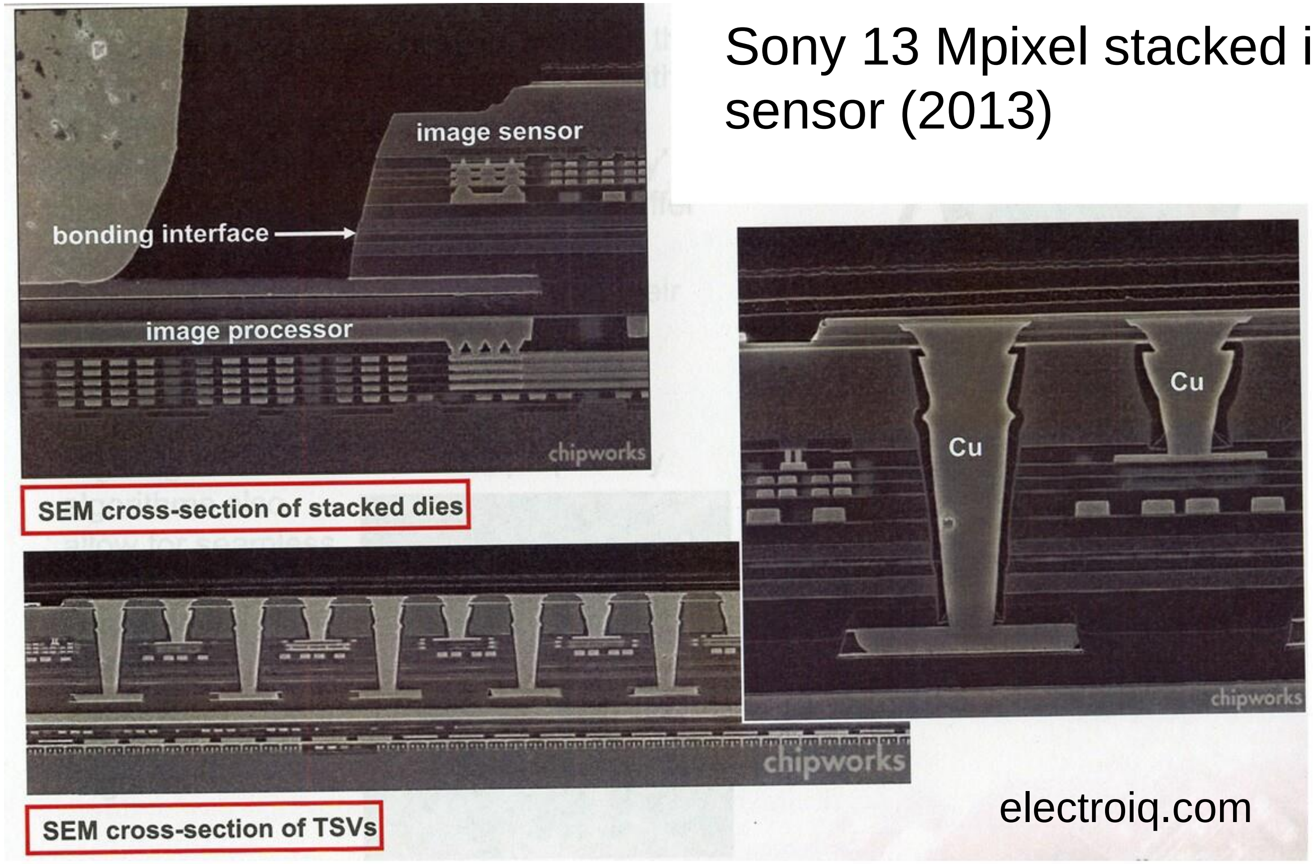


H.-S. P. Wong, Nature Nanotechnologies, 2015

3D: matching needs and possibilities

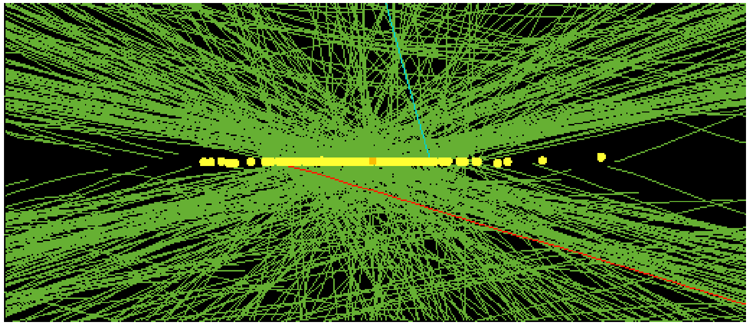
Synergies between research needs and technological possibilities offered by 3D processing and integration are still widely unexplored

Sony 13 Mpixel stacked image sensor (2013)



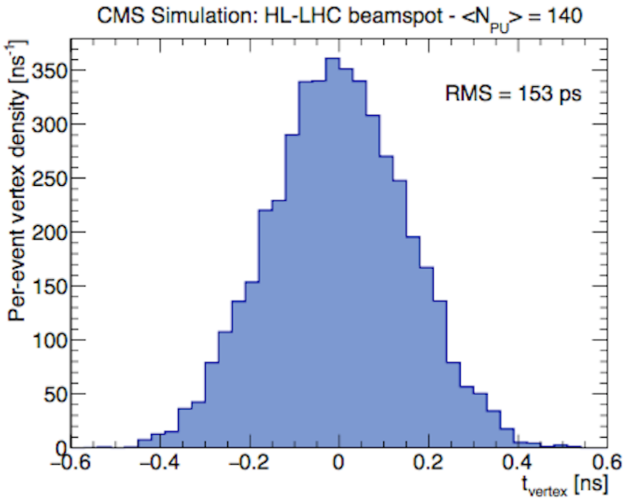
electroiq.com

Why do we need a 4th dimension?



The research into **4D tracking** is strongly motivated by the HL-LHC experimental conditions:

150-200 events/bunch crossing



According to CMS simulations:

- **Time RMS between vertexes: 153 ps**
- Average distance between two vertexes: 500 um
- Fraction of **overlapping** vertexes: 10-20%

At HL-LHC: Timing is equivalent to additional luminosity

In other experiments (NA62, PADME, Mu3e): Timing is key to background rejection

The effect of timing information

The inclusion of track-timing in the event information has the capability of changing radically how we design experiments.

Timing can be available at different levels of the event reconstruction.

1) Timing at each point along the track

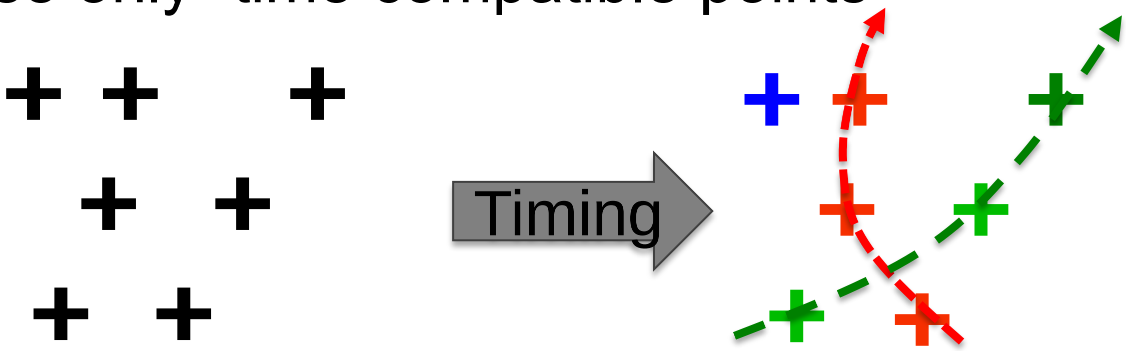
2) Timing in the event reconstruction

3) Timing at the trigger level

Timing at each point along the track

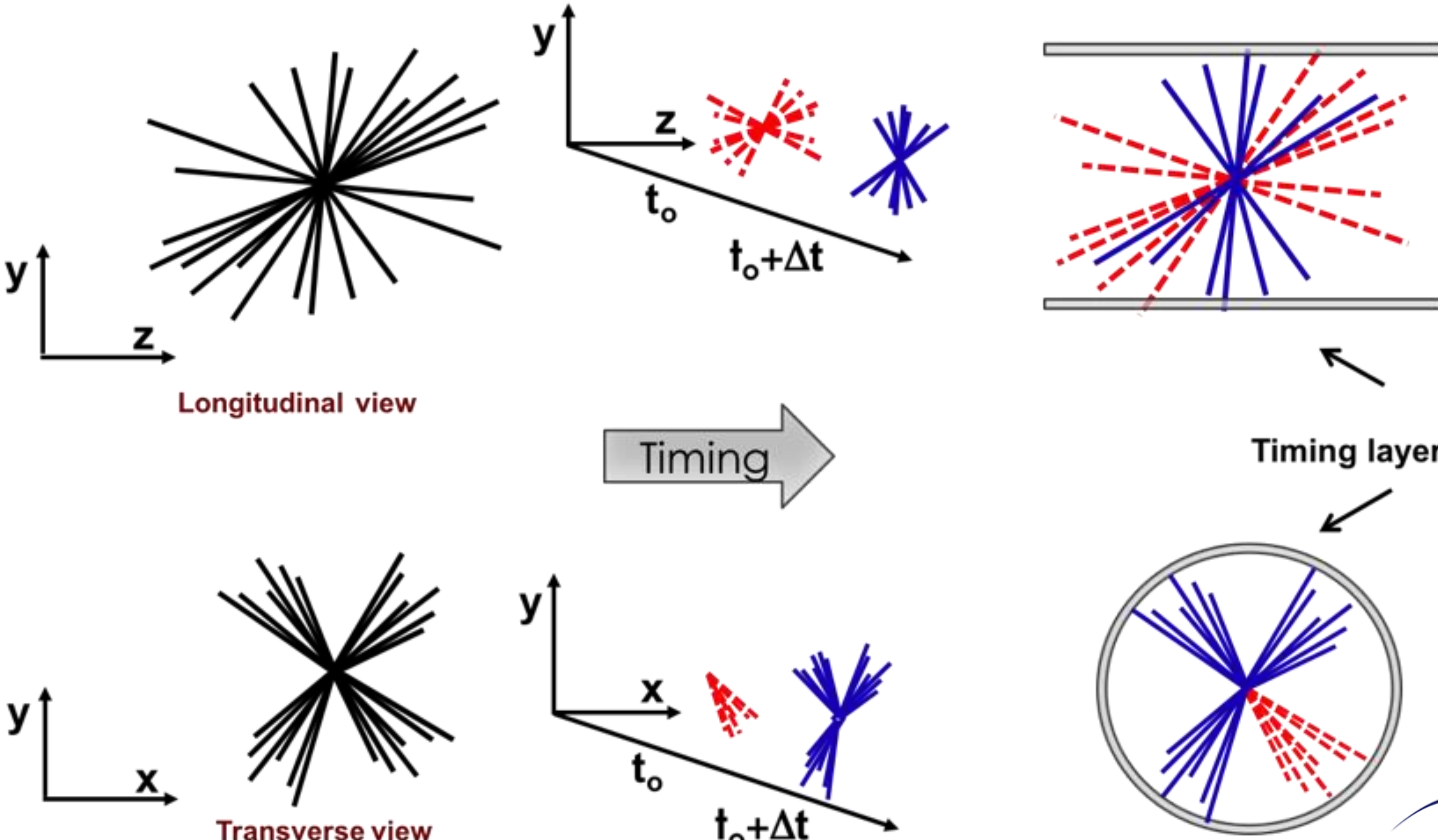
➔Massive simplification of patter recognition, new tracking algorithms will be faster even in very dense environments

➔Use only “time compatible points”



Timing in the event reconstruction

Timing allows distinguishing overlapping events by means of an extra dimension.



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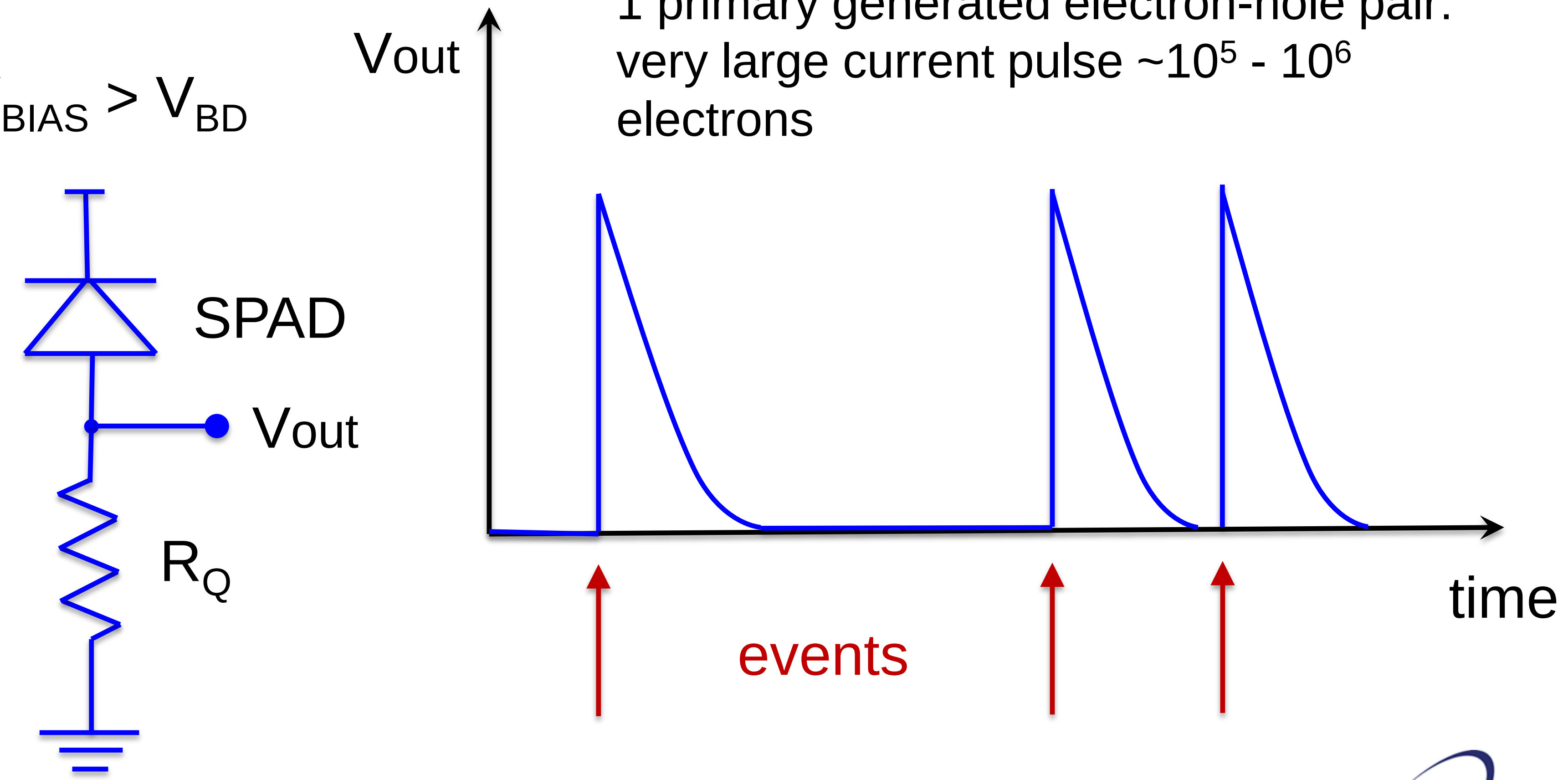
Geiger-mode avalanche detectors

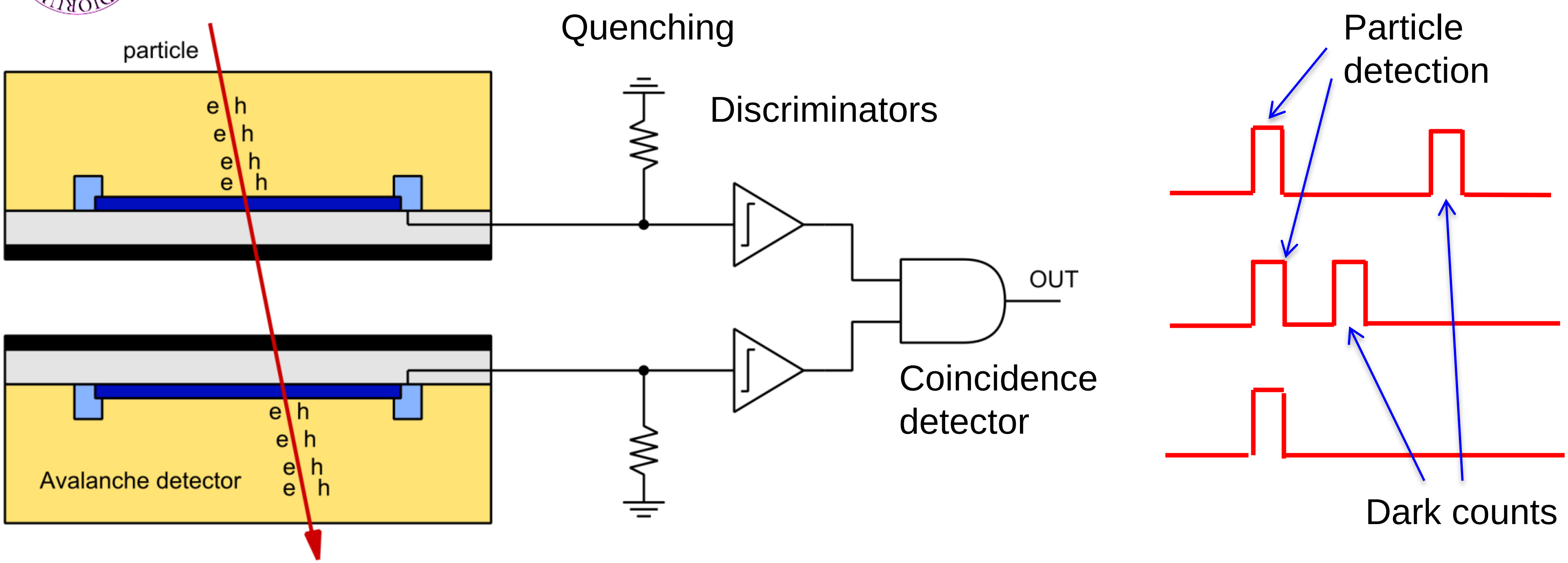
a.k.a. Single-Photon Avalanche Diodes (SPADs),
Silicon Photomultipliers

$V_{BIAS} > V_{BD}$

1 primary generated electron-hole pair: very large current pulse ~10^5 - 10^6 electrons



APiX particle detector concept



- Two Geiger-mode avalanche detectors in **coincidence**:

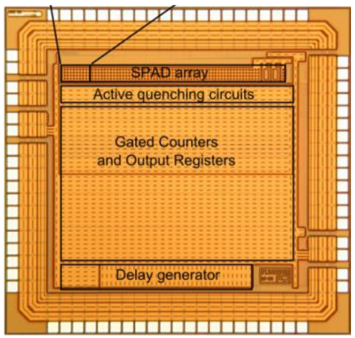
$$DCR = DCR_1 \times DCR_2 \times 2\Delta T$$

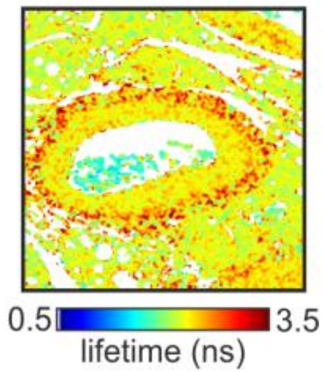
- In-pixel coincidence: integrated electronics is needed: **CMOS avalanche detectors**

V. Saveliev, US Patent. 8,269,181, 2012 N. D'Ascenzo et al., JINST 2014

CMOS SPAD arrays

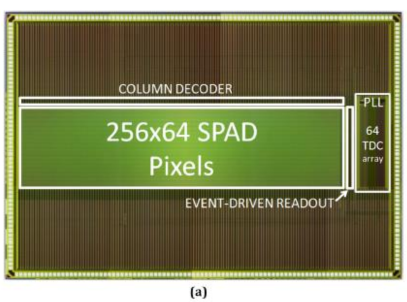
Visible-NIR **photon detection** applications

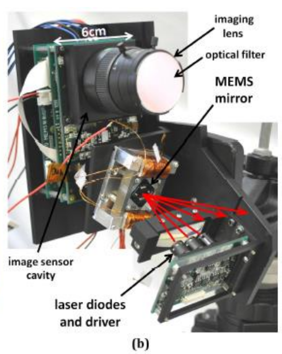




Fluorescence **microscopy**

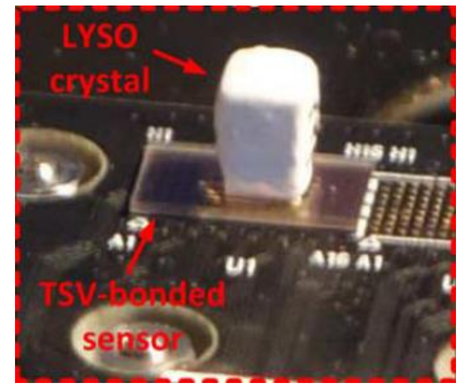
M. Popleteeva, Opt. Expr, 2015





Time-of-Flight **optical ranging**

C. Niclass, Opt. Express, 2012

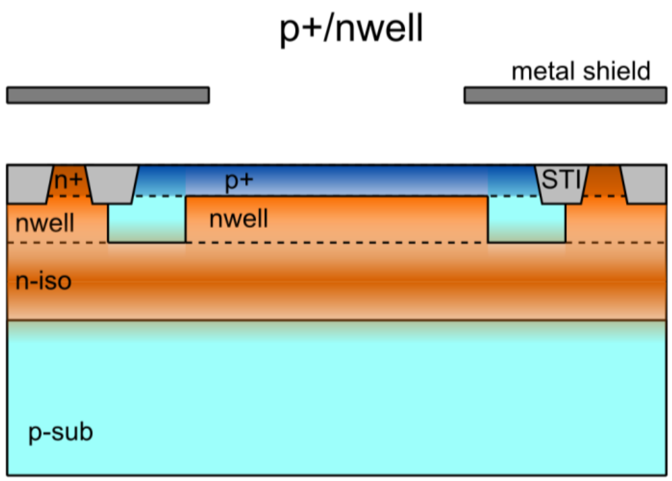


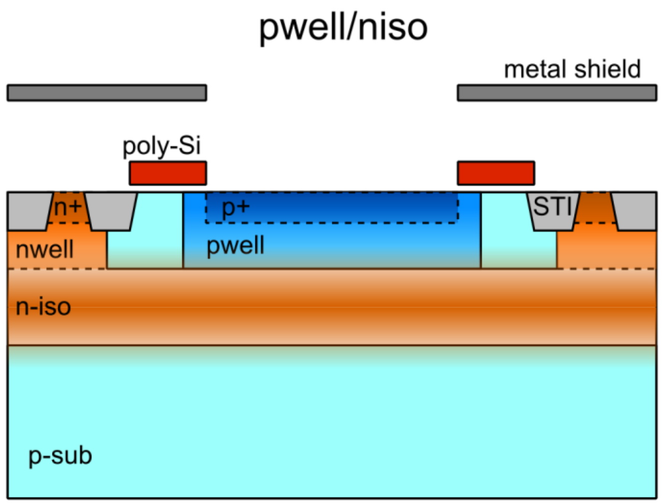
Digital SiPMs for **PET**

L. Braga, IEEE J. Solid-State Circuits, 2014

SPADs in 150nm CMOS process

- **Standard CMOS** process – no modifications
- Avalanche diodes in deep nwell: **isolated from substrate**





Type 1:

- Shallow step junction
- Active thickness ~ 1µm

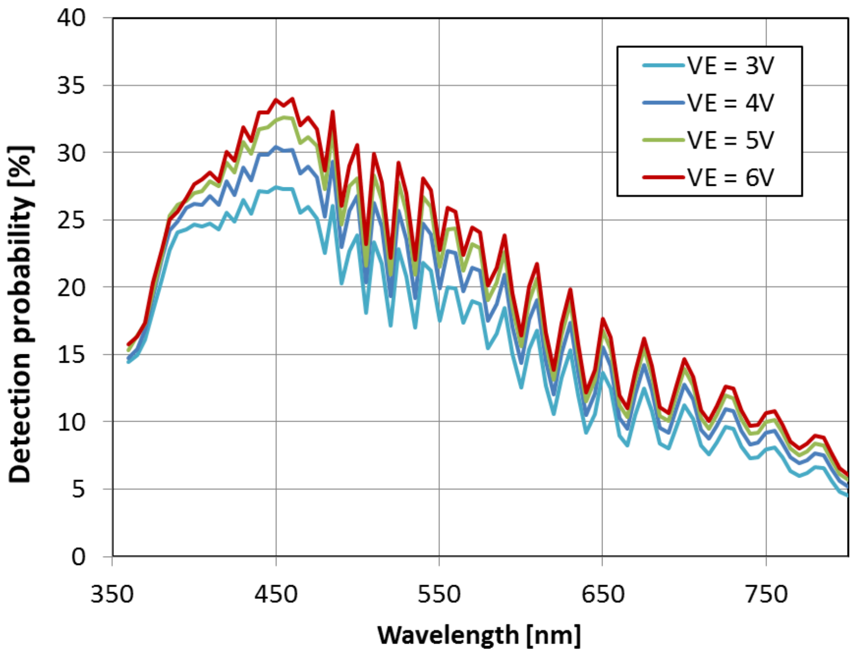
Type2:

- Deep graded junction
- Active thickness ~ 1.5µm

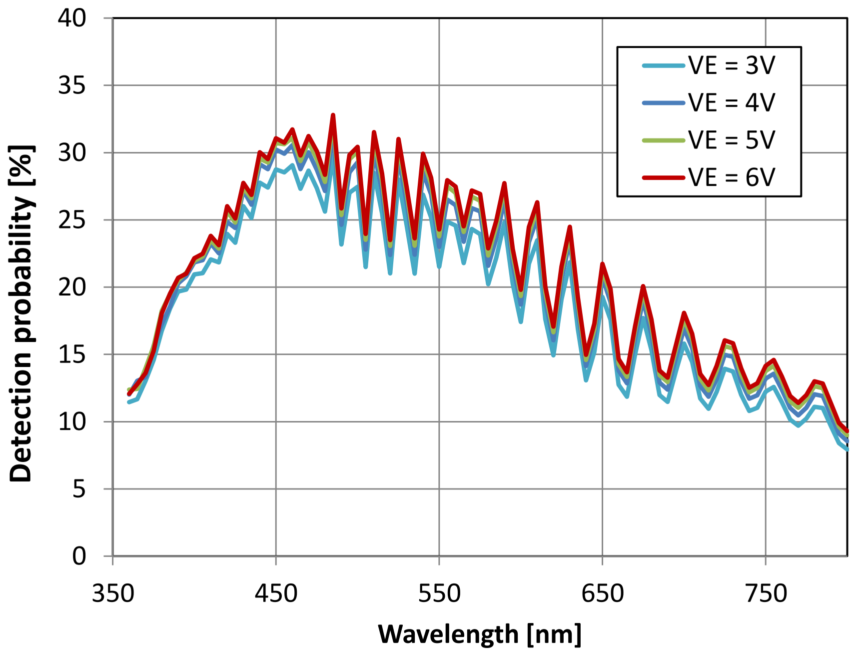
L. Pancheri, D. Stoppa, ESSDERC 2011

Photo-Detection Efficiency

Type 1: p+/nwell



Type 2: pwell/niso

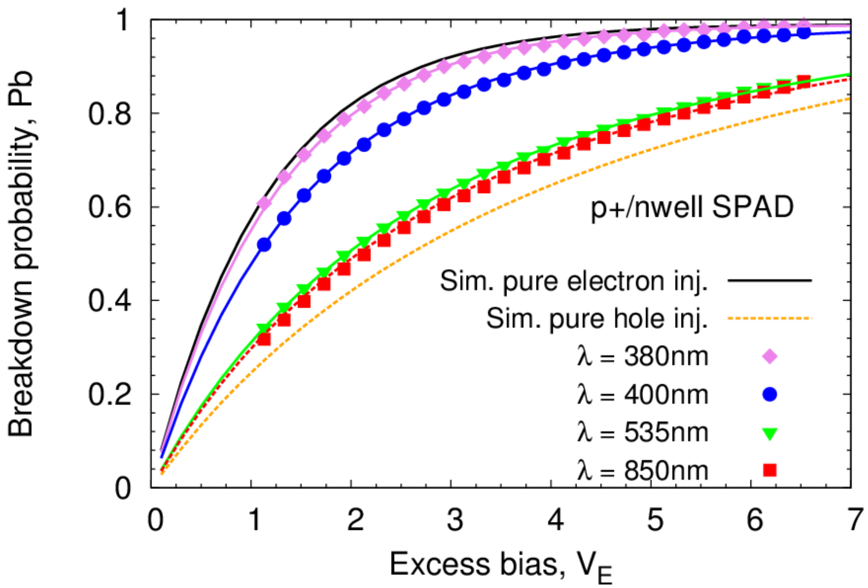


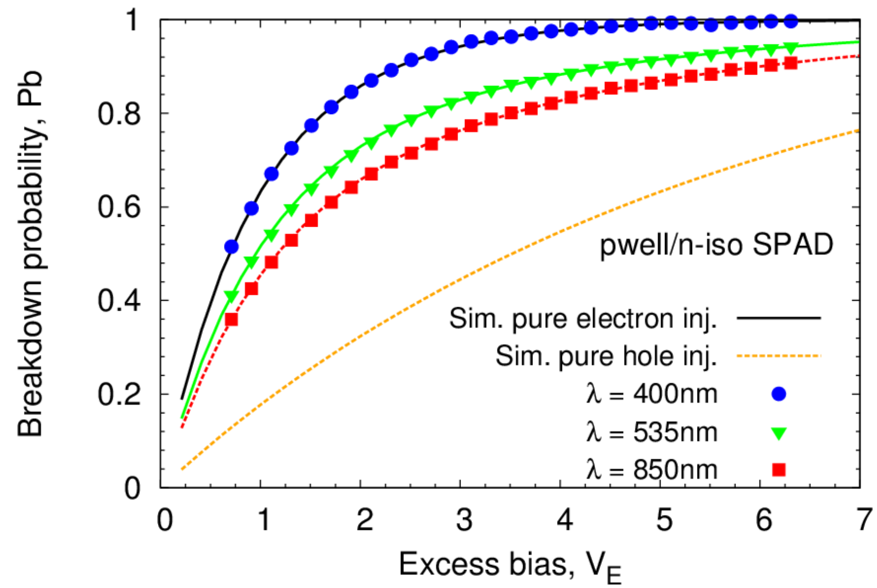
Shallower junction:
better NUV – Blue efficiency

Wider depletion region:
Better red-IR efficiency

L. Pancheri et al., J. Selected Topics in Quantum Electron, 2015

Breakdown probability (Pb)





IR light: uniform generation, Pb measured for a single photoelectron

Particles generate **N primary electrons:** $Pb_N = 1 – (1\text{-}Pb)^N$

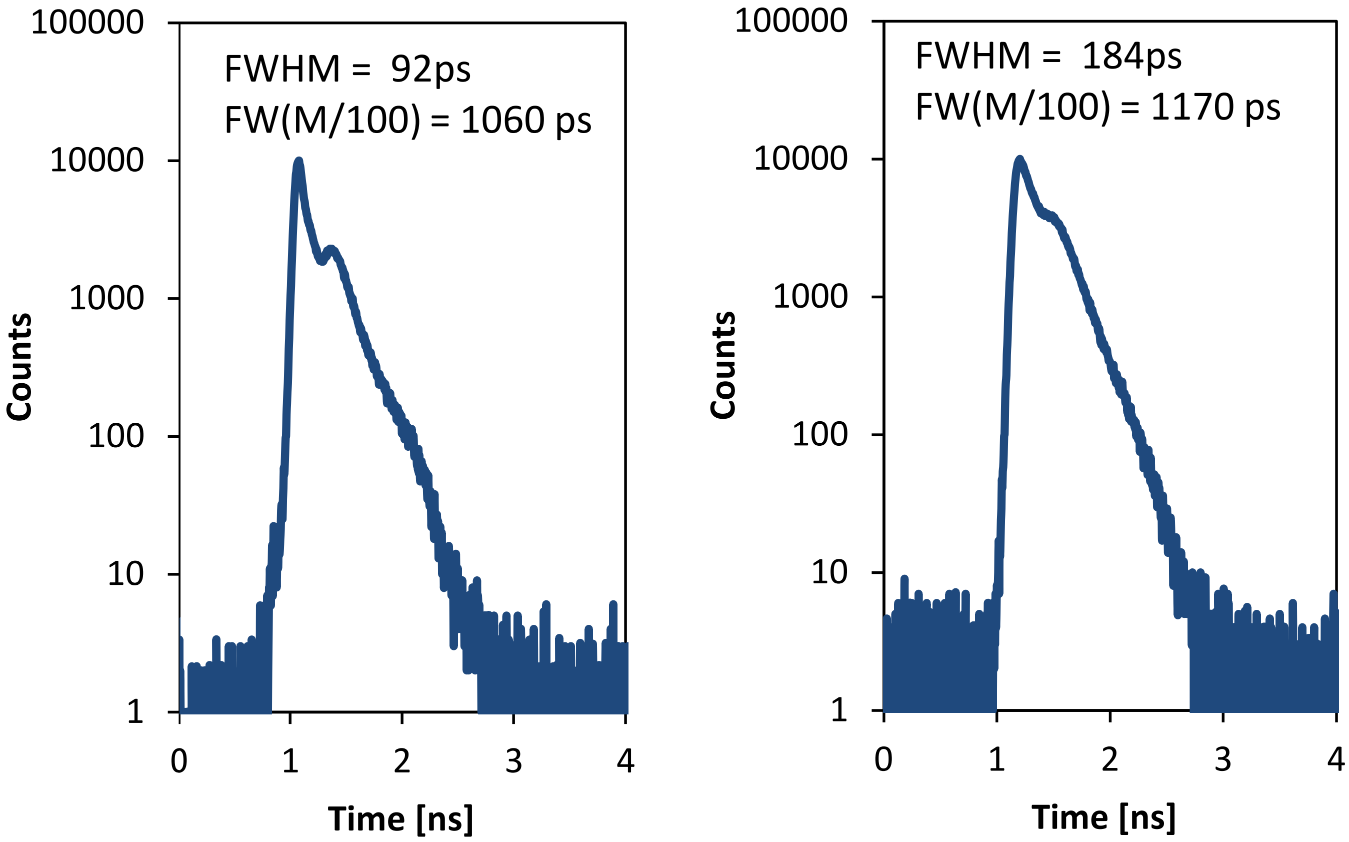
Example: single electron → Pb = 30%
10 electrons → $\mathbf{Pb_{10} = 97\%}$

L. Pancheri et al., J. Selected Topics in Quantum Electron, 2015

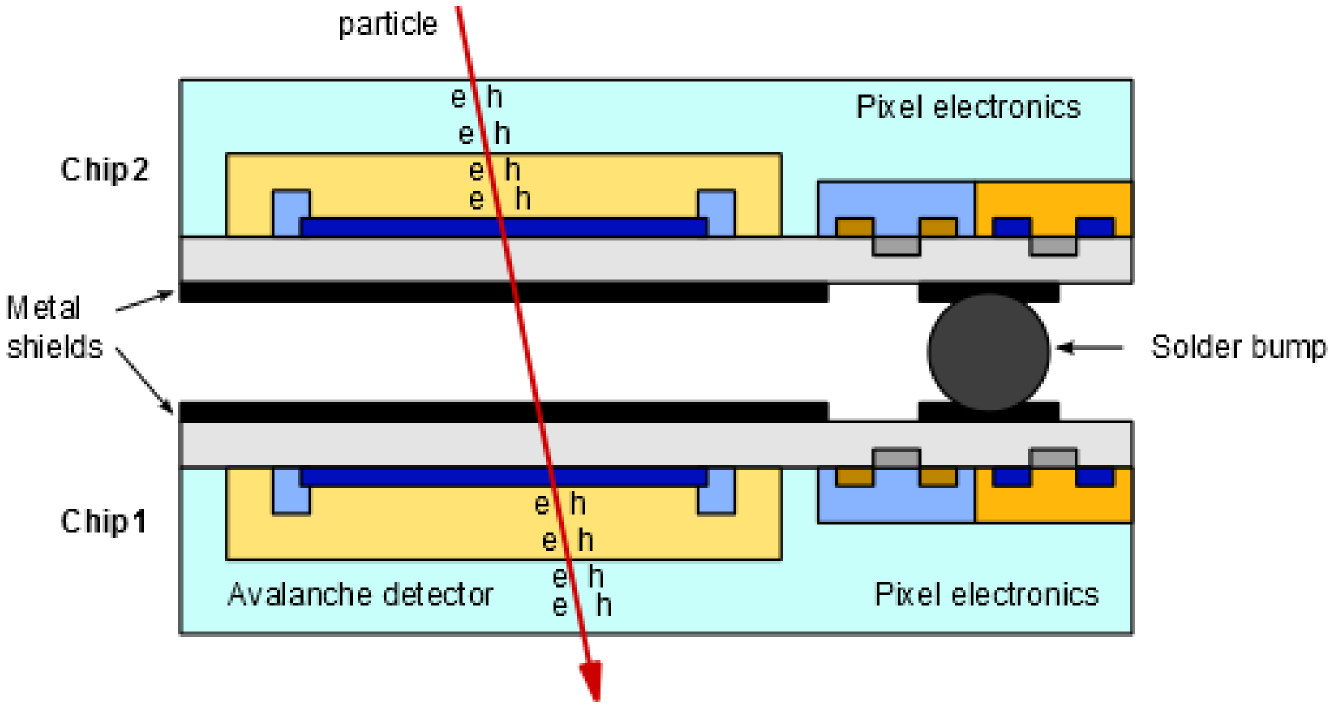
Single-photon timing resolution

Measured on 10-μm devices, with blue laser (470nm), 70ps FWHM

Type 1: **60ps FWHM** Type 2: **170ps FWHM**



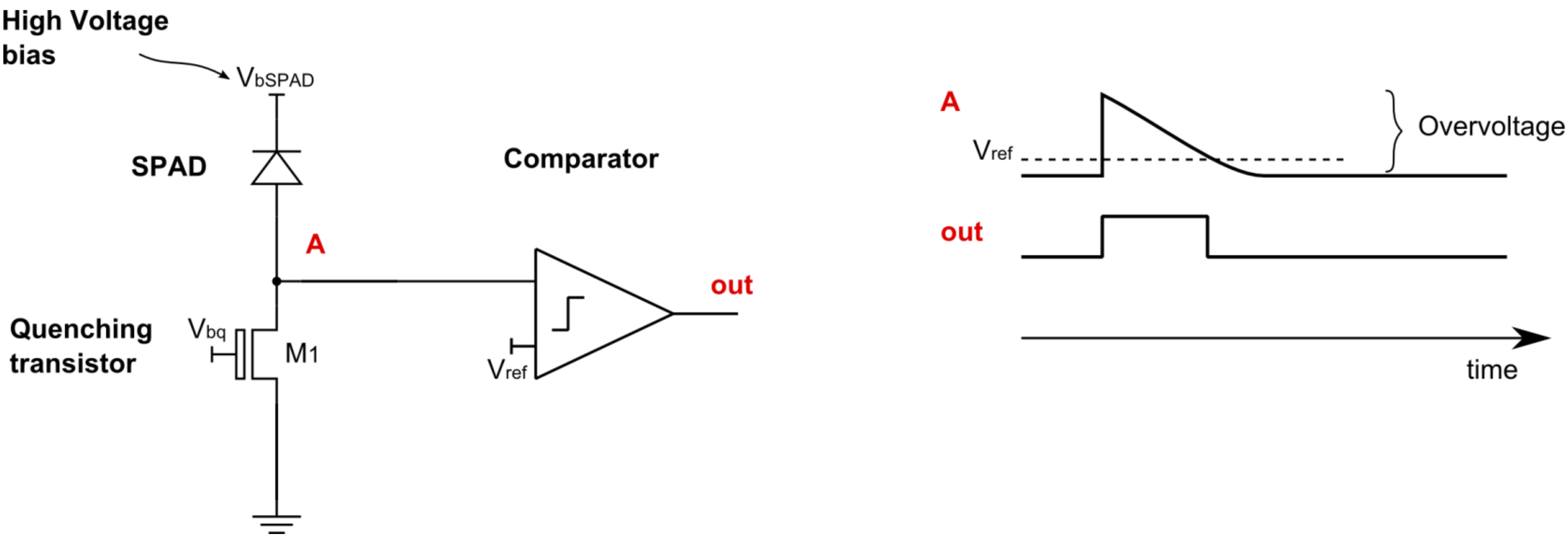
Proof-of-concept demonstrator



2-layer pixel cross section:

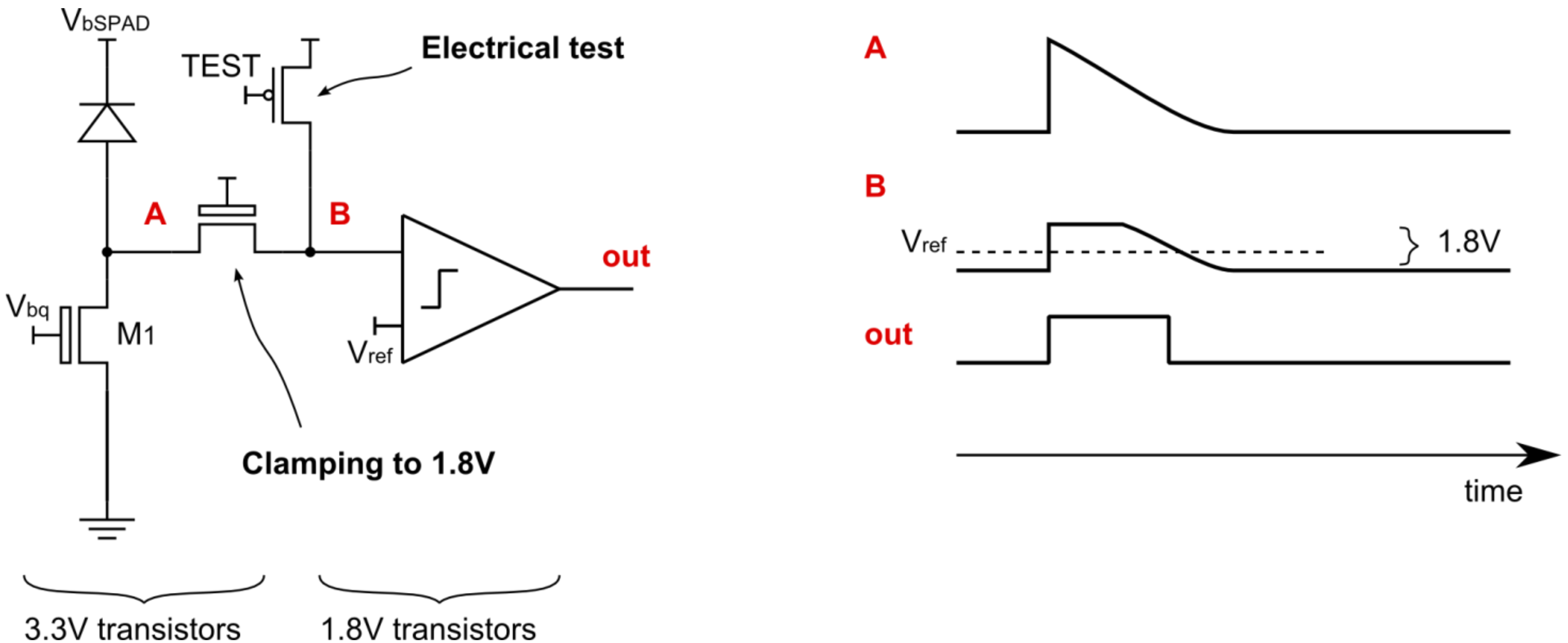
- Electronic readout on both layers
- **Metal shielding** from optical cross-talk
- Vertical interconnection by **bump bonding**

Pixel architecture



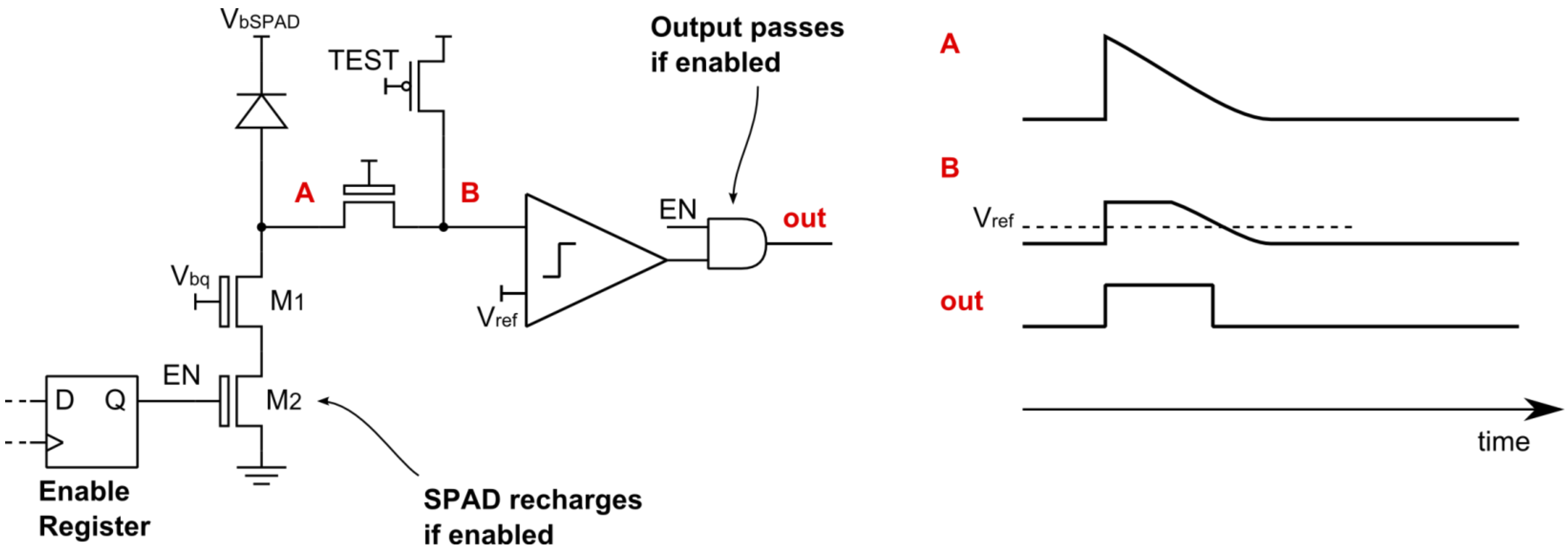
- **High voltage** V_{bSPAD} applied at nwell
- Maximum voltage at node A: $V_{ov} = V_{bSPAD} - V_{BD}$
- **Small capacitance** at node A
- Passive quenching with constant current recharge

Pixel architecture



- Front-end transistors: 3.3V → Maximum overvoltage 3.3V
- **Digital circuitry: 1.8V** compact – fast – low-power

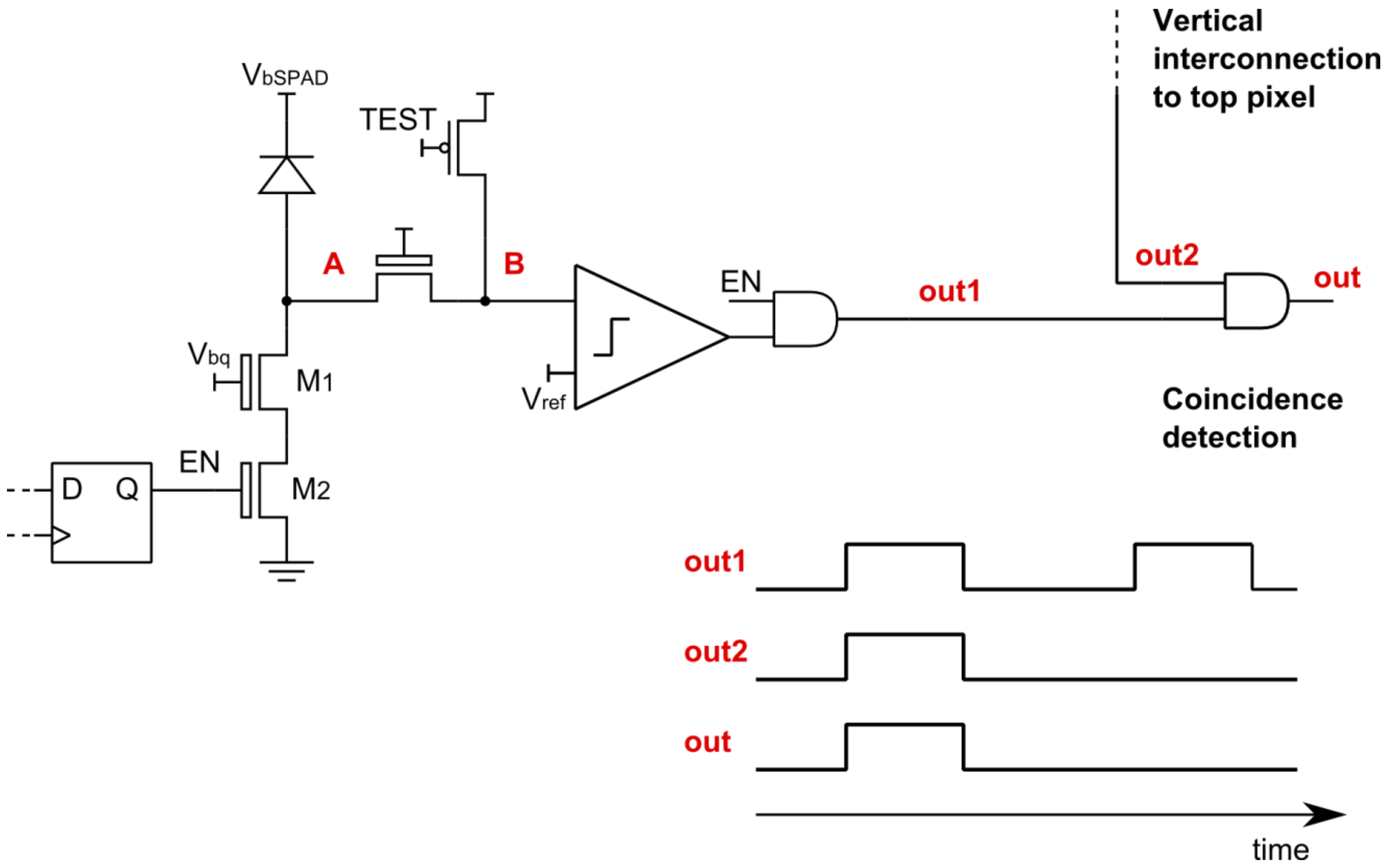
Pixel architecture: enable register



Pixels can be **individually disabled**:

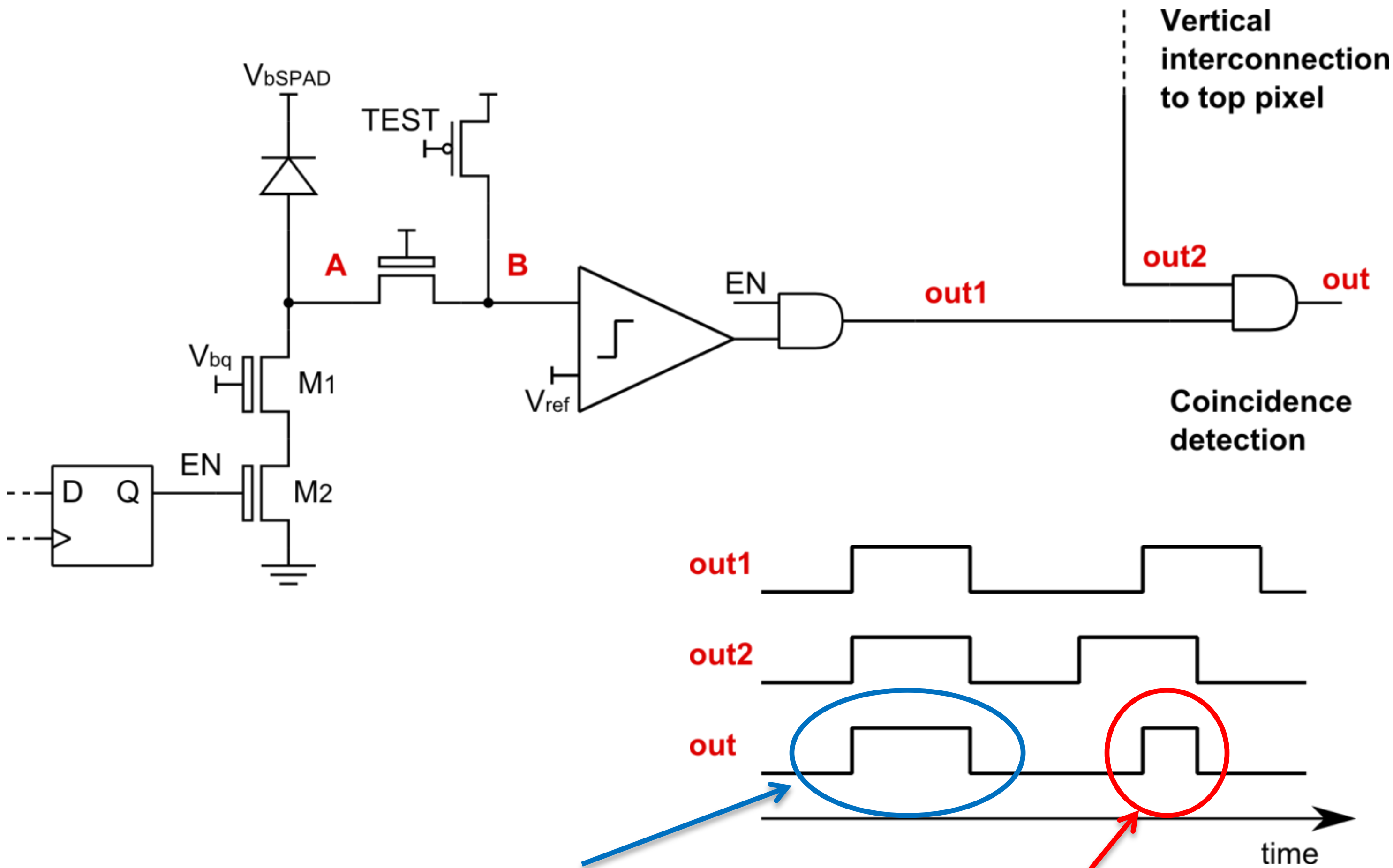
- M_2 disables recharge
- Output and gate blocks output pulses

Pixel architecture: coincidence



- Coincidence with top-layer pixel

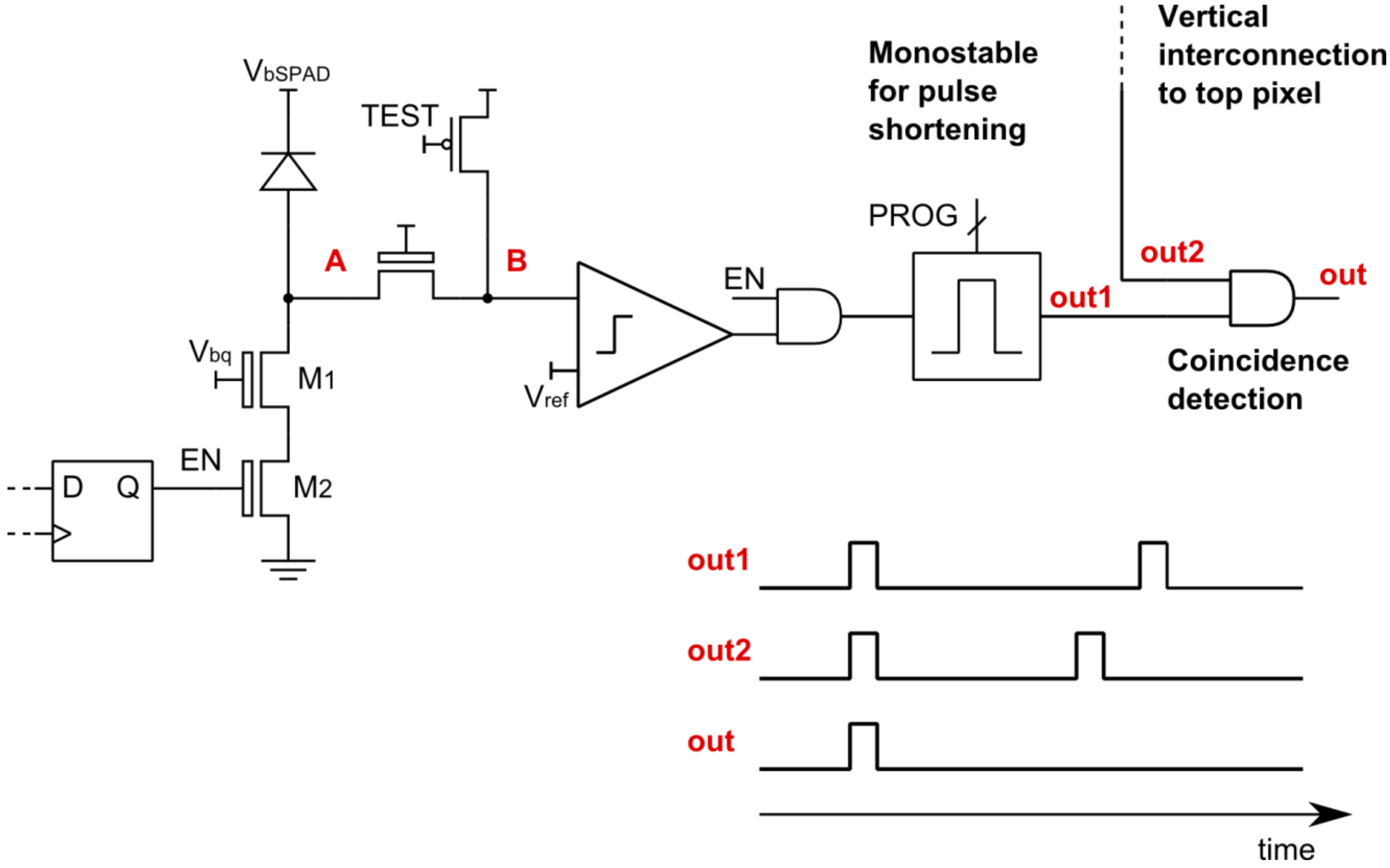
Pixel architecture: coincidence



Real coincidence

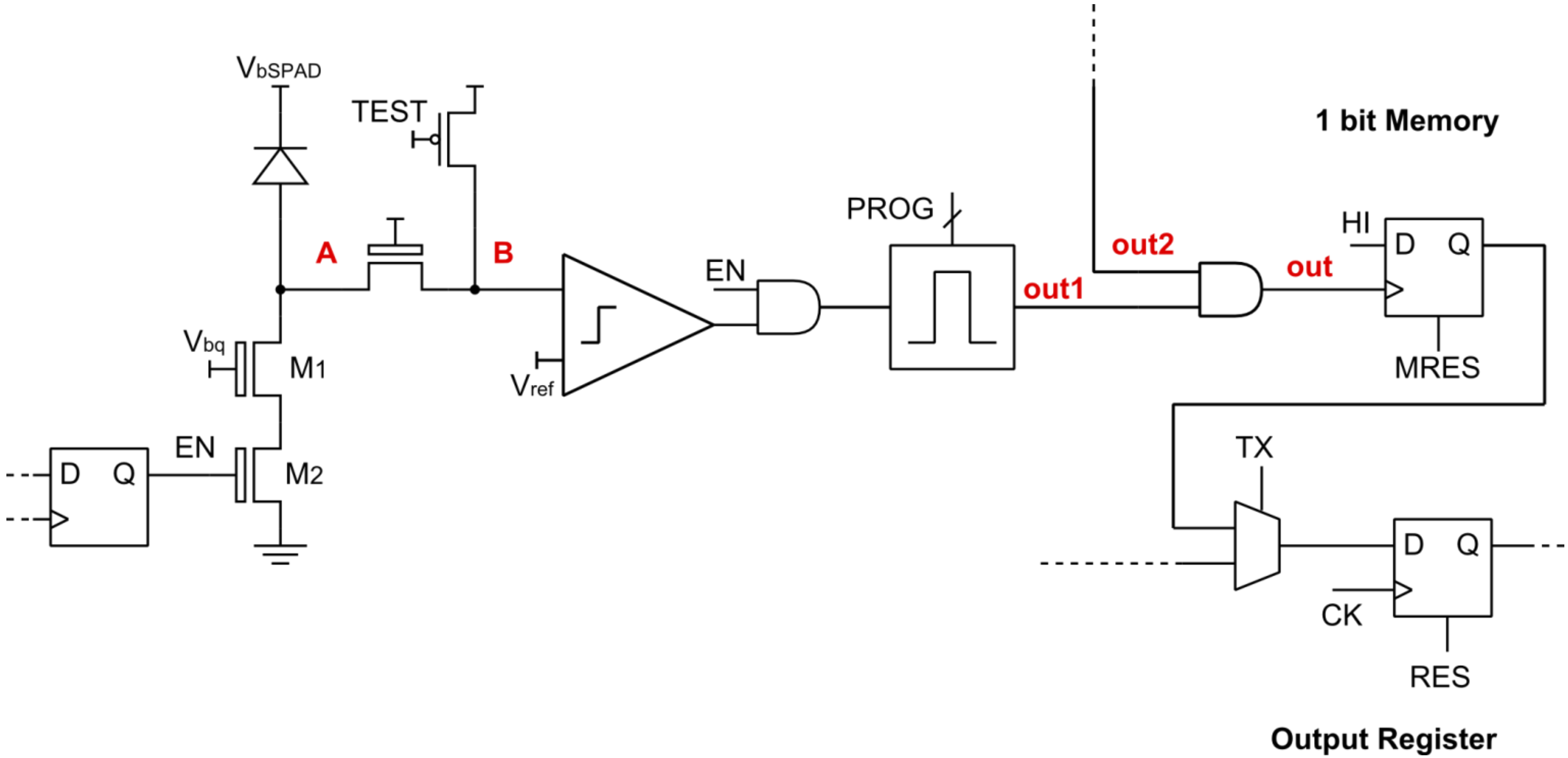
Accidental coincidence

Pixel architecture: monostable



- Pulse shortening: reduces the rate of accidental coincidence
- Programmable pulse width: **750ps, 1.5ns, 10ns**

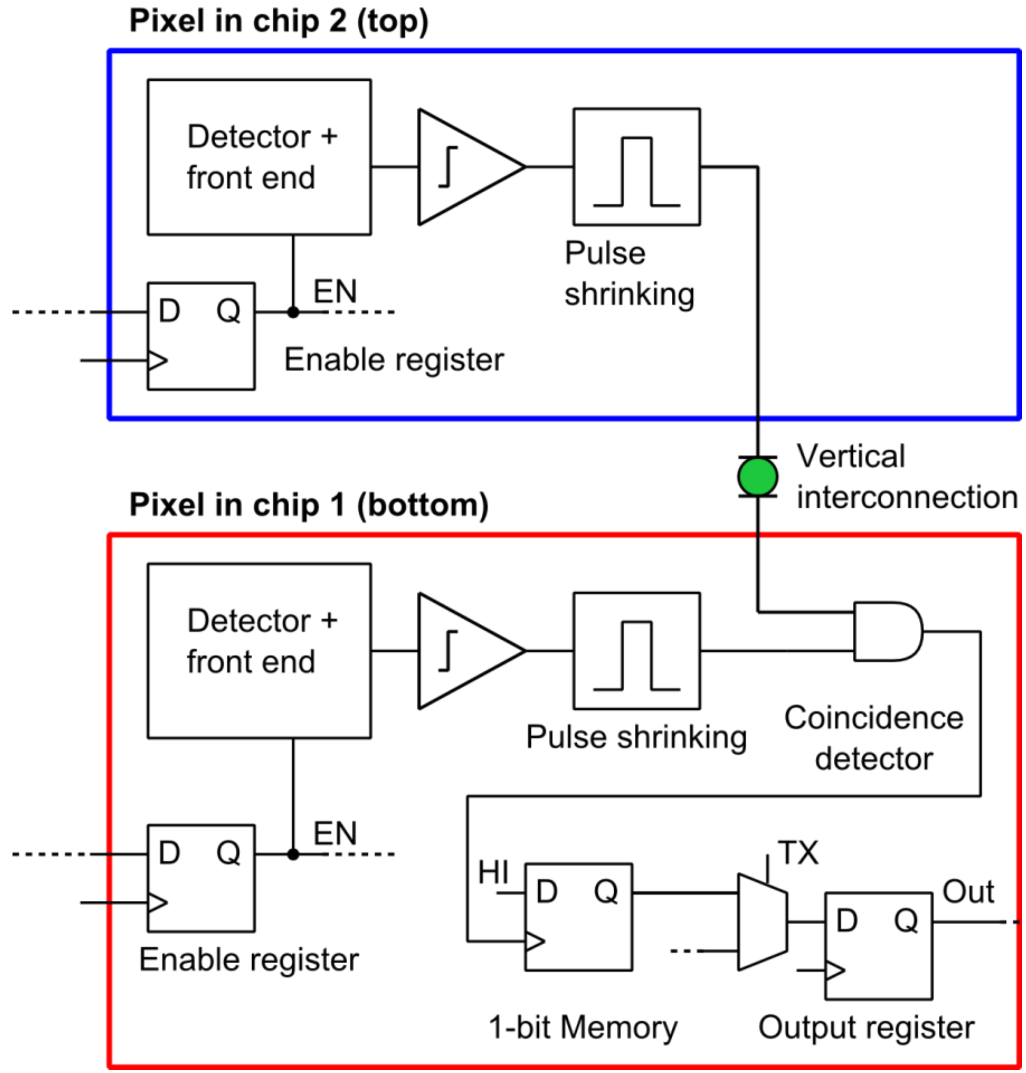
Pixel architecture: storage



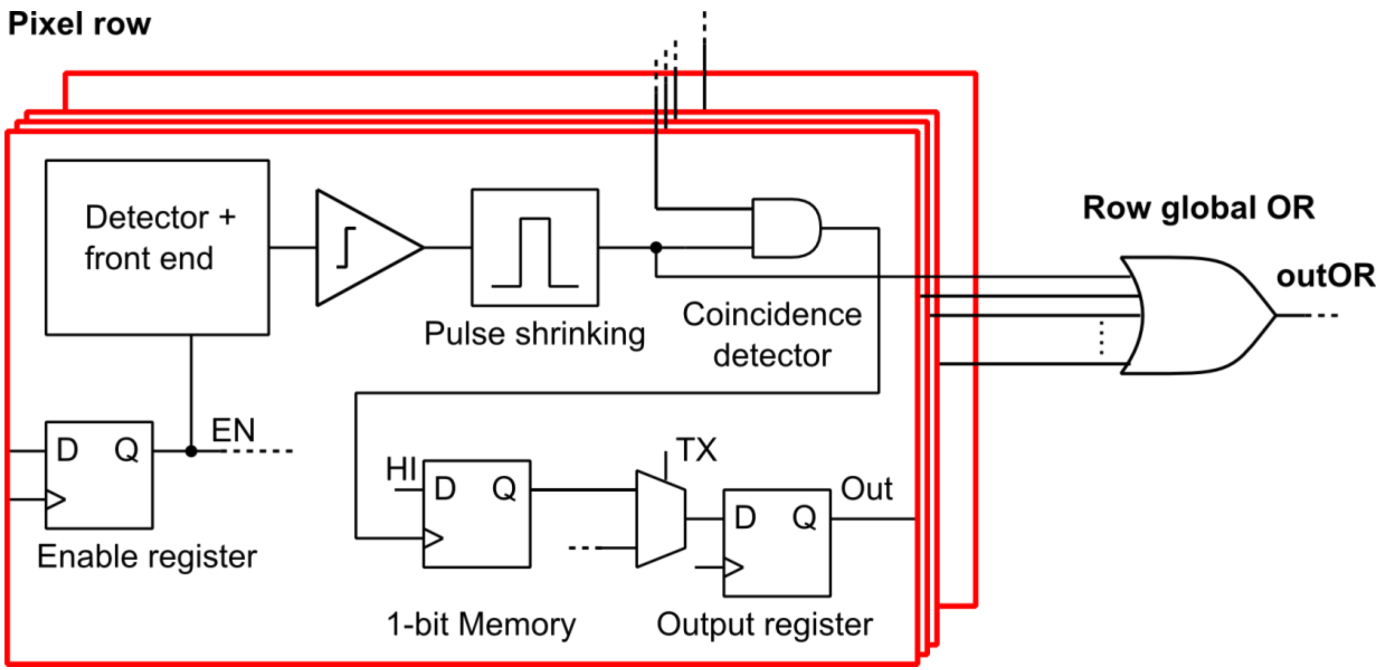
- **Global shutter** operation:
  - Fast transfer from memory to output register
  - Simultaneous accumulation and data output

2-level pixel schematic

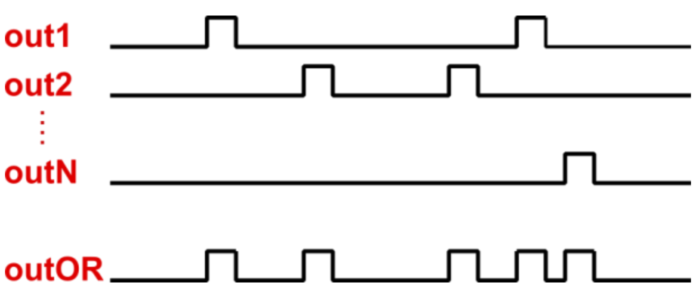
Top pixel: subset of bottom pixel



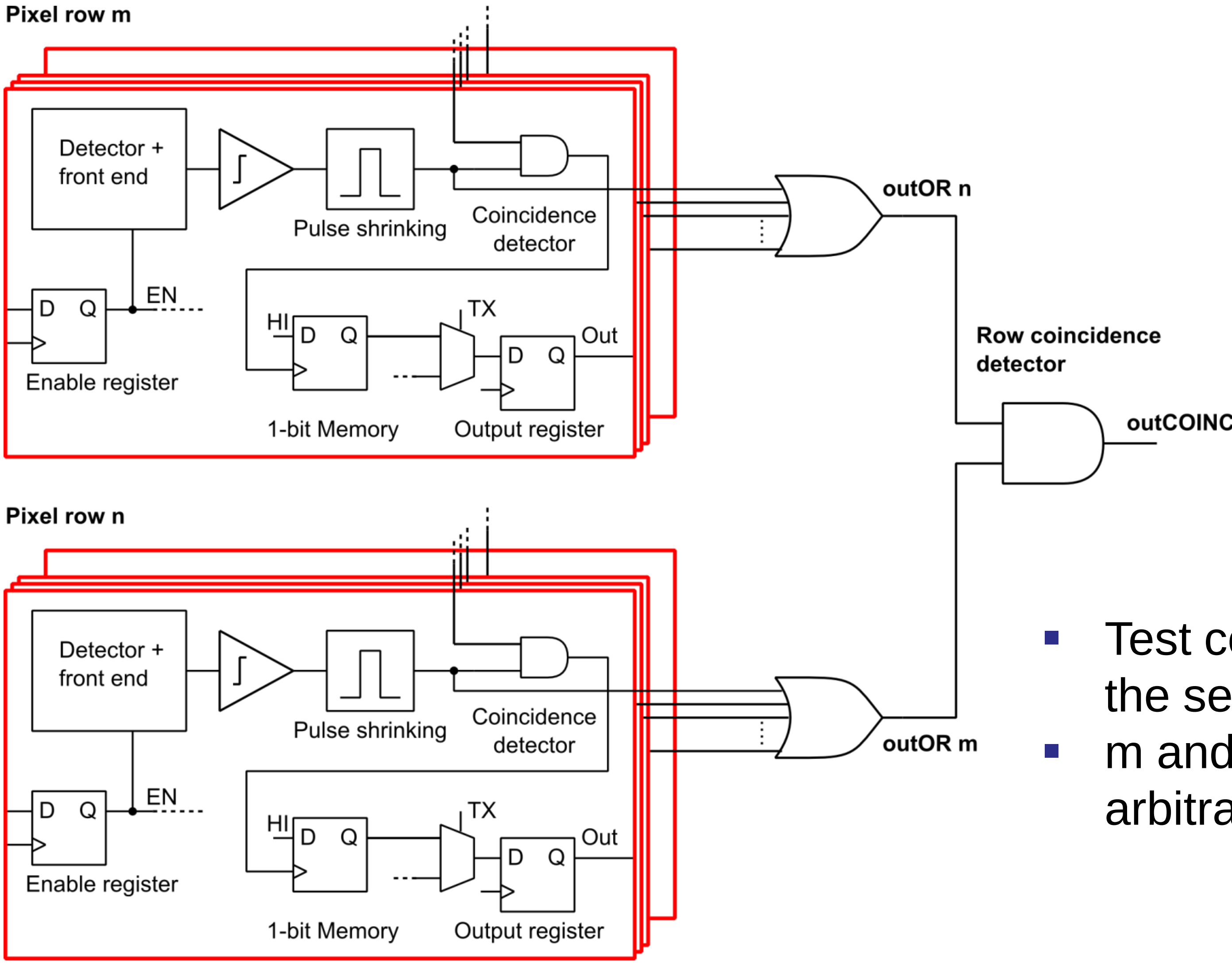
Sensor architecture: row-wise OR



Test output outOR: combination of all the active (enabled) pixels in the row

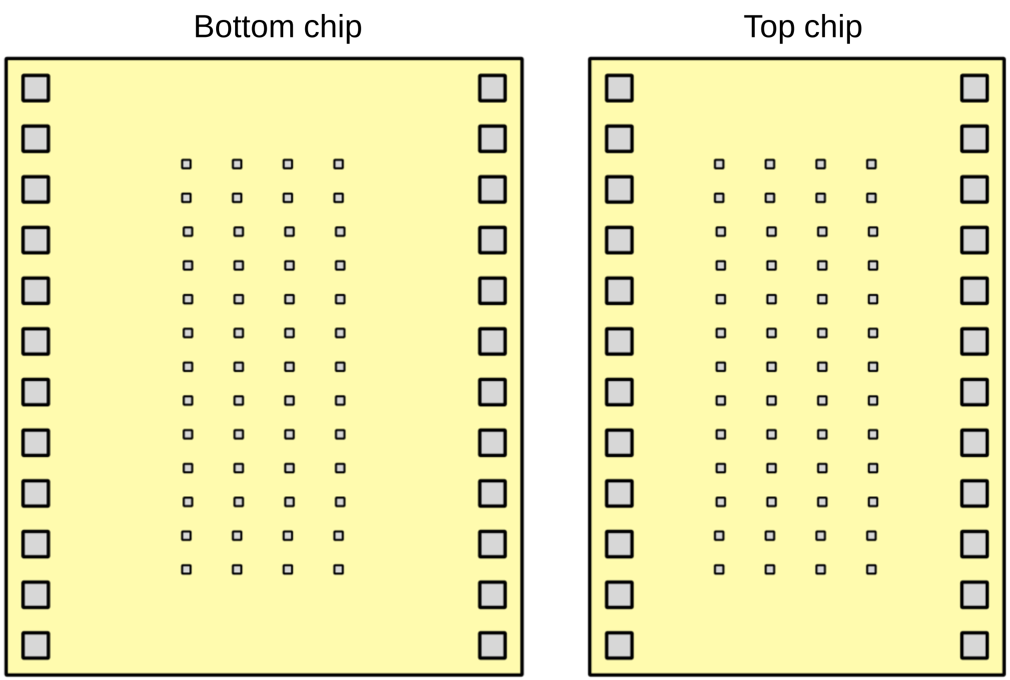


Row-wise coincidence circuit



- Test coincidence in the sensor plane
- m and n can be arbitrarily selected

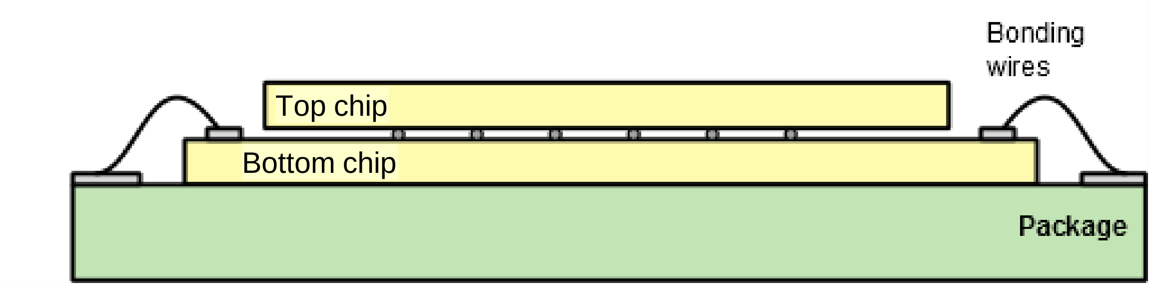
Sensor floorplan



Pads for wire bonding

Pads for bump bonding

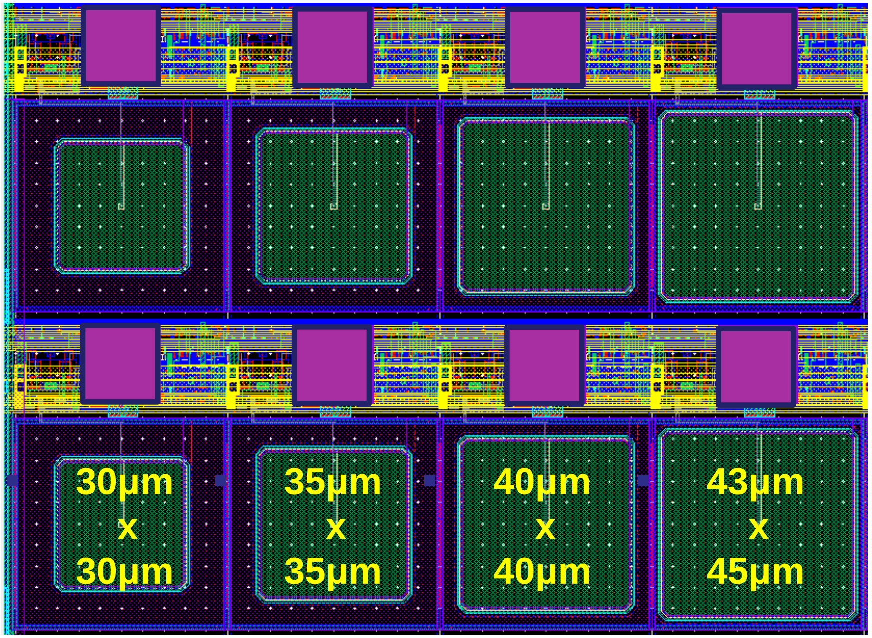
Wire bonding pads on chip 2: pre-integration test.



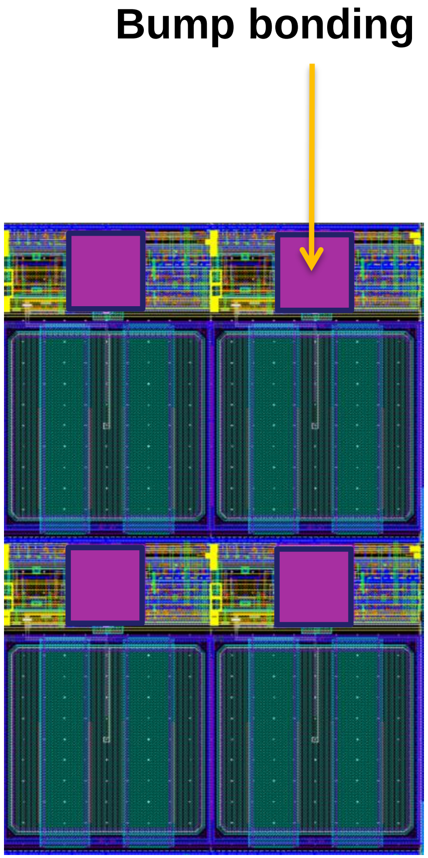
Final assembly

Pixel array

- 16 x 48 pixel array
- Pixel size: 50μm x 75μm
- Splittings in detector type and area



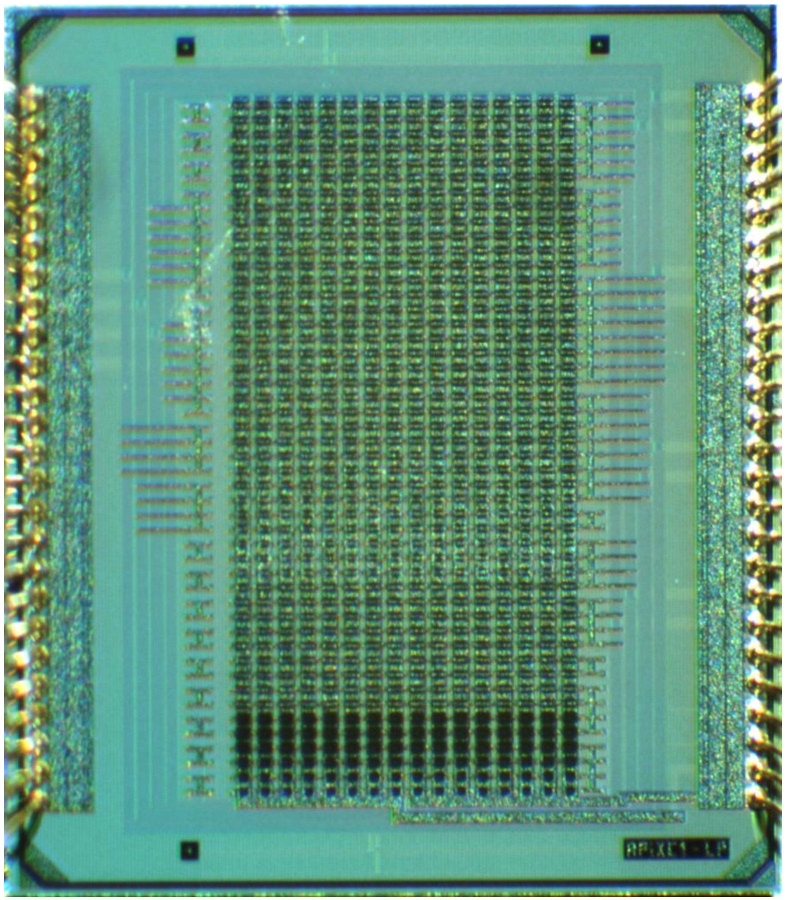
Pixels with different detector area (unshielded)



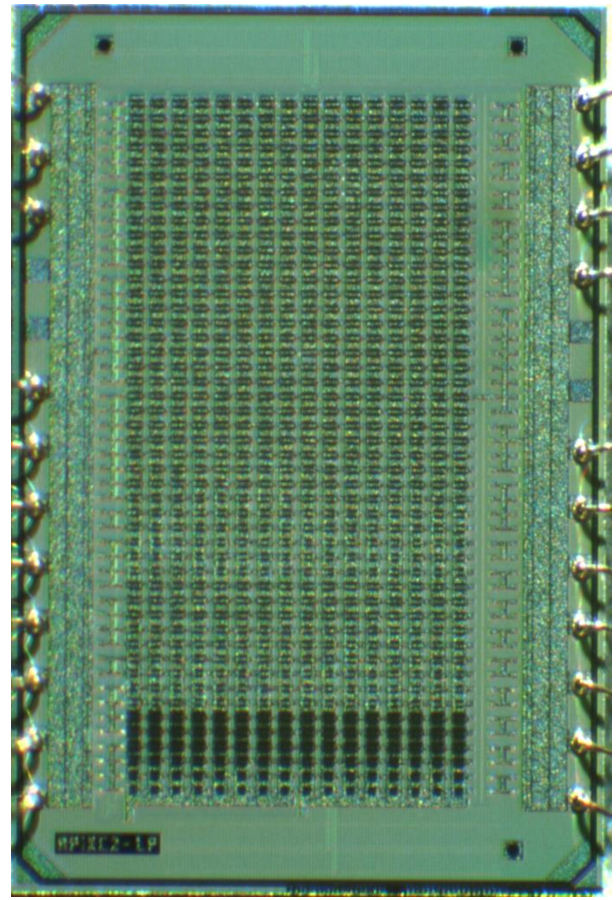
Pixels with shielded detectors

Sensor micrographs

Bottom chip



Top chip



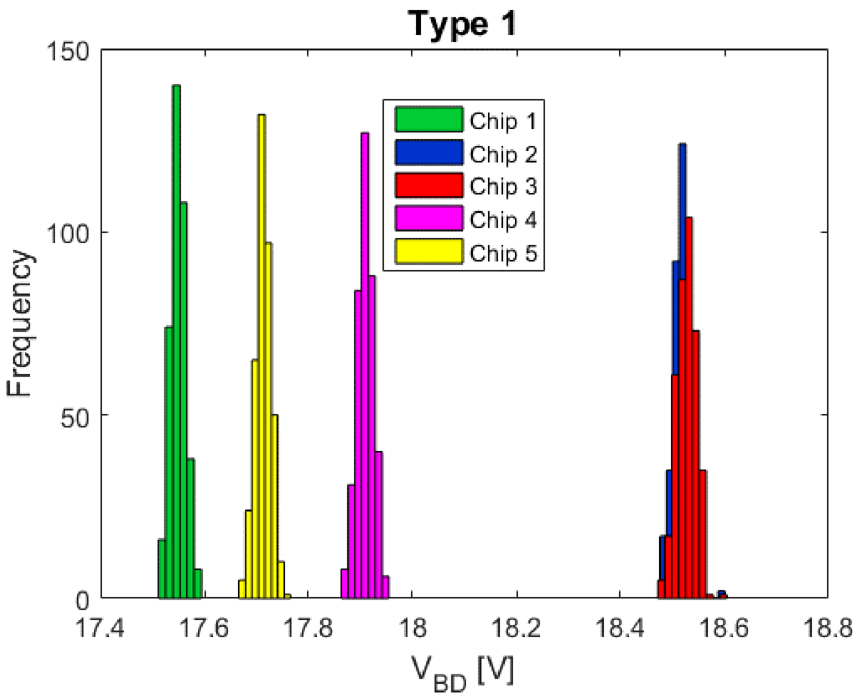
Experimental results - summary

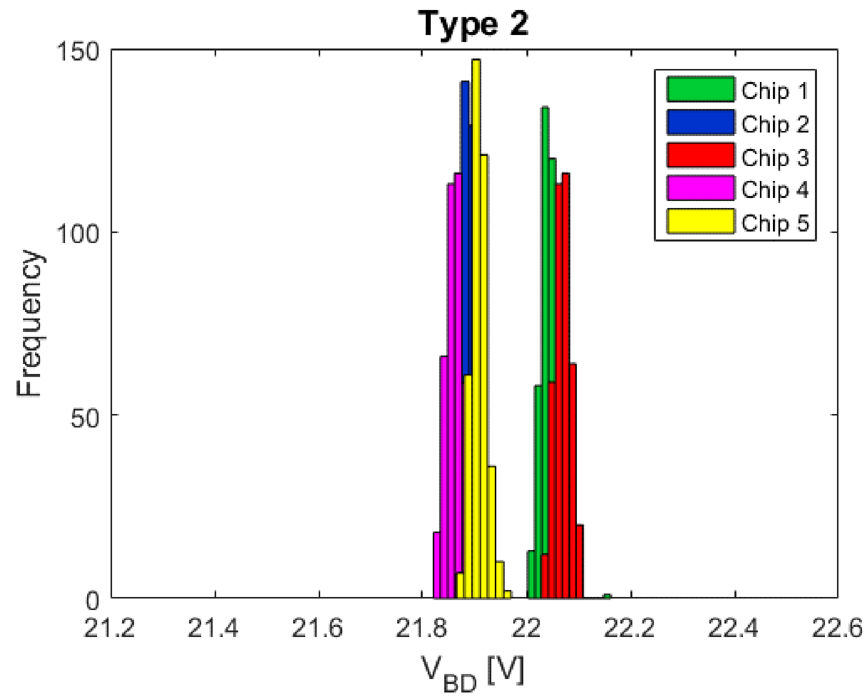
Characterization of **single-layer sensors**:

- **Core supply current (at 1.8V): 8mA**
- Breakdown voltage uniformity
- Dark count rate
- In-plane coincidence
- Timing resolution

Vertical integration of two-layer sensors with
bump bonding (IZM) almost completed
Expected delivery date: next week

Breakdown voltage uniformity

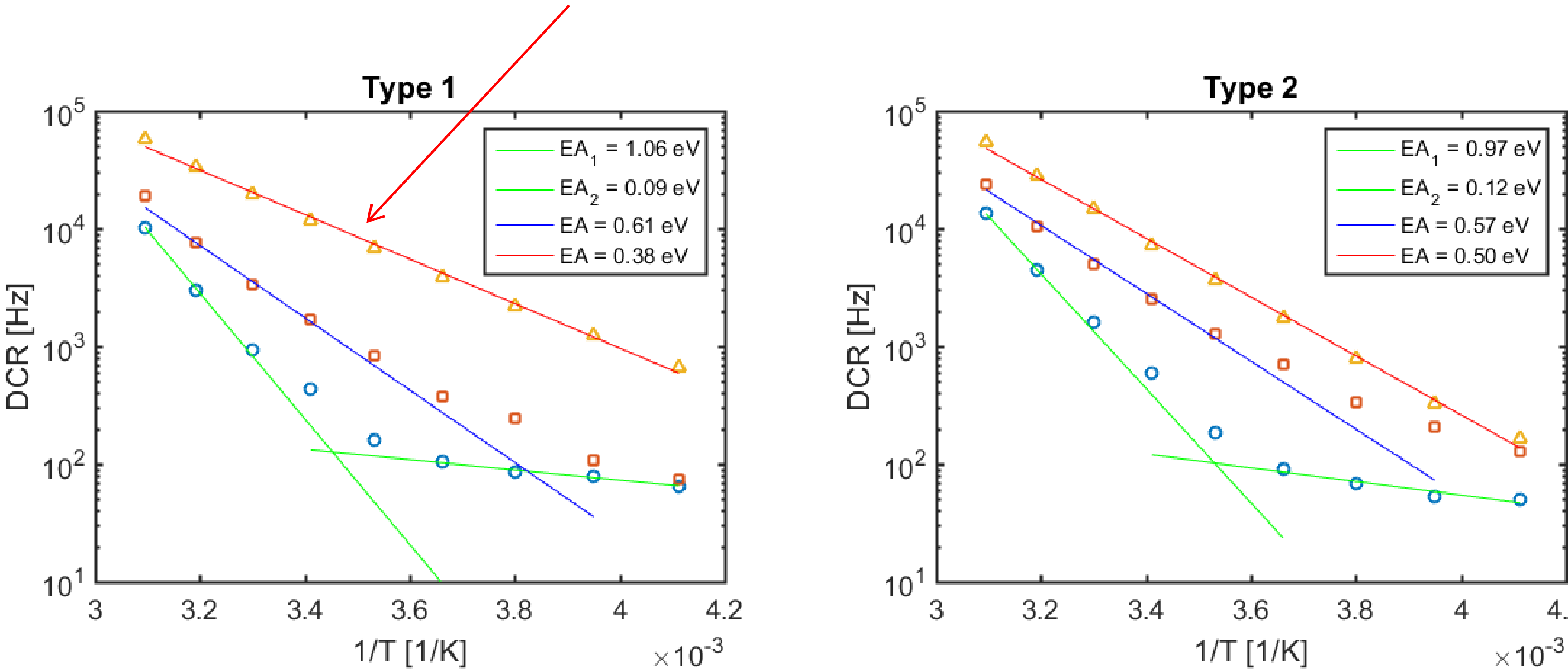




- Measurements on
  5 sample chips x 2 types x 196 devices per chip
- Very good uniformity on-chip (**σ < 20mV**)
- Large difference (1V) between different chips for type 1

DCR temperature dependence

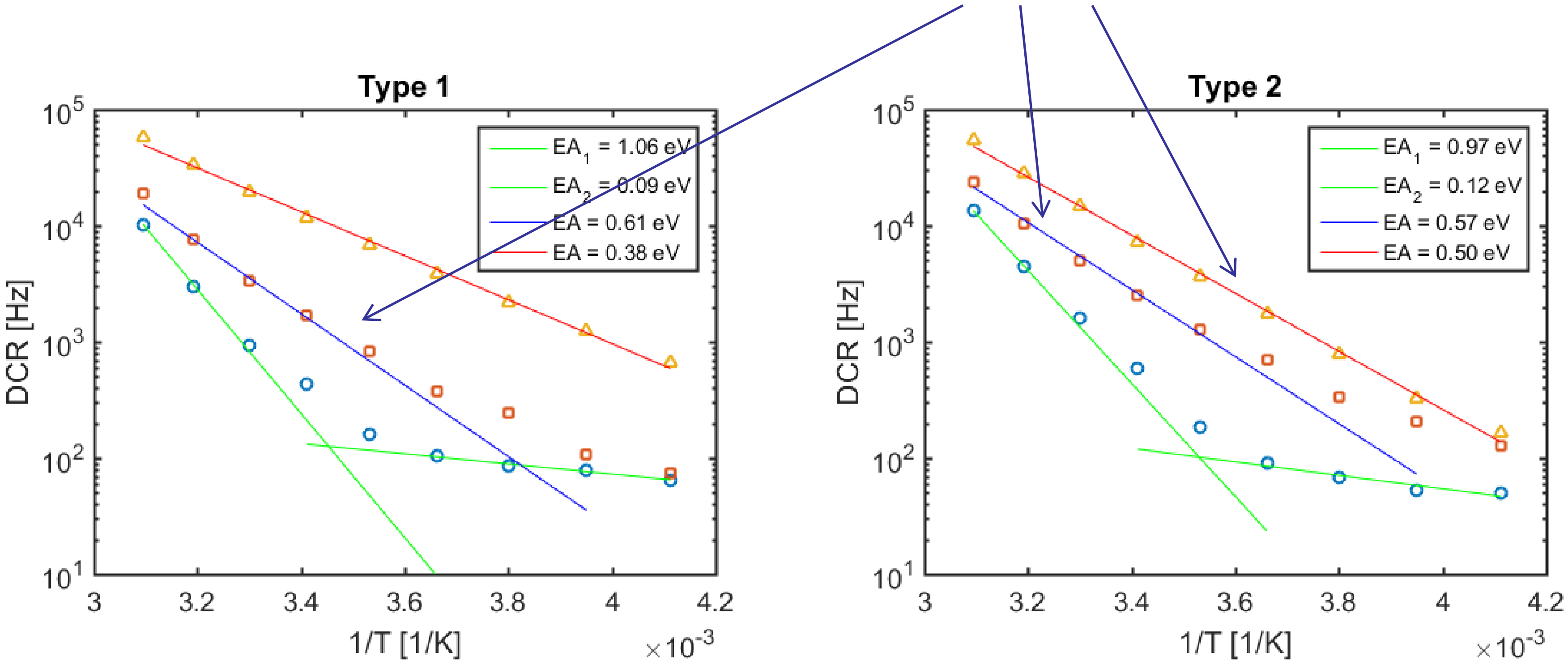
Trap-assisted tunneling: $E_A < E_G/2$



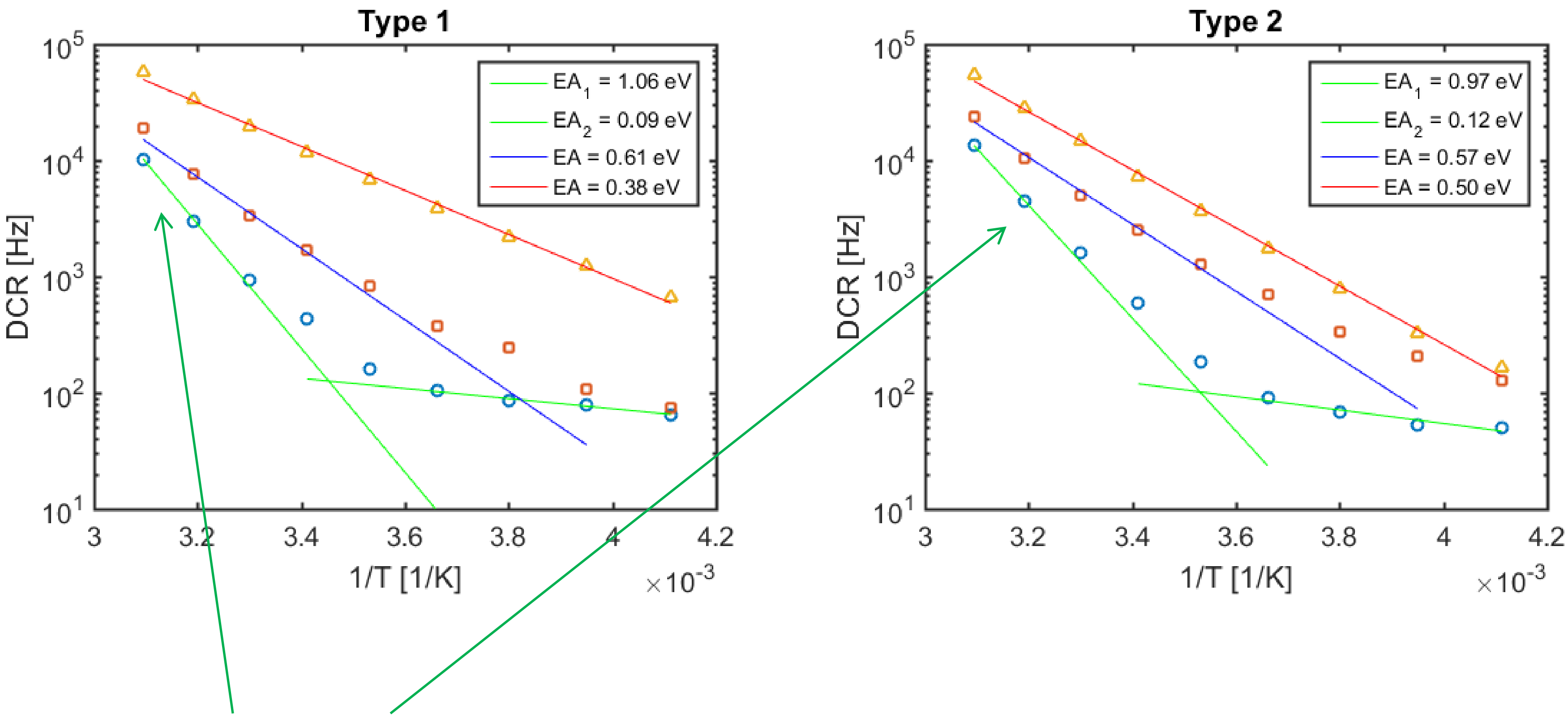
- Devices with 43μm x 45μm active area, but different DCR
- Measurements from **-30°C to 50°C** with 10°C steps
- Overvoltage: V_{OV} = 3.3V

DCR temperature dependence

SRH generation $E_A \sim E_G/2$

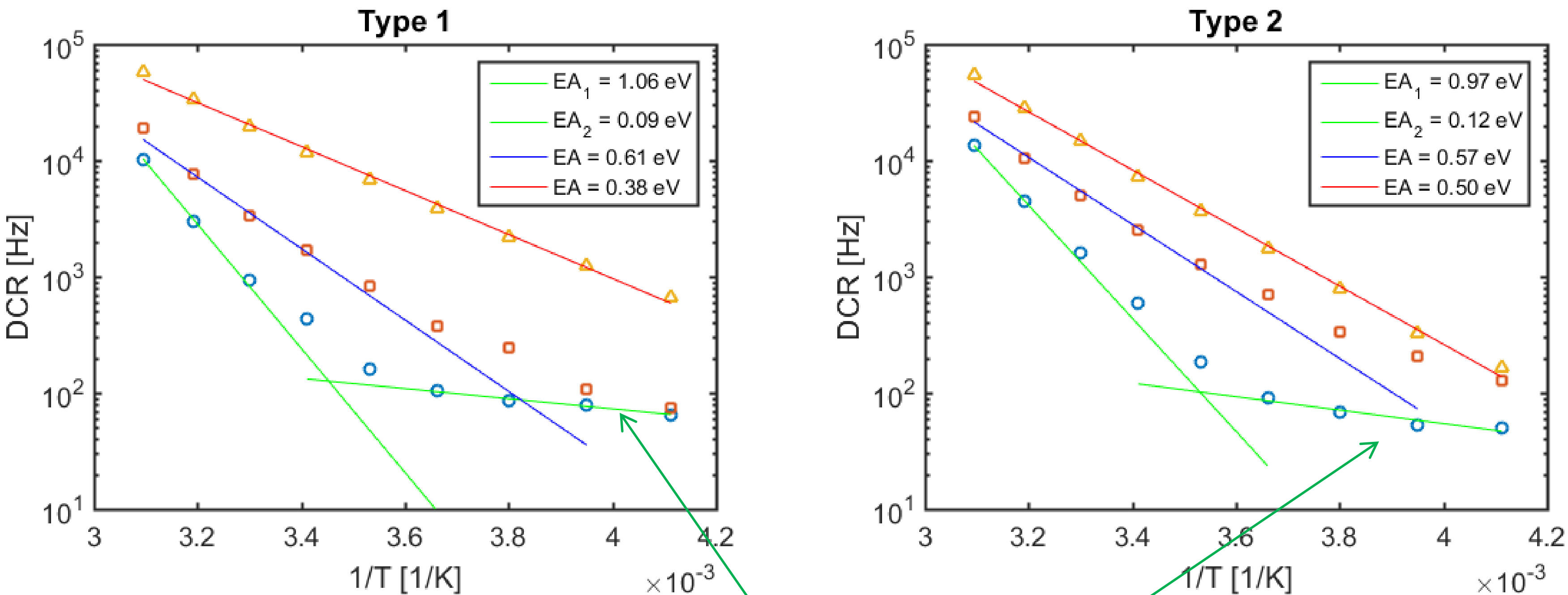


DCR temperature dependence



Injection from neutral regions: $E_A \sim E_G$

DCR temperature dependence

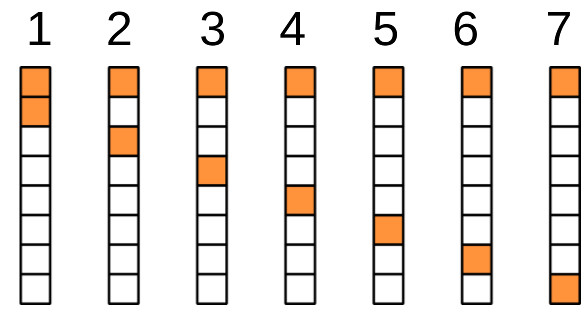


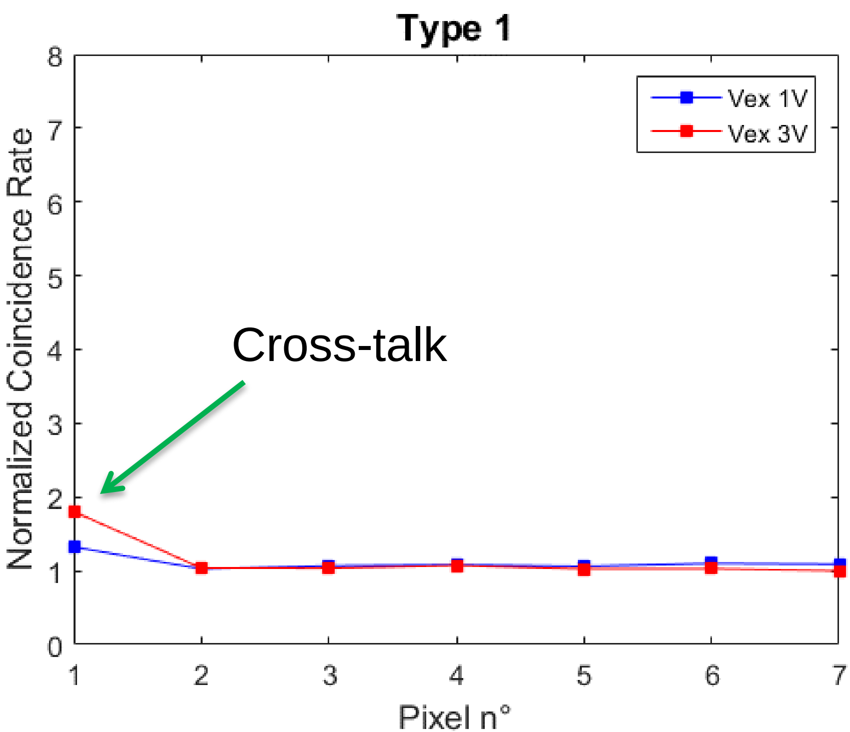
Band – to – band tunneling: $E_A \rightarrow 0$

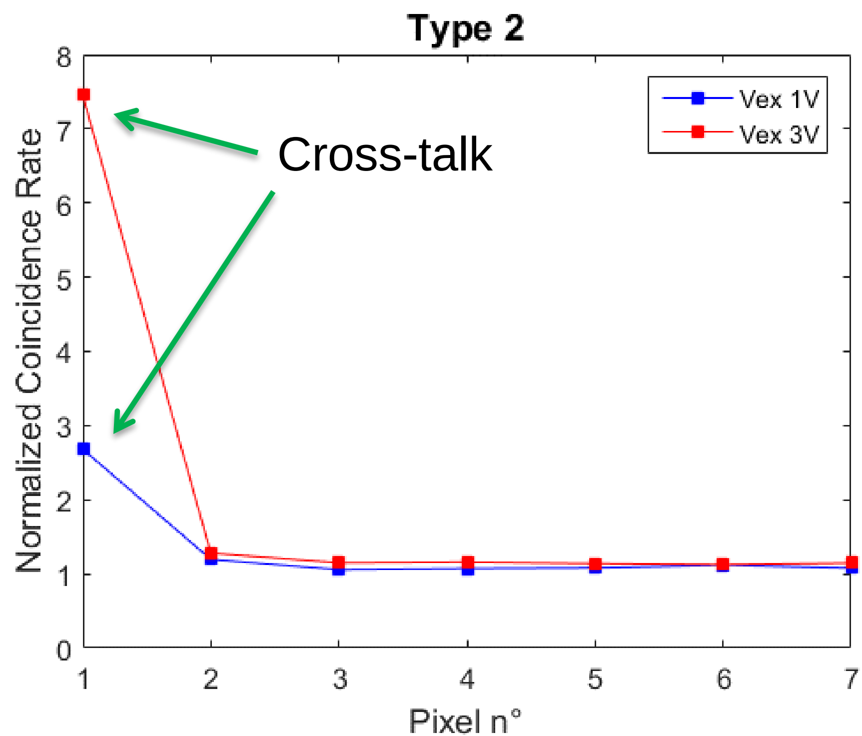
Coincidence detection

Count rate in coincidence between two pixels in the same column

Normalized rate: $\dfrac{CR_{Meas}}{2 \cdot CR_1 \cdot CR_2 \cdot \Delta T}$

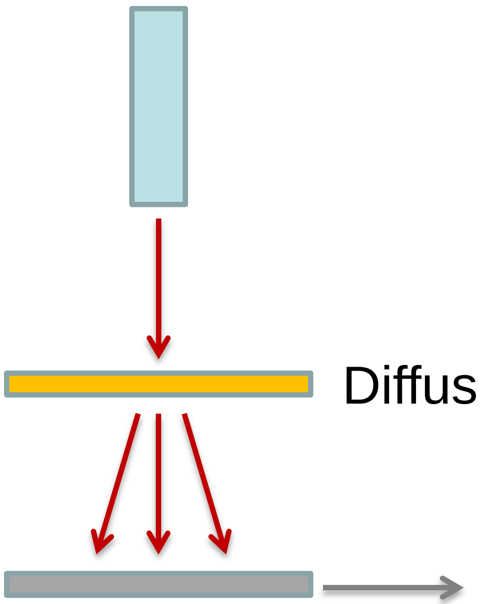






Timing resolution

IR laser (780nm)
50ps FWHM

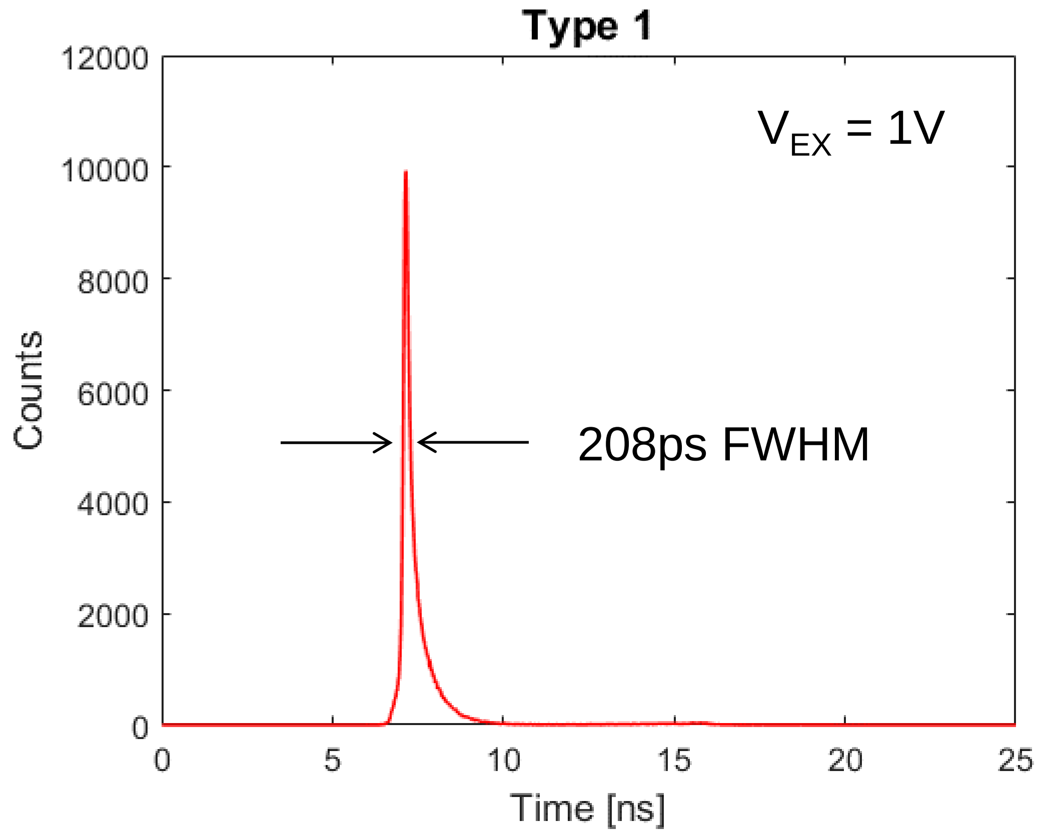


Diffuser

Sensor

Row coinc. output

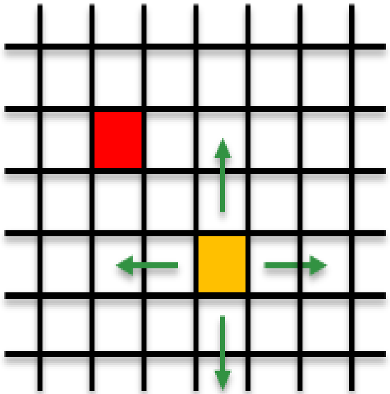
2 pixels enabled



Timing histogram between laser trigger and sensor coincidence output

N.B. Design not optimized for timing

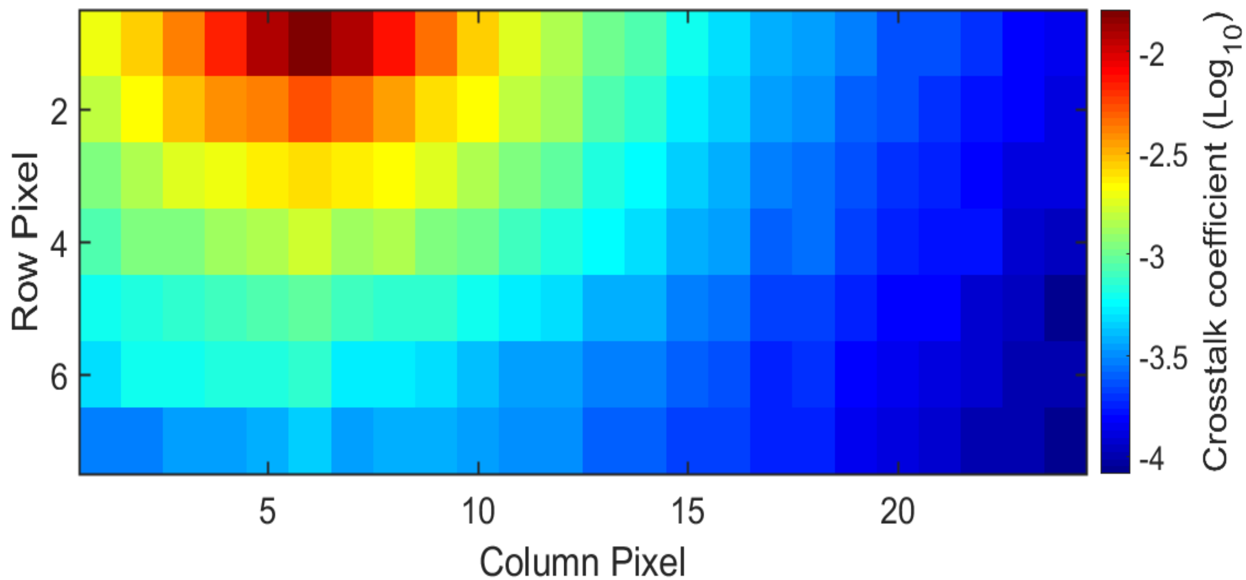
Crosstalk characterization



- Crosstalk coefficient

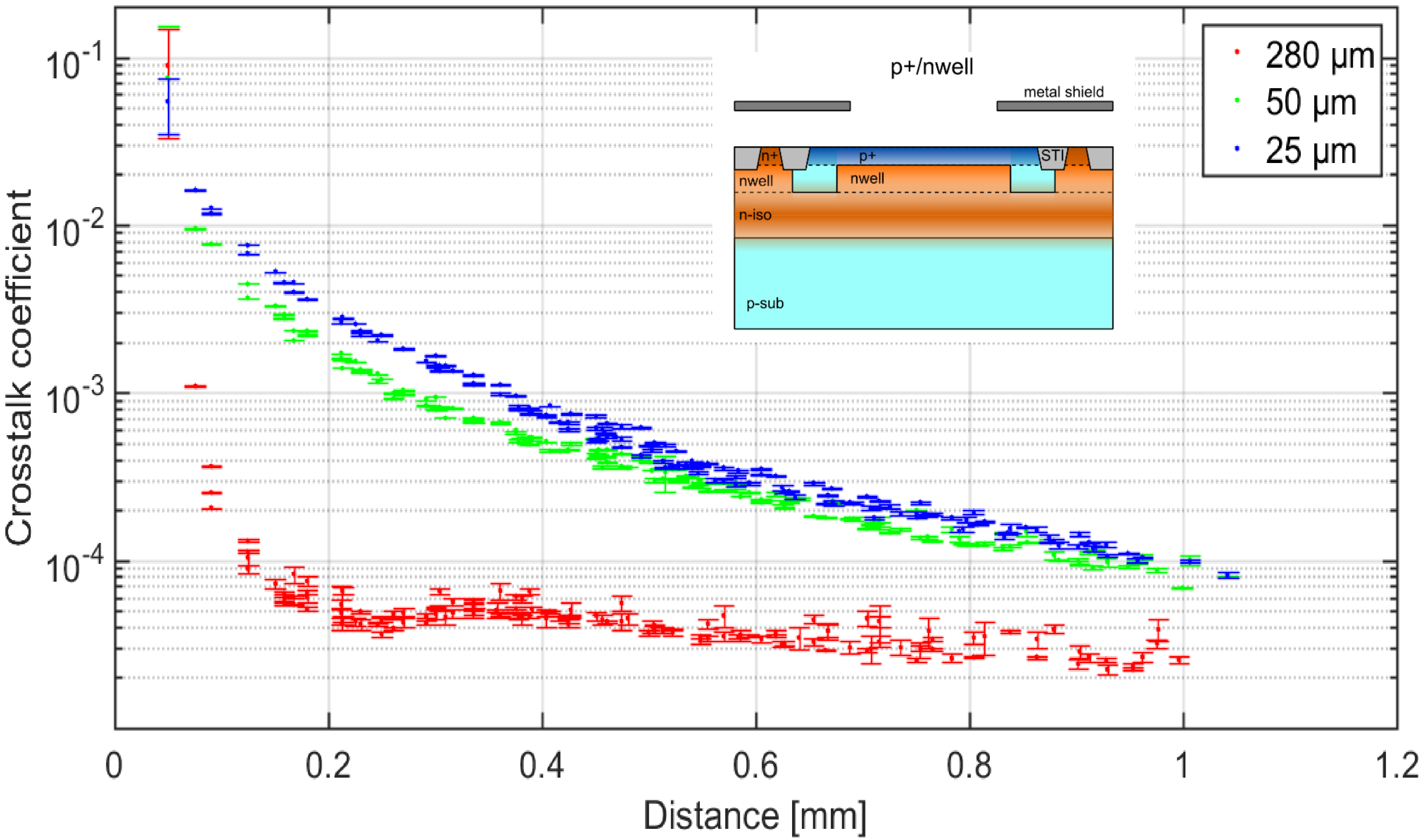
$$CR_m = DCR_e \cdot DCR_d \cdot 2\Delta T + \mathbf{K} \cdot (DCR_e + DCR_d)$$

- **Emitter** (fixed)
- **Detector** (scan)



Crosstalk map – Type 1, 25µm thickness

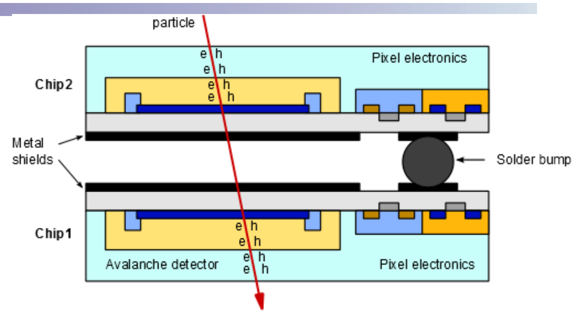
Crosstalk vs substrate thickness

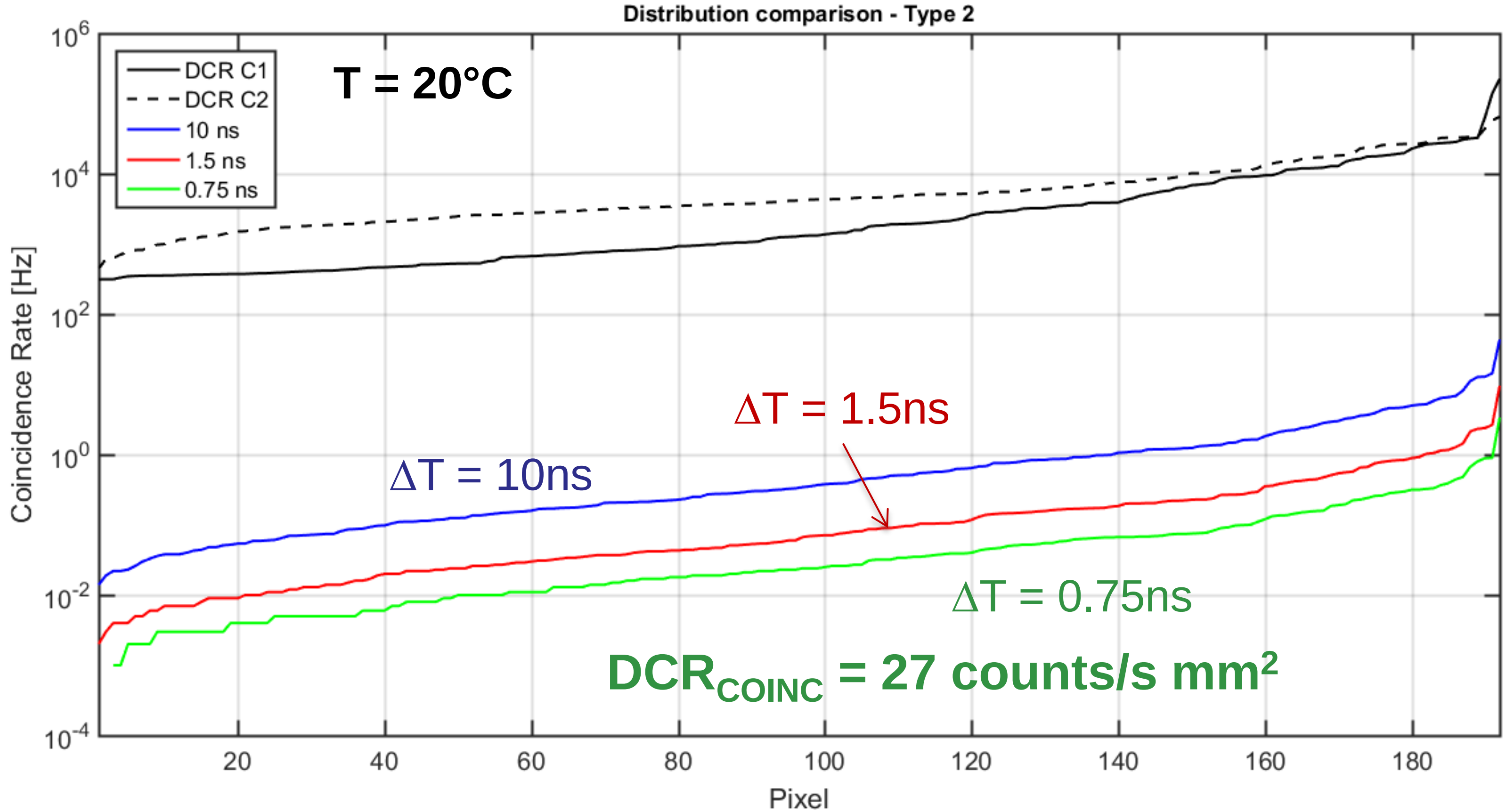


Vertically-integrated assembly

Dark Count Rate vs. coincidence time ΔT

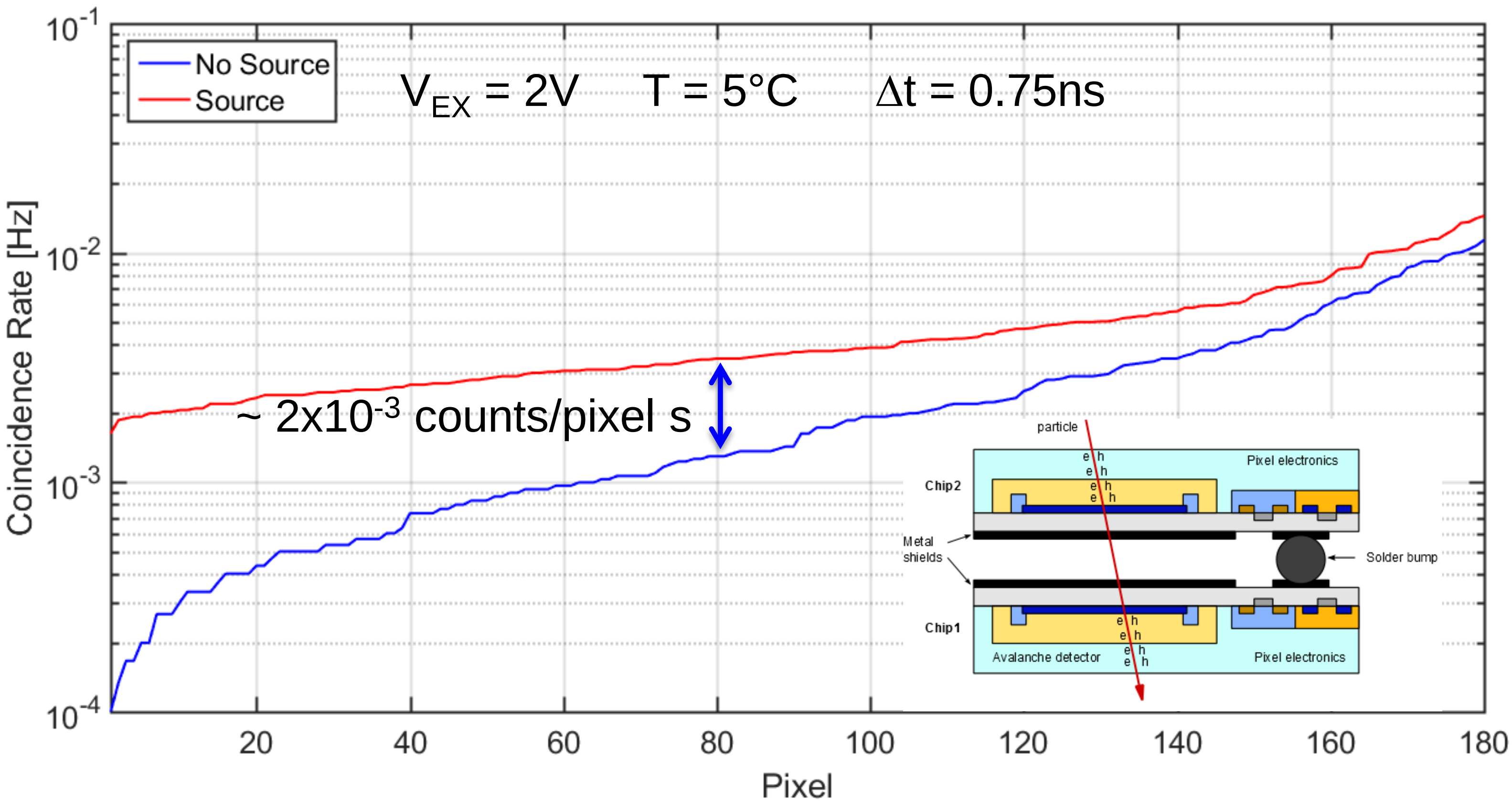
$$DCR_{COINC} = DCR_1 \times DCR_2 \times 2\Delta T$$





β-source measurements

^{90}Sr β source – 37kBq at 2mm distance from sensor



Count rate ~**0.5 counts/s mm^2**

APiX - Summary

Strengths:

- Can be thinned to a **few microns**: low material budget
- **Timing resolution**
- Low **power consumption**
- Early signal digitization

Weaknesses:

- Radiation tolerance (still to be assessed)
- Efficiency: guard ring and in-pixel electronics
- Cost and availability of 3D integration technologies

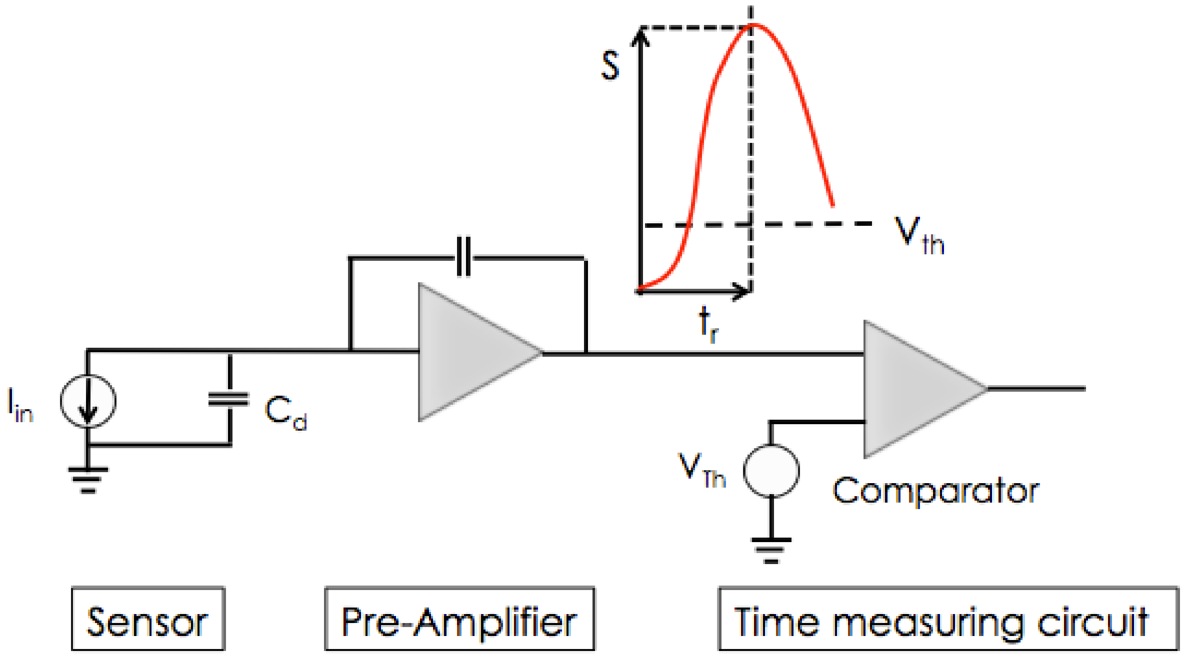
Current - future work

- Current prototype:
  - **Test beam** data analysis (in progress)
  - Radiation hardness studies
- Design of **new prototype**:
  - Improved fill factor
  - Larger array
  - Optimized timing

Outline

- Introduction
- APiX: Geiger-mode avalanche pixel detectors for ionizing particles
- Low Gain Avalanche Detectors
- 3D detectors
- PixFEL: a pixelated detector for application at future XFEL facilities

Time-tagging detectors



Time is set when the signal crosses the comparator threshold

The timing capabilities are determined by the characteristics of the signal at the output of the pre-Amplifier and by the TDC binning.

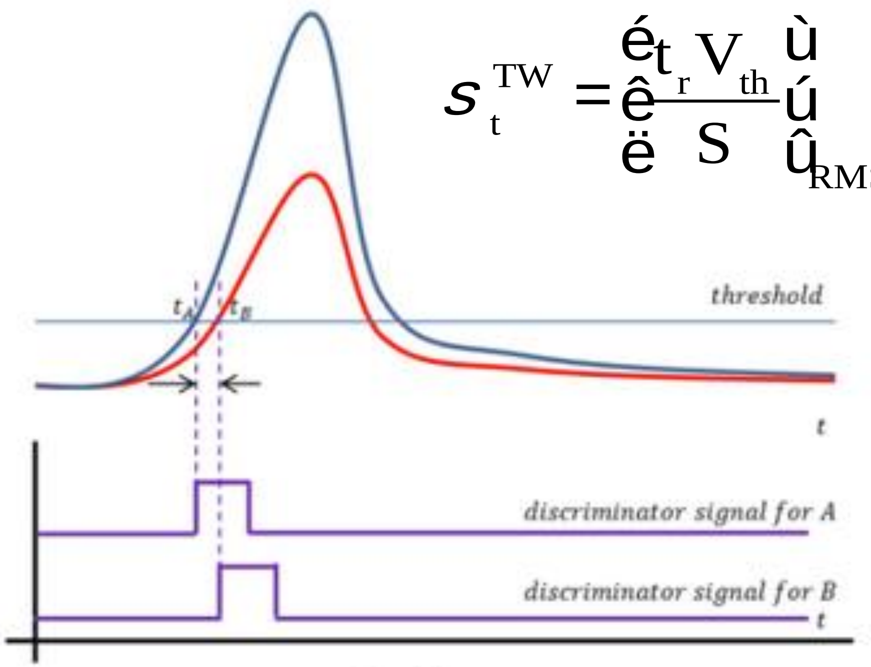
Strong interplay between sensor and electronics

2 important effects: Time walk and Time jitter

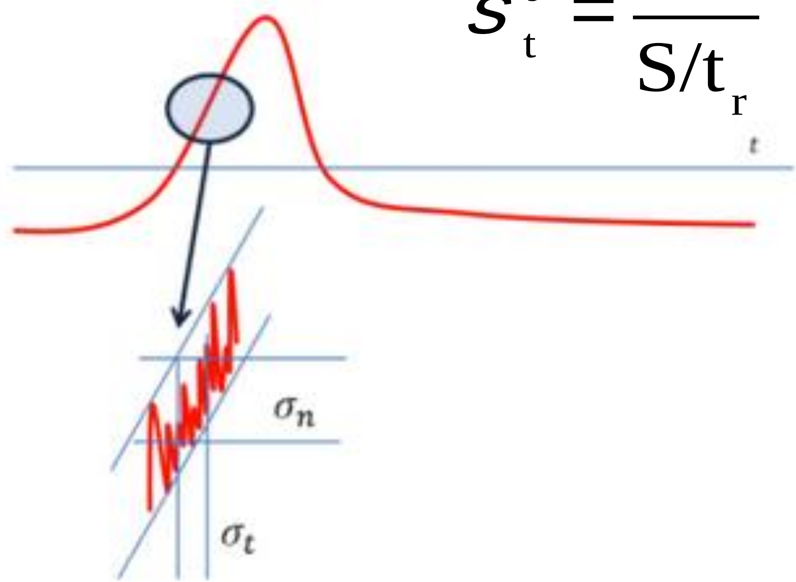
Time walk: the voltage value V_{th} is reached at different times by signals of different amplitude

Jitter: the noise is summed to the signal, causing amplitude variations

$$\sigma_t^{TW} = \left[\frac{t_r V_{th}}{S}\right]_{RMS}$$



$$\sigma_t^{J} = \frac{N}{S/t_r}$$



Due to the physics of signal formation

Mostly due to electronic noise

Time walk and jitter ~ $1/(S/t_r) = 1/(dV/dt)$

Time resolution

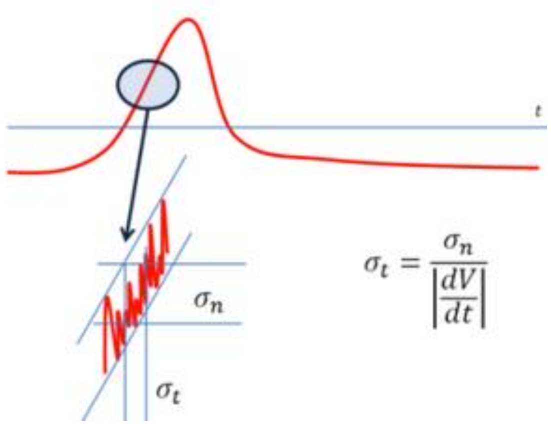
$$\sigma_t = \left(\frac{N}{dV/dt}\right)^2 + (\text{Landau Shape})^2 + \text{TDC}$$

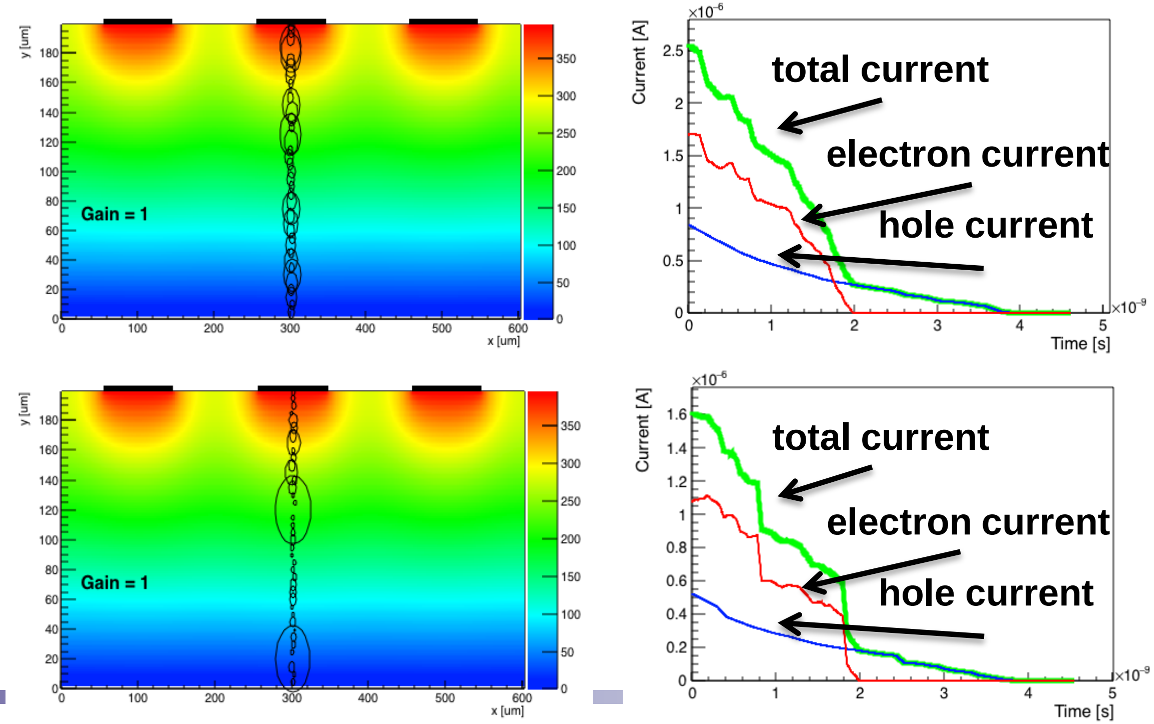
Usual "Jitter" term

Here enters everything that is "Noise" and the steepness of the signal

Time walk: time correction circuitry

Shape variations: non homogeneous energy deposition





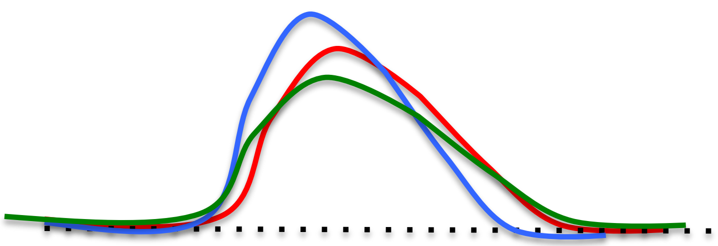
Not all geometries are good

Signal shape is determined by Ramo's Theorem:

$$i \;\mu\; qvE_w$$

Drift velocity

Weighting field

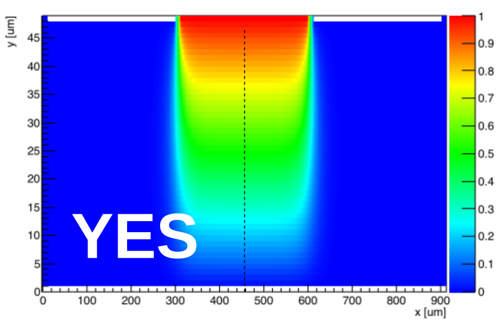


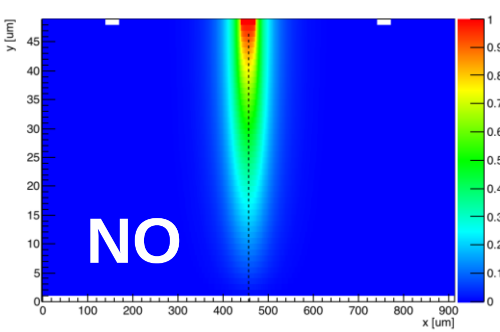
The key to good timing is the uniformity of signals:

Drift velocity and **Weighting field** need to be **as uniform as possible**

Basic rule: parallel plate geometry: strip implant ~ strip pitch >> thickness

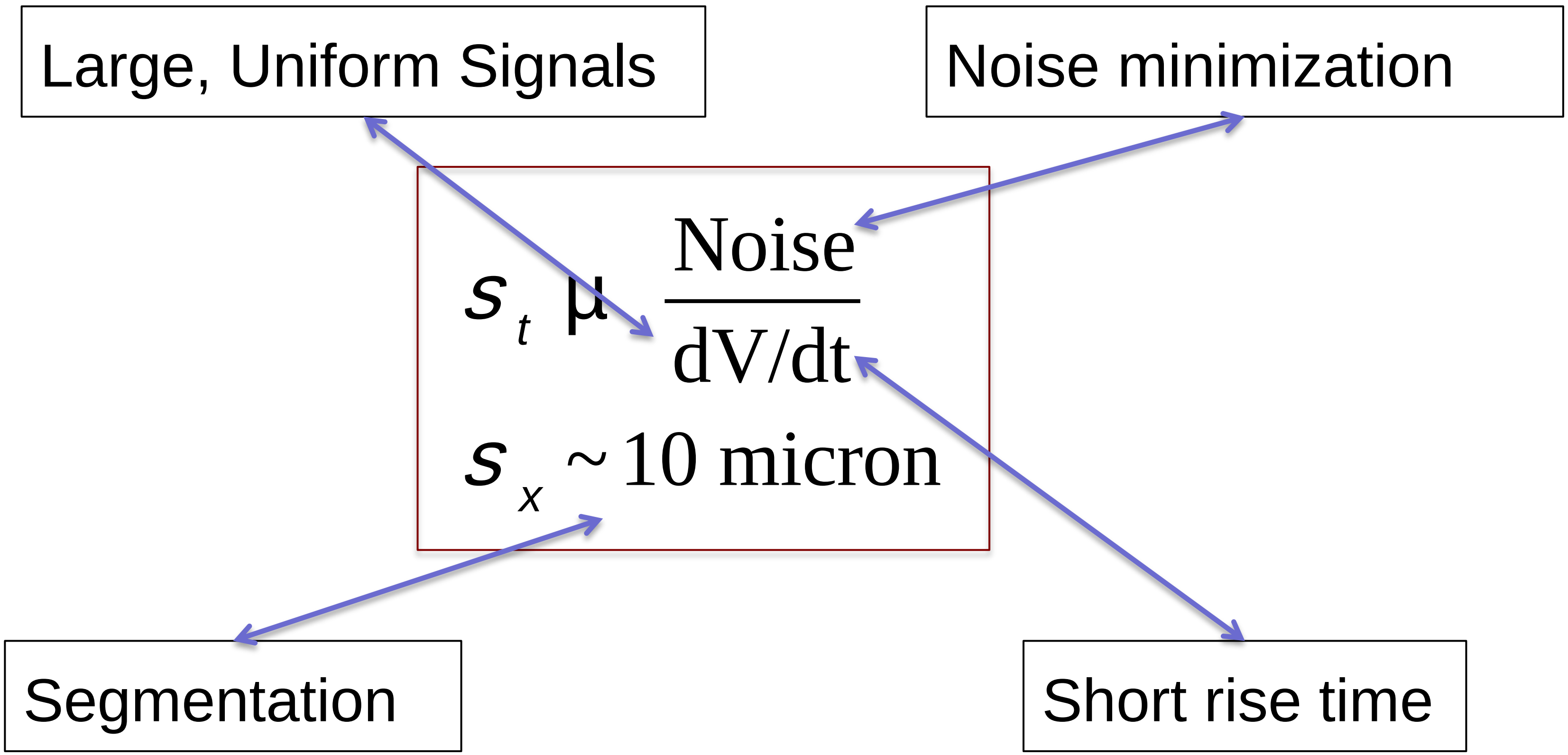
Everything else does not work



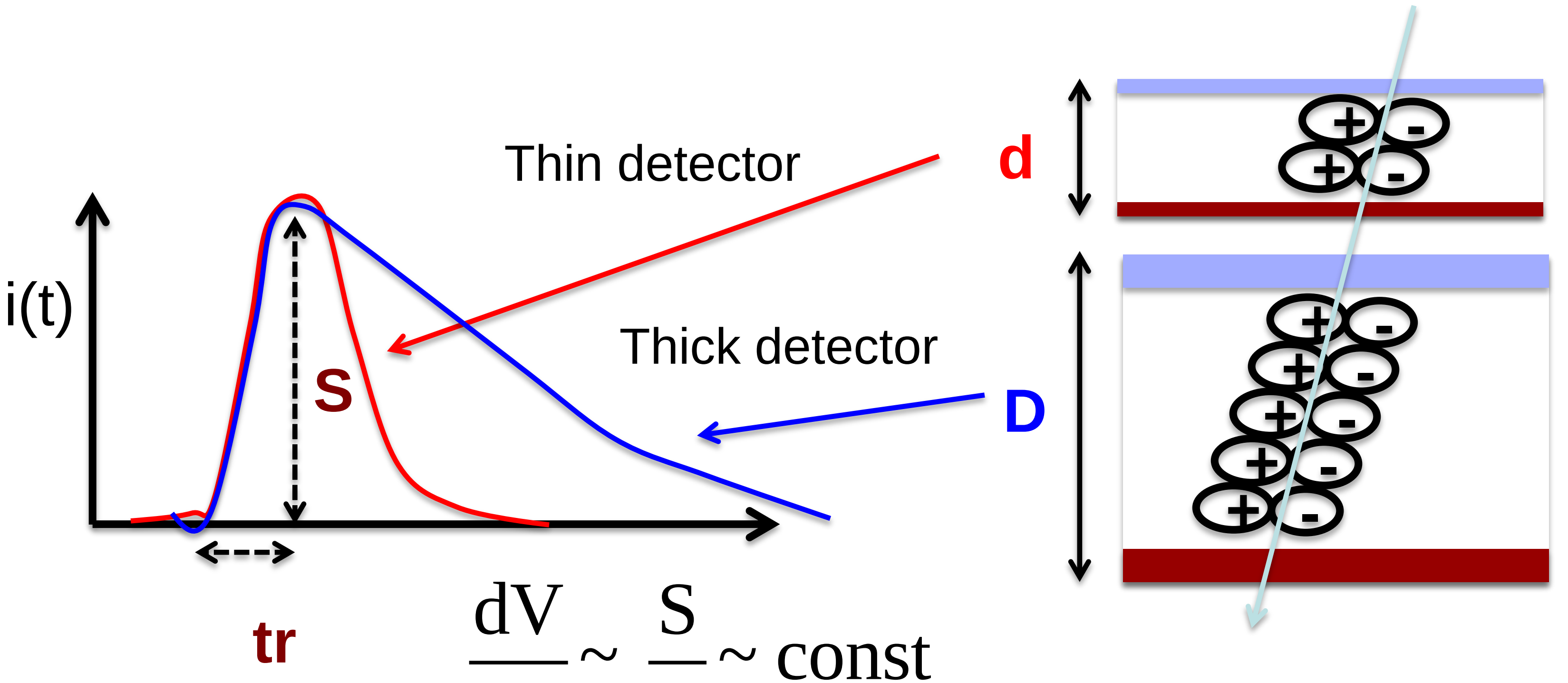


4-Dimensional High Precision Tracking

The R&D program



Thin vs Thick detectors



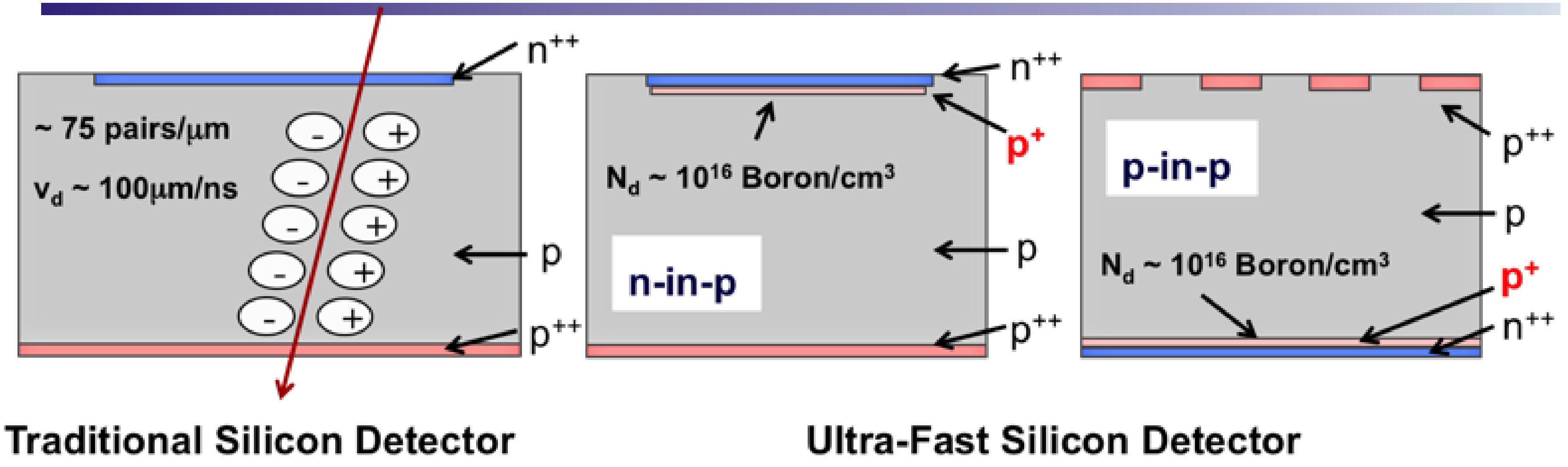
$$\frac{dV}{dt} \sim \frac{S}{t_r} \sim \text{const}$$

Thick detectors have longer signals, not higher signals

Best result : NA62, 150 ps on a 300 x 300 micron pixels

How can we do better?

LGAD - Ultra-Fast Silicon Detector



Highly doped p-implant near the p-n junction:

High electric field that accelerates the electrons enough to start multiplication.

Same principle of reach-through APDs, but with much lower gain.

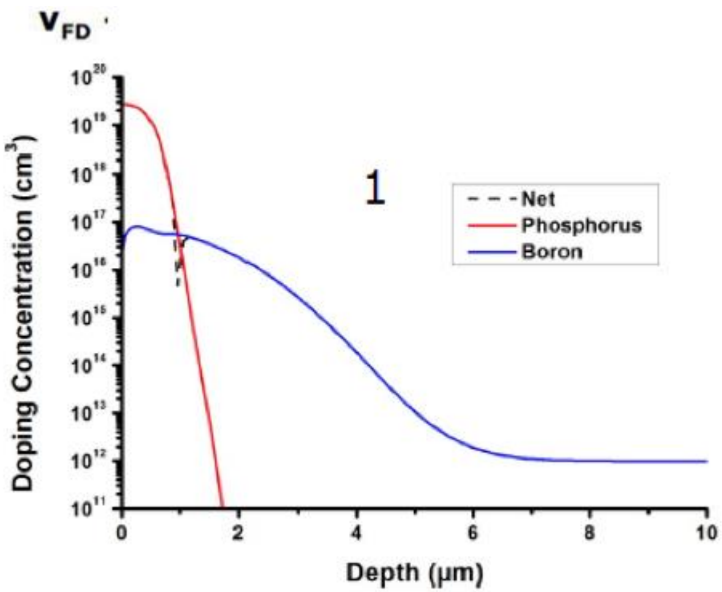
Gain changes very smoothly with bias voltage.

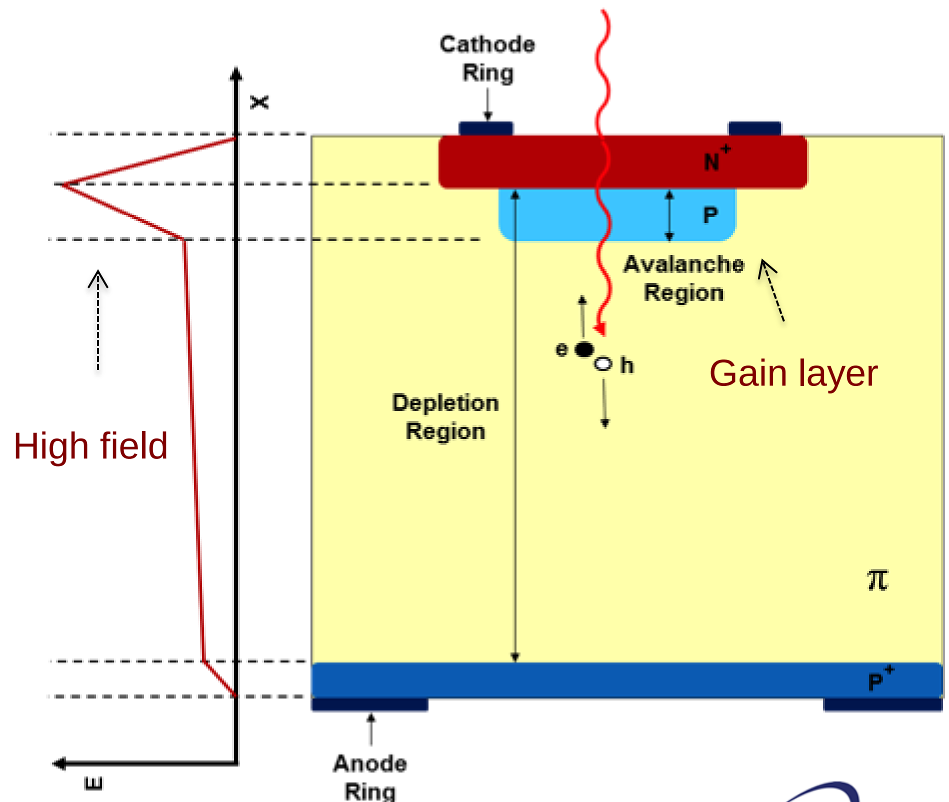
⬇

Easy to set the value of gain requested.

Low Gain Avalanche Detectors (LGADs)

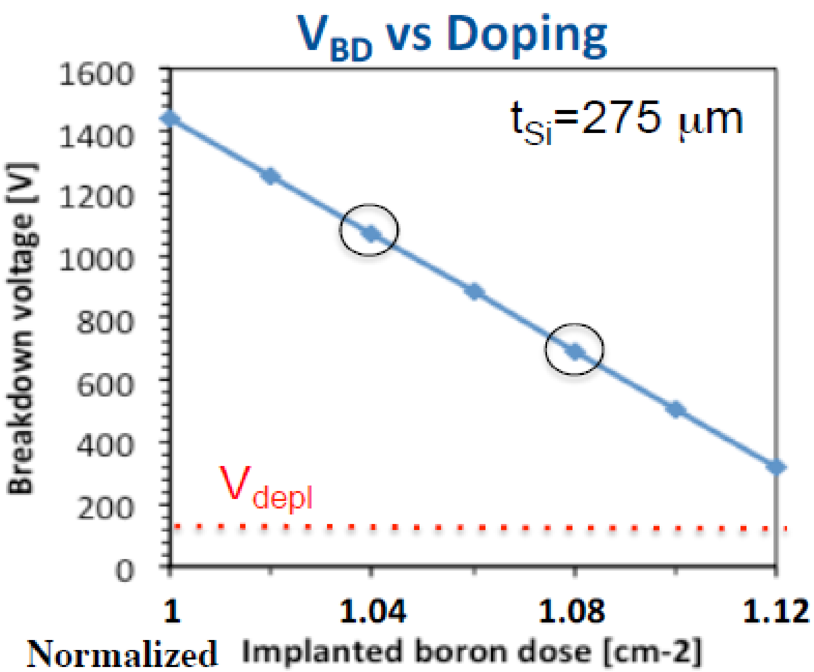
- LGAD sensors: high field near the surface
- First produced at CNM, Barcelona
- E ~ 300 kV/cm, close to breakdown voltage

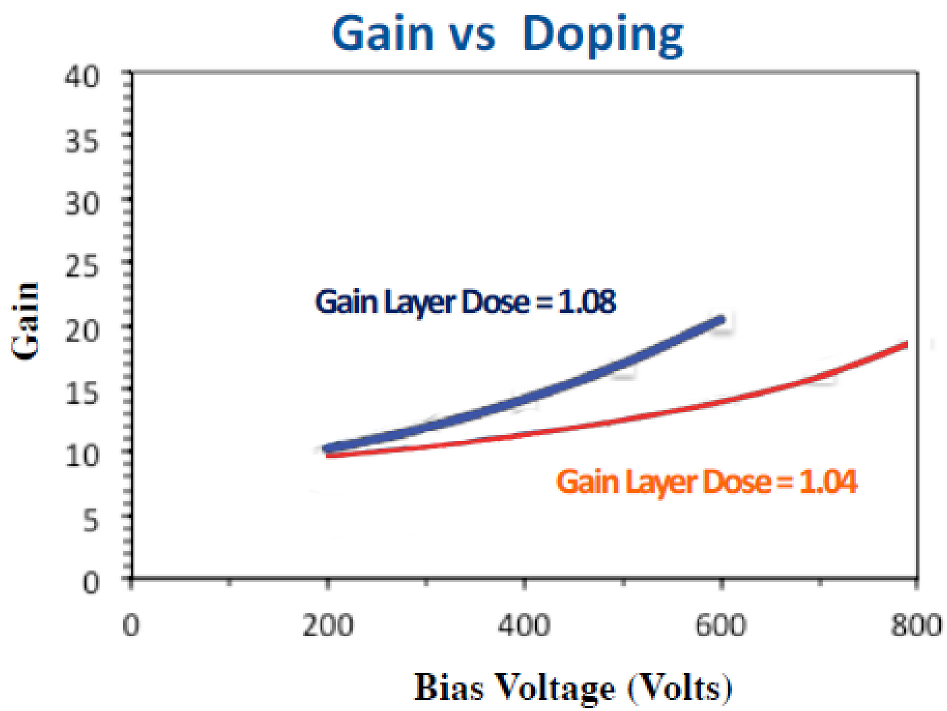




Design of the gain layer

- The Gain Layer doping profile has been **finely tuned** to reach the target Gain and high Breakdown Voltage





Both the Gain and the Breakdown Voltage are very sensitive to the doping level of the gain layer!

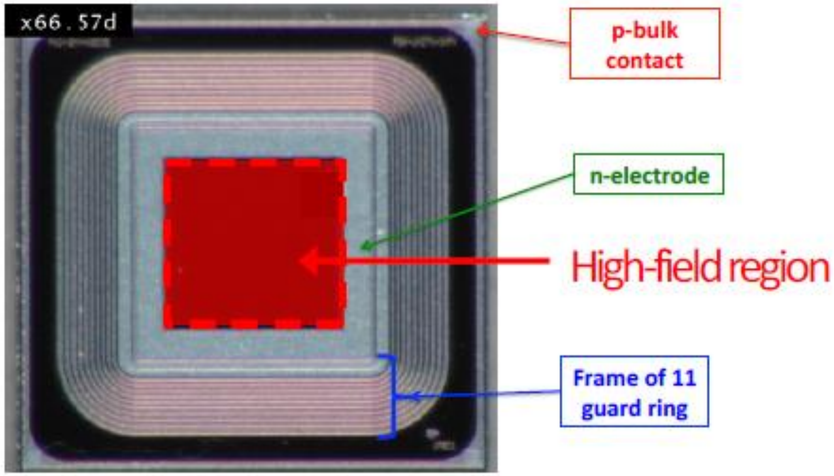
Trento UFSD technology

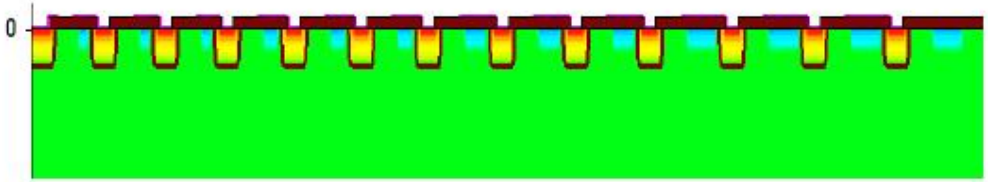
Edge termination

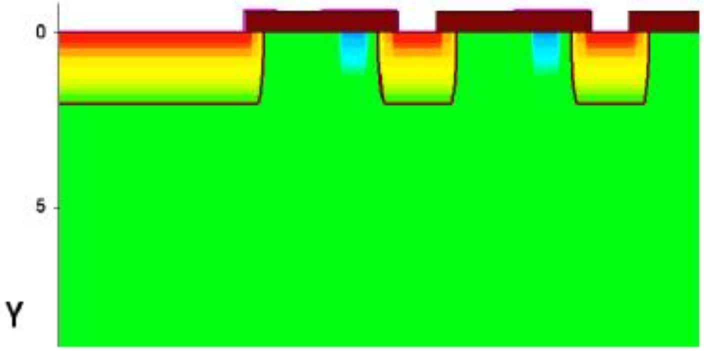
Goal: design an edge termination structure able to support $V_{BD} > 1000V$ after irradiation!

- 12 rings Guard-ring structure supporting n-deep and p-stop rings
- Radiation damage is taken into account ($N_{OX} = 1e12$) in simulations

Simulated Breakdown = 1270 Volts After irradiation!

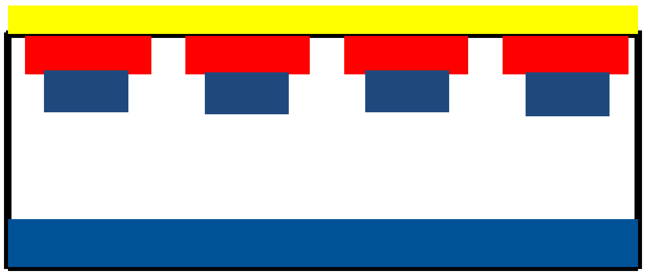






Detector segmentation

3 different approaches:

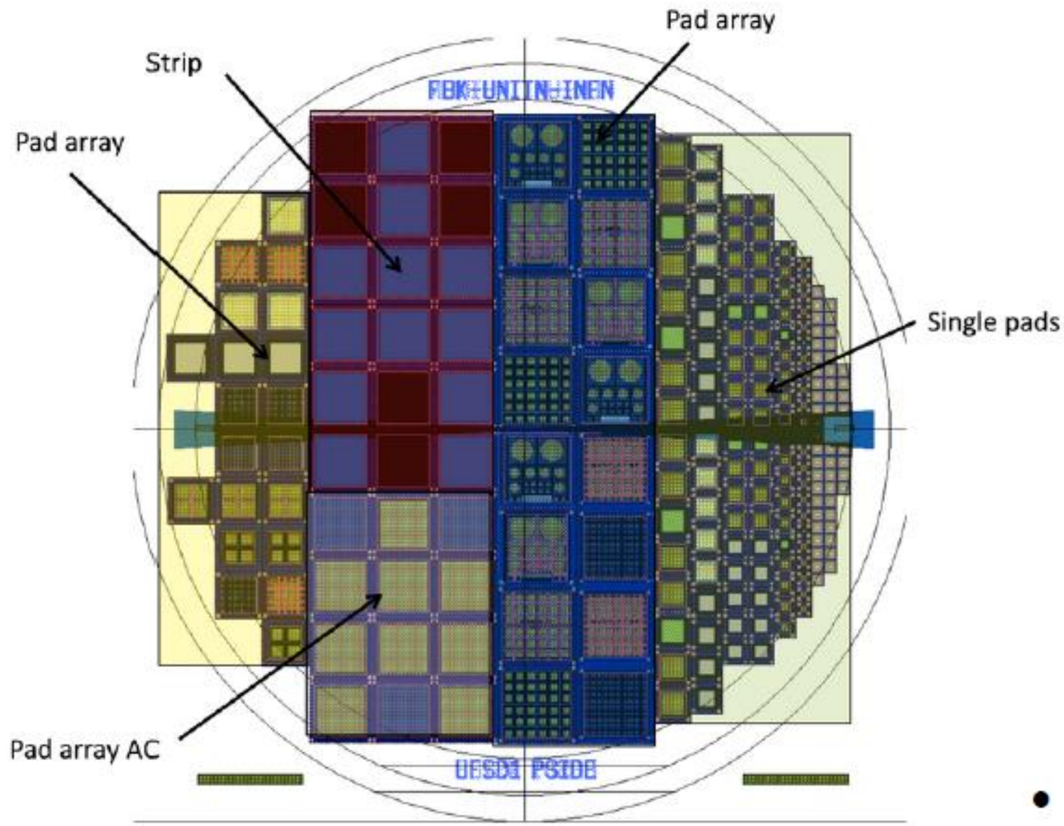


1. N-side segmentation: both n+ and the gain layers are segmented (some concerns about E field uniformity)

2. P-side segmentation: the p layer opposite to the gain layer is segmented (the signal from holes is read -> worse timing)

3. AC coupling: The signal is frozen on the resistive sheet, and it's AC coupled to the electronics

First UFSD production at FBK



Wafer Layout for the 300µm production

Characteristics:

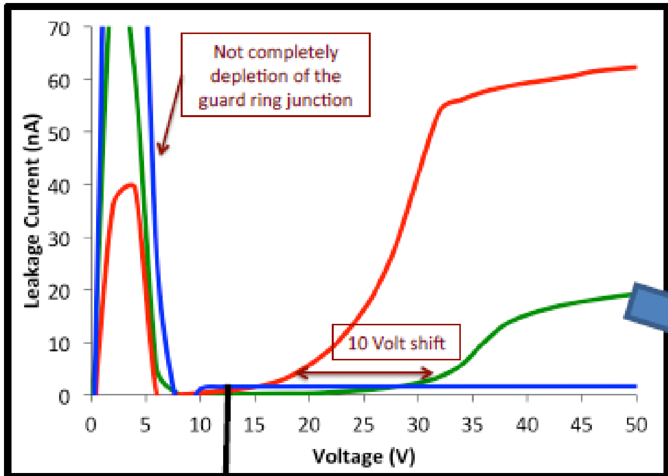
- Thickness 300µm;
- 13 Wafers produced;
- 5 Splits of gain in 2% steps;
- Multiple structures (single pad, multi-pad, array, strip);
- n-side segmentation;
- p-side segmentation;

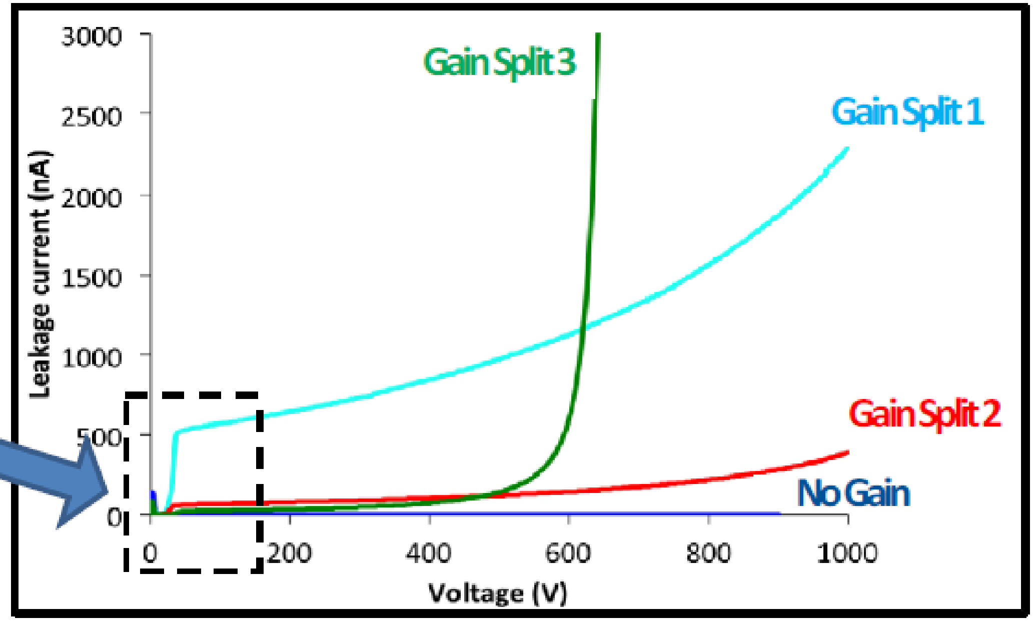
Goals of this production:

- **Investigate the gain layer**
- **Demonstrator of LGAD technology at FBK**

UFSD characterization

I-V curves





The foot at low voltage indicates the indicates the depletion of the gain layer.

The Breakdown Voltage decreases by increasing the gain layer doping

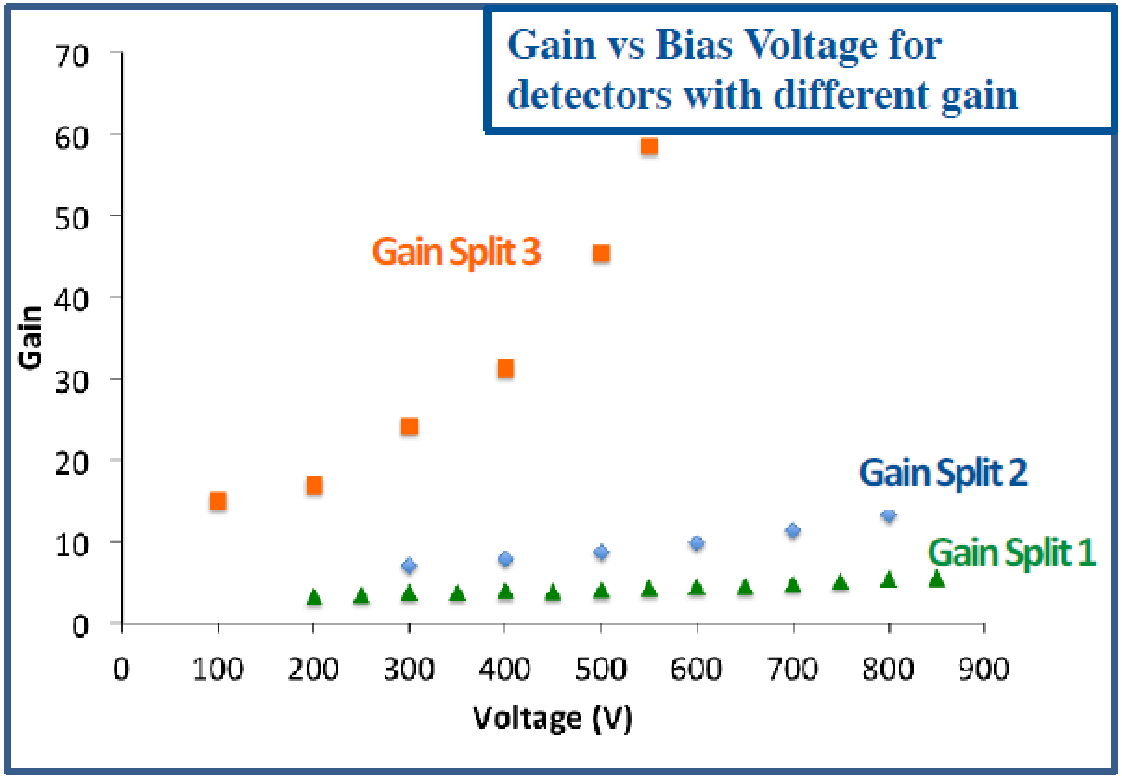
Simulated BD:

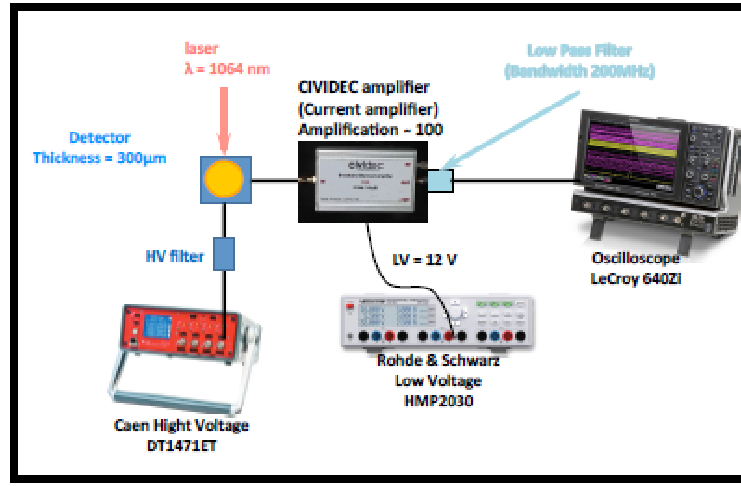
Split 1: 1100 Volts

Split 2: 880 Volts

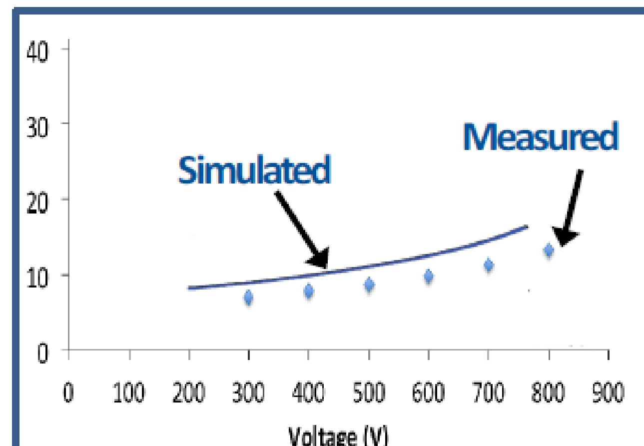
Split 3: 500 Volts

UFSD characterization: gain





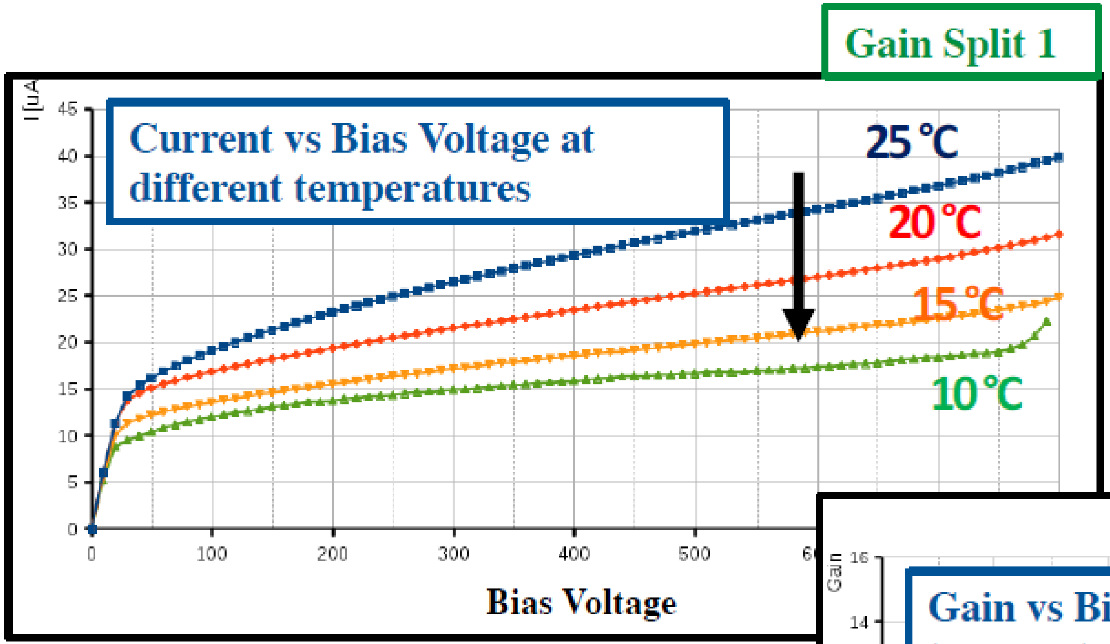
Gain measured with a laboratory setup by using a laser at 1064 nm



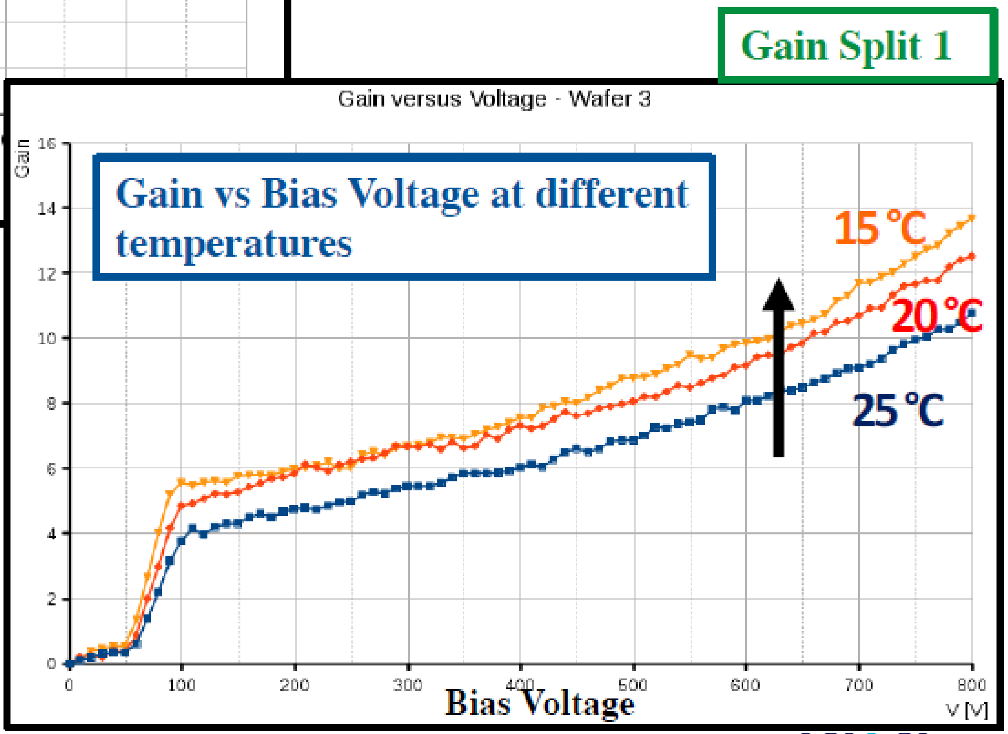
Good agreement between simulated and measured Gain.

INFN Istituto Nazionale di Fisica Nucleare

UFSD characterization vs. Temperature

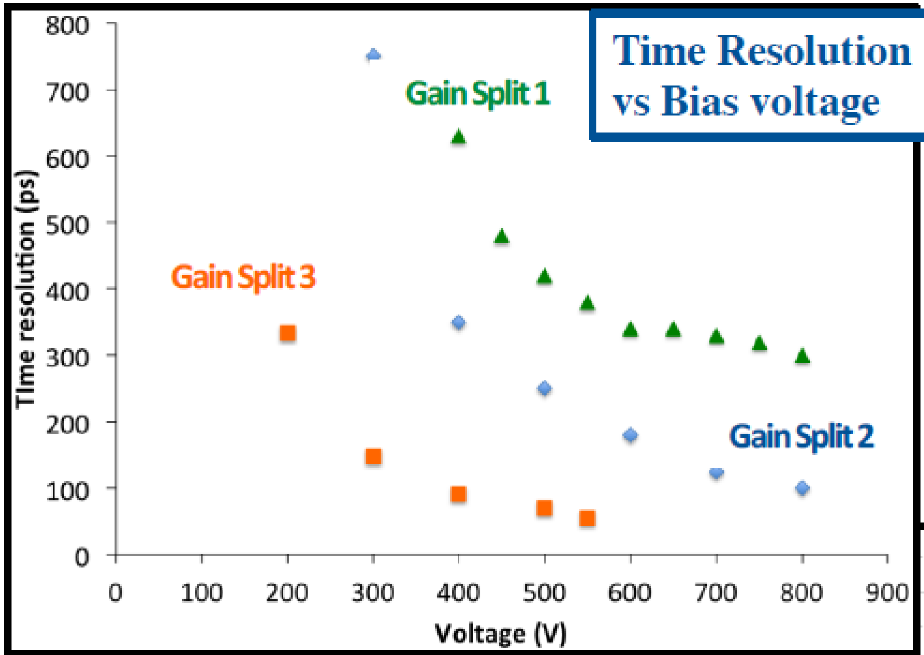


- decreasing of the leakage current in the sensor (thermal noise)



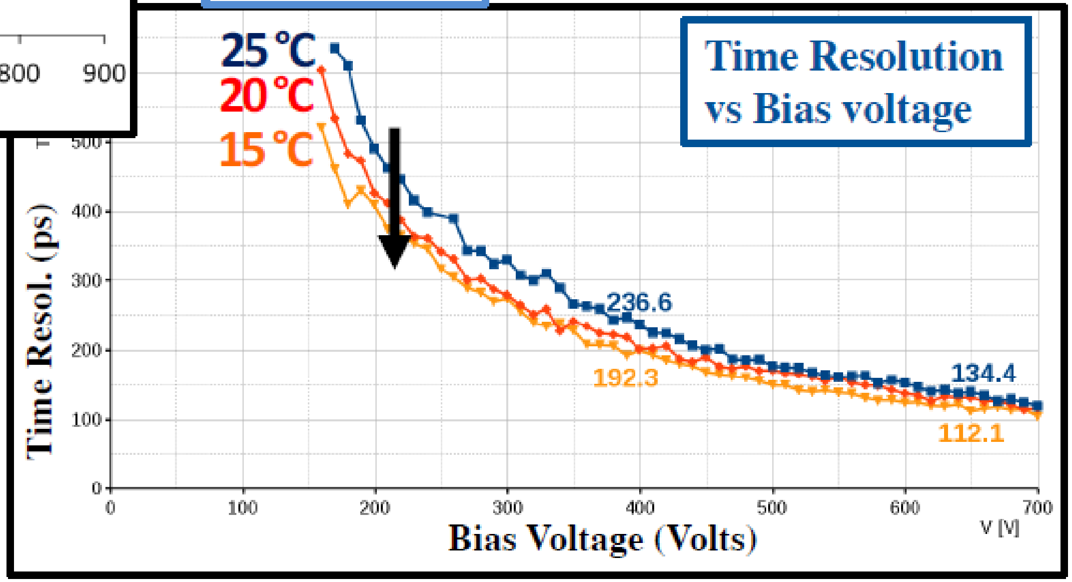
- The impact ionization rates vary greatly with temperature leading to an increase of the gain

UFSD characterization: timing



Gain Split1: σ_t(@800V) ≃ 300ps
Gain Split2: σ_t(@800V) ≃ 90ps
Gain Split3: σ_t(@550V) ≃ 55ps

Gain Split 2

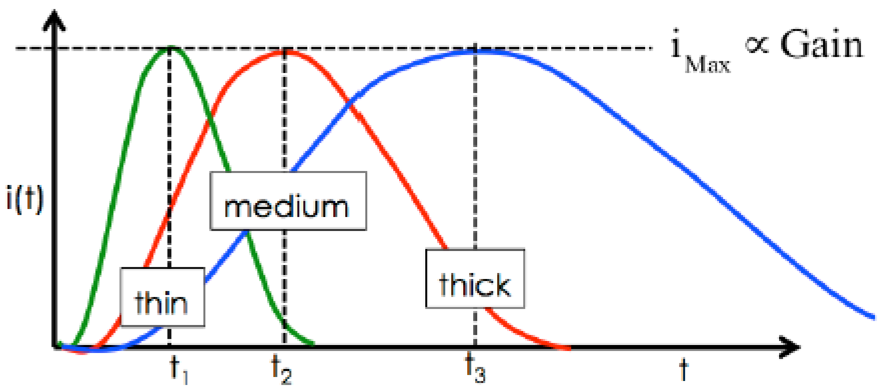


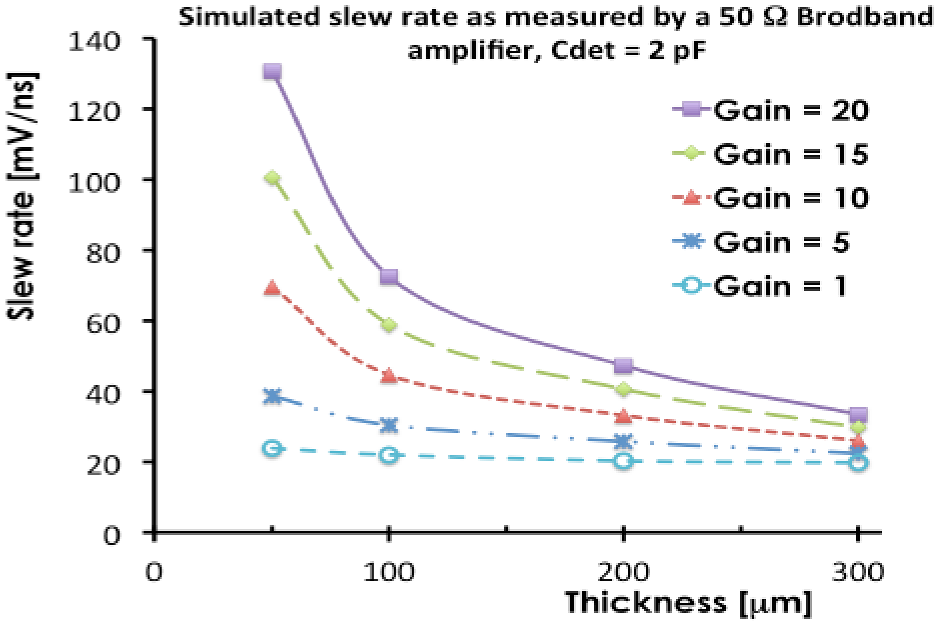
Very good timing performance obtained with the two splits with higher gain (considering a 300µm thick substrate!)

Next activities

The slew rate:

- Increases with gain
- Increases ~ 1/thickness



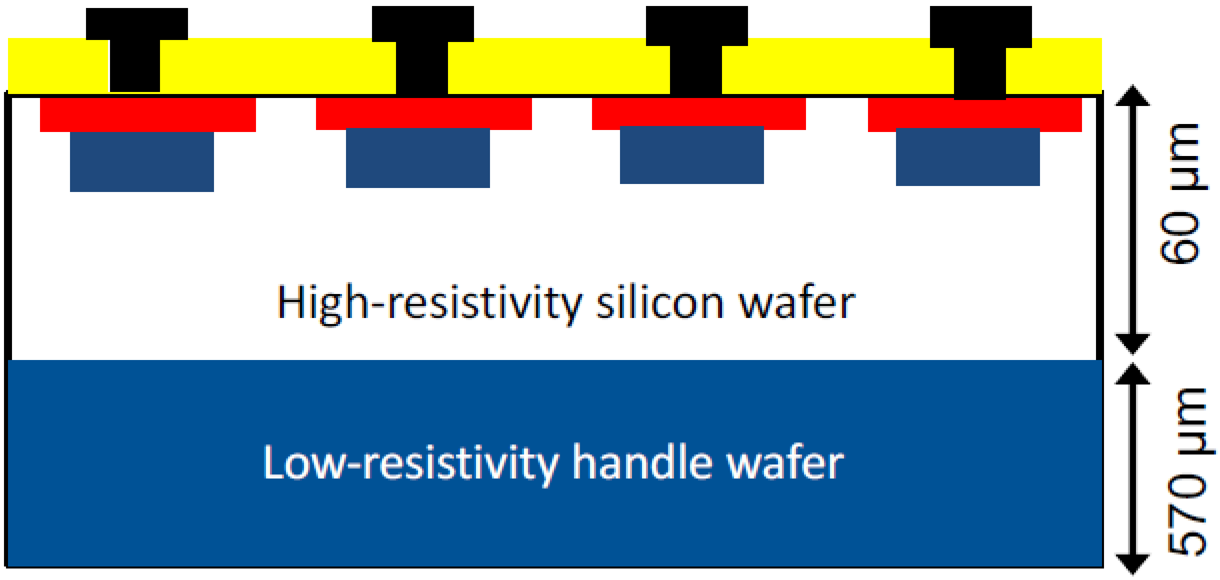


Improvements in timing resolution requires thinner detectors!

N. Cartiglia presented at AIDA 2020 annual meeting, Hamburg 2016

Next activities

A new production batch on 60µm thick substrates will start soon in FBK



- 60 µm active thickness
- Single side process
- N+ segmentation
- Single pads, pixel arrays and strips

LGAD - summary

- First production run in FBK:
  devices are fully functional and perform according to simulations.
- Main features:
  - Breakdown voltage: 500V - >1000V (depending on split)
  - Gain: 5 – 40
  - Excellent timing resolution (for 300 μm)
- The production of a **60-μm thickness** production run will start soon: improved timing resolution expected