

## SNRI Lab session 1

Characterization of a new type of  
CMOS Geiger mode pixel detector

- 1) Introduzione chip APIX
- 2) Misure e Strumenti

G.Collazuol  
E.Fioretto  
R.Stroili

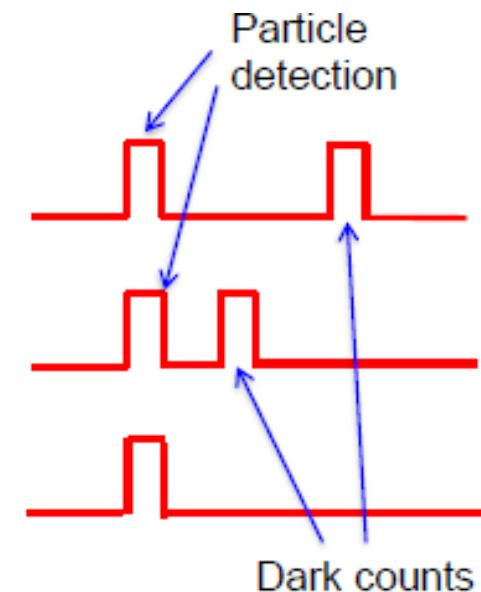
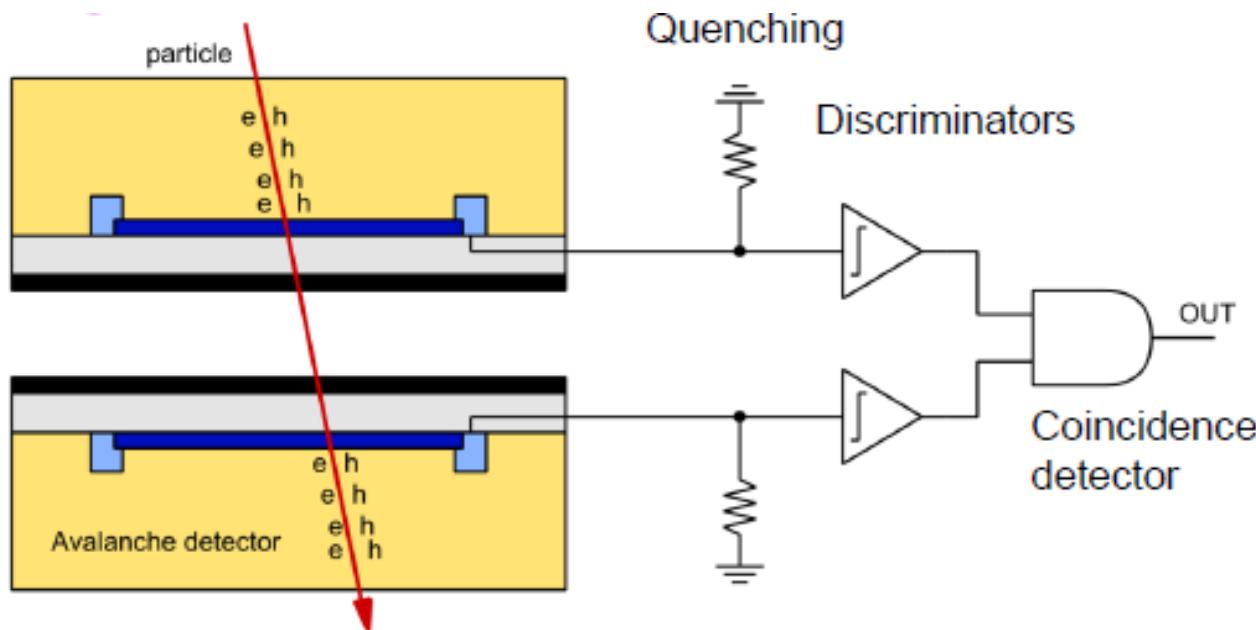
# The Avalanche Pixel Sensor (APIX) concept

**Innovative Silicon tracker** based on

- 1) thin sensitive volumes (pixels)
- 2) producing large signals
- 3) high timing resolution



- reduced material budget
- reduced power consumption
- enhanced S/N → “simple” electronics
- better radiation hardness
- high rate capability



- Two Geiger-mode avalanche detectors in **coincidence**:  
$$DCR = DCR_1 \times DCR_2 \times 2\Delta T$$
- In-pixel coincidence: integrated electronics is needed:  
**CMOS avalanche detectors**

# The APIX2 Project

"Development of an Avalanche Pixel Sensor for tracking applications"

Funded by **INFN** – CSN5

Project coordinator:

**Pier Simone Marocchesi**, INFN Pisa and University of Siena

Collaboration:

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F.Morsani<sup>1)</sup>, L.Pancheri<sup>3)</sup>, L.Ratti<sup>4)</sup>, A.Savoy-Navarro<sup>5)</sup>

- 1) University of Siena & INFN Pisa
- 2) University of Padova & INFN Padova
- 3) University of Trento & TIFPA
- 4) University of Pavia & INFN Pavia
- 5) Laboratoire APC, University Paris-Diderot/CNRS Paris

# Innovative silicon pixel sensor for charged particle → tracking and imaging

Physics, technology, preliminary results and context  
in the following talk

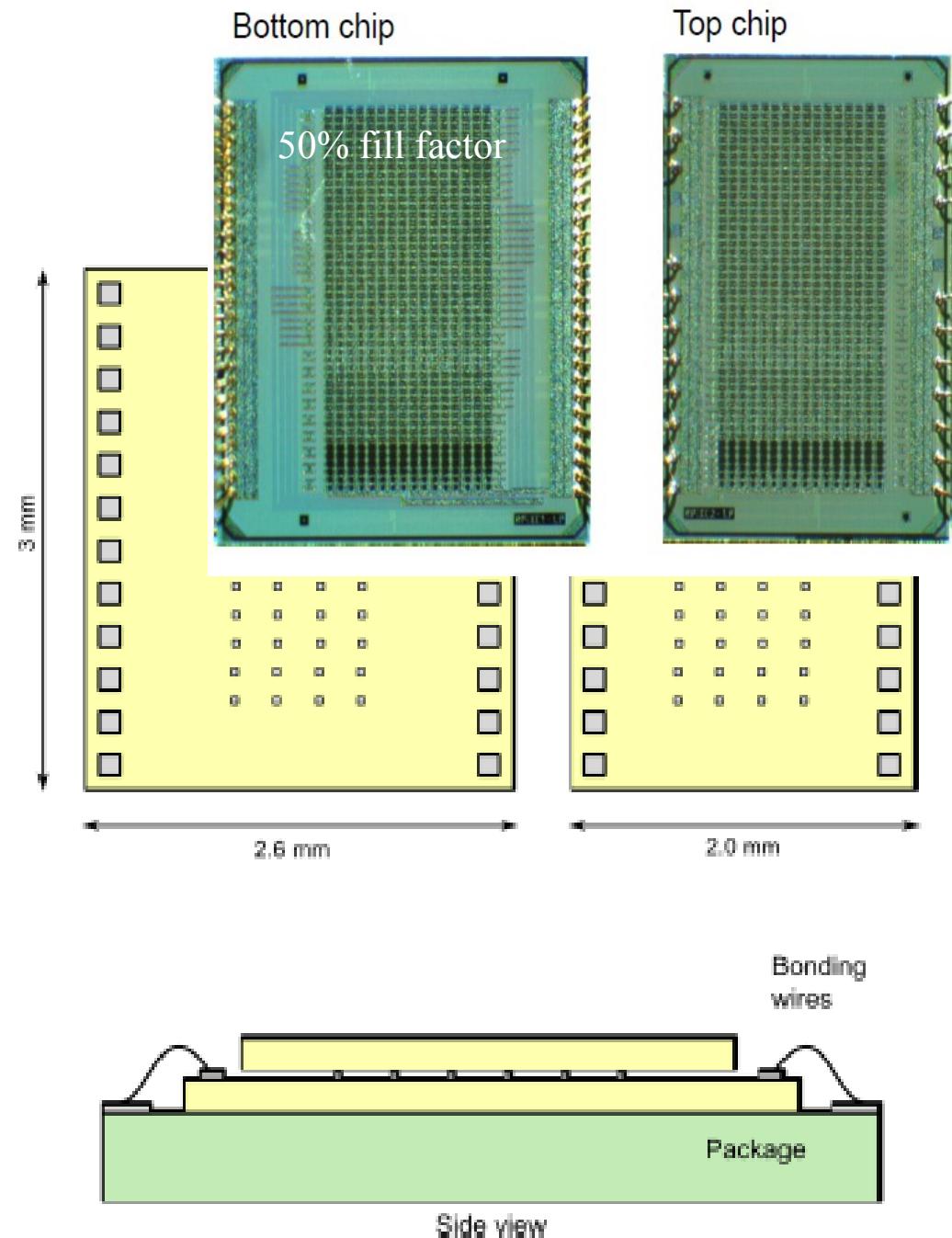
The status and the perspectives of  
the silicon 3D and 4D pixel detectors

by L.Pancheri ("father" of the APIX chips and...  
... author of almost all the following slides)

Lectures on Wed 23/10 and Thu 24/10 at 9:30

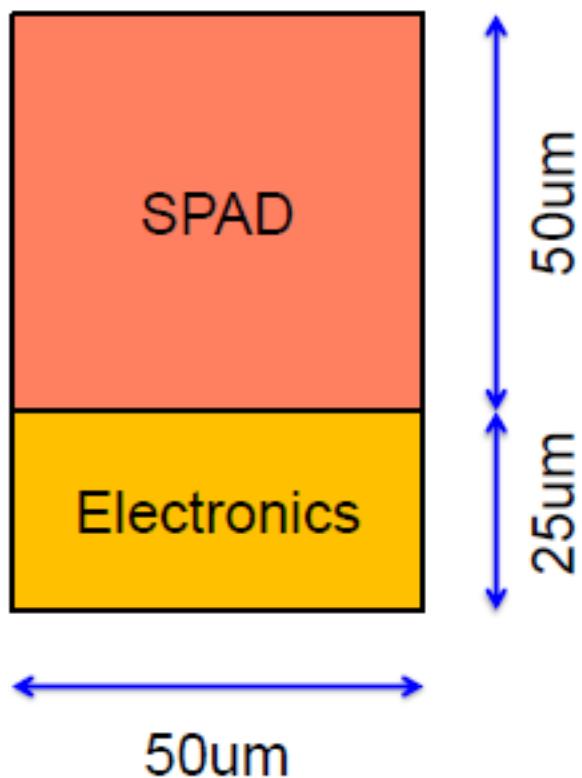
# APIX array prototype

- Process: LFOUNDRY 150nm CMOS
- 2 different chips: APIXC1 ( $8\text{mm}^2$ ) “father” and APIXC2 ( $6\text{mm}^2$ ) “son”
- Vertical interconnect: **per-pixel coincidence detection**
- Chips can be tested independently before vertical integration
- Chip-to-chip stacking (IZM bump bonding)
- Stacked sensor assembly:
  - Wire bonding on chip 1
  - Power supply and communication with top chip handled by bottom chip

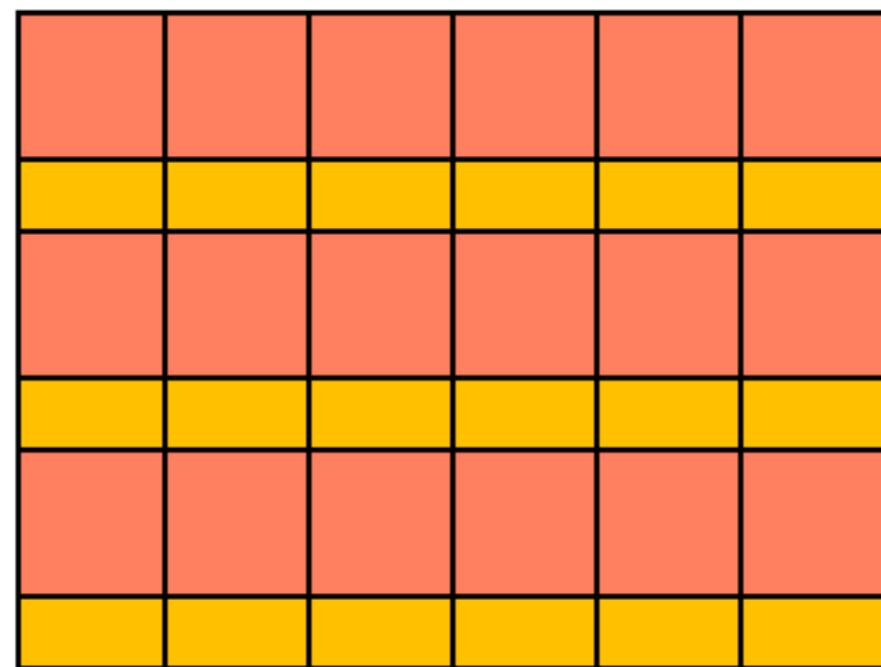


# Pixel layout

Single pixel



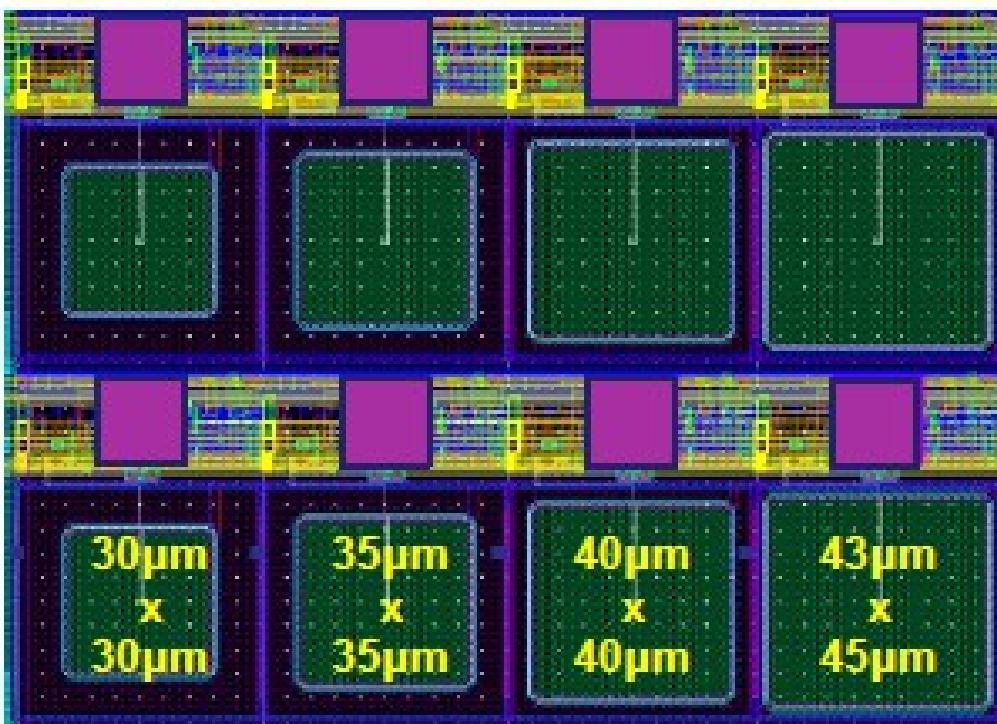
Array arrangement



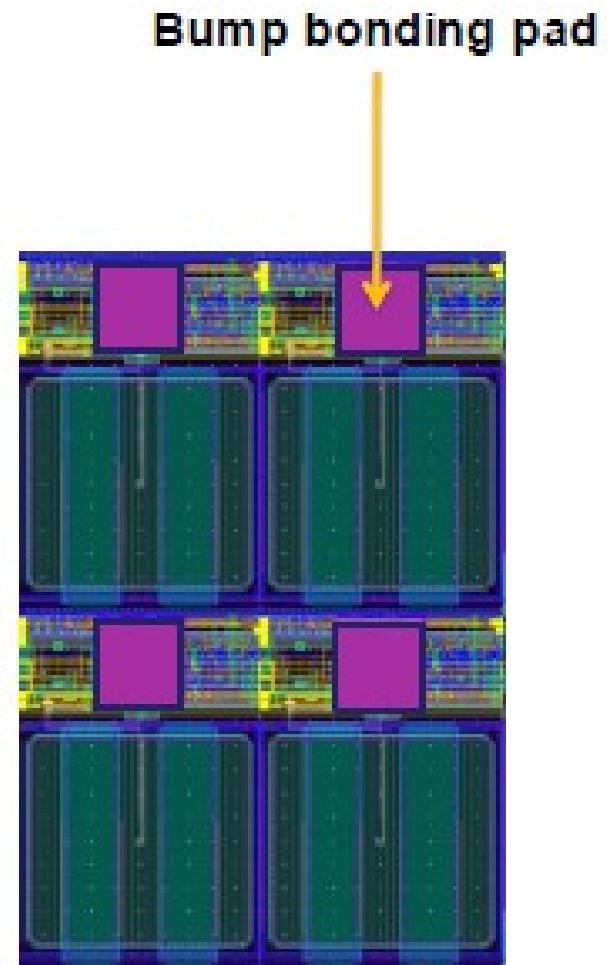
# Pixel array prototype

- 16 rows: total width  $16 \times 75\mu\text{m} = 1.2\text{mm}$
- 48 SPADs per row: total length  $48 \times 50 = 2.4\text{mm}$

- 16 x 48 pixel array
- Pixel size:  $50\mu\text{m} \times 75\mu\text{m}$
- Splittings in detector type and area

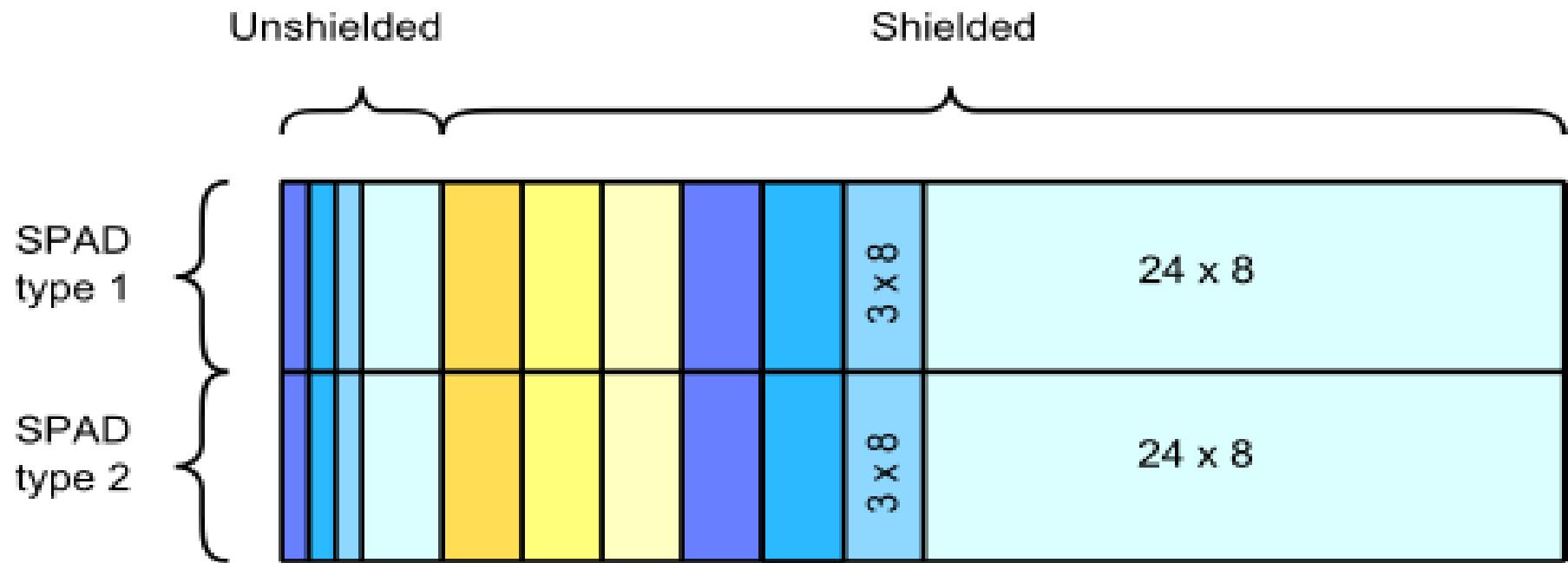


Pixels with different detector area  
(unshielded)



Pixels with shielded  
detectors

# Array partitioning



Array size: 48 x 16

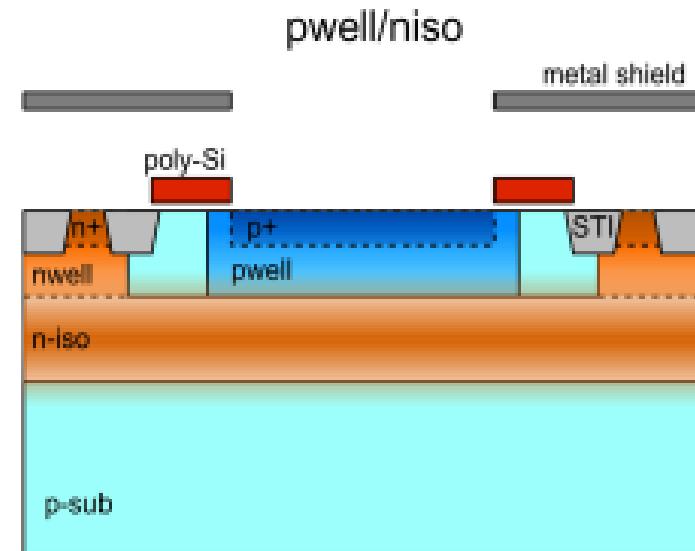
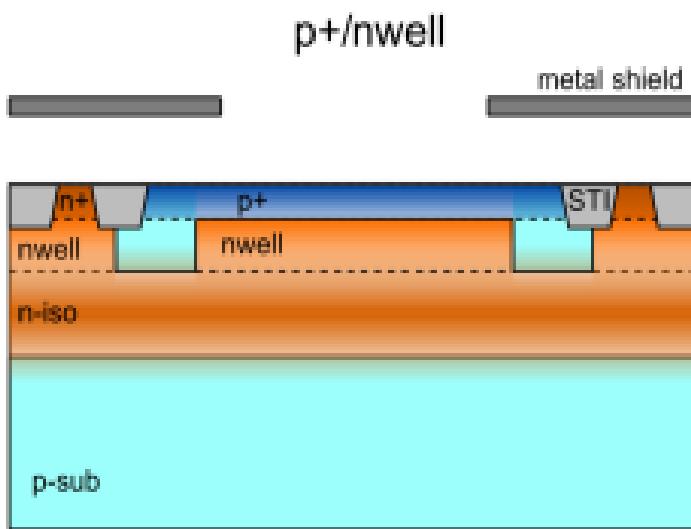
SPAD active area sizes:  
A: 45um  
B: 40um  
C: 35um  
D: 30um

SPAD pairs size combinations  
(Chip1 - Chip2)

	A - A		A - B
	B - B		A - C
	C - C		A - D
	D - D		

# SPADs in 150nm CMOS process

- Standard CMOS process – no modifications
- Avalanche diodes in deep nwell: isolated from substrate



## Type 1:

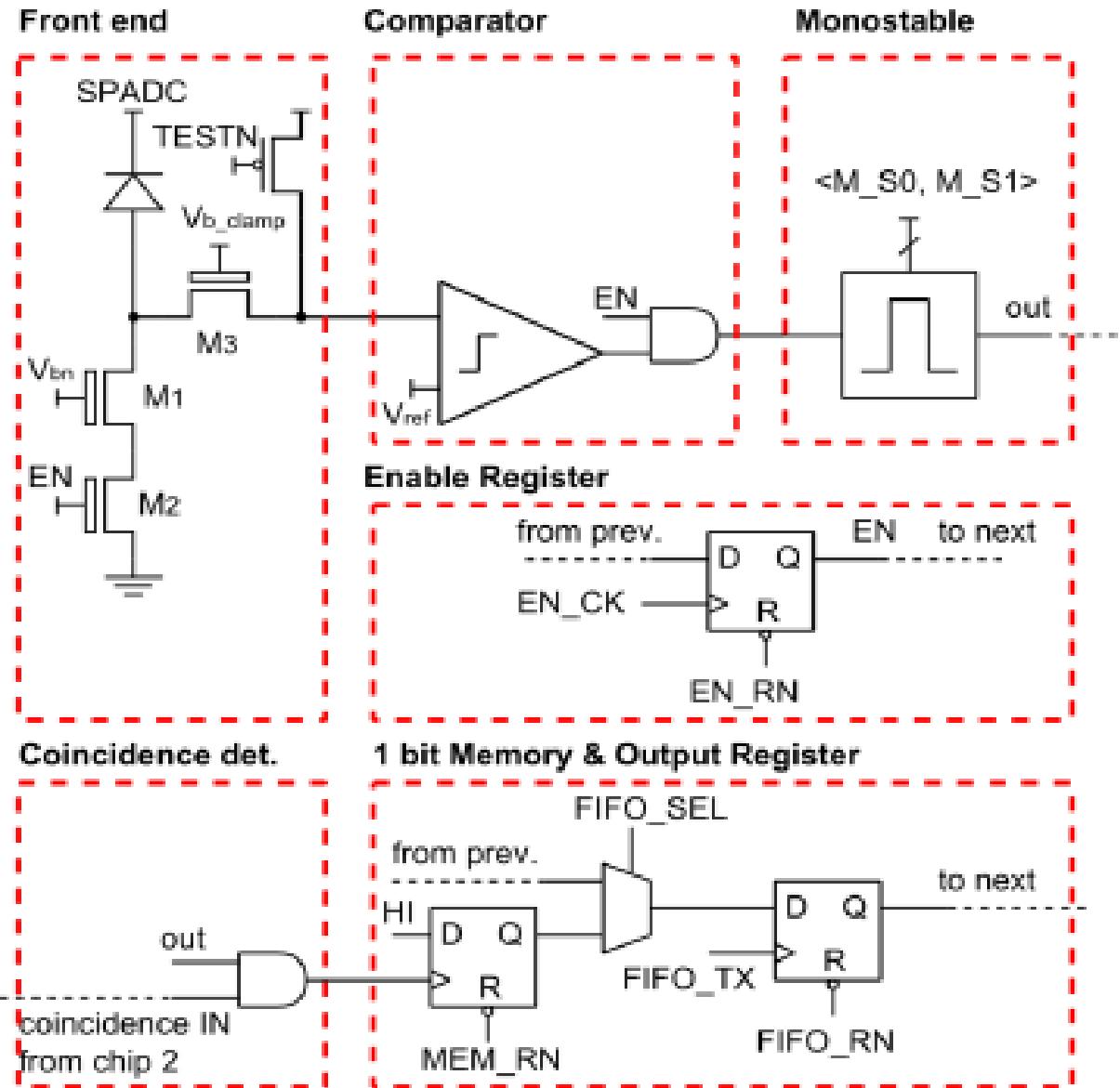
- Shallow step junction
- Active thickness  $\sim 1\mu\text{m}$

## Type 2:

- Deep graded junction
- Active thickness  $\sim 1.5\mu\text{m}$

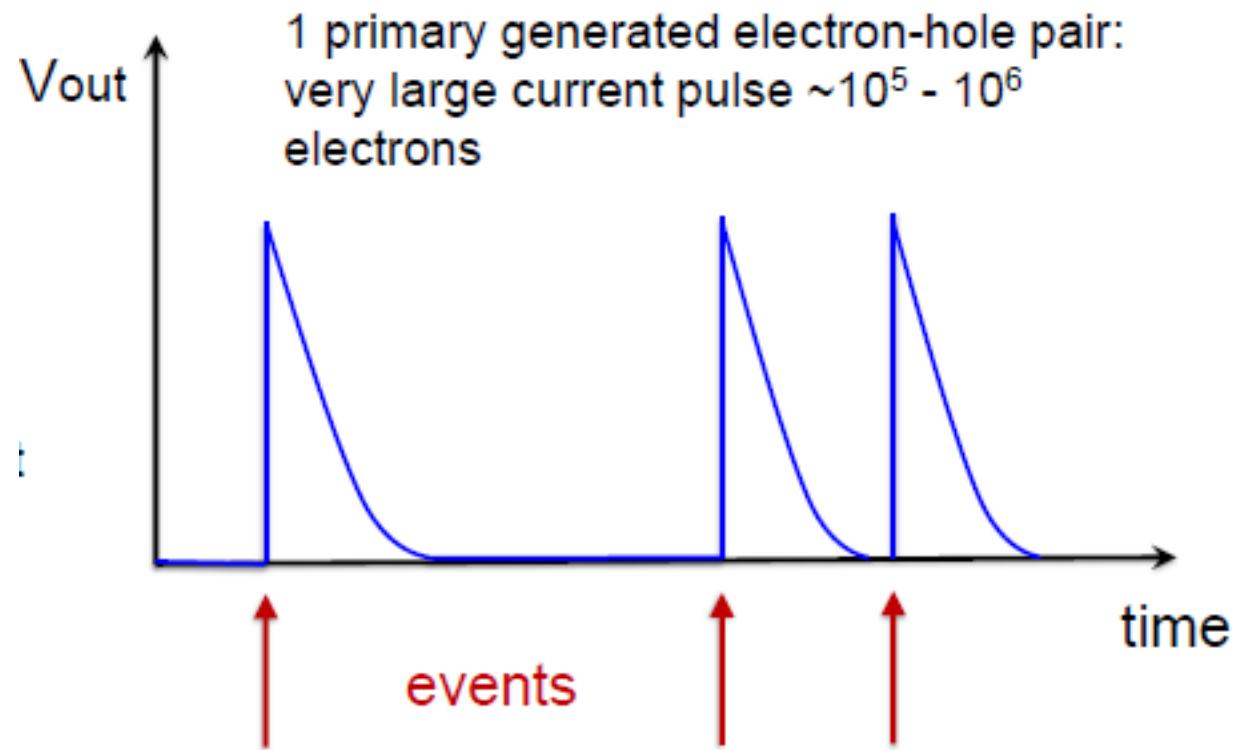
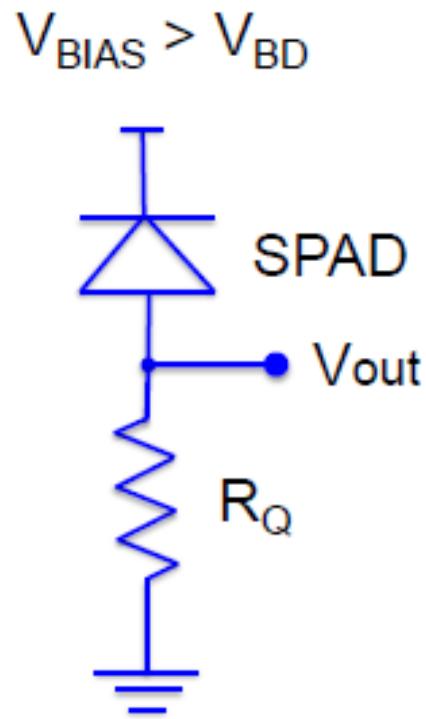
# Pixel Schematics

Common to  
Chip 1 and 2

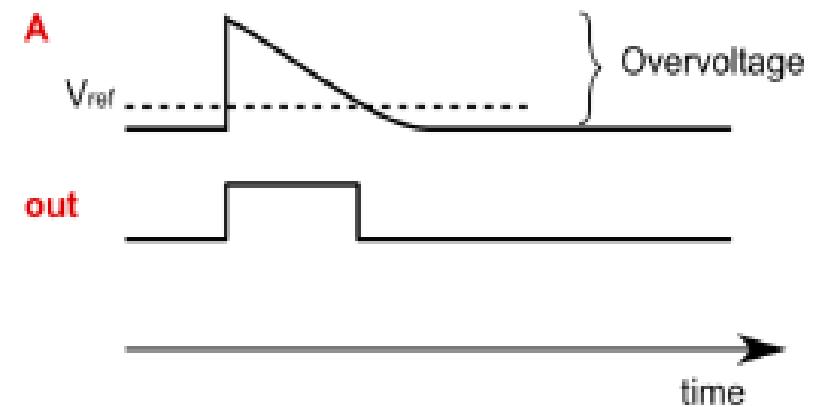
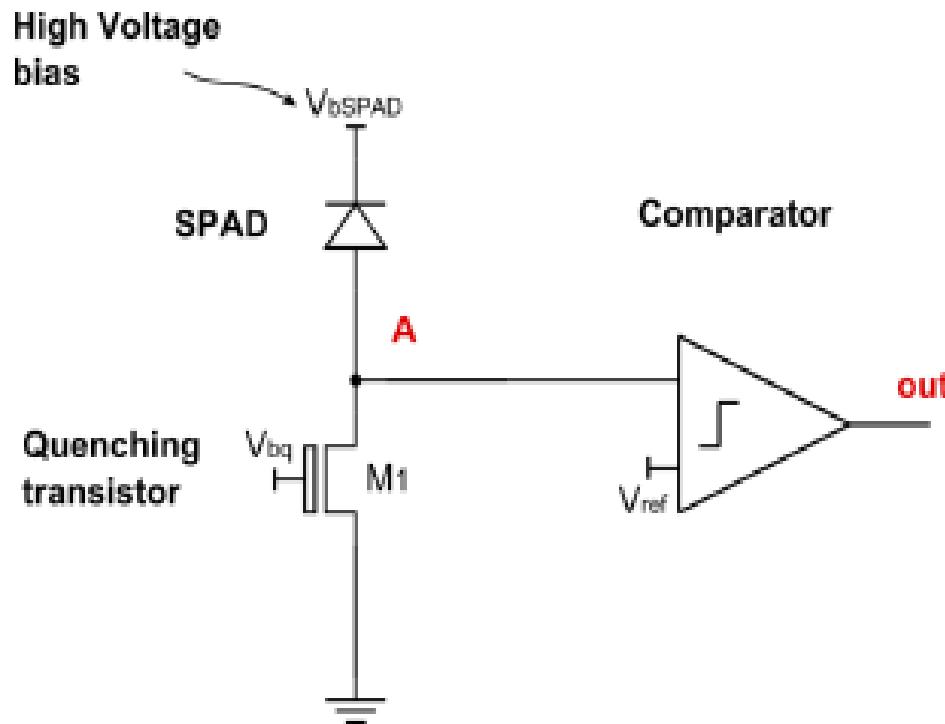


Only in chip 1

# Geiger mode avalanche detectors

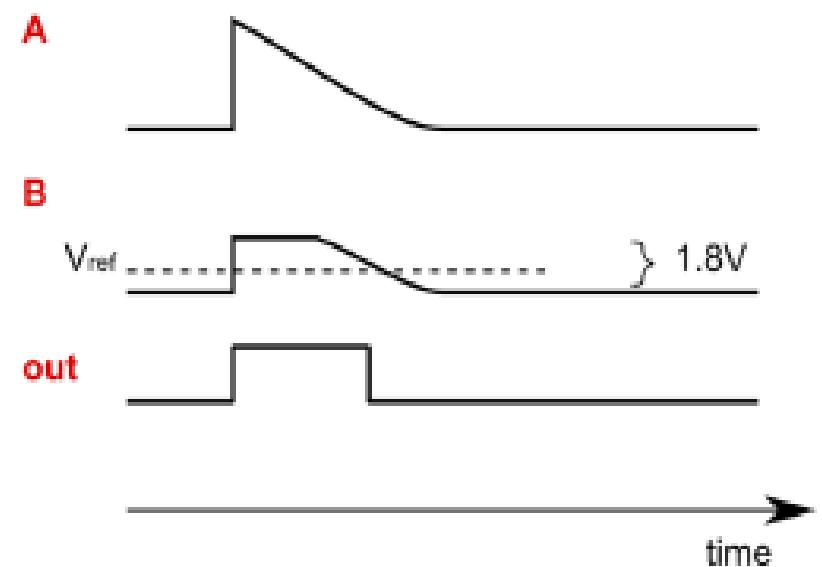
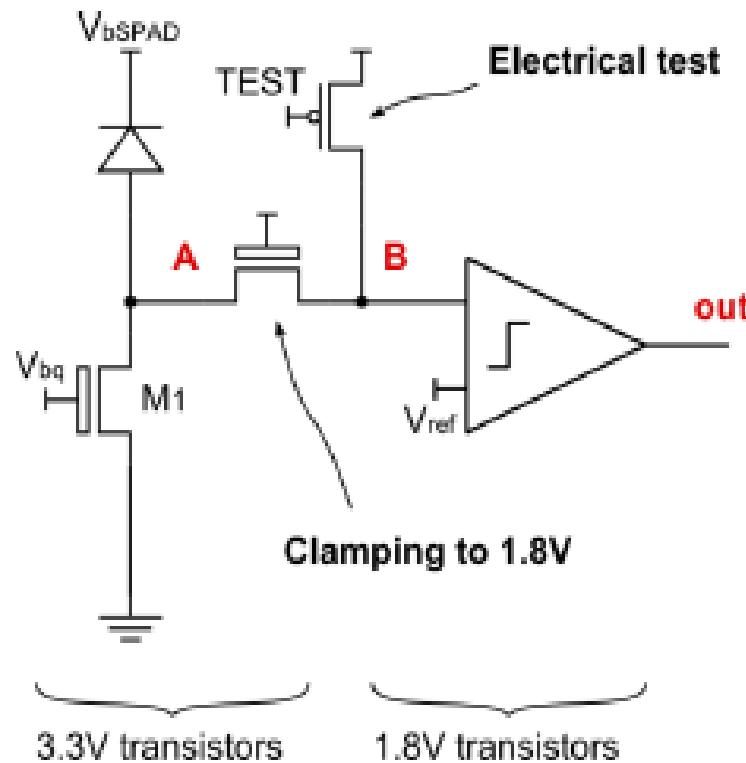


# Signal propagation



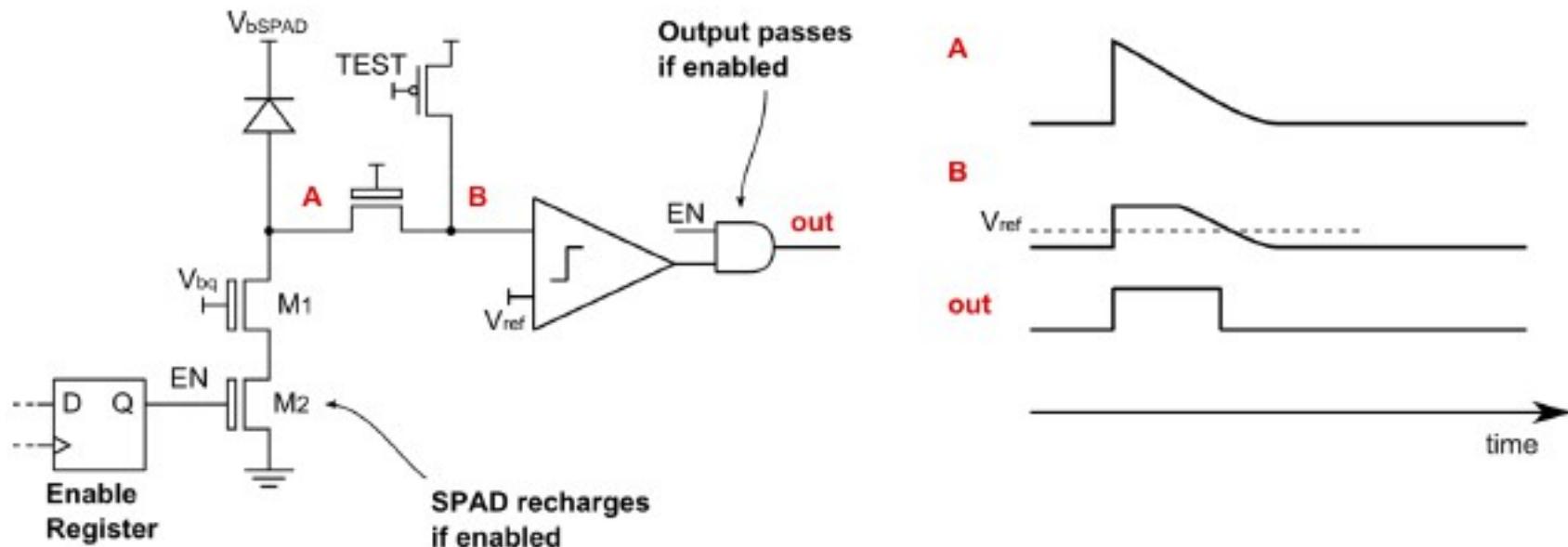
- **High voltage**  $V_{b\text{SPAD}}$  applied at nwell
- Maximum voltage at node A:  $V_{ov} = V_{b\text{SPAD}} - V_{BD}$
- **Small capacitance** at node A
- Passive quenching with constant current recharge

# Signal propagation



- Front-end transistors: 3.3V → Maximum overvoltage 3.3V
- Digital circuitry: 1.8V compact – fast – low-power

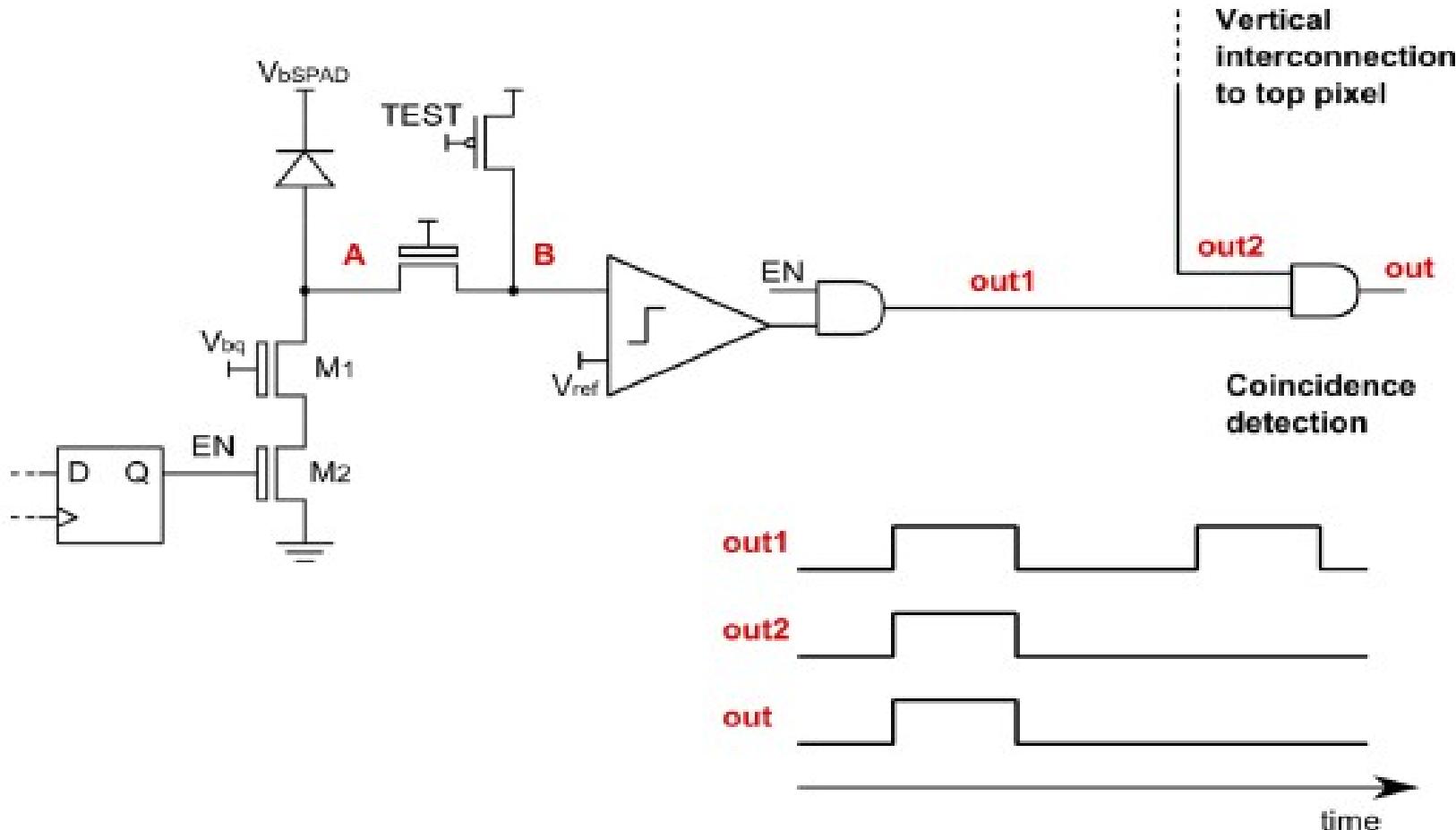
# Signal propagation



Pixels can be individually disabled:

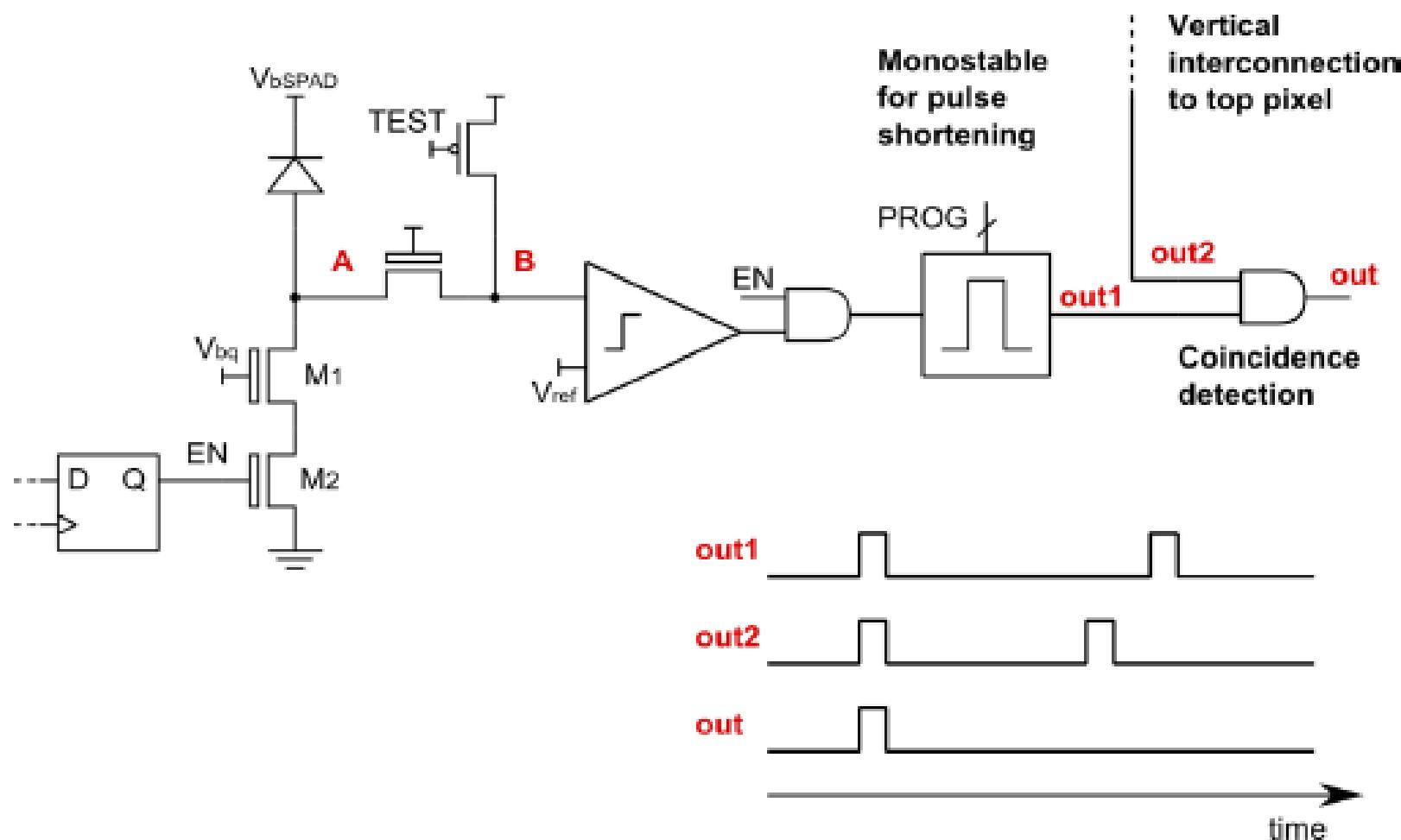
- $M_2$  disables recharge
- Output and gate blocks output pulses

# Signal propagation



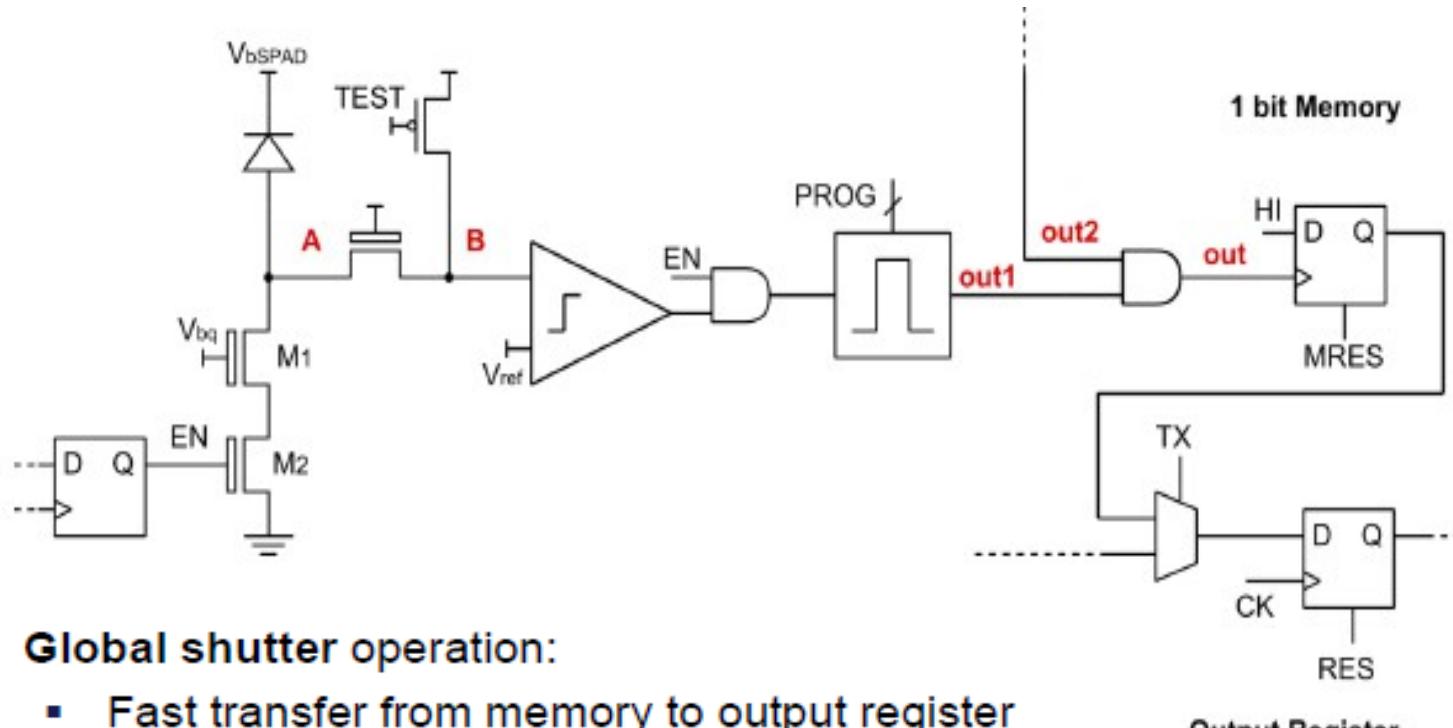
- Coincidence with top-layer pixel

# Signal propagation

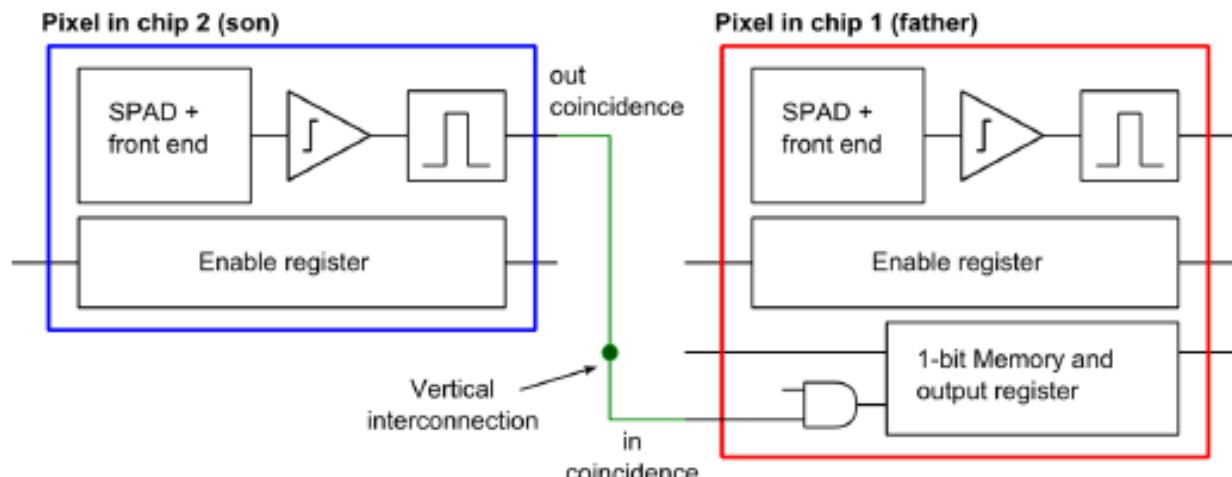


- Pulse shortening: reduces the rate of accidental coincidence
- Programmable pulse width: 750ps, 1.5ns, 10ns

# Signal propagation

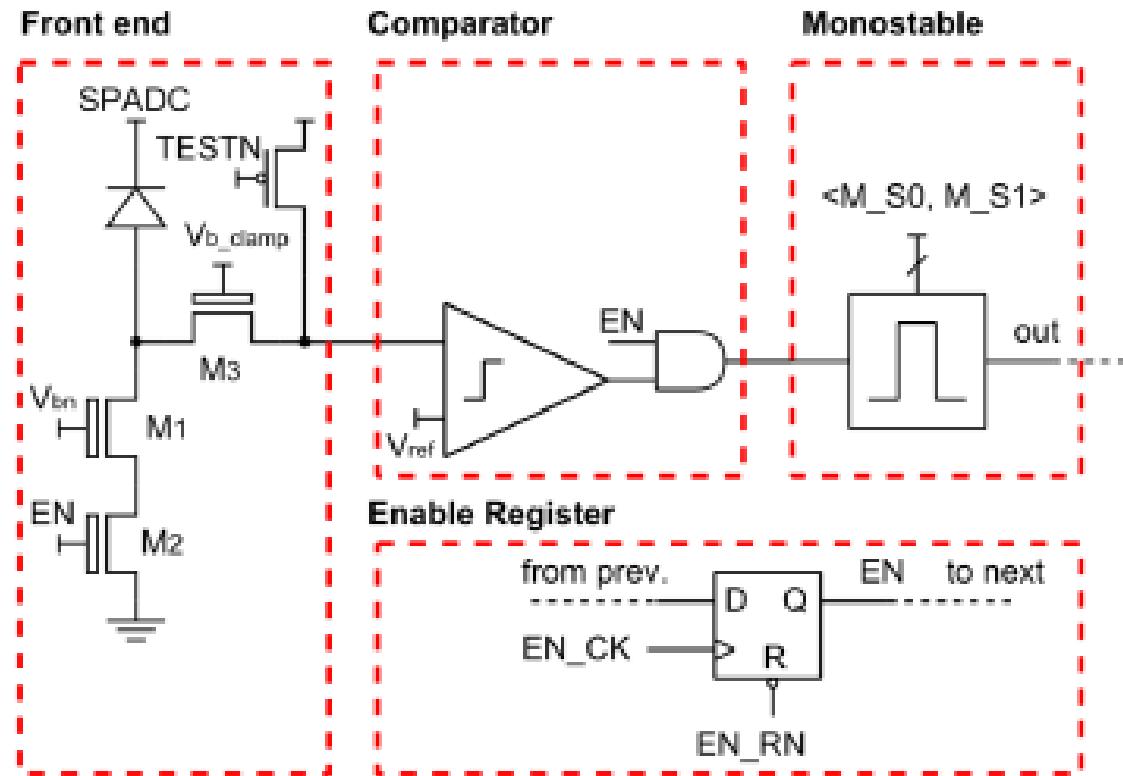


- **Global shutter operation:**
  - Fast transfer from memory to output register
  - Simultaneous accumulation and data output

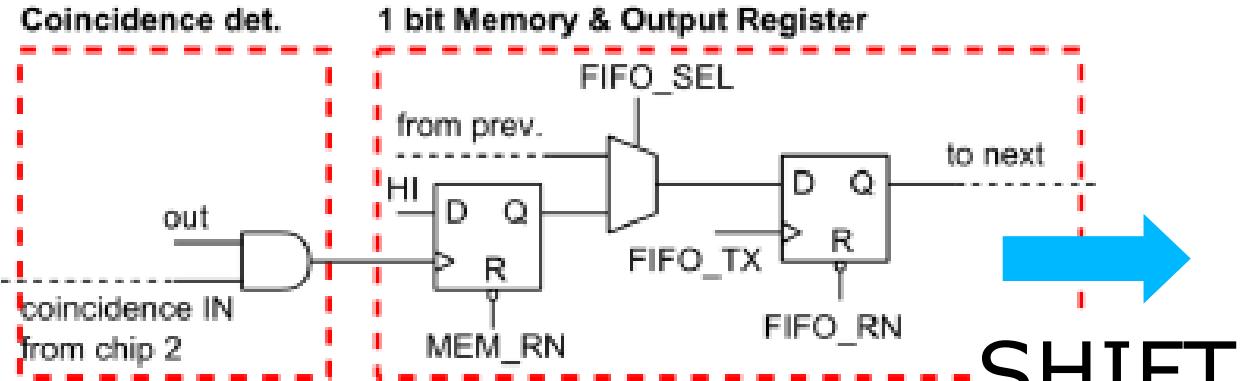


# Output FIFO (Shift Register)

Common to  
Chip 1 and 2

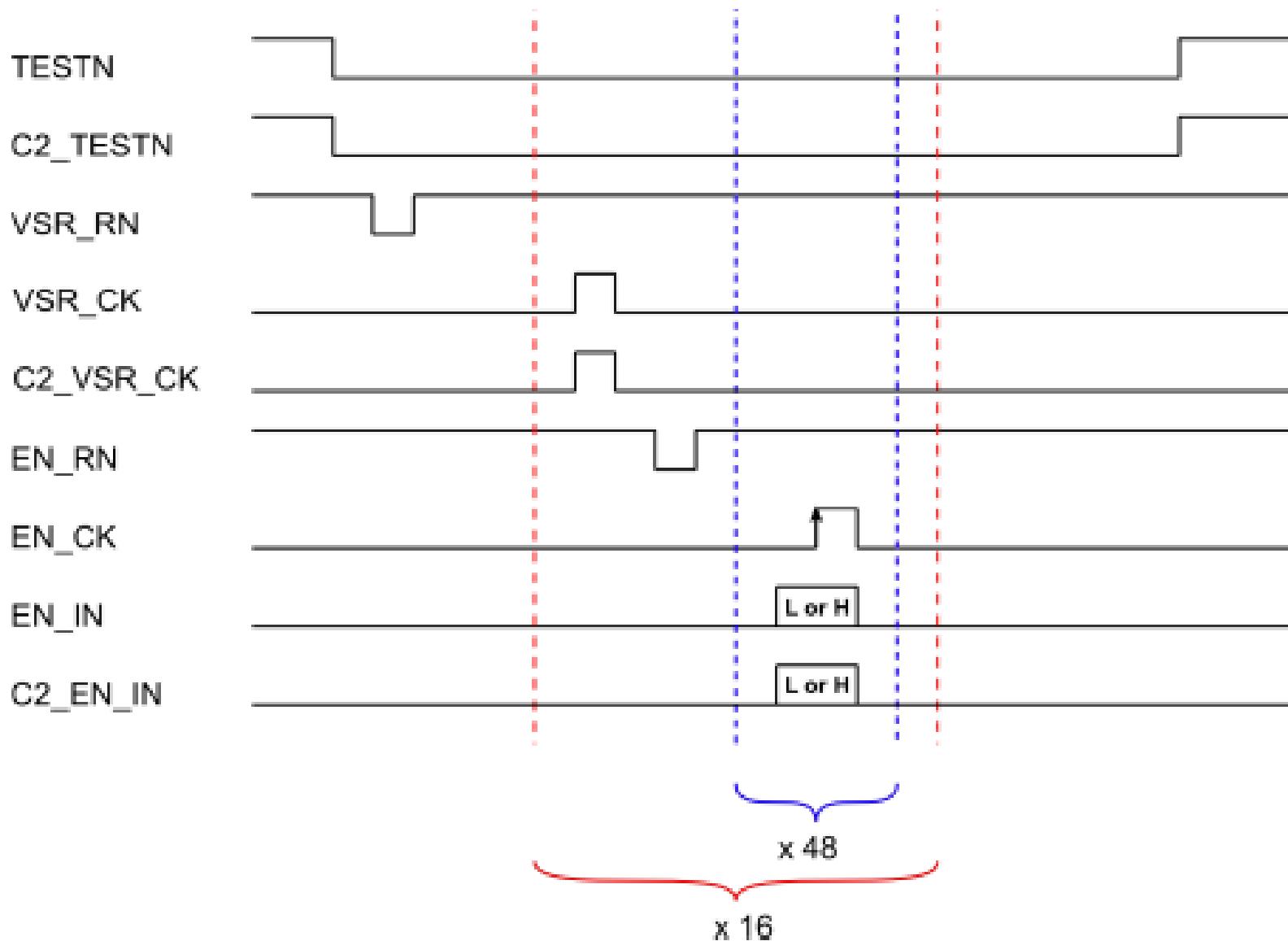


Only in chip 1

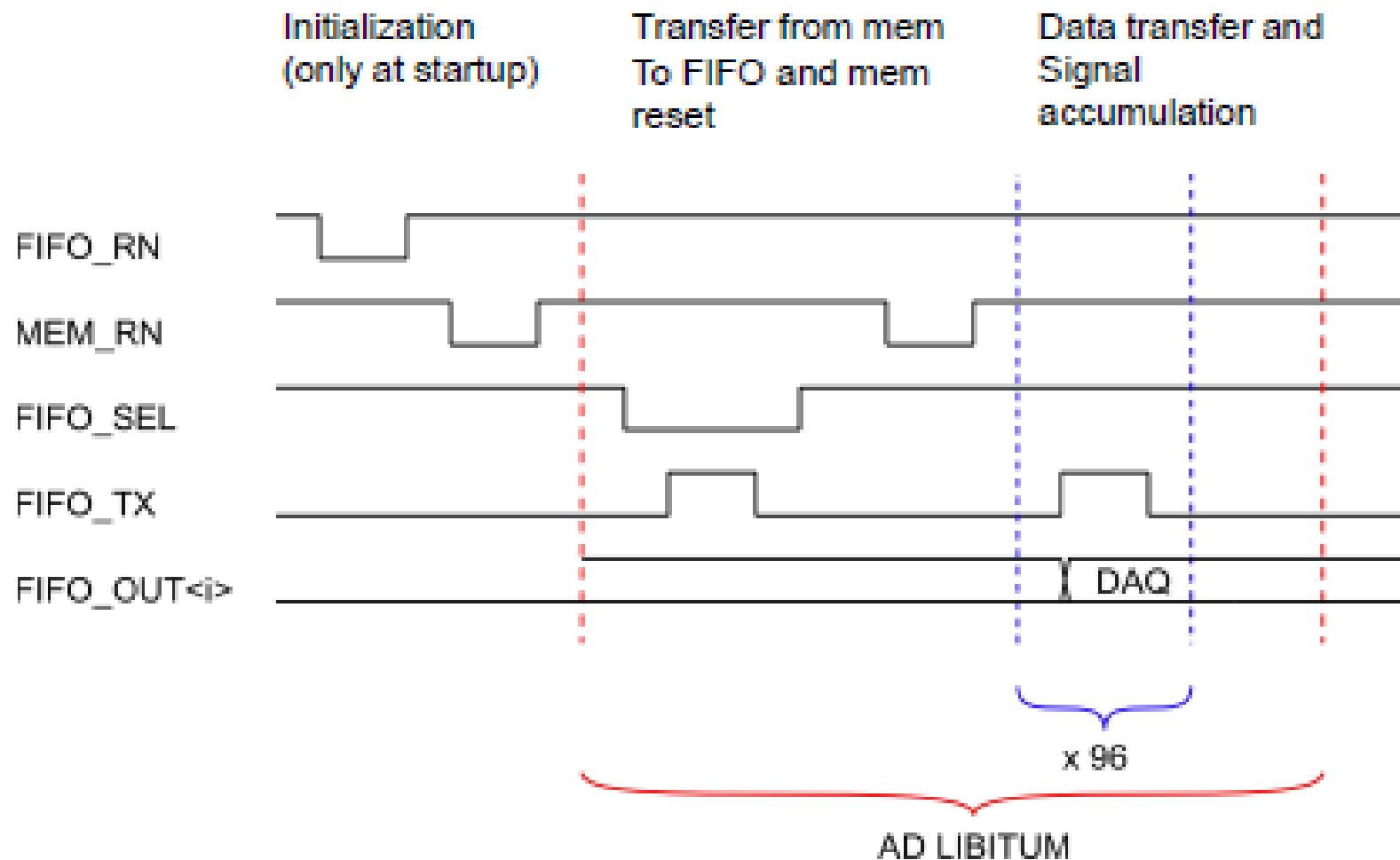


96 cells

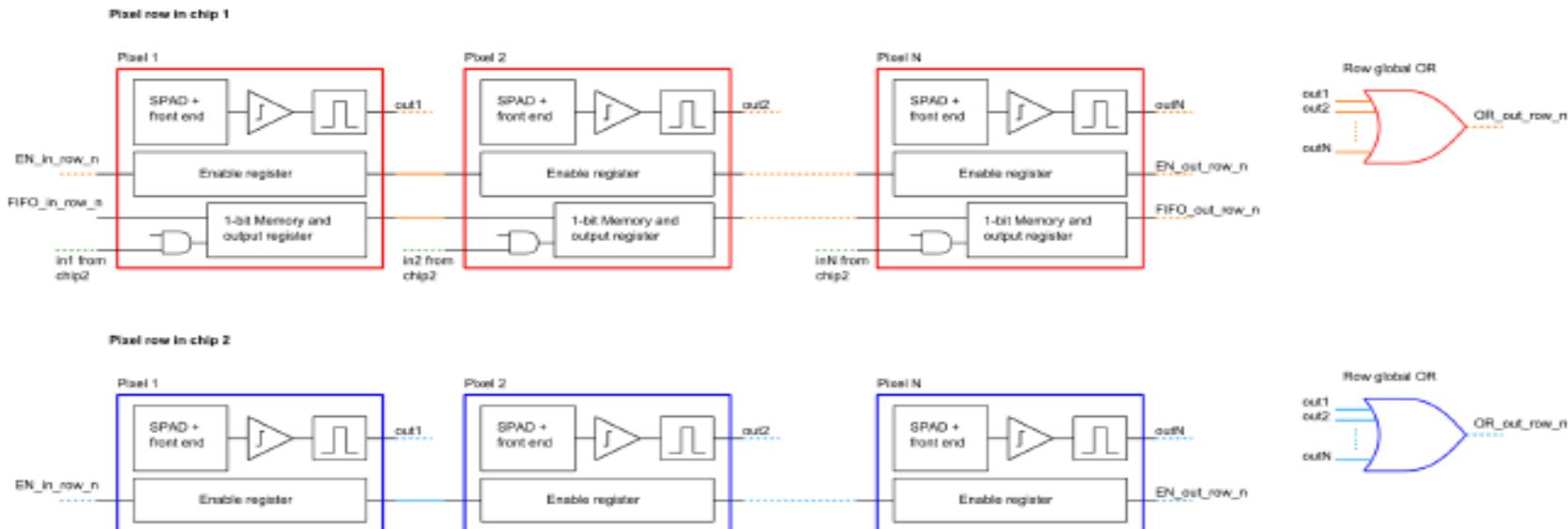
# Timing diagram: enable register loading



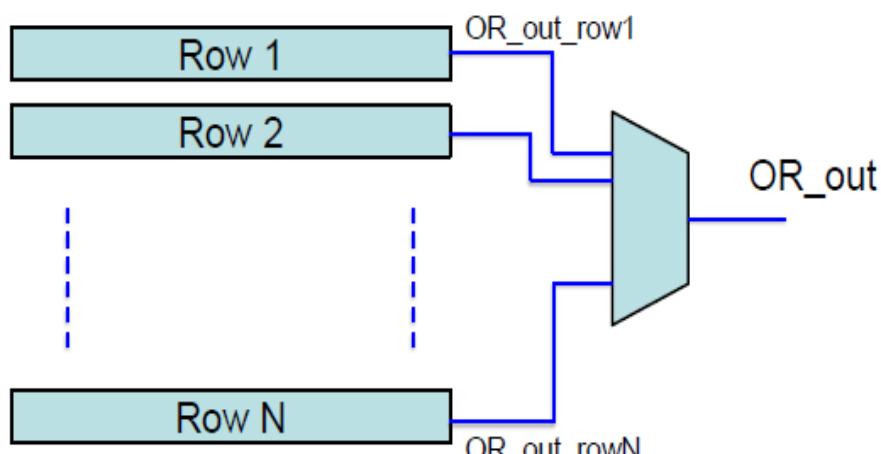
# Timing diagram: data readout



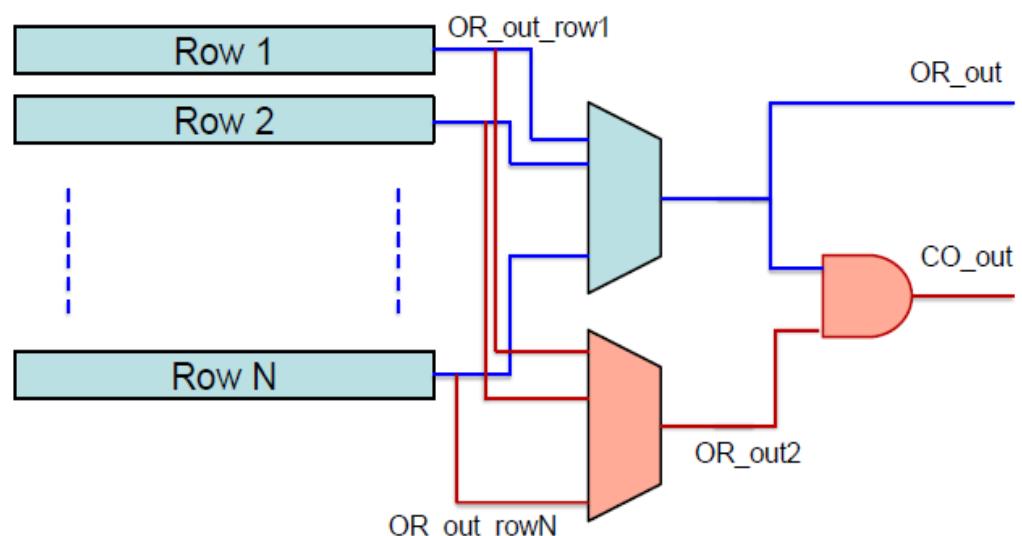
# Additional readout mode: Row OR outputs



Multiplexer selects only 1 row for output



Additional MUX and row coincidence circuit:  
only on Chip 1

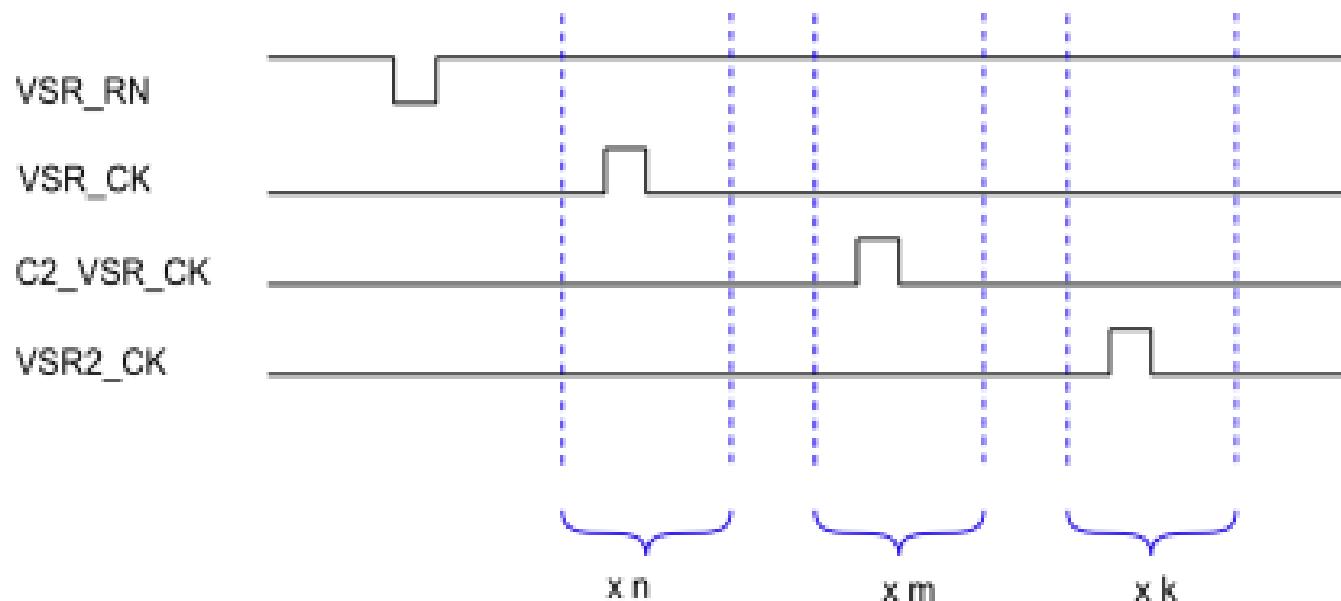


# Timing diagram: row selection

Optional: use only if row and coincidence output need to be observed.

Output setting:

- OR\_out (row n of Chip1)
- C2\_OR\_out (row m of Chip2)
- CO\_out (row coincidence between row n and row k)



# Laboratory: measurements & tools

1. pixels Dark Rate measurement → breakdown voltage

- Oscilloscope / scalers

2. Cross-talk measurement

both horizontal (bottom chip) and vertical (Top-Bottom)

- Coincidence circuits (on-chip/external)

3. Timing resolution

- pulsed laser (30ps, 375nm)
- TAC (5ps) / Waveform digitizer (5GSs)

4. Afterpulsing

- Waveform digitizer / TDC

5. absolute Photo-Detection Efficiency (unshielded cells)

- pulsed laser (30ps, 375nm) / pulsed diodes
- calibrated photo-diode
- $1/r^2$  method

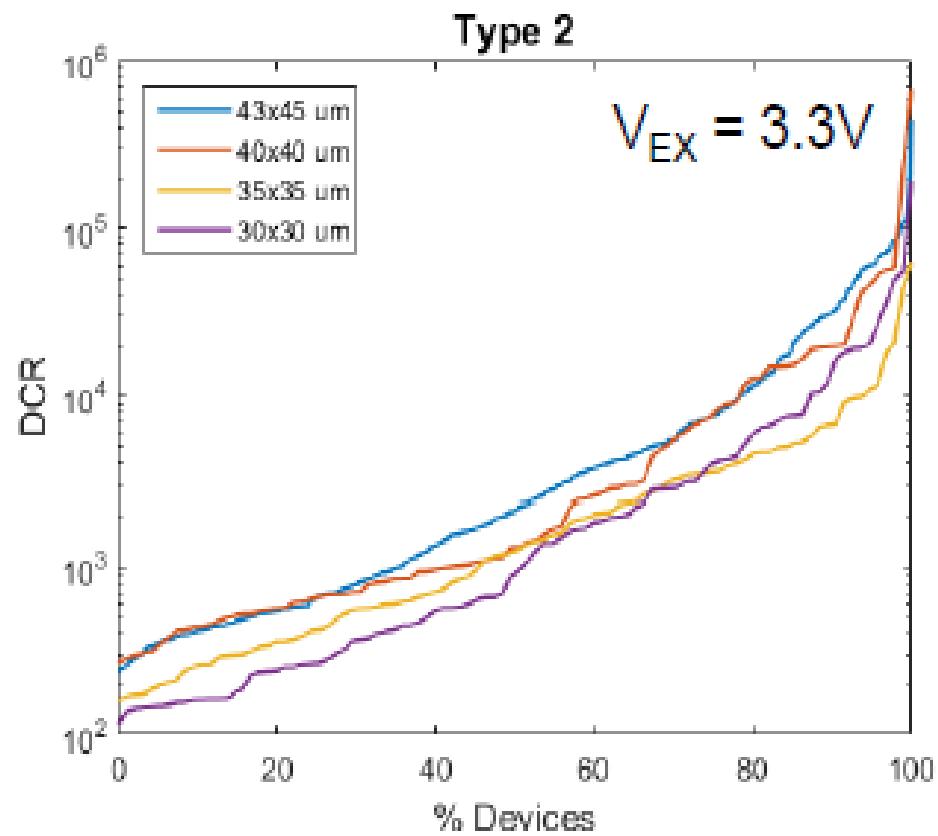
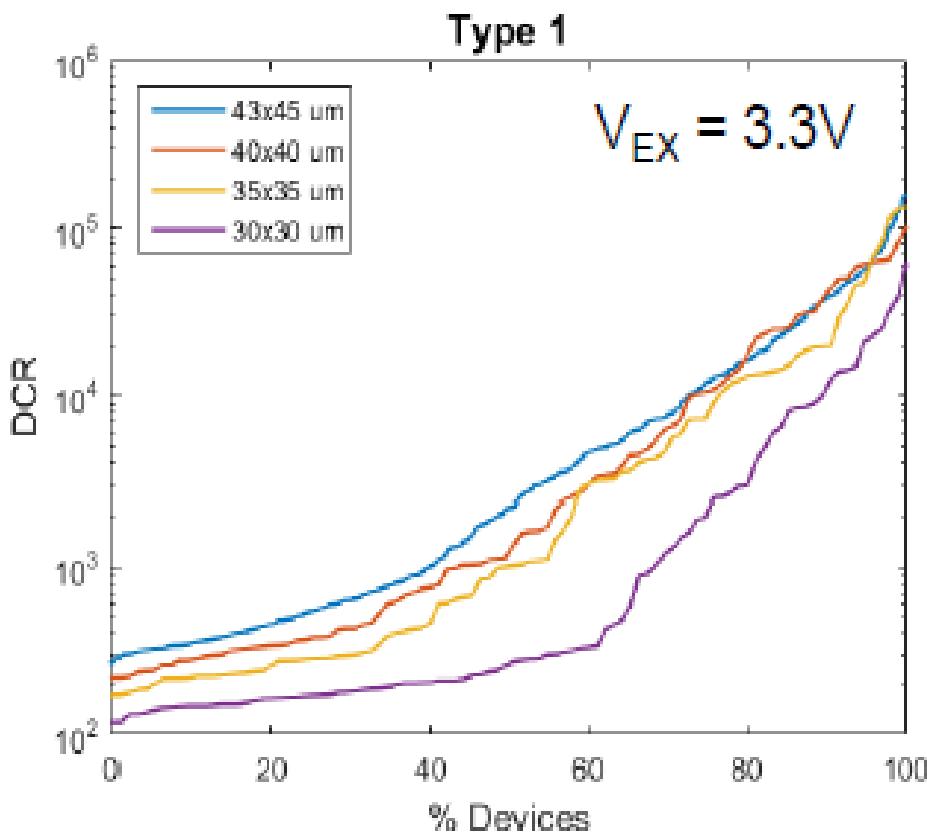
(5'. Optional) relative PDE

- halogen lamp
- monochromator

6. Sensitivity to  $\alpha$  and  $\beta$  sources

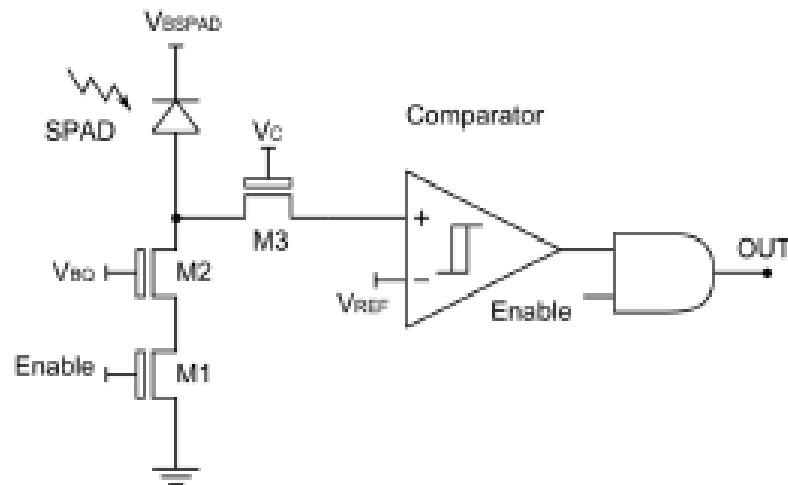
- scalers

# Reference - DCR



- Cumulative distribution, combined measurements on 3 chips
- 600 devices for largest size, 72 for smaller ones
- Median DCR = 2.2kHz for largest cell size of both types

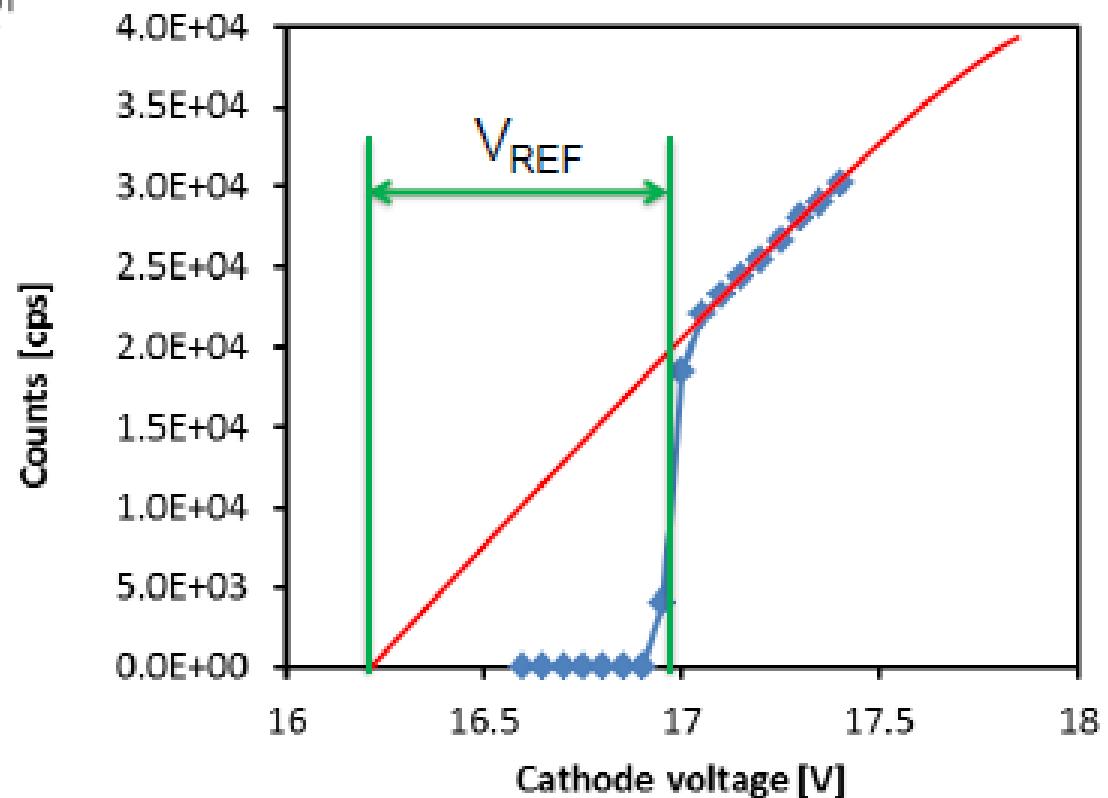
# Reference - $V_{bd}$ extraction method



L. Pancheri et al., Proc. IEEE ICMTS, 2014

$V_{BD}$  extraction from I-V curves:  
not possible

$V_{BD}$  extracted from the dark  
count rate vs. voltage curve

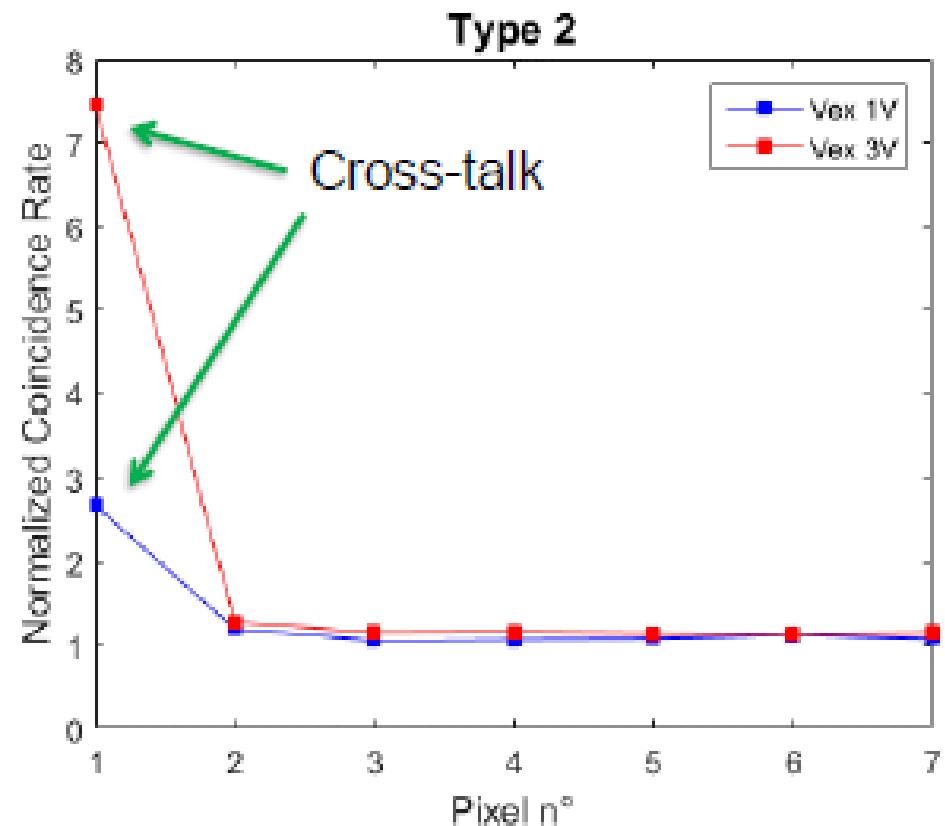
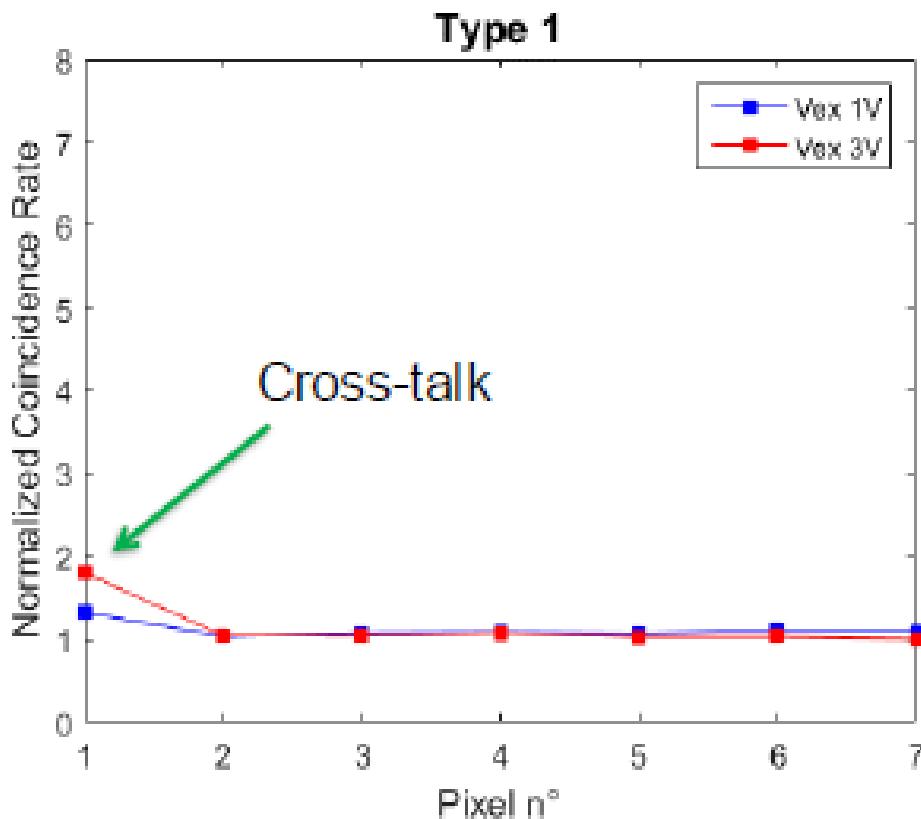
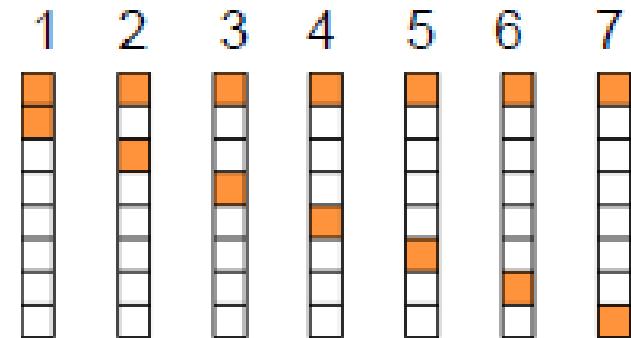


# Reference - Horizontal cross-talk

Count rate in coincidence between two pixels in the same column

Normalized rate:

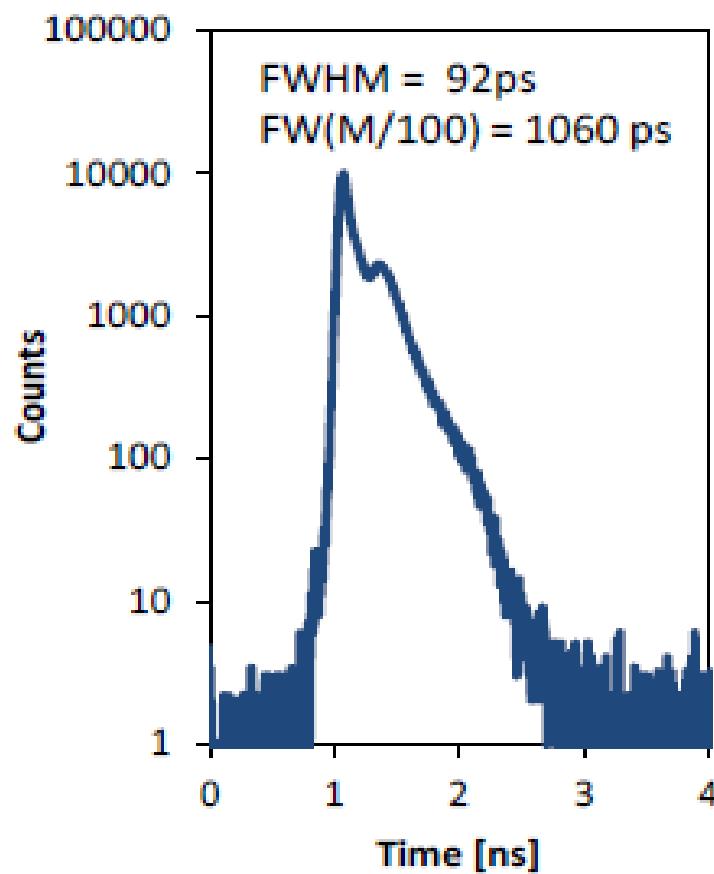
$$\frac{CR_{Meas}}{2 \cdot CR_1 \cdot CR_2 \cdot \Delta T}$$



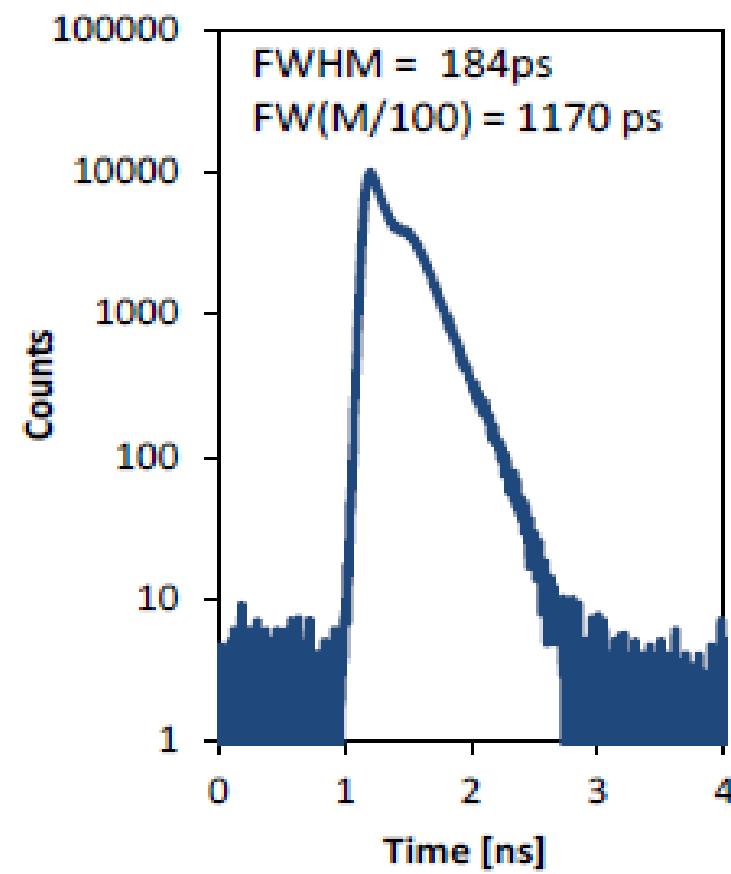
# Reference - SPAD timing

Measured on 10- $\mu\text{m}$  devices, with blue laser (470nm), 70ps FWHM

Type 1: 60ps FWHM

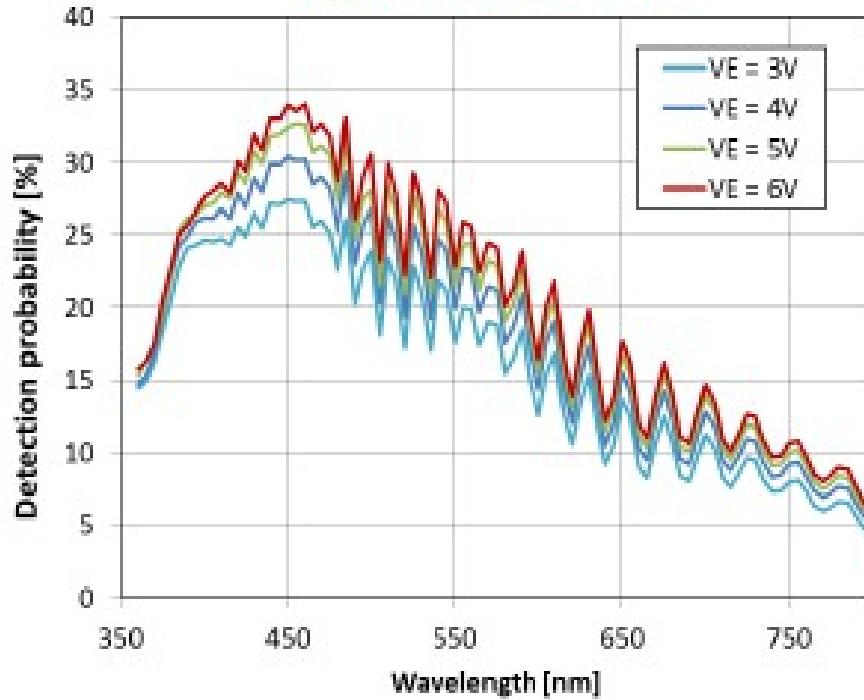


Type 2: 170ps FWHM

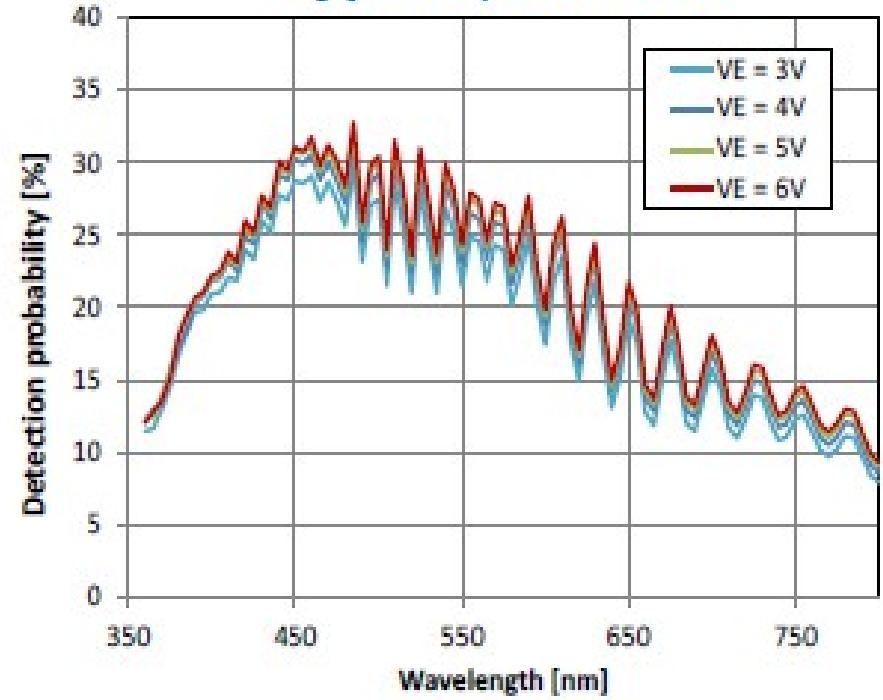


# Reference - SPAD PDE

Type 1: p+/nwell



Type 2: pwell/niso



Shallower junction:  
better NUV – Blue efficiency

Wider depletion region:  
Better red-IR efficiency

L. Pancheri et al., J. Selected Topics in Quantum Electron, 2015

**Enjoy the "APIX" SNRI Lab. 1 !!!**

**Lab. NUCLEX – Sala 3 - LNL**