4H-SiC defects

Nicolò Piluso

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Outline

- Introduction
  - Overview 4H-SiC (growth, properties, application)
- Defects
  - Bulk
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  - Raman Spectroscopy
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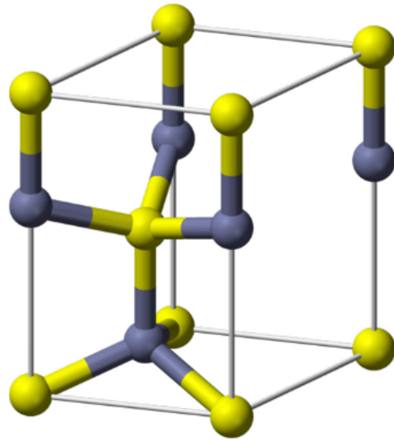
  - μ-PCD
  - KOH molten
  - Optical microscopy, TEM, SEM
  - Scattered Light

Introduction

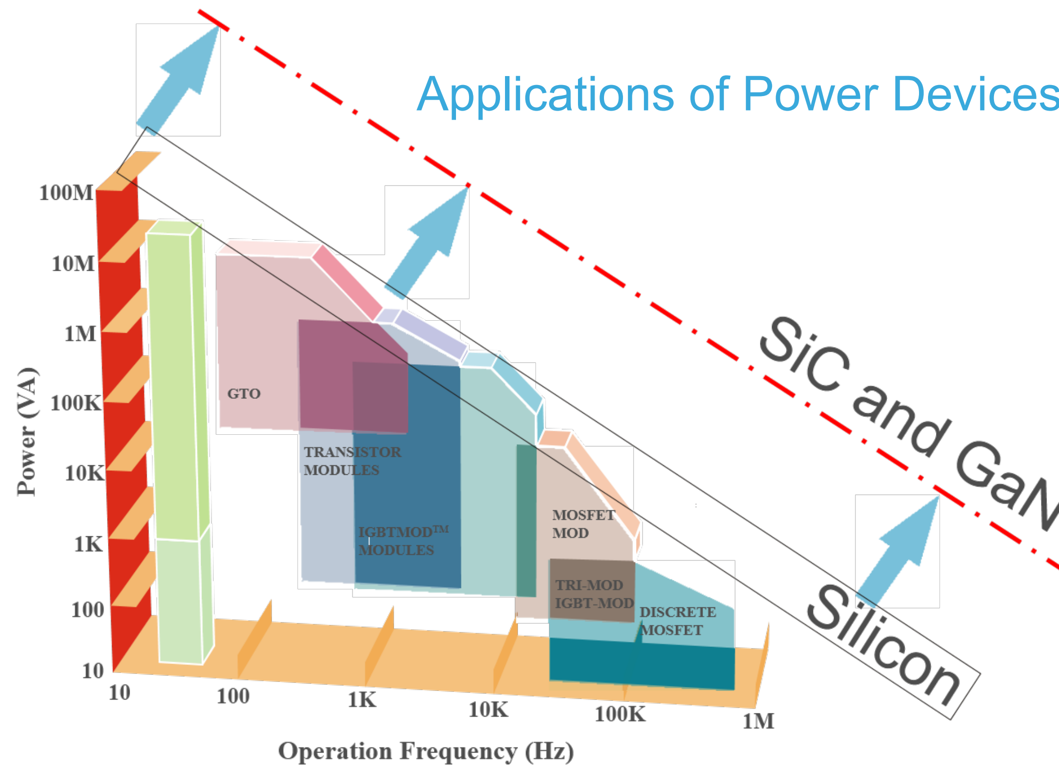
4H-SiC lattice (**Wurtzite unit cell**)



Semiconductor properties

at 300K	Si	GaAs	4H-SiC	GaN
E_g(eV)	1.12	1.4	3.2	3.4
E_c (MV/cm)	0.25	0.3	2.2	3
μ_n (cm2/Vs)	1350	8500	1000	1000
ε_r	11.9	13	10	9.5
V_{sat} (cm/s)	$1x10^7$	$1x10^7$	$2x10^7$	$3x10^7$
λ (W/cmK)	1.5	0.5	3-5	1.3

Some devices are pushing Si boundary
SiC and GaN offer promise for improvement



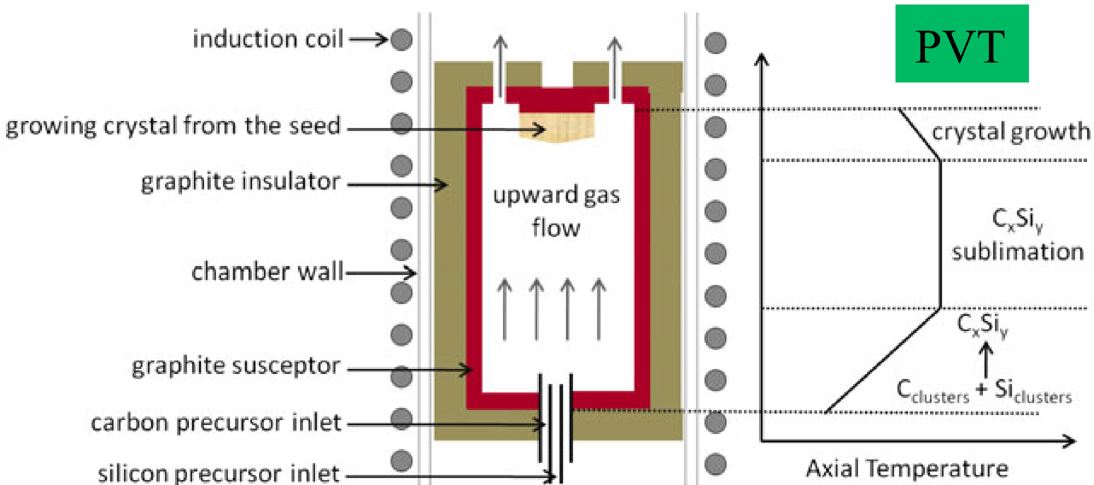
Slide from Prof. S. E. Sadd

Introduction

Growth Methods:

PVT - Bulk (thick, high doping)
CVD - Epitaxy (thin film, mid-low doping)

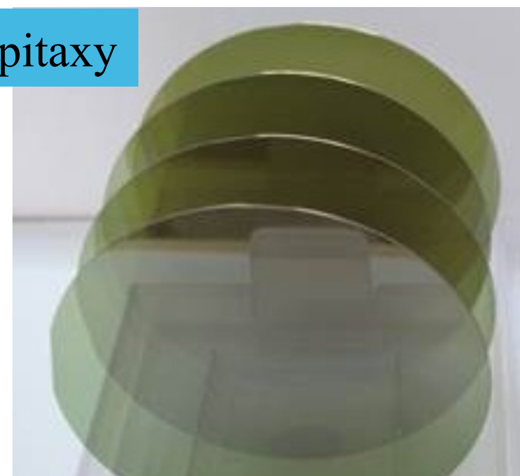
PVT



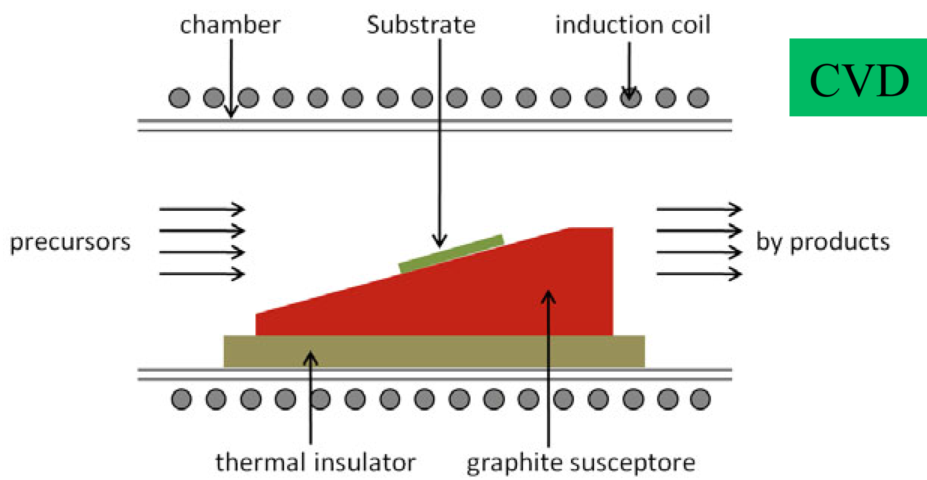
Ingot - Bulk

cutting

Epitaxy



CVD



Bulk Defects

Table 3.1 Major extended defects observed in SiC boules and wafers. The Burgers vector, major direction, and typical density of the extended defects in boules (wafers) prepared using state-of-art technology (for n-type 4H-SiC) are shown.

Dislocation	Burgers vector	Major direction	Typical density (cm^{-2})
Micropipe	n <0001> ($n > 2$)	<0001>	0–0.1
Threading screw dislocation (TSD)	n <0001> ($n = 1, 2$)	<0001>	300–600
Threading edge dislocation (TED)	<11$\bar{2}$0>/3	<0001>	2000–5000
(Perfect) Basal plane dislocation (BPD)	<11$\bar{2}$0>/3	in {0001} plane (preferably <11$\bar{2}$0>)	500–3000

Micropipe

Micropipe defects are indeed located at the center of a large spiral on the surface of the SiC boule, and the diameters of the pinholes range from 0.5 µm to several micrometers

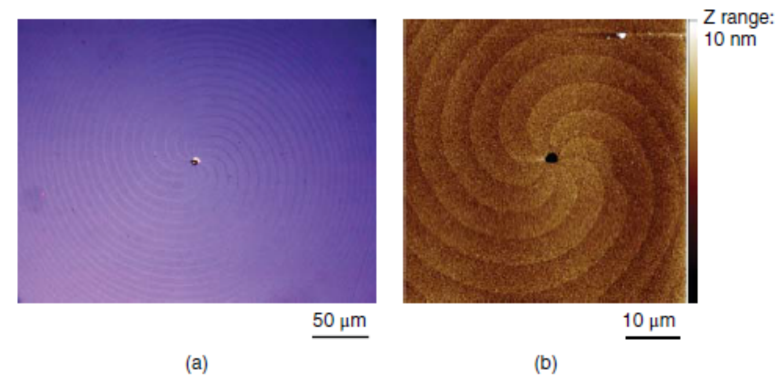


Figure 3.14 Micropipe in a 4H-SiC(0001) wafer, as observed by (a) optical microscopy and (b) atom force microscopy. (By courtesy of D. Nakamura and T. Mitsuoka, Toyota Central R&D Laboratories.)

TSD

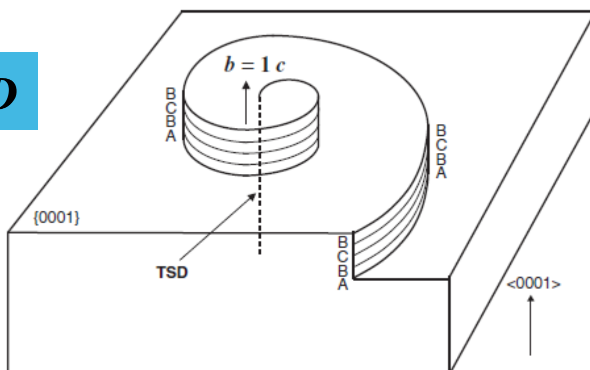


Figure 3.15 Schematic illustration of an elementary threading screw dislocation in SiC.

TED-BPD

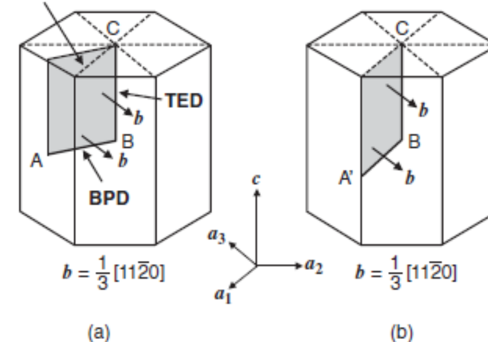


Figure 3.18 (a) Schematic illustration of an extra (or missing) half plane introduced into a SiC crystal. (b) Typical configuration of threading edge and basal plane dislocations, where the basal plane dislocation lies along a <11$\bar{2}$0> direction.

Polytype mixing during boule growth → switching, coalescence, nucleation →

Occurrence of ***spiral growth*** around TSD that is generated to remedy to mismatch of polytype

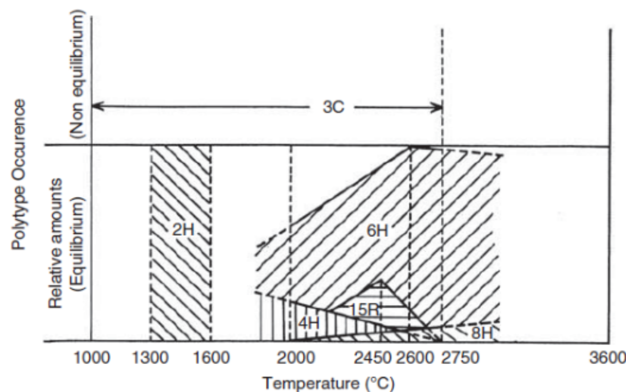


Figure 3.11 Empirical observations of relative stability (or occurrence) of individual polytypes in SiC bulk growth [3].

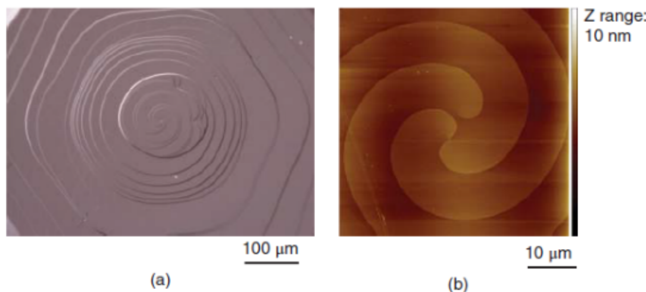


Figure 3.12 Typical surface morphologies of a 6H-SiC boule taken with (a) an optical microscope and (b) an atomic force microscope. (By courtesy of D. Nakamura and T. Mitsuoka, Toyota Central R&D Laboratories.).

3.2 Polytype Control in Sublimation Growth

For SiC wafers to be used in electronic applications, it is mandatory to grow a large SiC boule of a desired single polytype. Because of the low stacking fault energy of SiC, however, polytype mixing may happen during boule growth, when the growth conditions are not optimized. Knippenberg reported empirical observations of the relative stability (or occurrence) of individual polytypes in SiC bulk growth, as shown in Figure 3.11 [3]. According to this report, 3C-SiC is a metastable polytype, and 2H-SiC is believed to occur at relatively low temperatures, 1300–1600 °C. At high temperatures, above 2000 °C, at which sublimation growth is carried out, 6H-, 4H-, and 15R-SiC polytypes are often observed. However, from a materials science viewpoint, the kinetic and thermodynamic factors which determine the polytype actually grown are not well understood. Because SiC{0001} is usually employed as the seed crystal, polytype switching, or nucleation of foreign polytypes may occur during growth, unless intentionally controlled.

One obvious kinetic factor is the polytype replication through *spiral growth* around threading screw dislocations, after stable spiral growth has been established in the bulk. Figure 3.12 shows typical surface morphologies of a 6H-SiC boule taken with (a) an optical microscope and (b) an atomic force microscope.

These images indicate that spiral growth, via steps with a six-bilayer height, is dominant on the growing surface (in 6H-SiC growth). Along the step edges, the stacking information is provided, which ensures replication of that polytype in the growing crystal. Because the core of a threading screw dislocation acts as an infinite step source, this spiral growth is maintained throughout the growth, as long as the optimized growth conditions are maintained. In this sense, polytype replication via a spiral growth mechanism will become much more difficult in the future, when the threading screw dislocations in SiC boules are almost eliminated. Polytype replication by step-flow growth is described in greater detail in Chapter 4.

Although spiral growth is favorable for polytype replication, nucleation on the terraces (flat regions between steps) can naturally take place in the initial stages of growth as well as during growth. Therefore, it is essential to understand and to control the key factors which stabilize a desired polytype.

> C/Si Ratio
> Polarity (Si or C face)
> Hexagonality of the polytype
- 4H-SiC (0.5 Hex), more stable in C-rich ambient

BPD generation during boule growth

A doping variation affects the BPD generation due to the lattice parameters variation.

A stress reduction could reduce the BPD generation

Most TEDs are formed by conversion from BPDs along the growth direction during growth.

easily introduced into the growing boule when the resolved shear stress exceeds a certain (critical) value. A major source of the stress is thermal stress, which develops during sublimation growth when the temperature profile is not appropriate. Both radial and axial temperature gradients cause inhomogeneous thermal expansion inside the boule. Furthermore, the difference in the thermal expansion coefficients of the SiC and graphite parts causes severe thermal stress during cooling. Figure 3.19 shows a schematic illustration of the shear stress, the associated dislocations, and the bending of a basal plane in a growing SiC boule, taking into account typical radial and axial temperature gradients [69]. The temperature is higher along the periphery of the boule than in the center because of radiation from the crucible walls. The temperature of the growing surface is higher than the seed temperature because of the temperature gradient designed to promote mass transport from the source to the seed. Under these circumstances, thermal expansion is not uniform inside the boule; this causes significant thermal stress and bending of basal planes. Consider the components of stress inside a boule grown along <0001> (Figure 3.20). The resolved shear stress (σ_{RZ}) along <$11\bar{2}0$> inside a basal plane is expressed by [58]:

$$\sigma_{RZ} = (\sigma_{rr} + \sigma_{rz}) \cos \phi - \sigma_{\phi\phi} \sin \phi \tag{3.11}$$

where σ_{rr}, σ_{rz}, and $\sigma_{\phi\phi}$ are the components of shear stress, as shown in Figure 3.20 [20]. The resolved shear stress is a direct cause of dislocation nucleation, while too high a value of $\sigma_{\phi\phi}$ can also lead to cracking of SiC boules.

Figure 3.21 shows the critical stress in 6H-SiC as a function of temperature [70]. One has to consider two different critical stresses, (i) the *critical shear stress* resolved to a basal plane, which induces *basal plane slip* and (ii) the *critical normal stress,* which induces *prism plane slip*. In SiC, the critical shear stress along a basal plane is much smaller, and the value decreases greatly at high temperature. Therefore, at the temperature of sublimation growth (over 2200 °C), the critical shear stress becomes

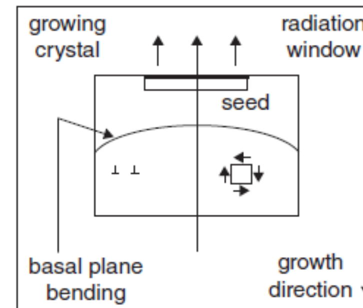
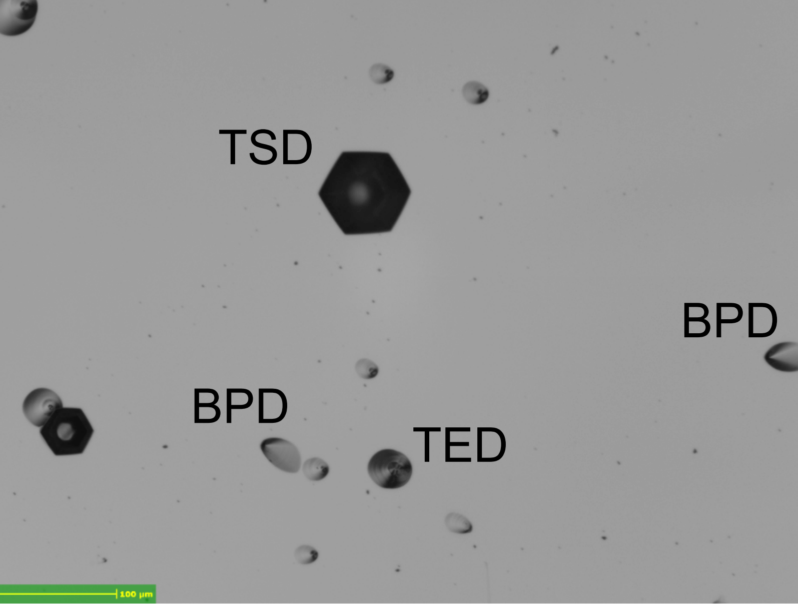


Figure 3.19 Schematic illustration of the shear stress, the associated dislocations, and the bending of a basal plane in a growing SiC boule, taking into account typical radial and axial temperature gradients



TSD generation and removal

Threading screw dislocations are basically replicated from a seed crystal, as also occurs for micropi
A major cause of threading-screw-dislocation nucleation in SiC sublimation growth is the generatio
a half loop at the initial stage of bulk growth, as shown in Figure 3.16. It is reported that the num
of TSDs with a Burgers vector of $+1c$ is almost the same as that with $-1c$, and that $+1c$ and $-1c$
locations are often observed nearby as if they are a pair [64]. At the very initial stage of growth, sta
spiral growth or layer-by-layer growth is not well established. When the growth conditions (e.g., ef
tive C/Si ratio, temperature profile, and other factors) deviate from the optimum conditions, nuclea
of foreign polytypes may occur at a microscopic scale. In this case, TSDs can be generated becaus
stacking mismatch (e.g., between a 4H-SiC host and a small 6H-SiC island), although the microsc
islands will eventually be overgrown [65]. In a similar manner, when a surface precipitate is overgro
the growth fronts meet at the precipitate and coalesce with misalignment under the influence of str
To accommodate this misalignment, a pair of screw dislocations of opposite signs is generated [65,
The surface quality of the seed is also important. Polishing-induced damage and surface graphitiza
during temperature ramping should be completely eliminated. Furthermore, micropipe dissociation
ing growth is another source of TSDs, as described above. Under optimized conditions, the densit
TSDs clearly decreases with increasing boule length [67]. There are two reasons for this: (i) pairs of
and $-1c$ TSDs can merge and annihilate and (ii) TSDss can be bent to the basal planes and eventu
reach the periphery of the boule.

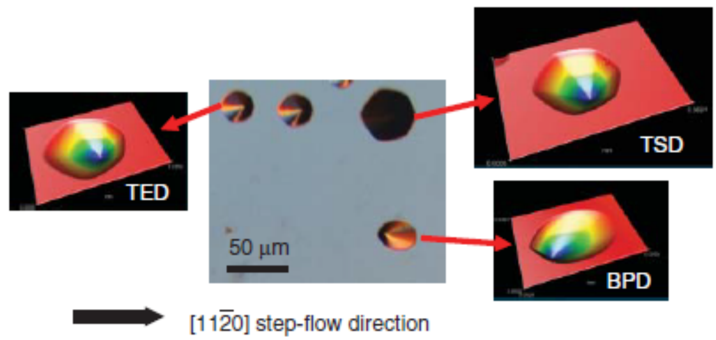


Figure 5.18 Off-axis 4H-SiC(0001) surface after etching in molten KOH at 500 °C for 10 min.

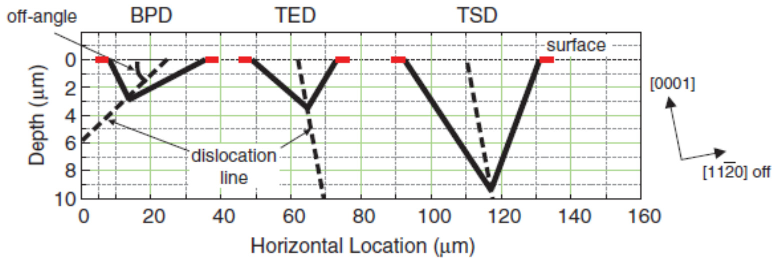


Figure 5.19 Cross-sections near the etch pits which were formed on off-axis SiC(0001), where
lines for the TSD, TED, and BPD are indicated by broken lines.

From Ch5,p144 Kimoto-Cooper Book

Vendor Value
EPD = TSD+TED+BPD

Defects reduction (Bulk)

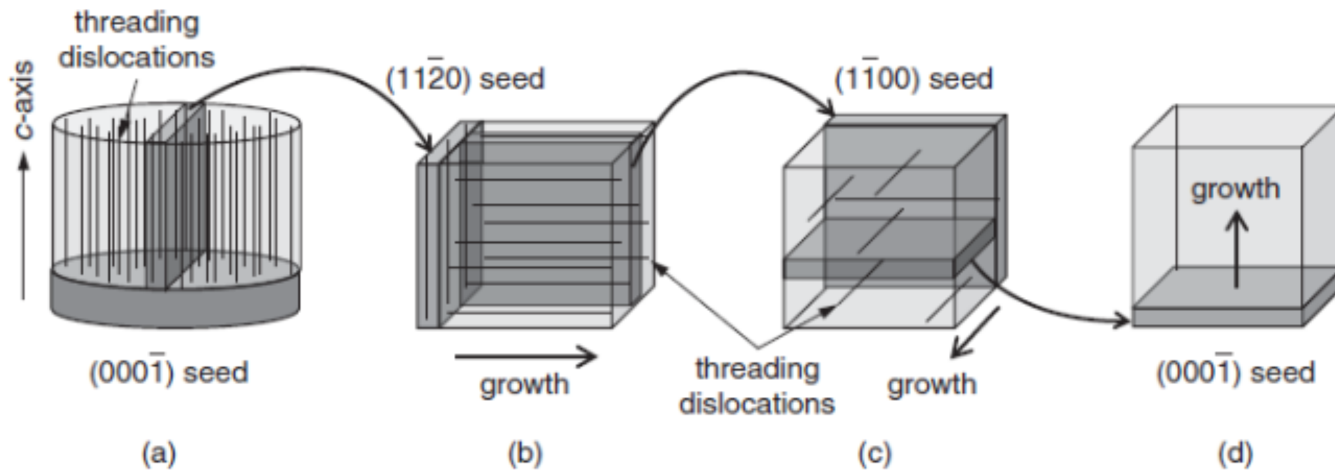


Figure 3.23 (a–d) Schematic illustration of the repeated *a*-face process in SiC boule growth.

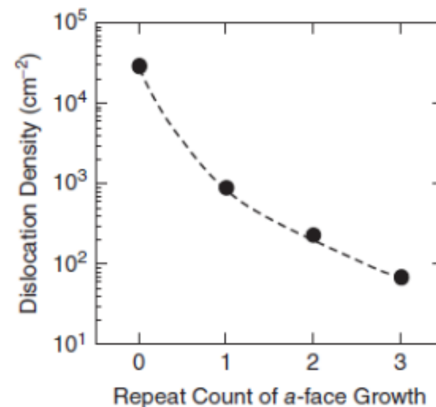


Figure 3.24 Total density of dislocations as a function of the number of *a*-face (or *m*-face) growth steps [78].

Epi Defects

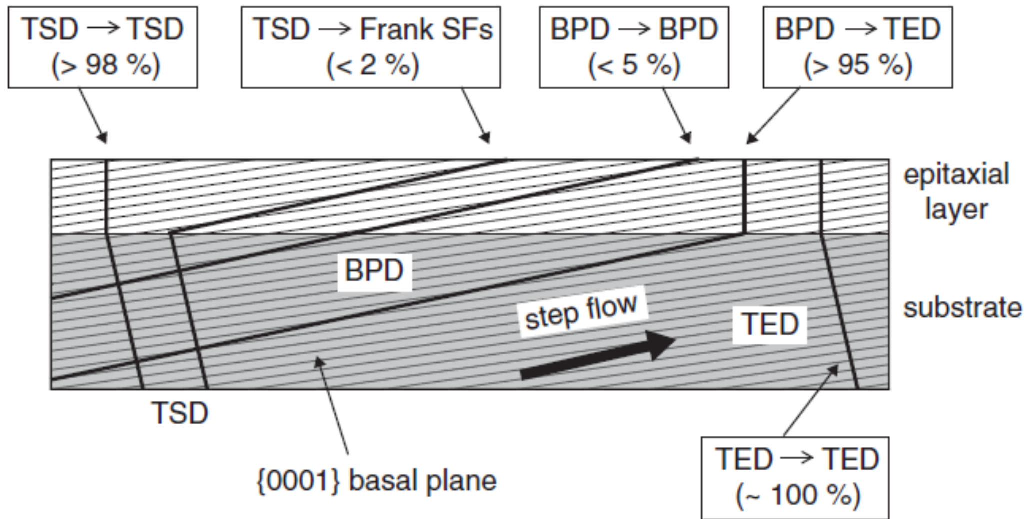


Figure 4.25 Schematic illustration of dislocation replication and conversion typically observed in 4H-SiC epitaxial layers grown on off-axis {0001} by CVD.

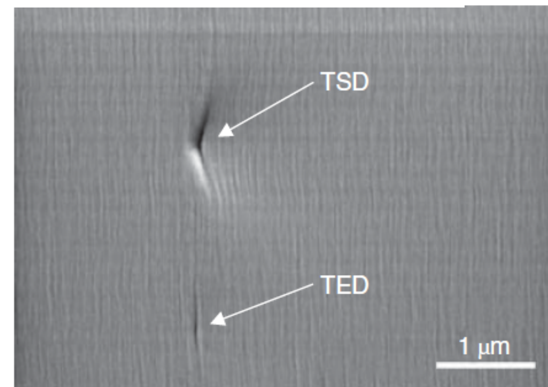
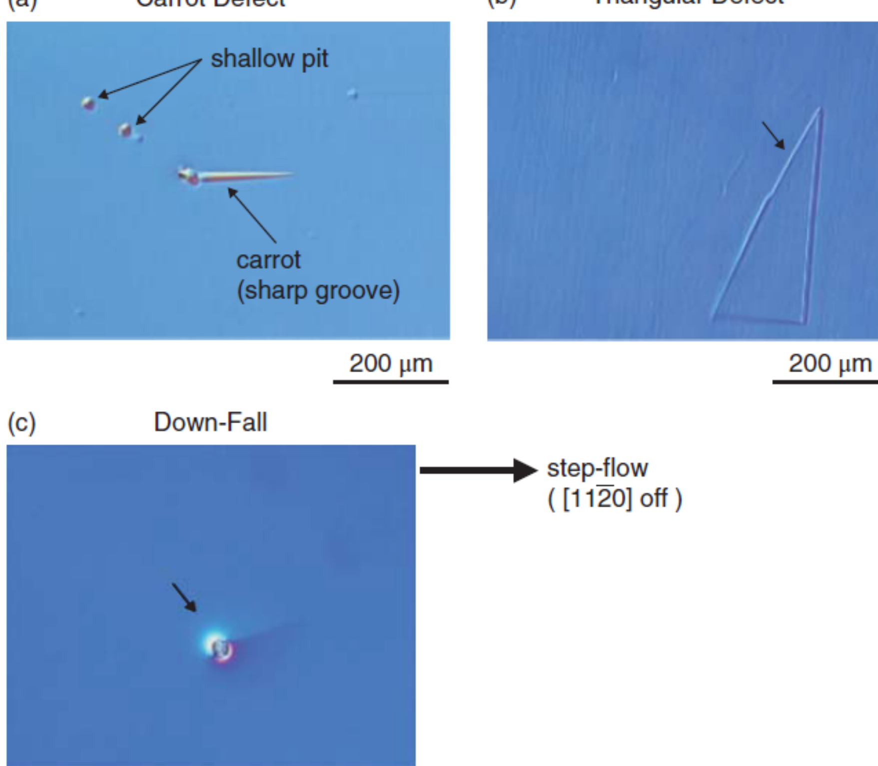


Figure 4.23 Surface morphology of a 4H-SiC epitaxial layer observed by scanning electron microscopy (SEM) ([105] reproduced with permission from The Electrochemical Society (ECS)). The image is taken with low acceleration voltage SEM to enhance the resolution.

Epi Defects

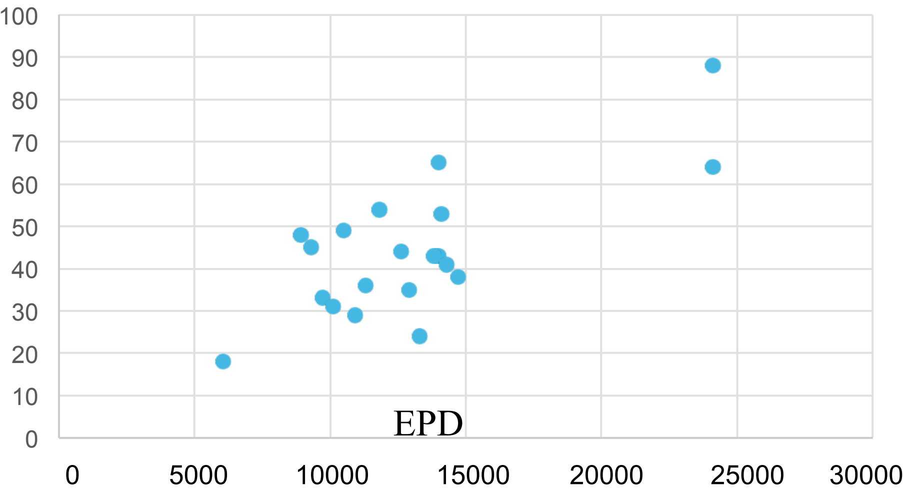


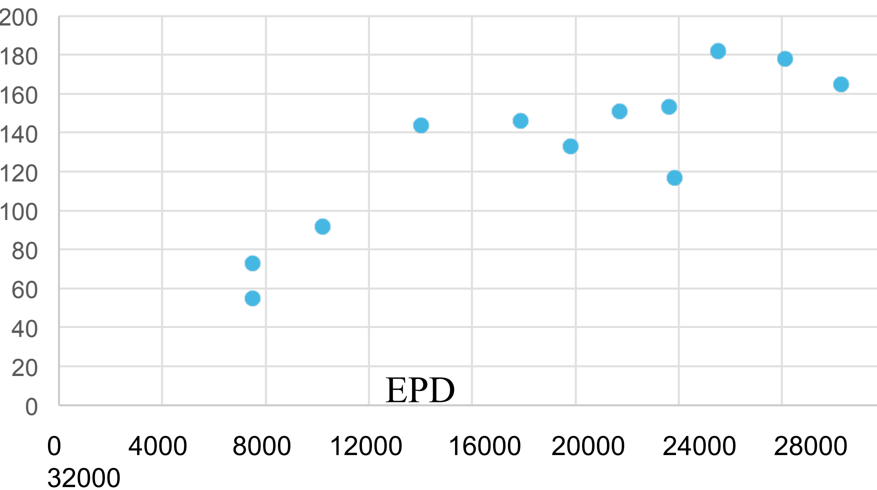
gure 4.20 Typical surface defects observed in 4H- and 6H-SiC{0001} homoepitaxial layers: (a) "car-t" defect and shallow pit, (b) triangular defect, and (c) down-fall.

CVD process
Si-rich → Carrot
C-rich → Triangle

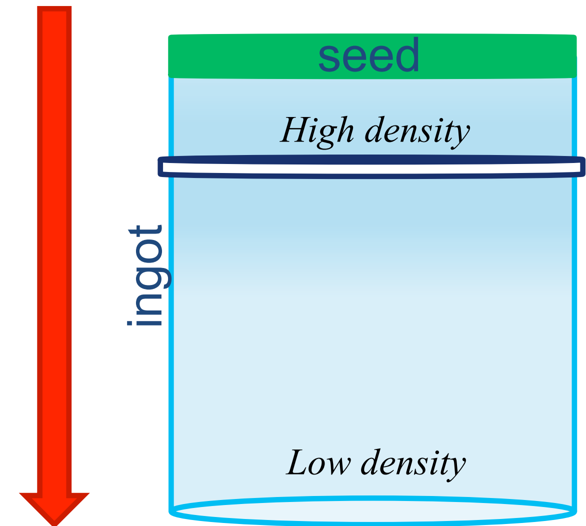
Extended epi defect	Current Density (cm^{-2})
Down Fall	0.1
Triangular defects / Comets	0.2
Carrots / Pit	0.5-1
Stacking Faults	1

Dislocations Vs Epi defects



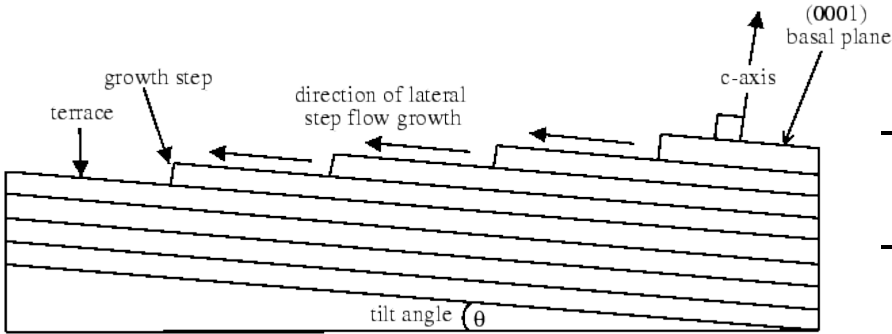


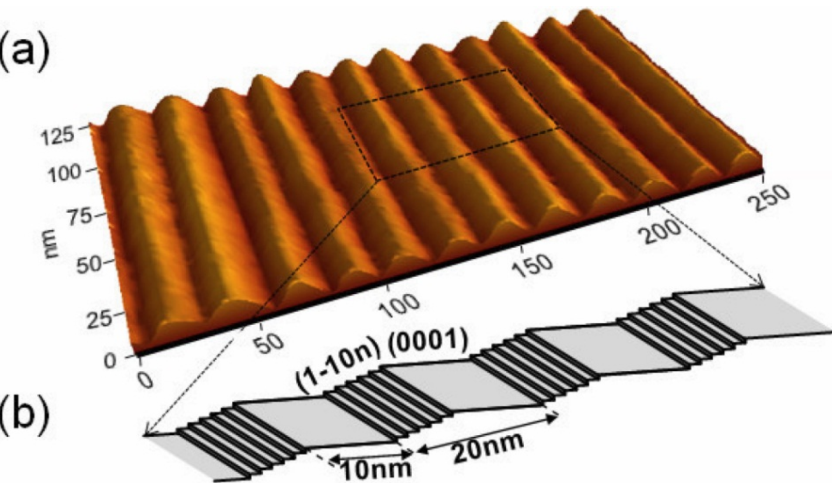
EPD=TSD+TED+BPD



The spread observed is mainly due to uncorrect EPD value declared.
EPD decrease along the bulk growth.
The EPD value is, typically, detected by etching a wafer within or on the edge of the ingot. This method produce a reference value for all the ingot, but, truly speaking, it is only an approximate value for all the wafers.

Epi defect: Step bunching and roughness





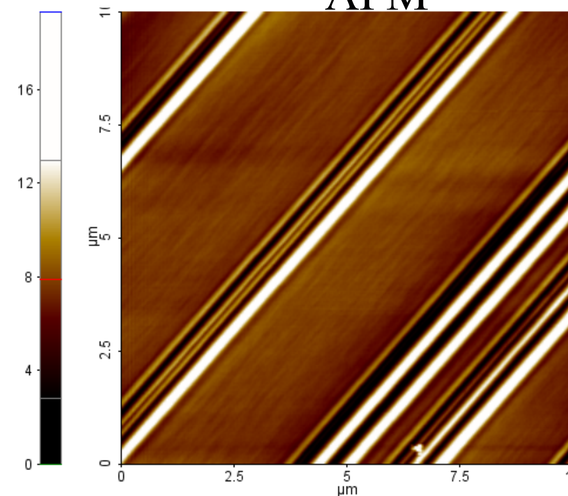
-Step Flow

-Epitaxial process parameters

-No relevant effects on device performances

- Crucial growth parameters: Temperature, growth rate, Si/C

AFM



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Data Gain	-110.99E-6 (µm/step)

Rq < 1nm

Stacking Faults

perfect 4H 1SSF 2SSF 3SSF 4SSF

c
h
3
1
6
5
4
4
3
2
2
2
Slip plane
C atom
Si atom
A B C A B C A B C A B C A B C A B C A B C A B C A B C A B C A B C A B C

(a) 2 2 2 4 4 2 2 2 1 nm
(b) 2 2 2 5 3 2 2 2 1 nm
(c) 2 2 2 2 6 2 2 2 2 1 nm

Band gap diagramme

4H- SiC
4H- SiC
SF

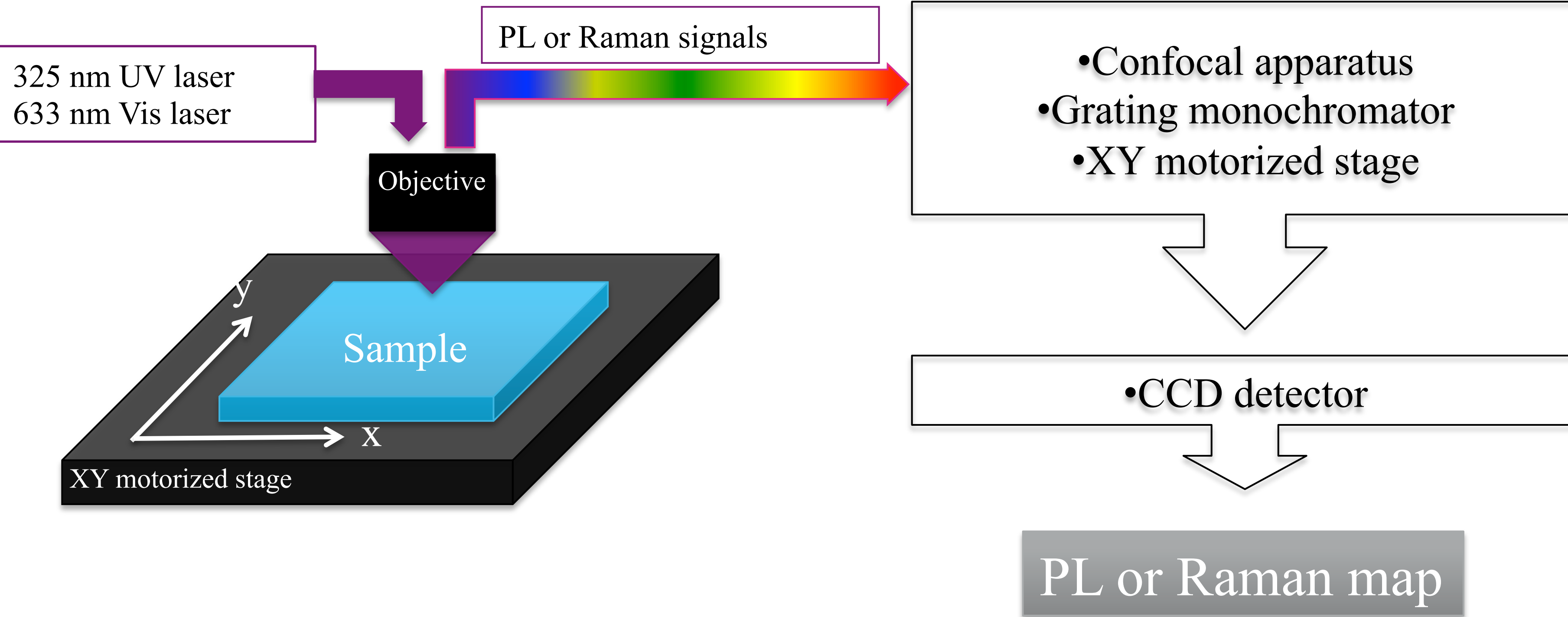
Photon Energy (eV)
3.6 3.4 3.2 3 2.8 2.6 2.4
PL Intensity (a.u.)
1.2x10^4
1.0x10^4
8.0x10^3
6.0x10^3
4.0x10^3
2.0x10^3
0.0
350 400 450 500 550
(a) Bar-shaped SF
(b) 2SSF(6,2)
(c) 4SSF(4,4)
4H-SiC (no SFs)

Impacts of epi defects on devices

Current Density (cm^{-2})	Defect	SBD	MOSFET, JFET	Pin, BJT, Thristor, IGBT
~ 0	**Micropipe**	V_B reduction (by 50-80%)		
500	**TSD (without pit)**	NO	NO	NO, but can causes local reduction of carrier lifetime
3000	**TED (without pit)**	NO	NO	NO, but can causes local reduction of carrier lifetime
1000	**BPD (including interface dislocation, half loop array)**	NO, but can cause degradation of MPS Diode	NO, but can cause degradation of body diode	Bipolar degradation (increase of on-resistence and leakage current)
0.01 - 1	**In-grown SF**	V_B reduction (by 20-50%)	V_B reduction (by 20-50%)	V_B reduction (by 20-50%)
0.1 - 1	**Carrot, triangular defect**	V_B reduction (by 30-70%)	V_B reduction (by 30-70%)	V_B reduction (by 30-70%)
0.1 - 1	**Down fall**	V_B reduction (by 50-90%)	V_B reduction (by 50-90%)	V_B reduction (by 50-90%)

SBD = Schottky barrier diode; MOSFET = metal-oxide-semiconductor field effect transistor; JFET = junction field effect transistor; BJT = bipolar junction transistor; IGBT = insulated gate bipolar transistor; MPS = merged pin-Schottky

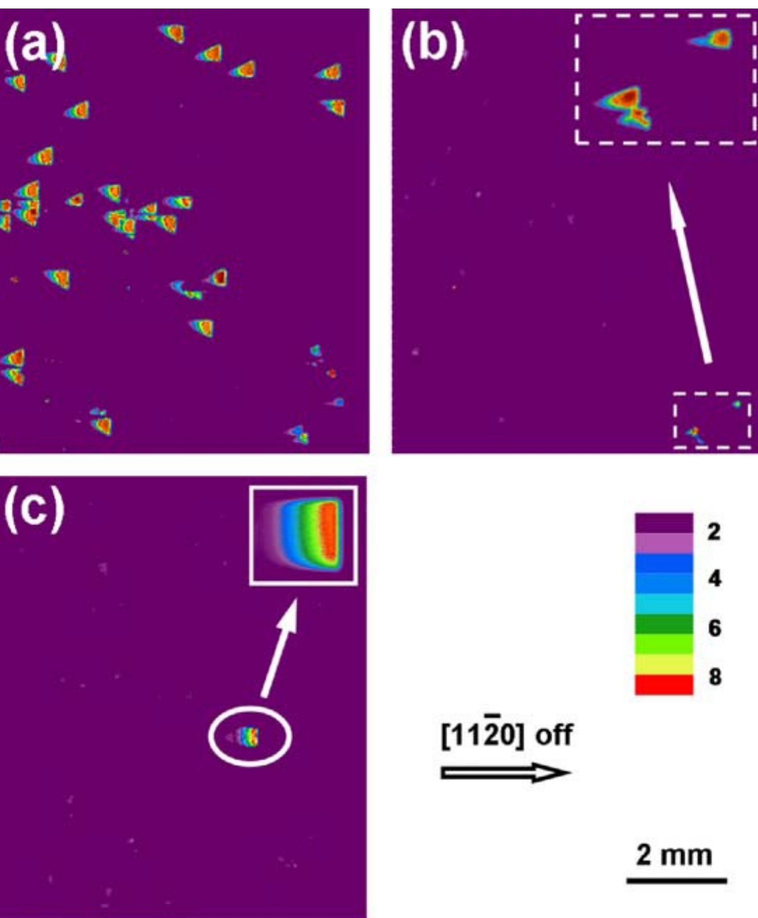
Spatially resolved micro-photoluminescence and micro-Raman setup



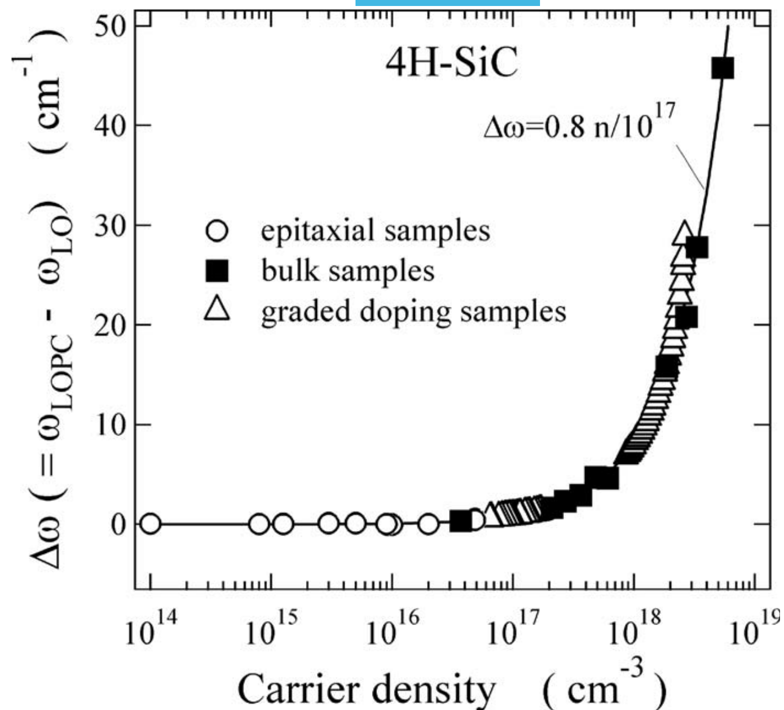
Evaluations of:

- **Crystallographic defect (PL and Raman)**
- **Doping (PL and Raman)**
- **Stress (Raman)**
- **Polytype inclusion (PL and Raman)**

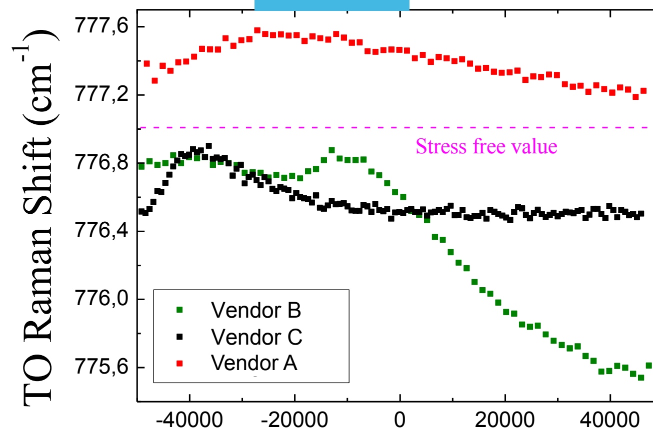
Stacking Faults



Doping

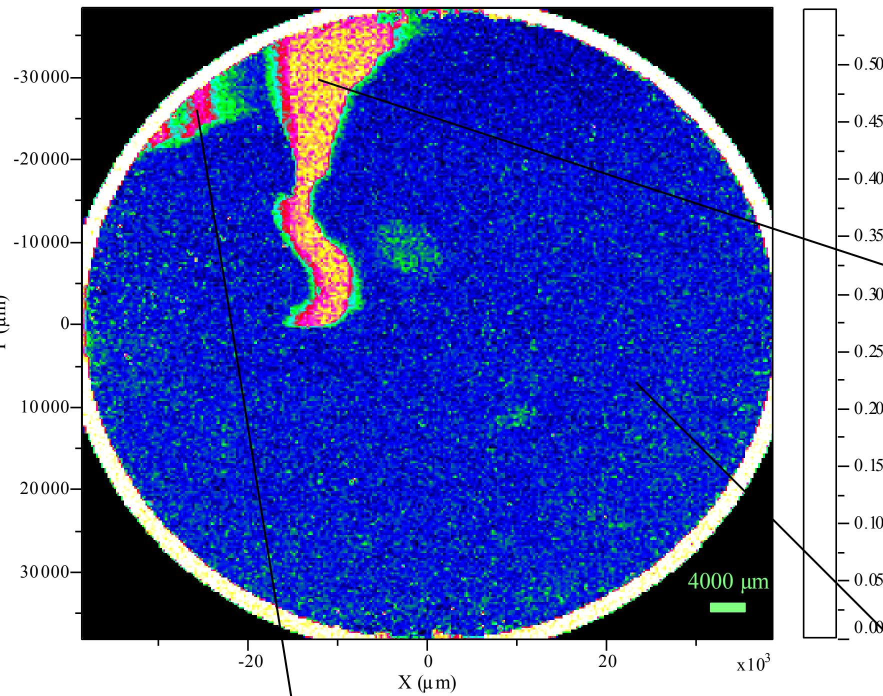


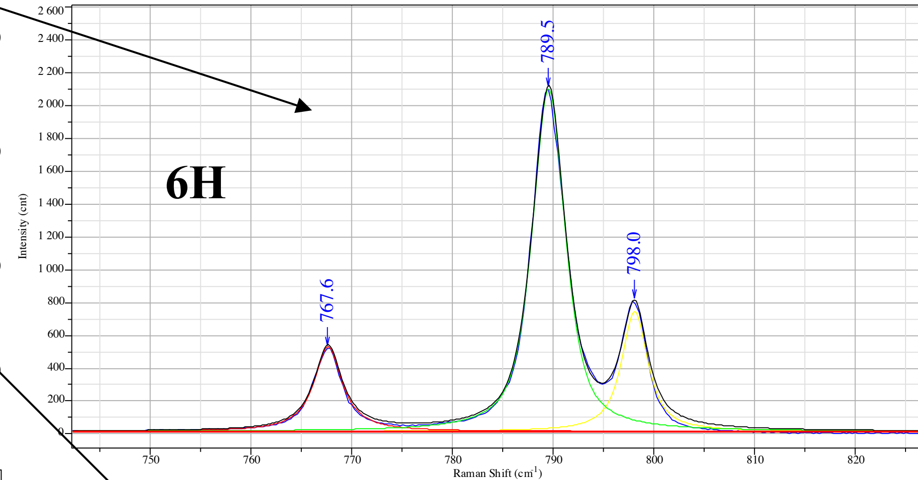
Stress

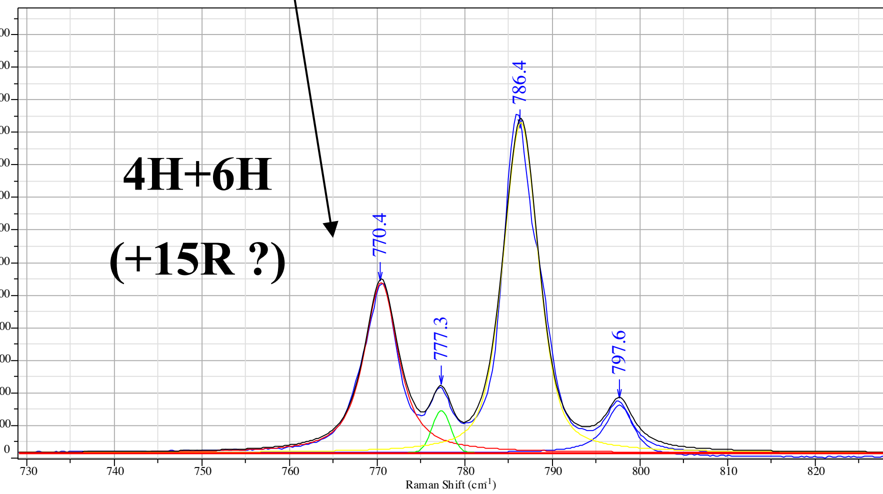


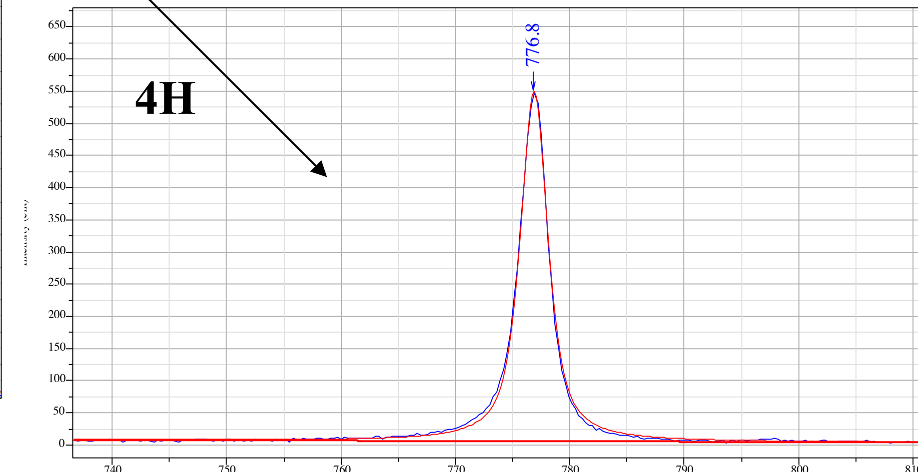
Polytype inclusion analysis (HeNe)

Transverse optical mode (TO)



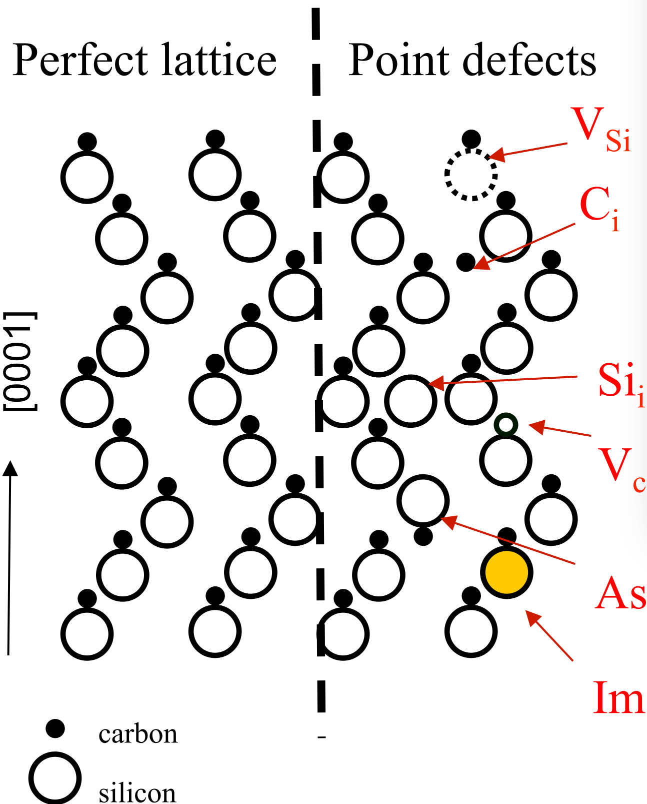


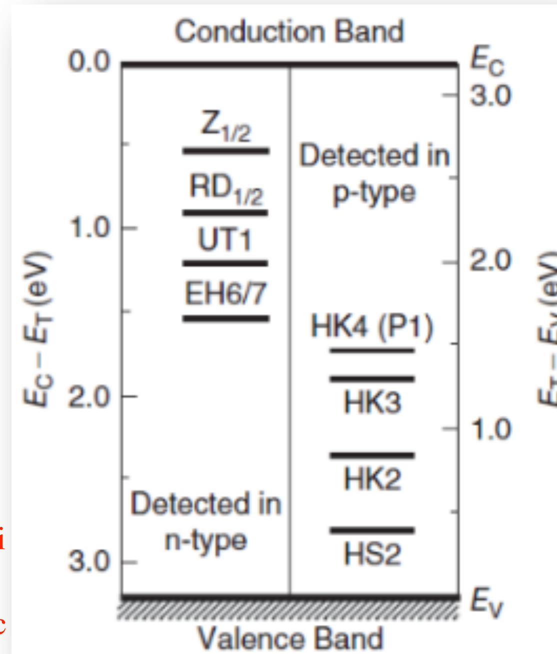




Point Defects

- Intrinsic (interstitial, vacancy, antisite)
  Si_i, C_i, V_{si}, V_c, C_{si}, etc
- Extrinsic (impurity)
- Complex





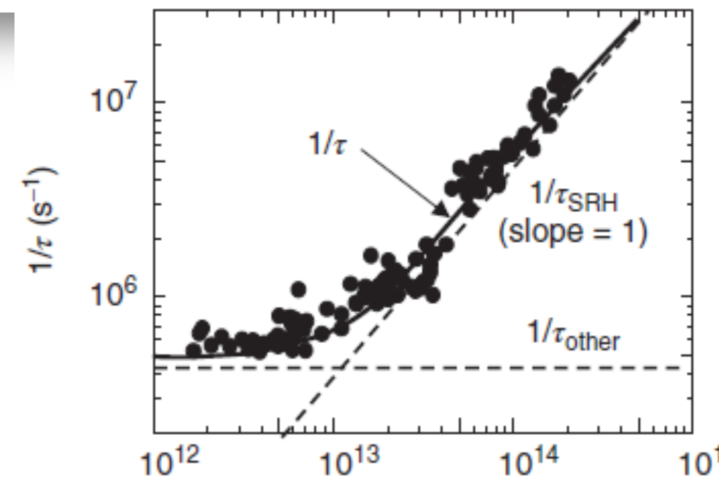
Energy levels of major deep levels observed in as grown n-type and p-type 4H-SiC epitaxial layers

After Annealing at 1600°C, $Z_{1/2}$ and $EH_{6/7}$ remain important level

$EH_{6/7}$ is a carbon vacancy

Also, the origin of the Z1⁄2 center was identified as the acceptor levels of a carbon vacancy

$Z_{1/2}$ = Ec-0.63eV
$EH_{6/7}$ ~ Ec/2 eV



μ-PCD and DLTS methods

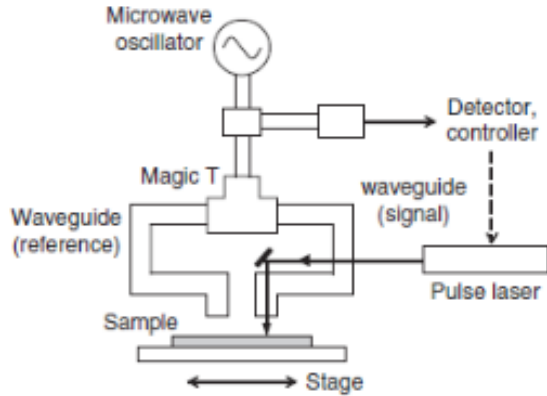


Figure 5.13 Schematic illustration of a differential μ-PCD measurement set-up.

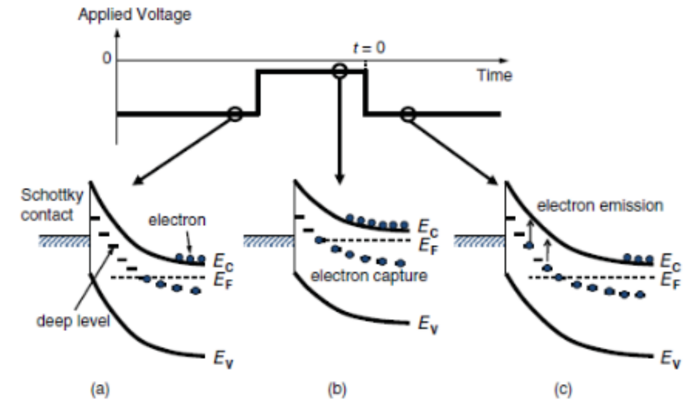
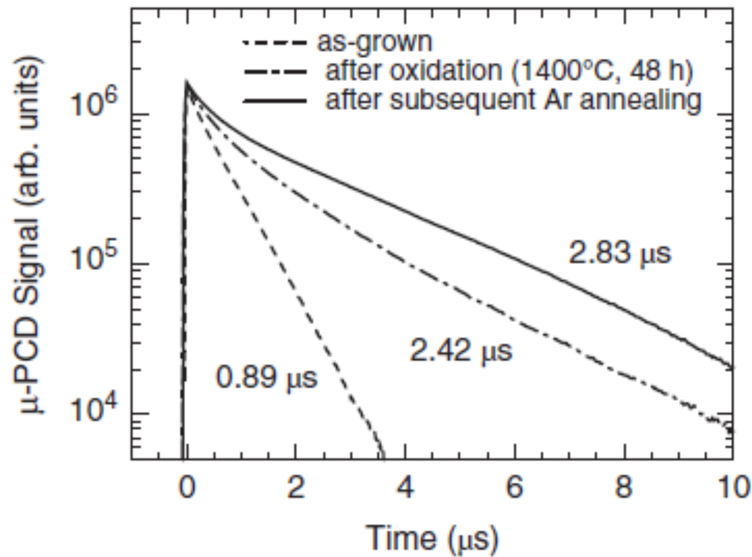
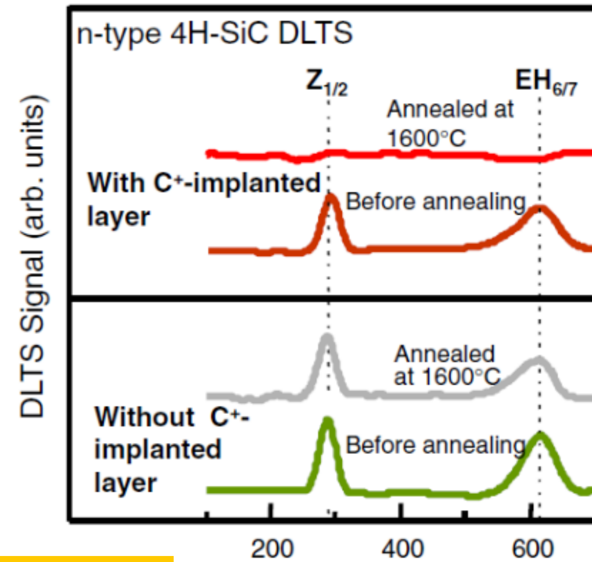
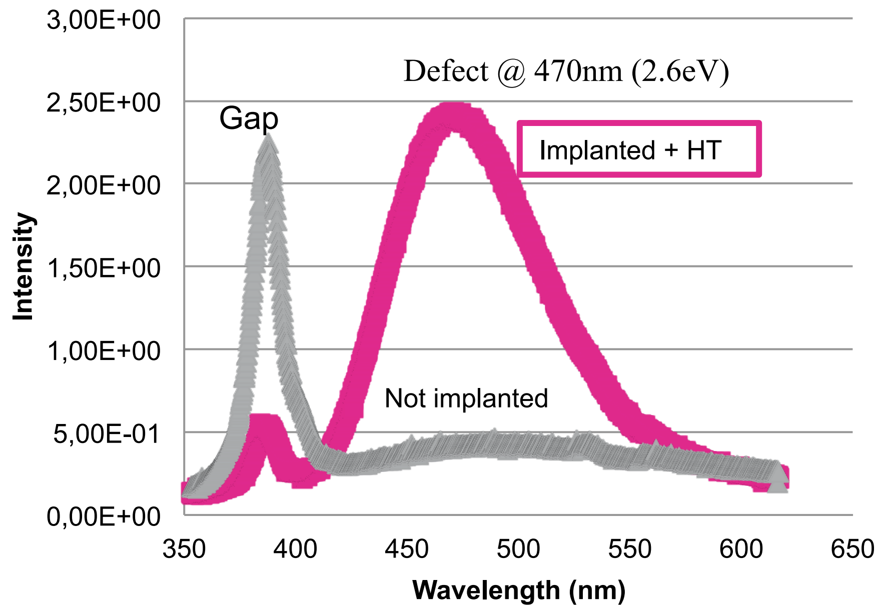


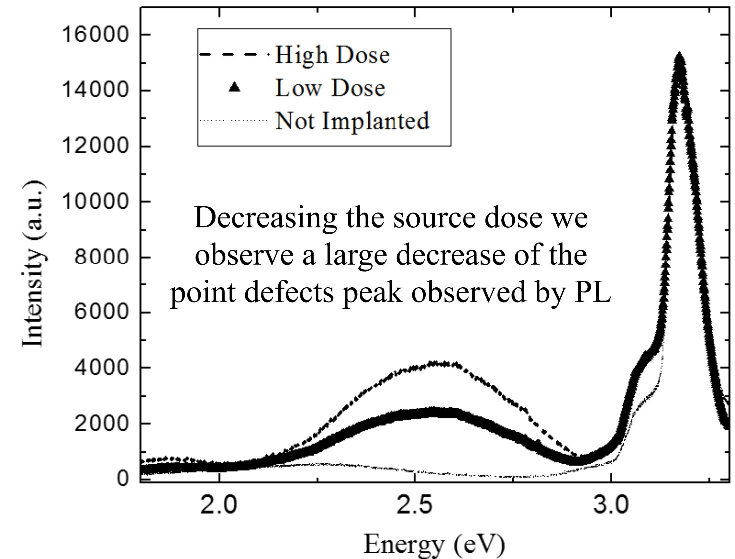
Figure 5.28 Typical bias voltage sequence that is applied during DLTS measurements of an n-type semiconductor (Schottky structure), along with the energy band diagrams, which correspond to (a) the steady state under a reverse bias voltage, (b) during application of a pulse voltage, and (c) after application of the pulse voltage, respectively.



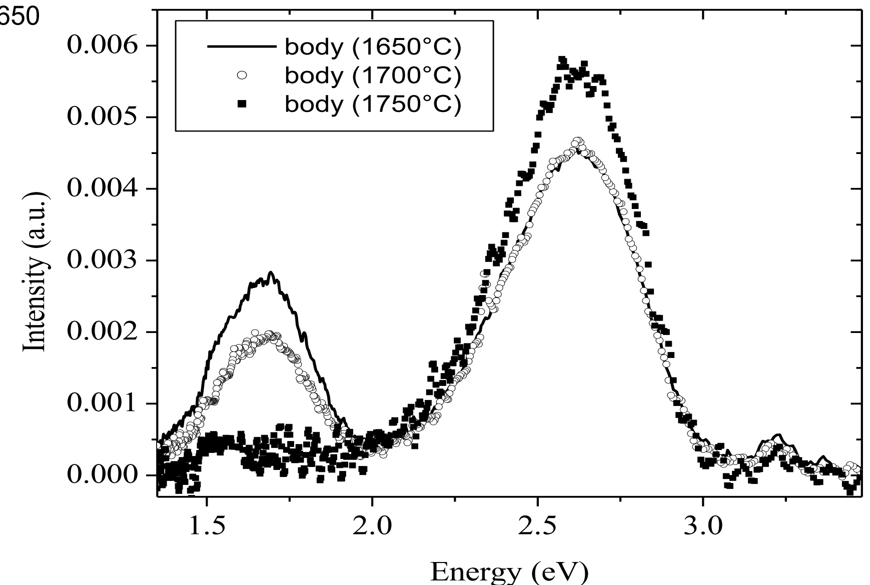


Defects from implantation



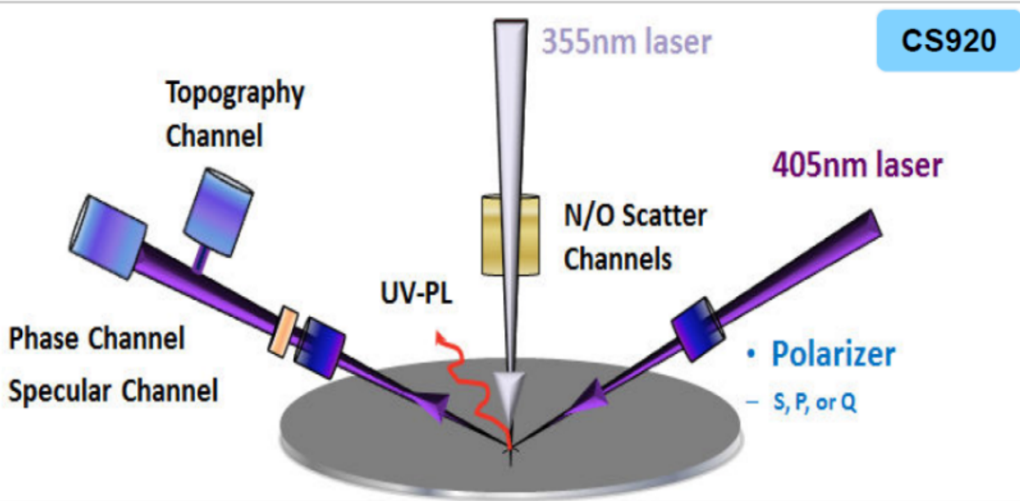


Implantation process produces a damage on the lattice crystal. By performing an annealing at high temperature (T > 1600 °C) the crystal is partially recovered. However, an agglomeration of defects is still present and observed by PL characterization.



An optimization of Ion dose and Ann. temperature is on going

Candela tool (scattered light)



Candela CS920

✓ *Designed and developed for MACRO & MICRO defect detection & auto classification to meet industry's requirement*

✓ *Improved FS / BS signal separation on transparent and semi-transparent wafers*

✓ *Dual laser implementation along with new robust, repeatable and reliable handler with higher throughput*

✓ *Use of UV laser integrating surface and photoluminescence detection in single platform & auto classification of sub-micron KILLER defects*

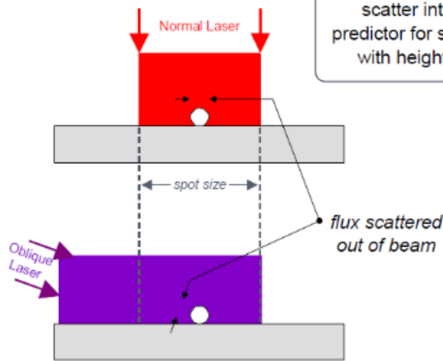
✓ *Delivers higher Throughput @ higher Sensitivity*

✓ *New software platform for mass production use case and higher throughput, with better stability → ease of use*

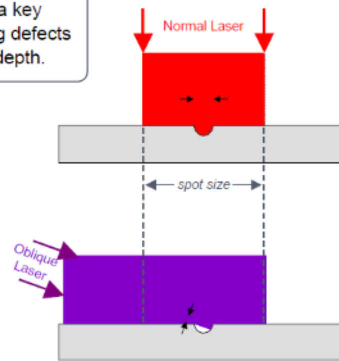
✓ *Improved tool to tool matching*

✓ *Hi Resolution Imaging mode allows for clear review of defects*

The ratio of Normal to Oblique scatter intensity is a key predictor for separating defects with height versus depth.



flux scattered out of beam



Particle Response

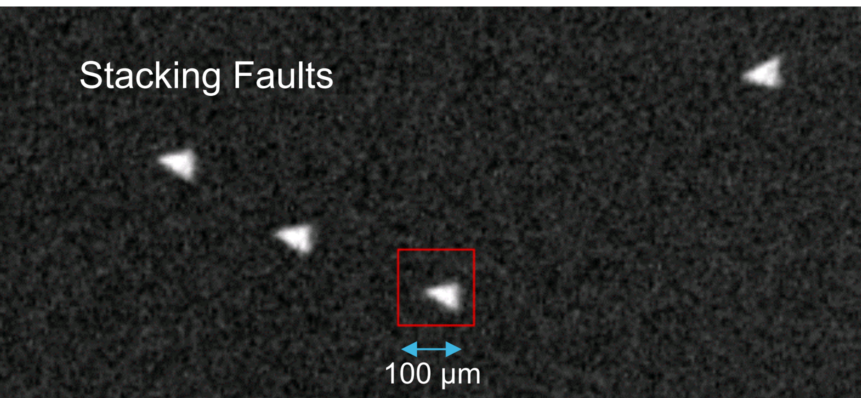
$$\frac{\text{Normal Scatter Intensity}}{\text{Oblique Scatter Intensity}} < 1$$

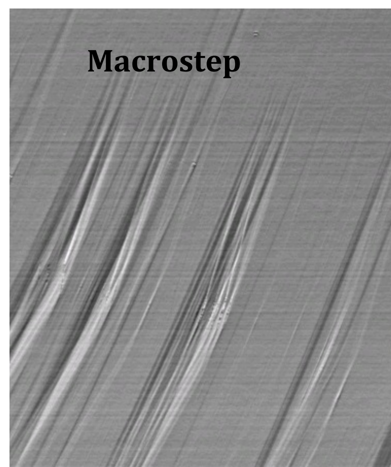
Micro-Pit Response

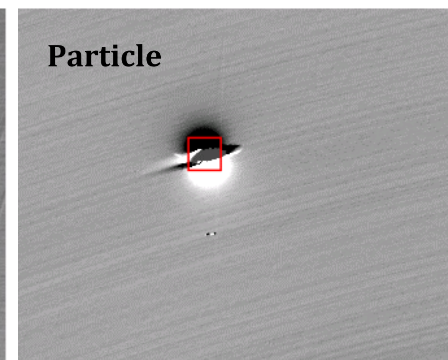
$$\frac{\text{Normal Scatter Intensity}}{\text{Oblique Scatter Intensity}} > 1$$

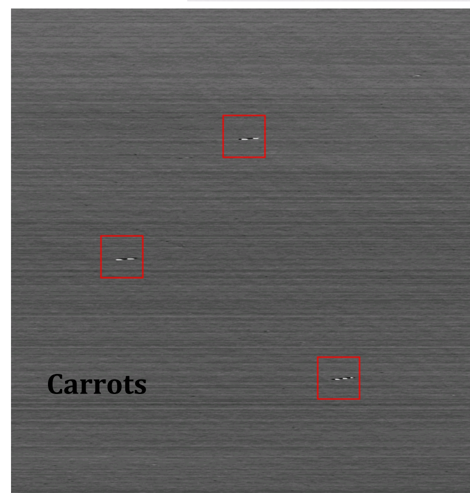
KLA Tencor Accelerating Yield

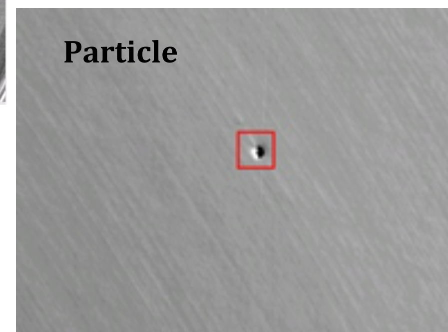
EPI 4H-SiC defects (Candela CS920 Images)

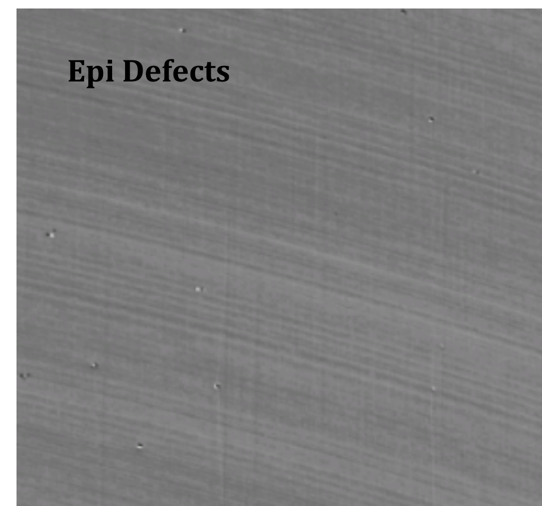






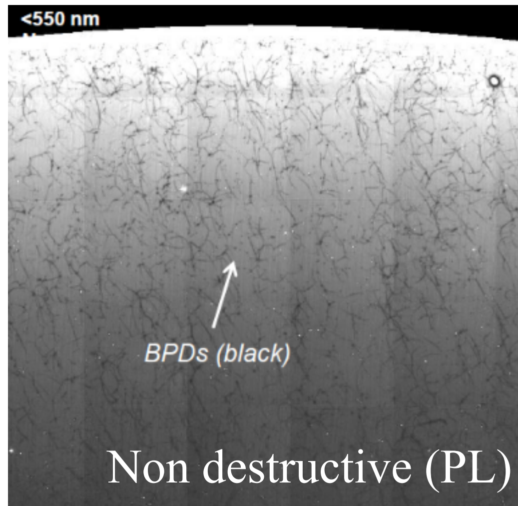


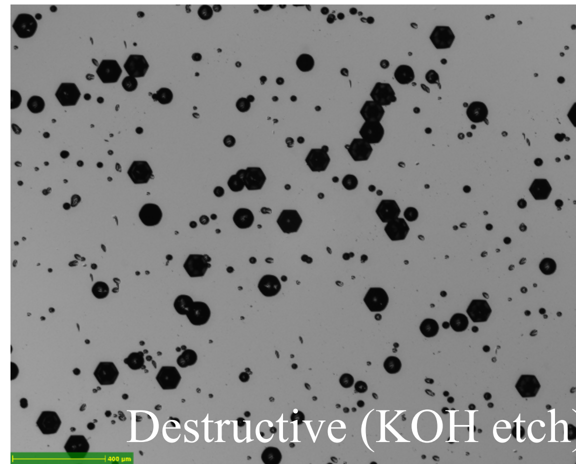




Conclusions

- Continuous quality improvement
- Wide choice in characterization techniques
- Different quality from different vendors
- Non destructive VS destructive characterization methods (dislocation density)





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