FRONT-END AND READ-OUT ELECTRONICS FOR THE NUMEN FPD

D. LO PRESTI

D. BONANNO, F. LONGHITANO, D. BONGIOVANNI, S. REITO

INFN- SEZIONE DI CATANIA

INFN Istituto Nazionale di Fisica Nucleare

SICILIAE STVDIVM GENERALE 1434

OVERVIEW

- *NUMEN -> Upgrade of Cyclotron and Detector -> Higher Event rate*
- *Needed upgrade of the front-end and read-out electronics for the Focal Plane Detector (FPD):*
  - *Tracker;*
  - *ΔE-E Telescopes;*
- *Definition of the front-end and read-out architecture:*
  - *Choice of the technologies;*
- *Design and test of the building blocks:*
  - *Front-end based on the VMM2 chip by BNL;*
  - *Read-out based on the SOM by National Instruments.*
- *Design and construction of the FPD detector:*
  - *Detector interface to front-end;*
  - *Interconnections, cabling…*
  - *Power distribution;*
  - *Slow control;*
  - *…*

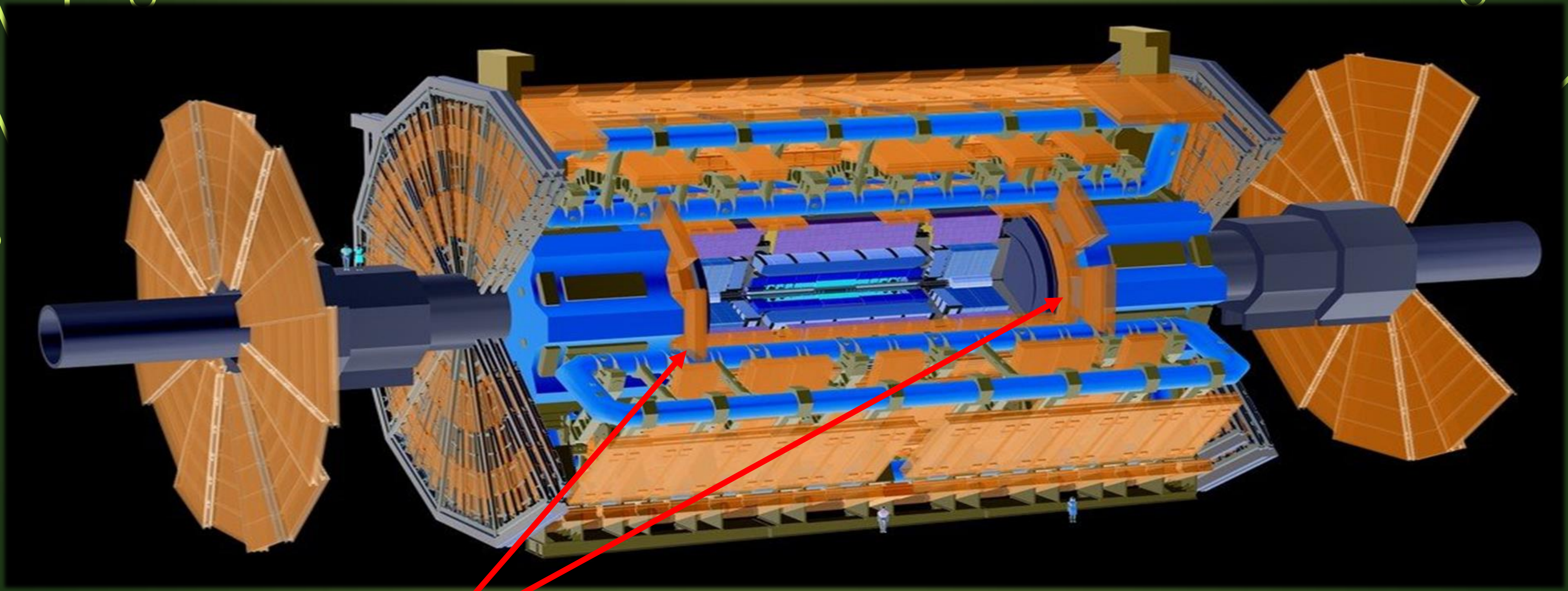
FOCAL PLANE DETECTOR (FPD) *specifications*

- ***Tracker***:
  - *16 layers, 1 m width, segmented in 0,5 mm steps =32000 channels (2000 ch.)*
- ΔE-E Telescopes :
  - *40*100 ΔE-E SiC Telescopes (1x1 cm^2)= 4000 channels*

*Event Rate foreseen after the upgrade of the cyclotron: **100 KHz/cm***

- ***Modularity***
- ***Ease of maintenance***
- ***Re-configurability***
- ***Radiation Tolerance***
- ***Low Power***
- ***Low Cost***

ASIC for ATLAS Muon Spectrometer Upgrade



New Small Wheels

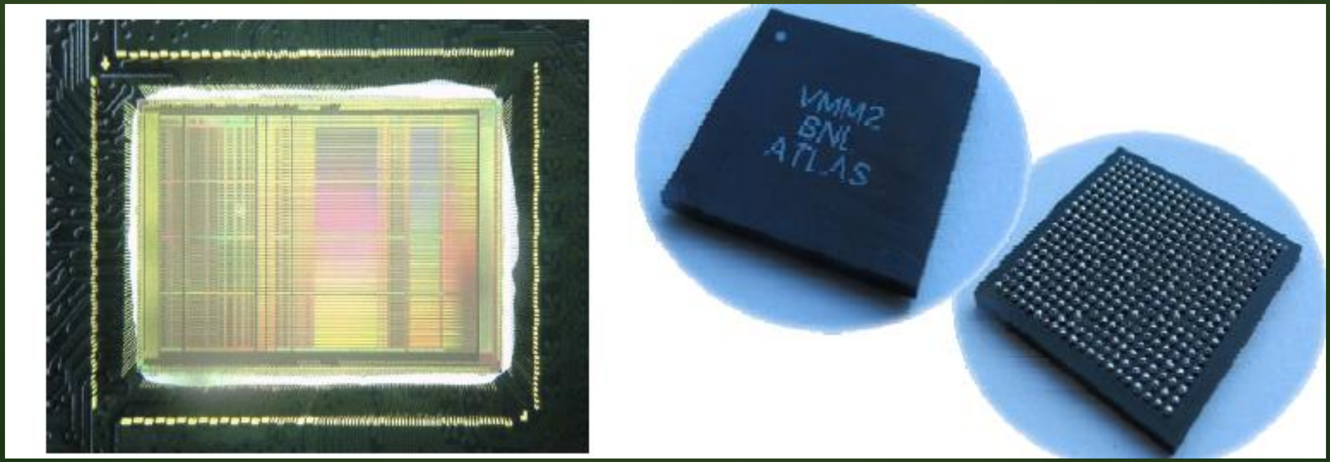
- sTGC
  Small Strip Thin Gap Chamber
- MM
  MicroMegas
  (MICROMEsh GAseous Structure)

Front-end Electronics (ASIC)

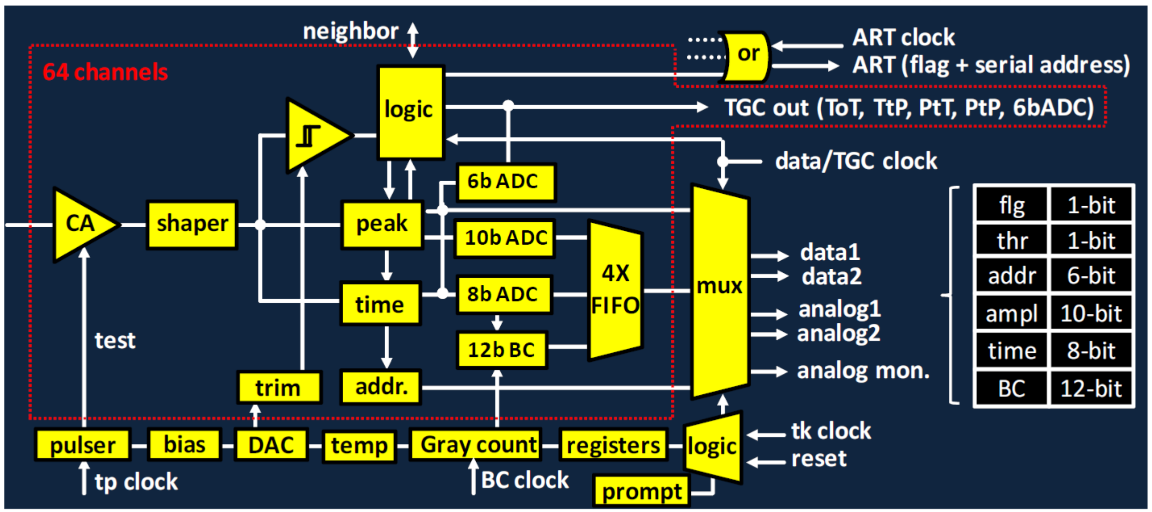
- more than 2.3 million channels total
- operate with both charge polarities
- sensing element capacitance 10-200 pF
- charge meas. up to 2 pC @ < 1 fC rms
- time meas. ~ 100 ns @ < 1 ns rms
- trigger primitives, neighbor logic
- low power, programmable

VMM2 CHIP
BROOKHAVEN NATIONAL LABORATORIES

- *Selected after a deep survey between available front-end ASICs;*
- *Designed for MicroMegas detectors in ATLAS;*
- *Collaboration established with the designer: **Prof. G. De Geronimo**;*
- *Radiation Tolerant;*
- *New version VMM3 could take in account the NUMEN specifications;*
- *Available in the future in big volume;*
- *All digital read-out compliant with the foreseen event rate;*
- *Suitable for all the detector types foreseen in the final FPD:*
    - *Tracker (GEM, MicroMegas);*
    - *Calorimeter- particle identification (SiC ΔE-E);*
    - *APD.*



VMM2 CHIP
BROOKHAVEN NATIONAL LABORATORIES



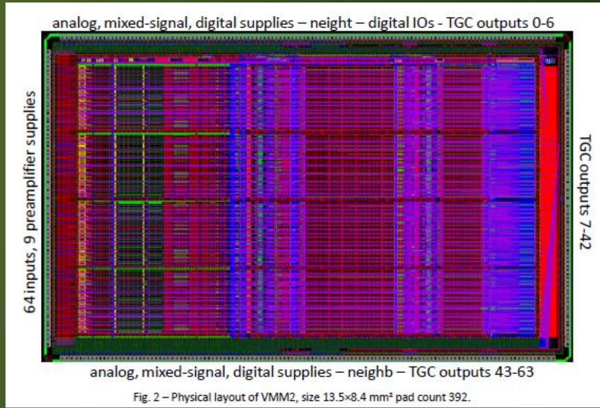


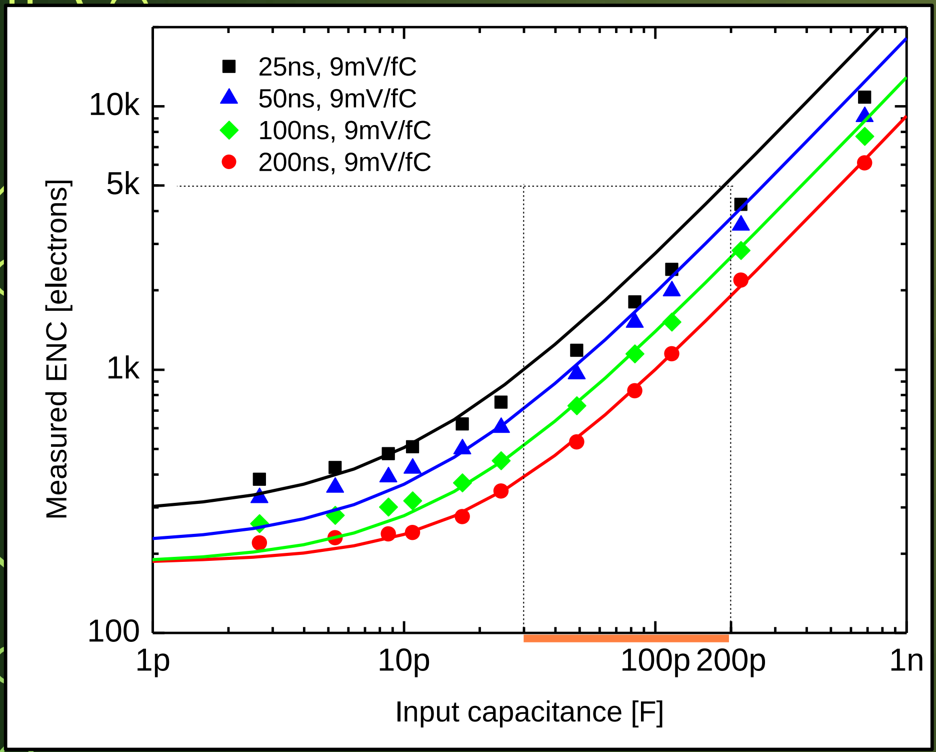
Fig. 2 – Physical layout of VMM2, size 13.5×8.4 mm² pad count 392.

130nm 1.2V 8-metal CMOS technology from IBM

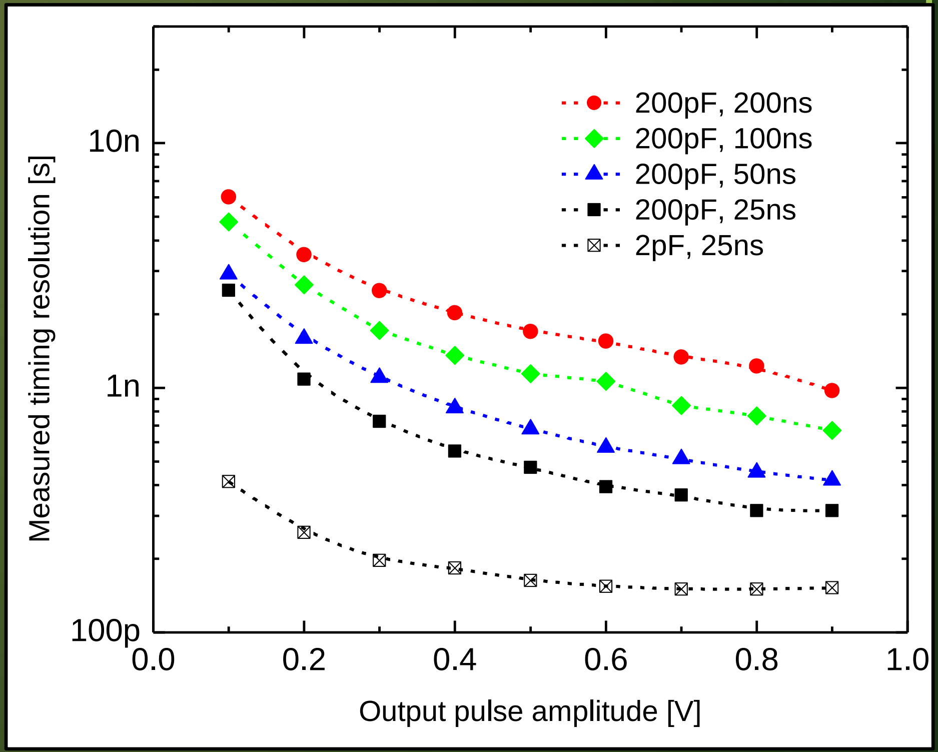
- *64 linear front-end channels:*
- *low-noise charge amplifier (CA) with adaptive feedback;*
- *test capacitor and pulse generator for calibration;*
- *adjustable polarity;*
- *optimized for a capacitance of 200pF and a peaking time of 25 ns.*
- *third-order shaper (DDF) - adjustable peaking time in four values (25, 50, 100, and 200 ns);*
- *Stabilized band-gap referenced baseline;*
- *Gain adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).*
- *Many mode of operation, selected "continuous digital":*
    - *38 bit generated for each event read-out @ about 200 MHz;*
    - *Id channel-peak amplitude (10b) - time stamp (10b);*
    - *4-event deep de-randomizing FIFO per channel, read-out token ring;*
    - *8 LVDS digital channel required for the read-out and control of the chip;*
- *Power dissipation 4 mW per channel.*

Resolution Measurements (VMM2)

charge resolution



timing resolution



G. De Geronimo, in "Medical Imaging" by Iniewski

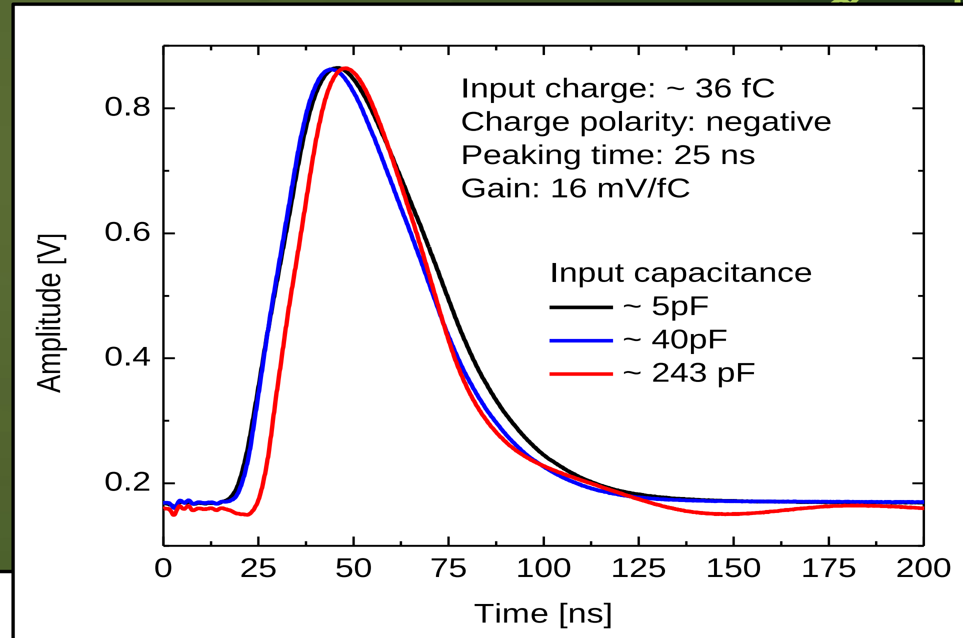
- *charge resolution ENC < 5,000 e⁻ at 25 ns, 200 pF*
- *analog dynamic range Q_{max} / ENC > 12,000 → DDF*
- *timing resolution < 1 ns (at peak-detect)*

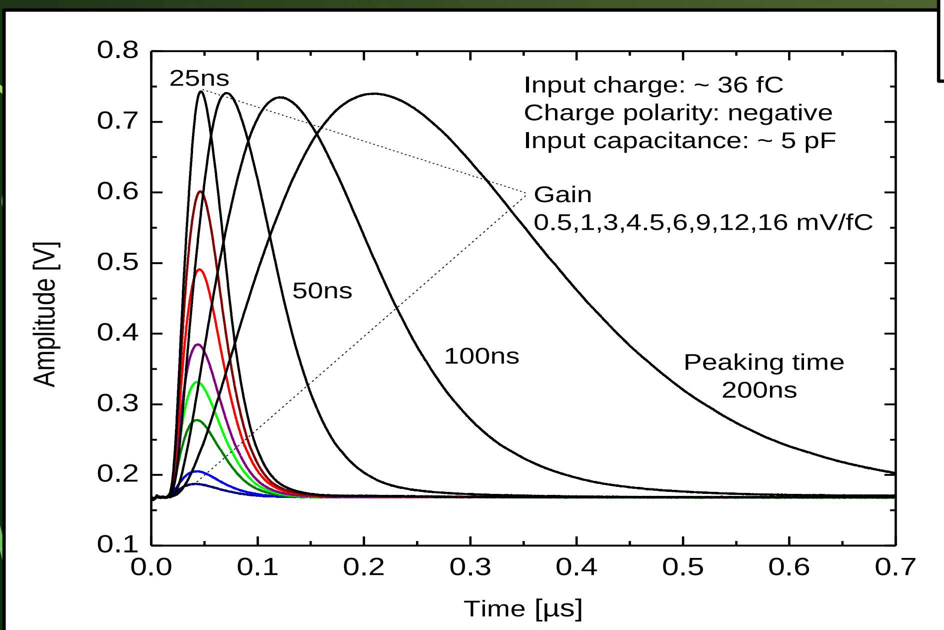
$$\sigma_t \approx \frac{ENC\ \tau_P}{Q} \frac{\lambda_P}{\rho_P}$$

≈ 0.3-0.8

Measured Pulse Response

- **Suitable for different detector capacitances**
- **Wide range of measurement parameters**
- **Test pulse pattern embedded**

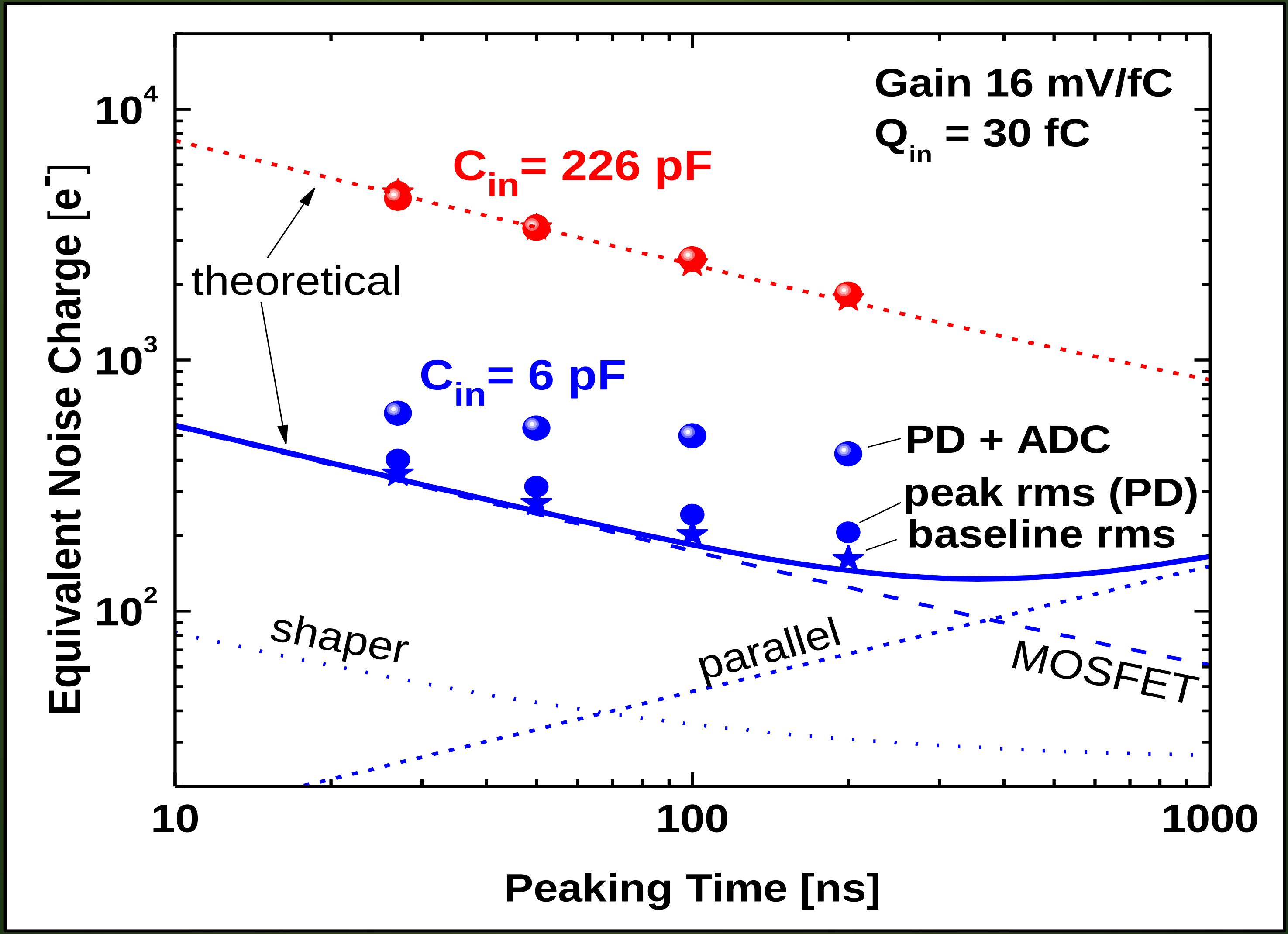




Peak-time ~26 ns

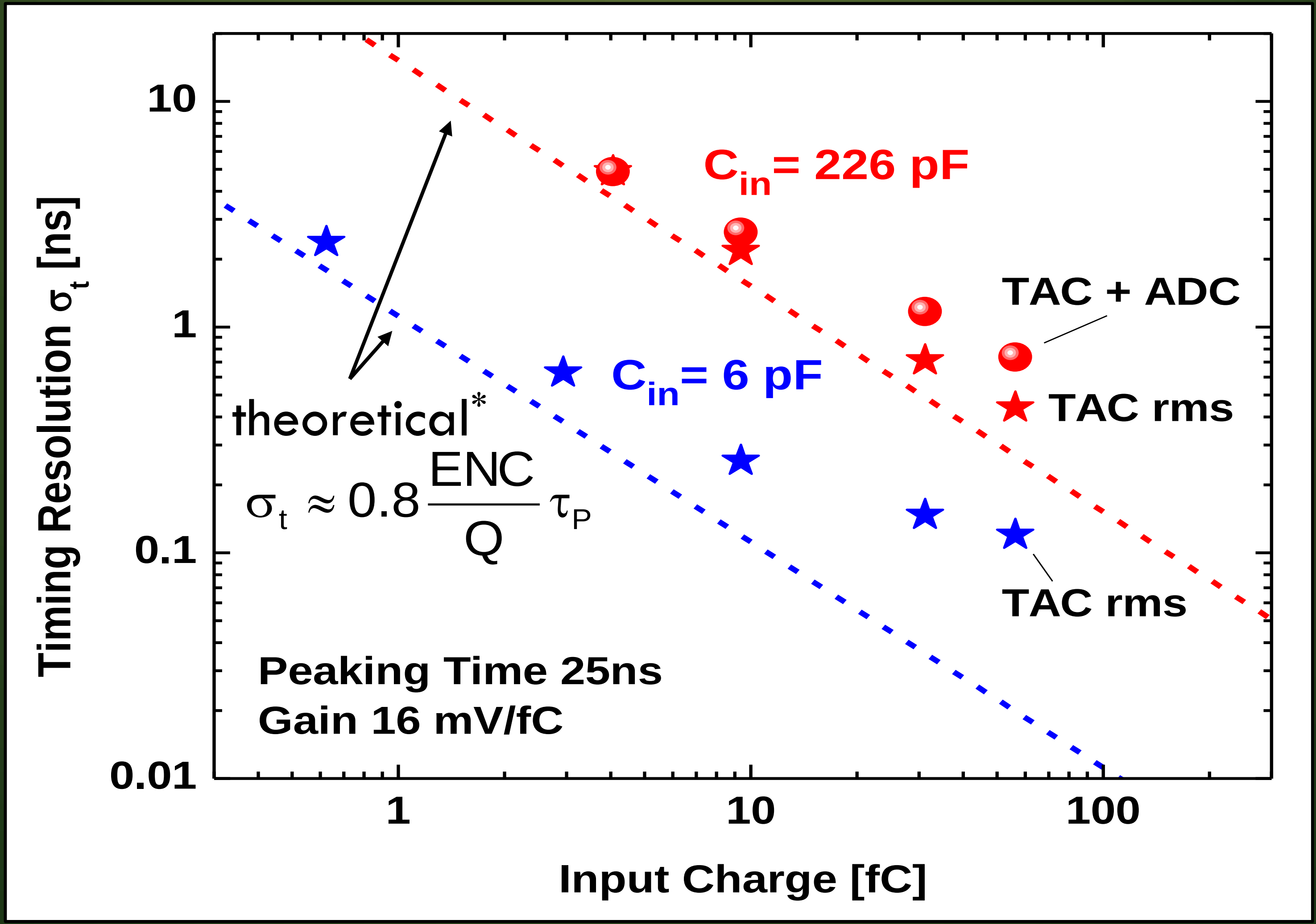
@ C_{in} = 240 pF

Measured ENC



ENC ~4,7k e⁻ (0.75 fC) at 25 ns, 226 pF (~5.6k at 0.5 mV/fC)

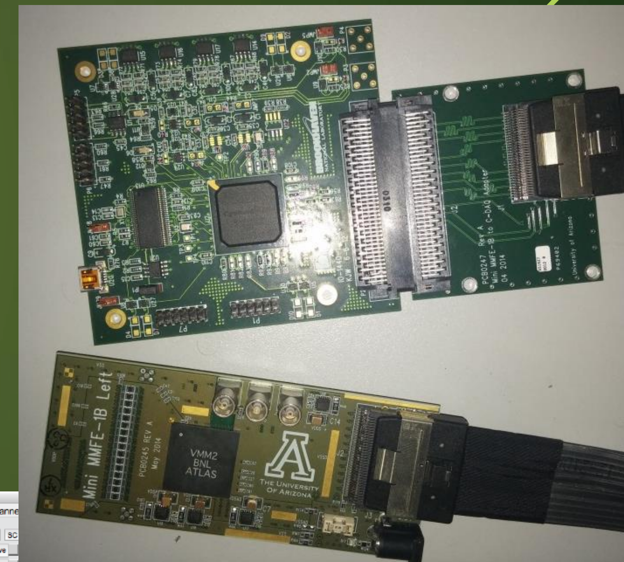
Measured Timing Resolution

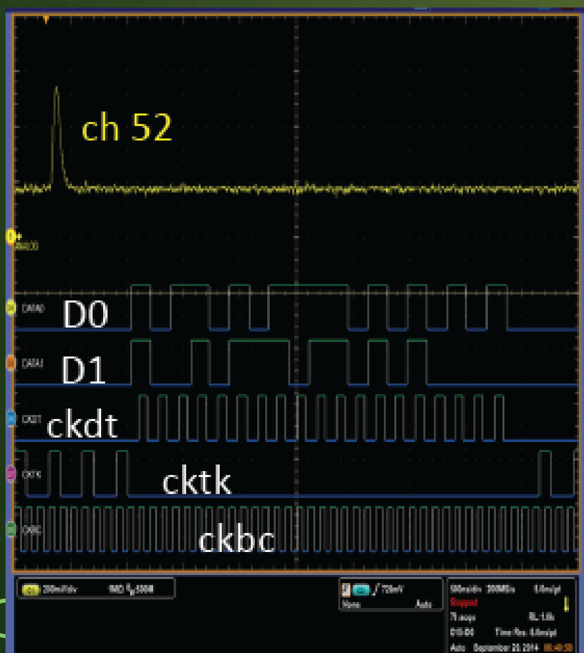


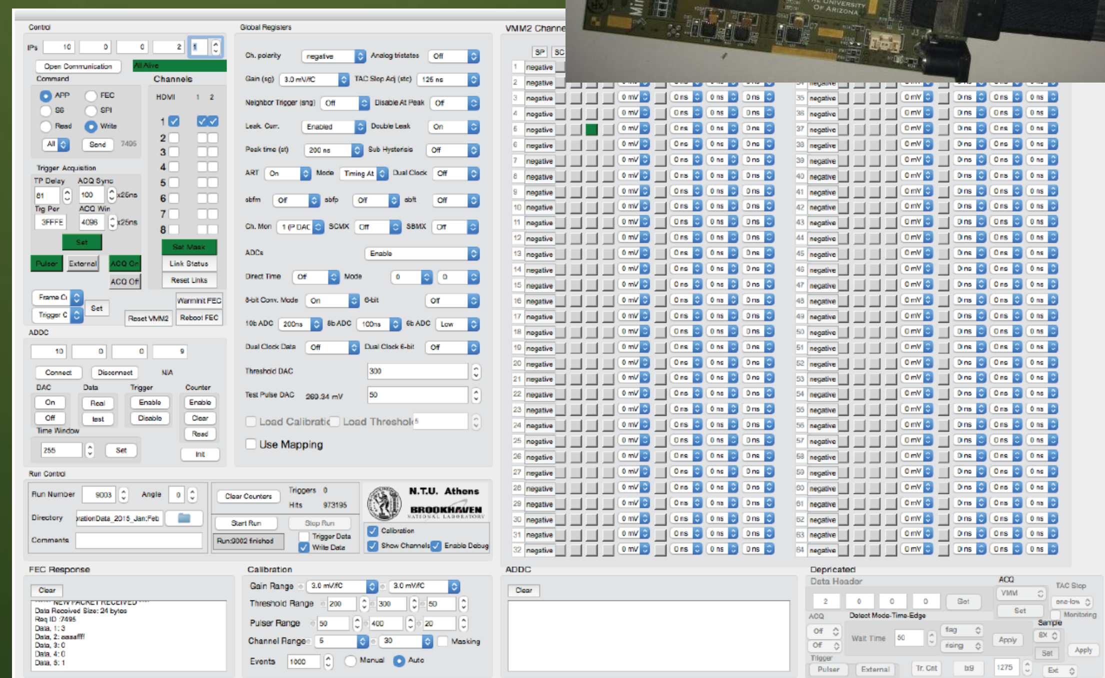
σ_t within few ns @ 25 ns, 226 pF

VMM2 Test board

Thanks to the collaboration with G. De Geronimo a complete FE-RO chain for one VMM2 chip is available from sept 2015. Control and read-out software included.





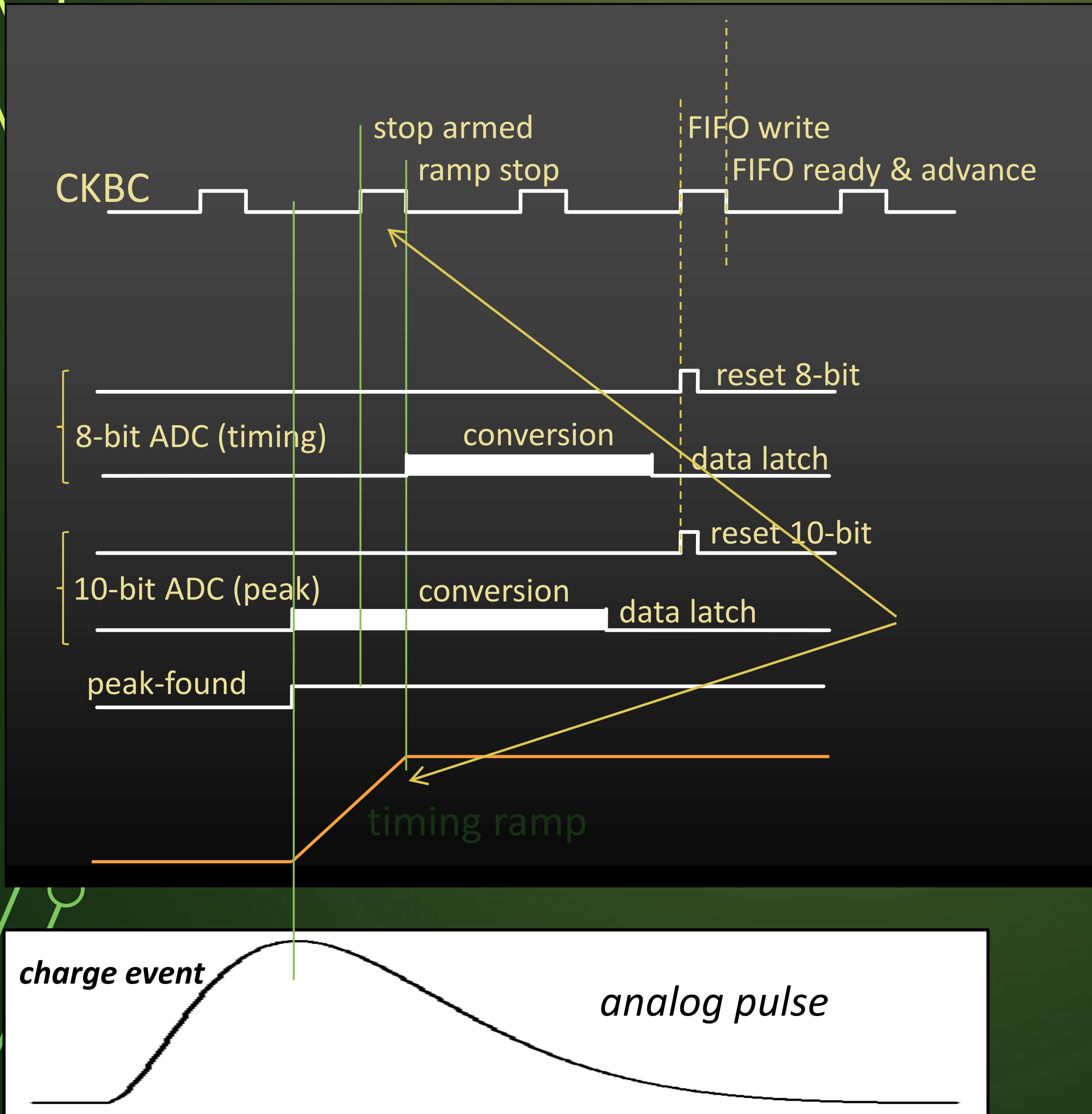


Continuous digital mode:

38 bit/event

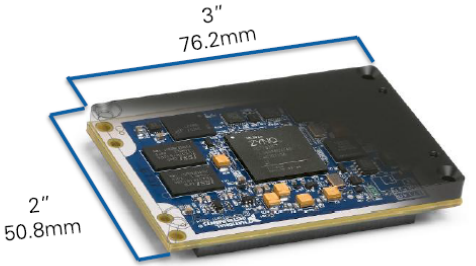
flg	1-bit
thr	1-bit
addr	6-bit
ampl	10-bit
time	8-bit
BC	12-bit

Timing Ramp Optimization



- *first ck of CKBC after peak-found stops ramp*
- *first ck of CKBC after latches writes FIFO*
- *8-bit ADC starts at stop of ramp, latches after conversion, resets at next rising edge of CKBC (after latch)*
- *10-bit ADC starts at peak, latches after conversion, resets at next rising edge of CKBC (after latch)*
- *timing ramp starts at peak-found; the next rising edge of CKBC arms the stop circuit; the next falling edge stops the ramp and starts the 8-bit ADC conversion*

NI System on Module (SOM) Specifications



Specifications

Processor SoC
Xilinx Zynq-7020 667 MH Dual-Core ARM Cortex-A9 Artix-7 FPGA Fabric
Size and Power
50.8mm x 78.2mm (2 in. X 3 in.) Typical Power: 3 W to 5 W
Memory
Nonvolatile: 512 MB DRAM: 512 MB
Operating Temperature
-40 °C to 85 °C Local Ambient

Read-out of VMMx chips will be performed by a SOM based board, custom designed for the experimental demands:

- *Low Power;*
- *Radiation Tolerance;*
- *Low Cost;*
- *Re-configurability;*

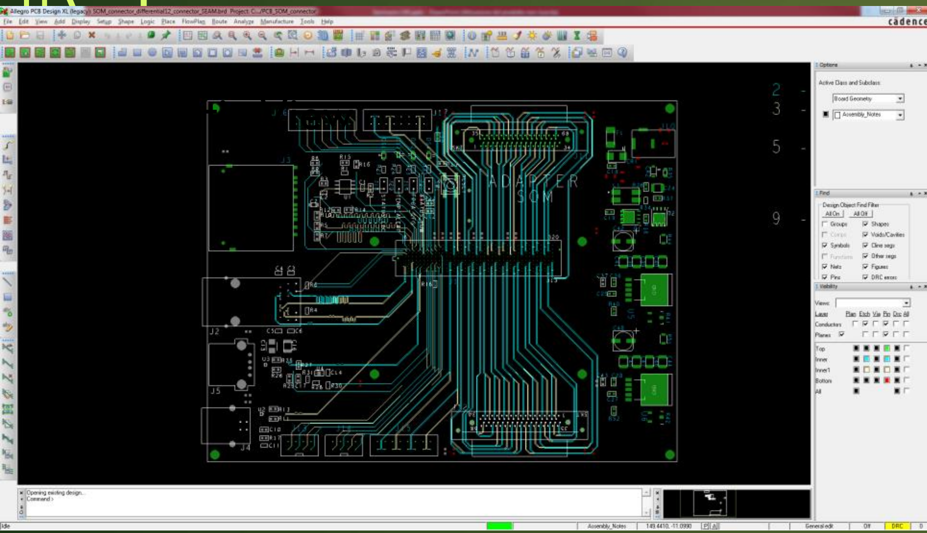
Re-programmable Intelligence on board will allow for:

- *composite trigger strategies;*
- *Slow control;*
- *Calibration;*
- *Overall synchronization;*
- *Gigabit Ethernet to maximize data throughput.*

Dedicated Processor I/O
Gigabit Ethernet
USB Host
USB Host/Device
SDHC
Serial TX/RX (console out)

FPGA I/O
16 SE fixed at 3.3V
144 SE/72 diff pairs with IO level selection
3 Banks with user supplied voltage
Configurable Peripherals: Gigabit Ethernet, RS232 x3, RS485 x2, CAN x2

Adapter SOM



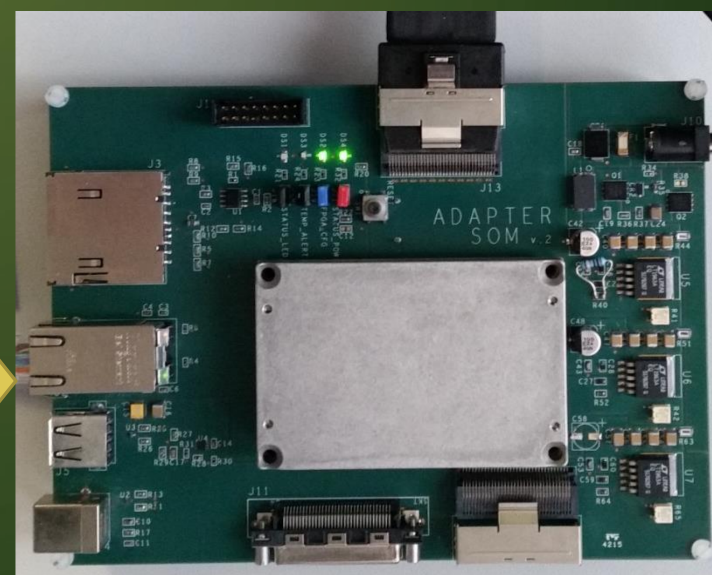
Full custom board hosting SOM and interfacing VMM2 Board through Molex twin-ax cable.

Measured Performance:

- ✓ *Sampling of 128 digital input SE @230MHz*
- ✓ *Sampling of 64 digital input SE @350MHz*

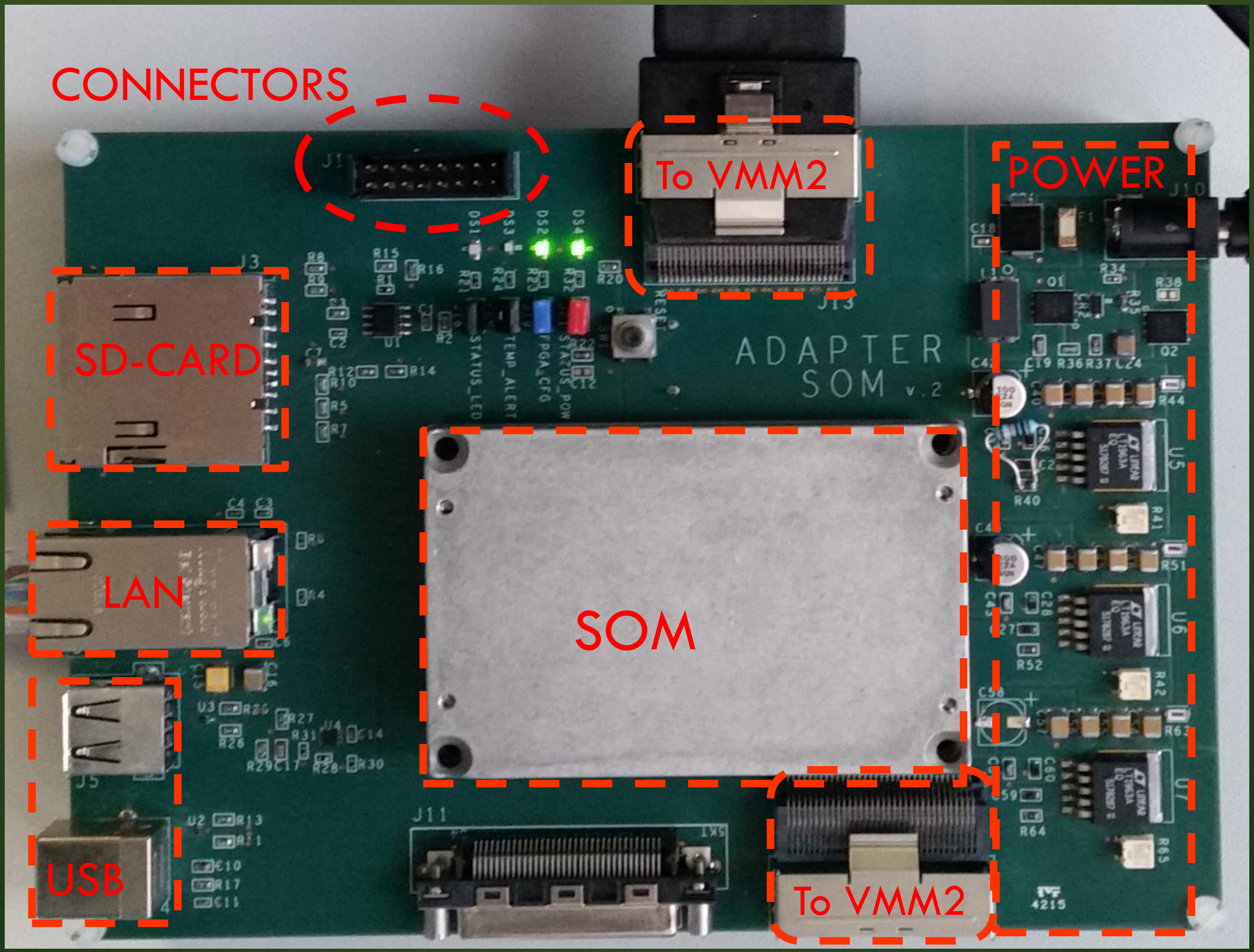
Applications:

- ✓ Real – Time characterization of a proton beam (position, size, fluence, energy);
- ✓ Imaging and radiography;
- ✓ Interfacing with:
  - ✓ DAC
  - ✓ ASICs (VMM2, MAROC)
  - ✓ SD – Cards, USB – HDD
  - ✓ Data transfer through Gigabit LAN



Design and Test SOM-VMM2 board by D. Bonanno and D. Bongiovanni.

Adapter SOM

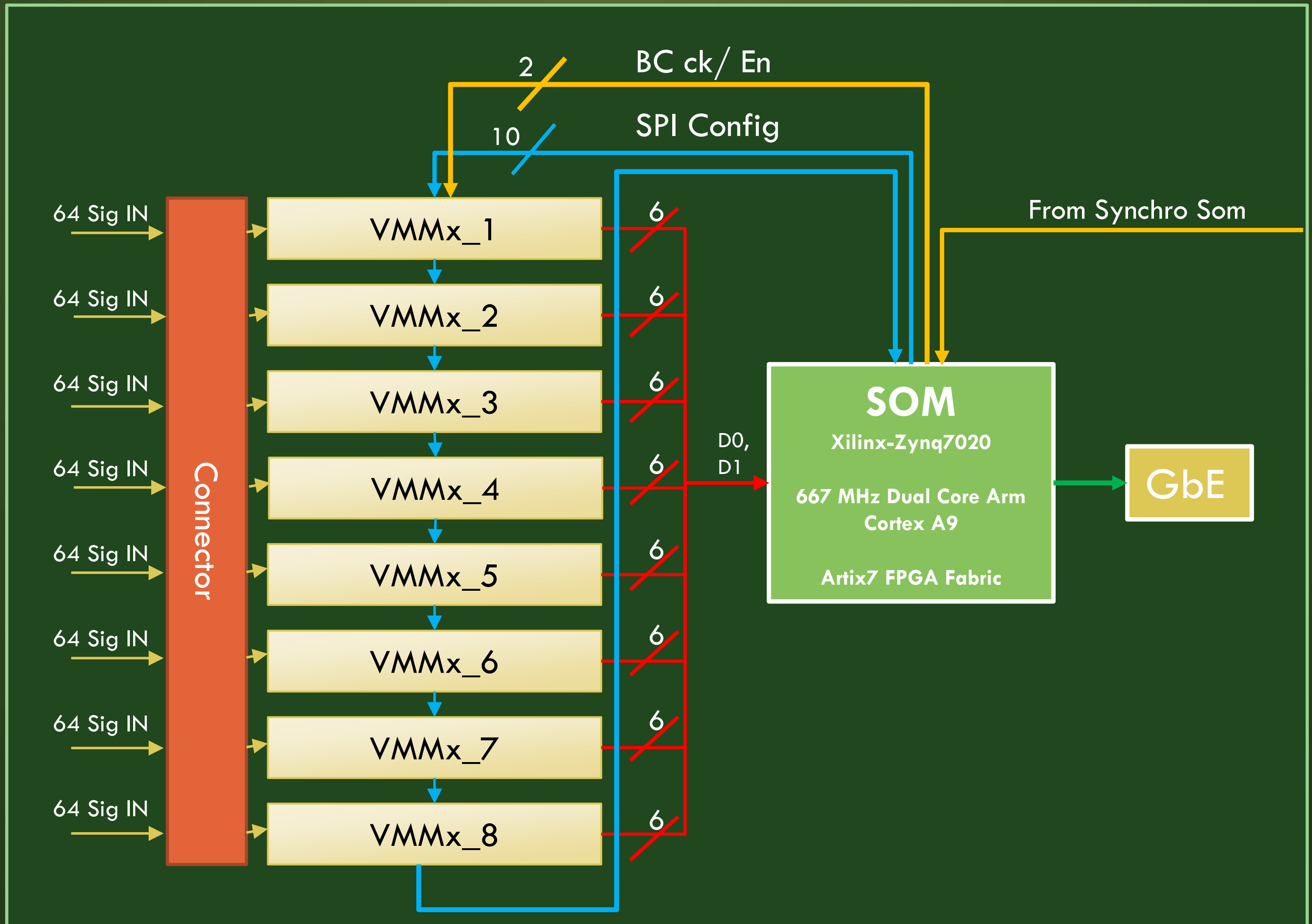


Test SOM-VMM2

D. Bonanno, D. Bongiovanni

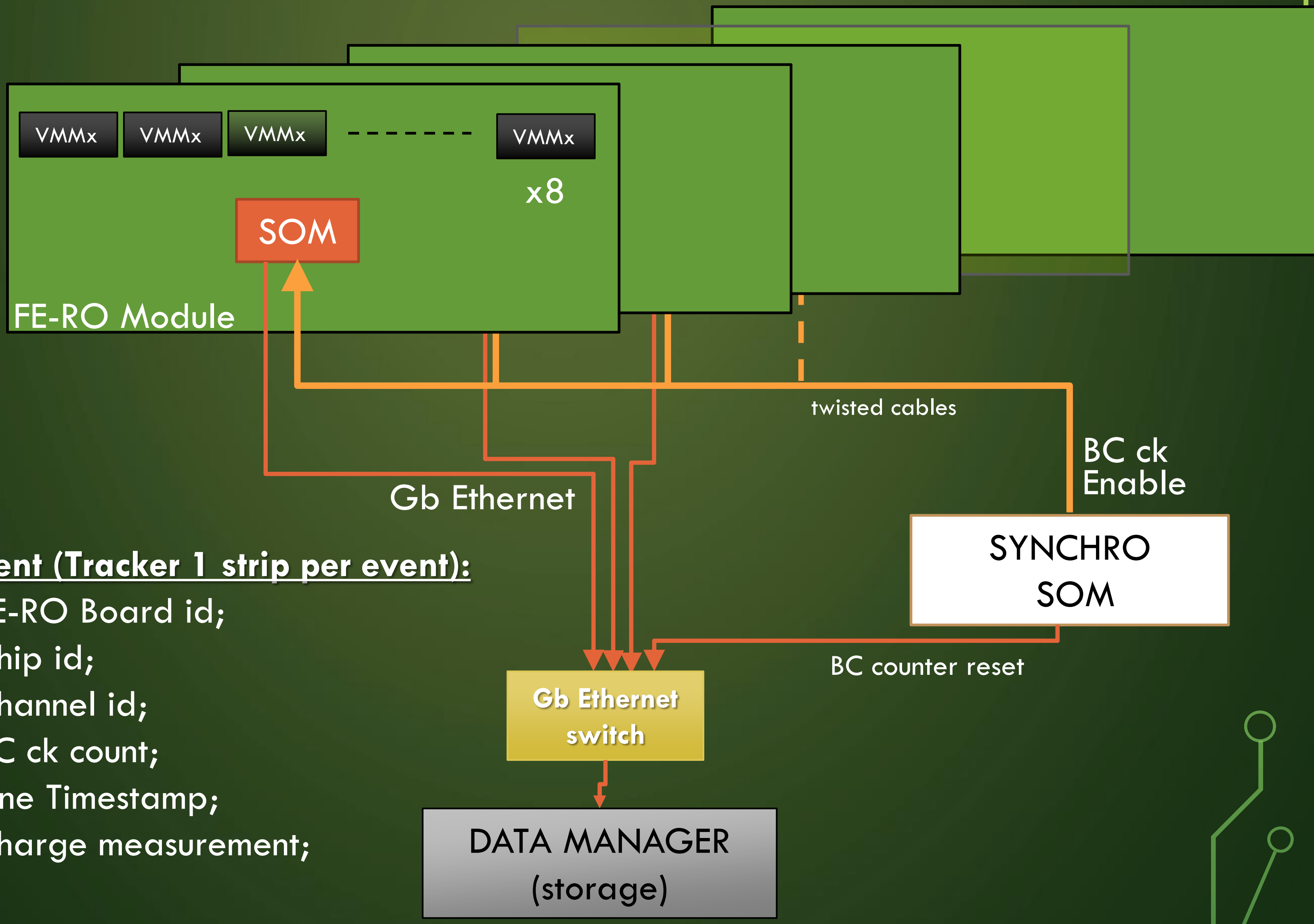
- *SOM-VMM2 board fully functional:*
  - *Configuration:*
    - *Calibration;*
  - *Synchronization:*
    - *Read-out;*
  - *LabView GUI:*
    - *Slow control;*
    - *DAQ*

FE-RO Module



- *8 VMMx chip read-out by 1 SOM is one* ***FE-RO Module;***
- ***Possible increase to 10 VMMx, to be confirmed!***

FE-RO ARCHITECTURE



1 event (Tracker 1 strip per event):

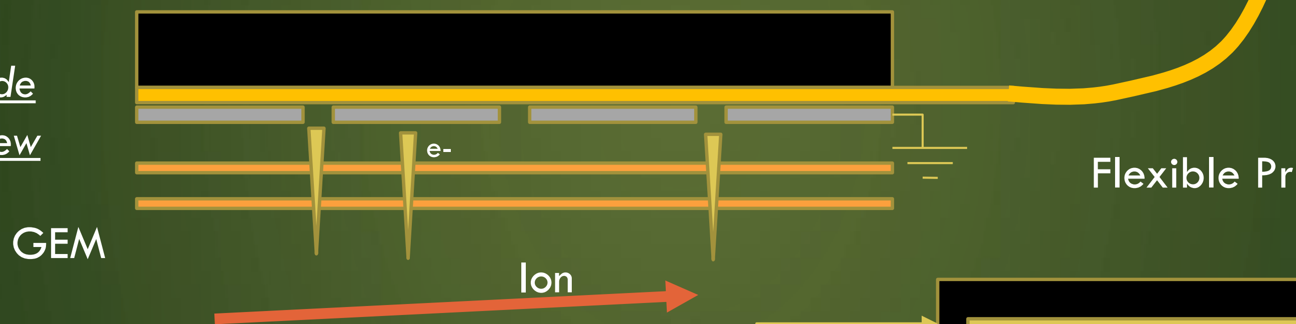
- FE-RO Board id;
- Chip id;
- Channel id;
- BC ck count;
- Fine Timestamp;
- Charge measurement;

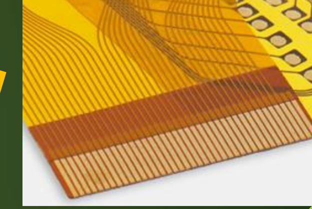
FE-RO ARCHITECTURE

- *FE-RO Module:*
  - *8 VMM2 chip -> 1 SOM*
  - *512 input -> 1 Gb/s Ethernet*
  - *If 0,5 mm pad -> 320 kHz average event rate per Module;*
  - *38 bit/event *number of strips involved = 38 bit/event (extra id chip and id Module);*
  - *Data Throughput = 12 Mb/s per Module;*
- *Timing strategy*
  - *Synchro SOM:*
    - *BC clock to all Modules = 10 MHz;*
    - *Enable all Modules;*
  - *Each Module (SOM):*
    - *counts BC clock edges up to 4096 = 409.6 μs;*
  - *Each VMMx chip measures time from peak to next BC edge @ 488 ps resolution.*

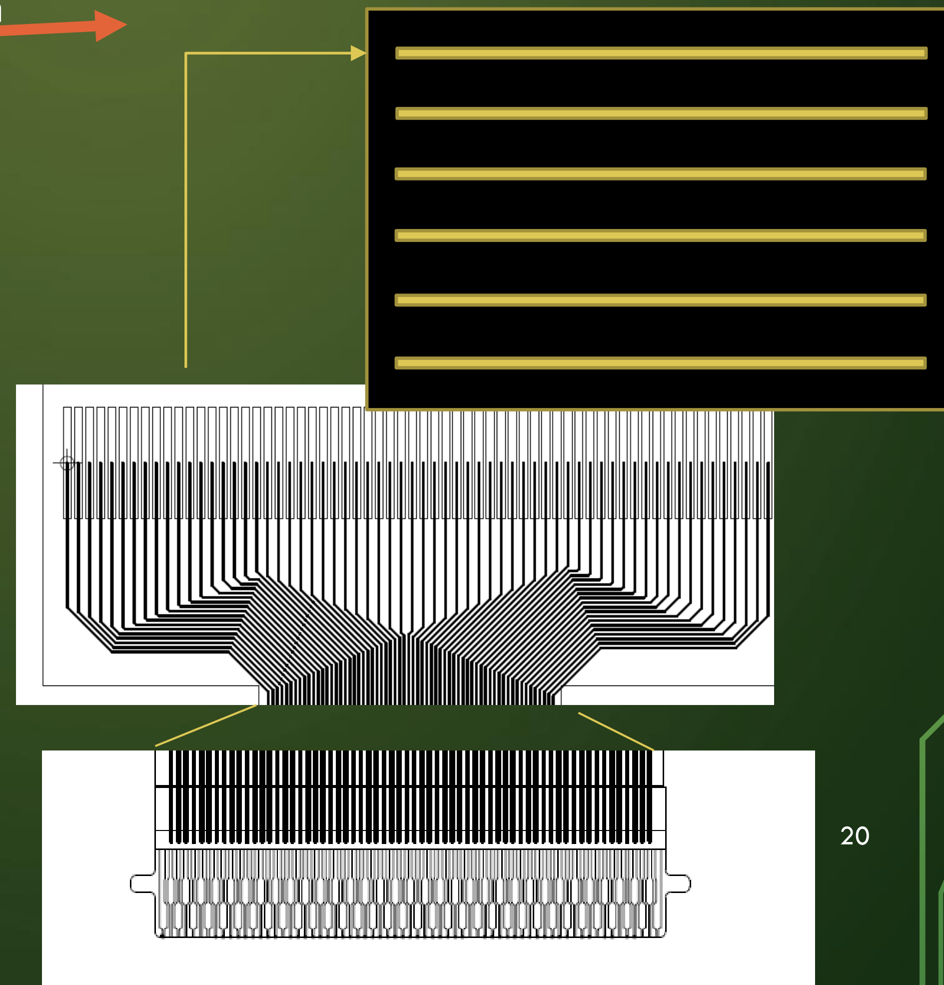
Study of the segmented read-out board

Side View



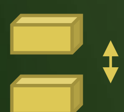


Flexible Printed Circuit

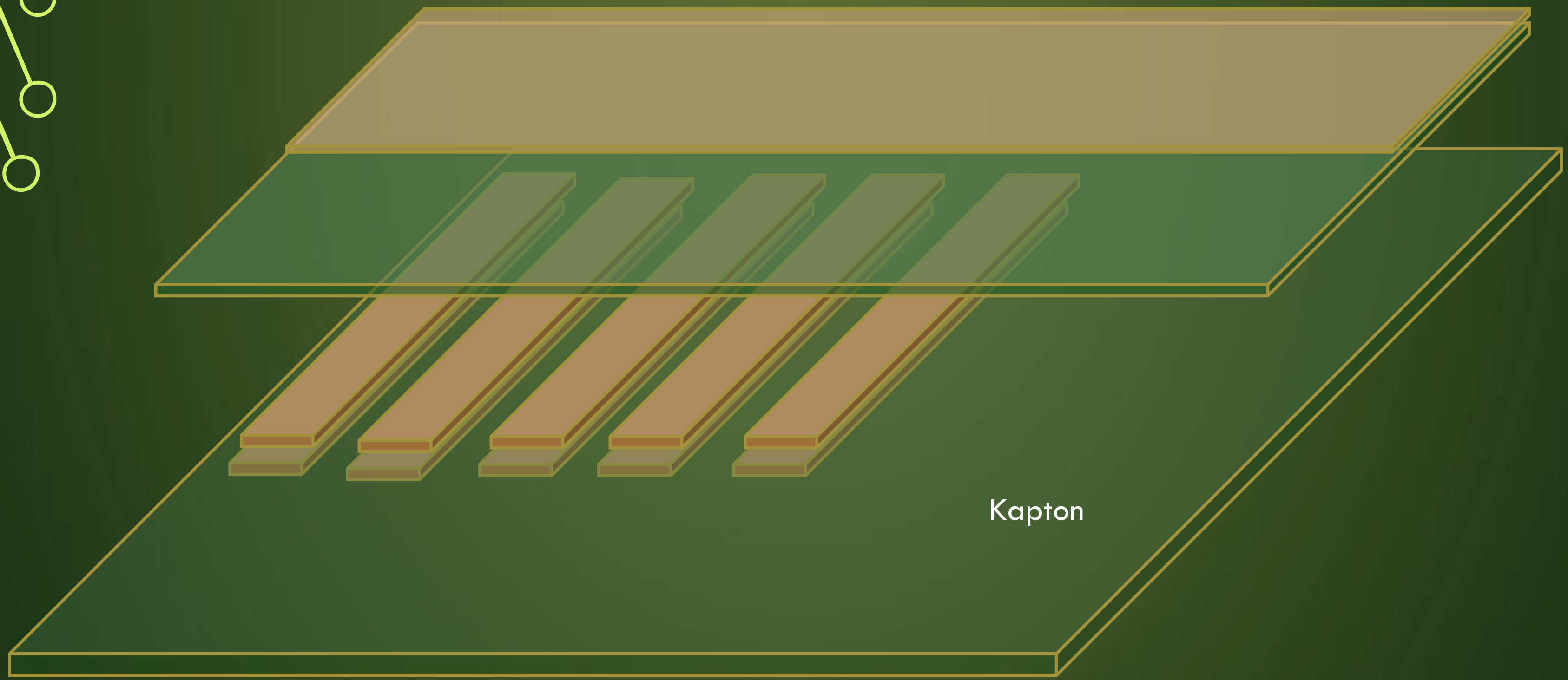


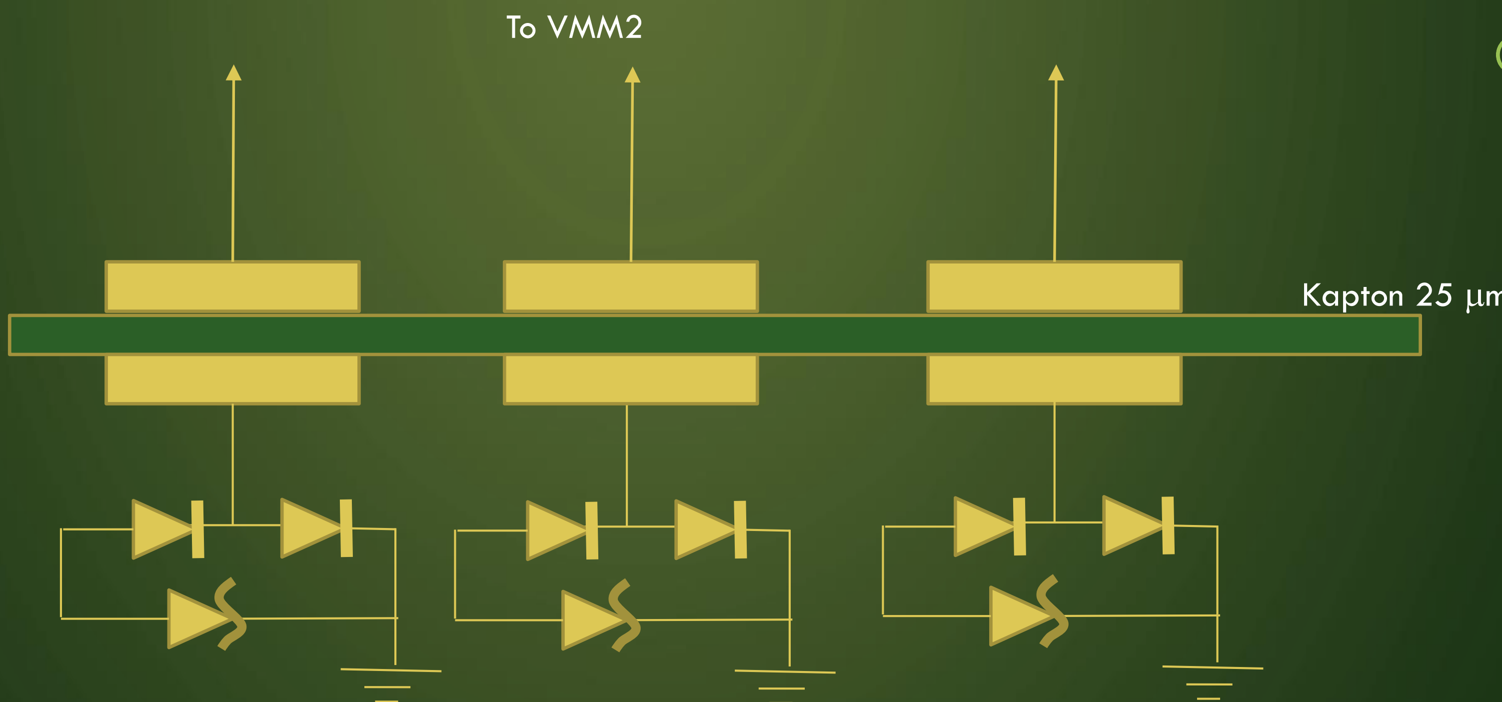
Top View

Read-out Pad



Exposed Pad


Kapton



$C=\varepsilon_o\ \varepsilon_r\ S/d = 8{,}854\ pF/m * 3{,}5 * (1{,}5E\text{-}6\ /\ 25E\text{-}6)\ m = 1{,}85\ pF$!!

CONCLUSIONS

- Design of a complete VMM2-SOM system, now under test;
- For the FE-RO Module final design we need:
  - the VMM3 details:
    - Definition of the overall architecture;
  - The FPD tracker final design:
    - Pitch, capacitance and interconnections;
    - (Vacuum sealing,…)

THANK YOU

CONTACTS
DOMENICO.LOPRESTI@CT.INFN.IT
SKYPE: DOMENICO.LO.PRESTI