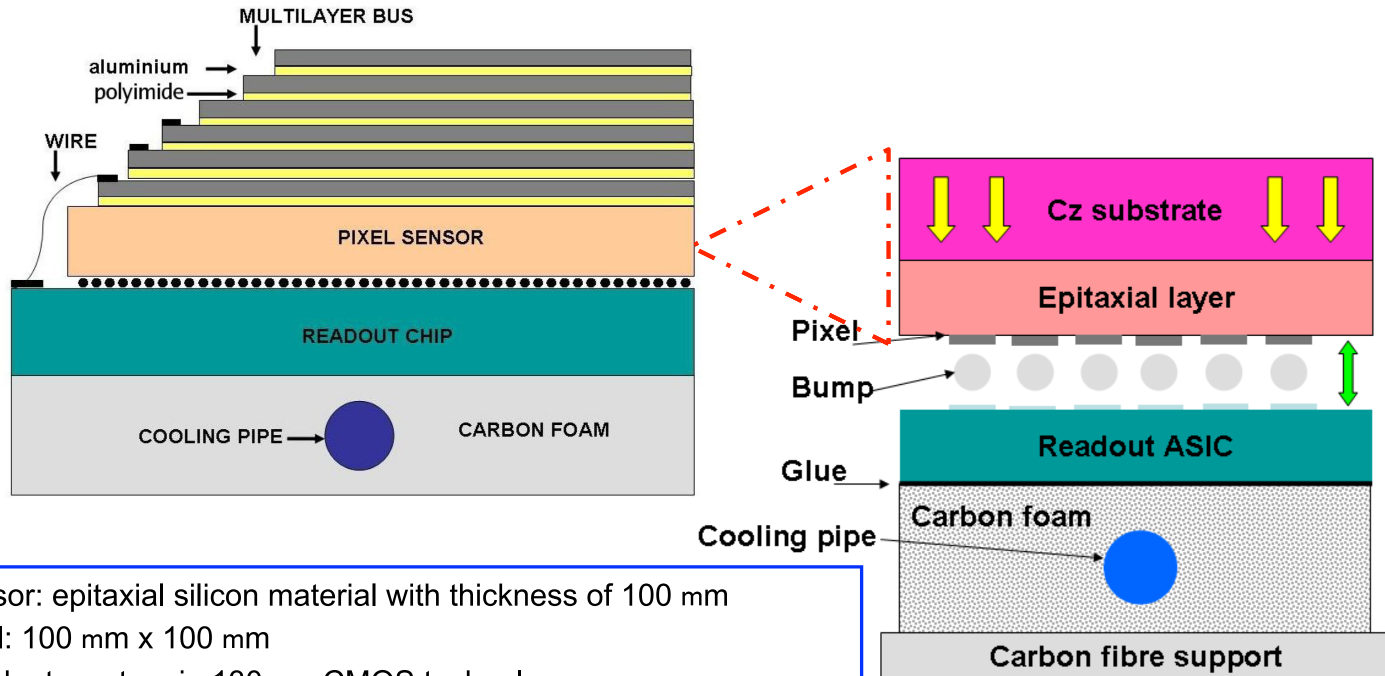
Use of epitaxial silicon material for hybrid pixels

- Introduction
- Material – blank wafer
- Patterned wafers
- Thinning process
- Guard rings
- Oxygen enrichment process
- Measurement results

Daniela Calvo
INFN - Torino

Hybrid pixel detector in PANDA



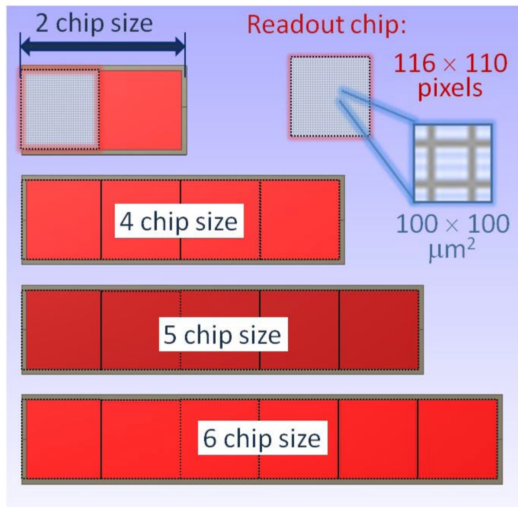
- Sensor: epitaxial silicon material with thickness of 100 mm
- Pixel: 100 mm x 100 mm
- Readout: custom in 130 nm CMOS technology
- Support structure: carbon fiber and/or carbon foam
- Cooling: water of a under pressure system
- Multilayer bus: aluminum tracks/ ground plane + polymide material

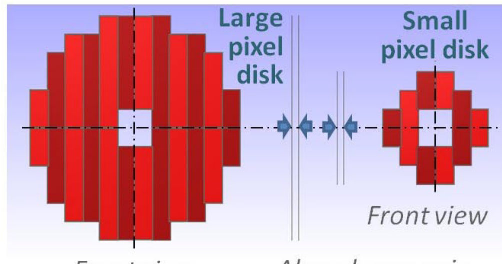
Radiation tolerance:

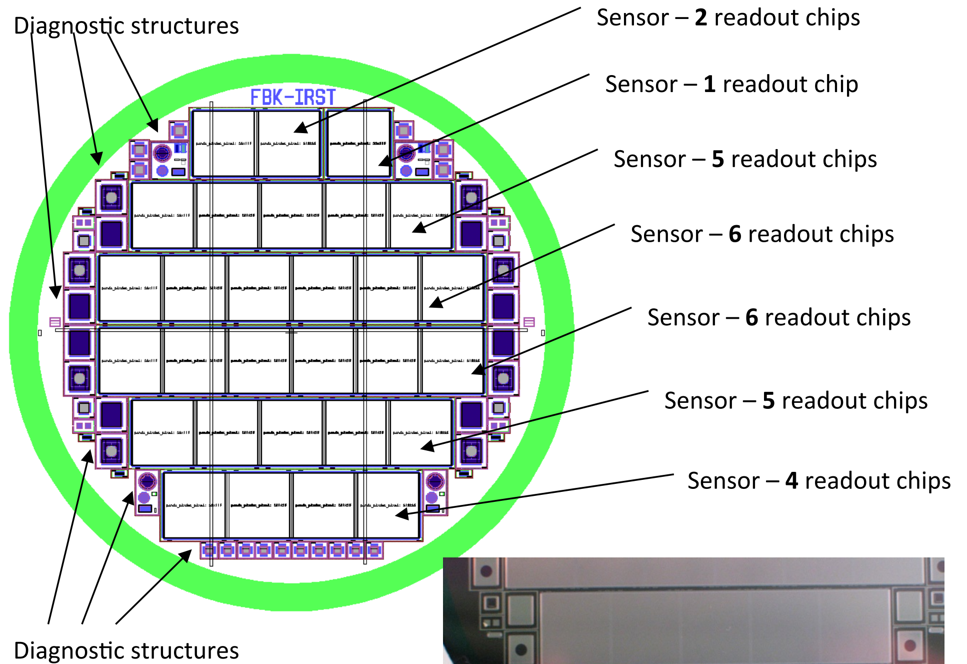
G. Kramberger et al., Superior radiation tolerance of thin epi silicon detectors, NIM A515:665-670,2003

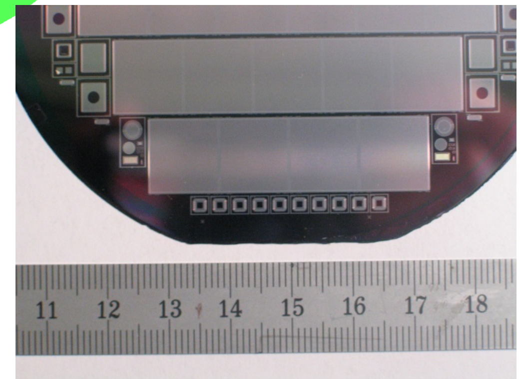
E. Fretwurst, Recent advancements in the development of radiation hard semiconductor detectors for S-LHC, RD50 Workshop, Helsinki, 2005

Hybrid pixel detector in PANDA









- Bump bonding technique to connect sensor and readout chips

Blank wafers

ITME (Warsaw, Poland)

- Limited wafer number, low cost
- Capability to make several epitaxial Si layer thickness (up to 150 mm), 4” wafer

Substrate

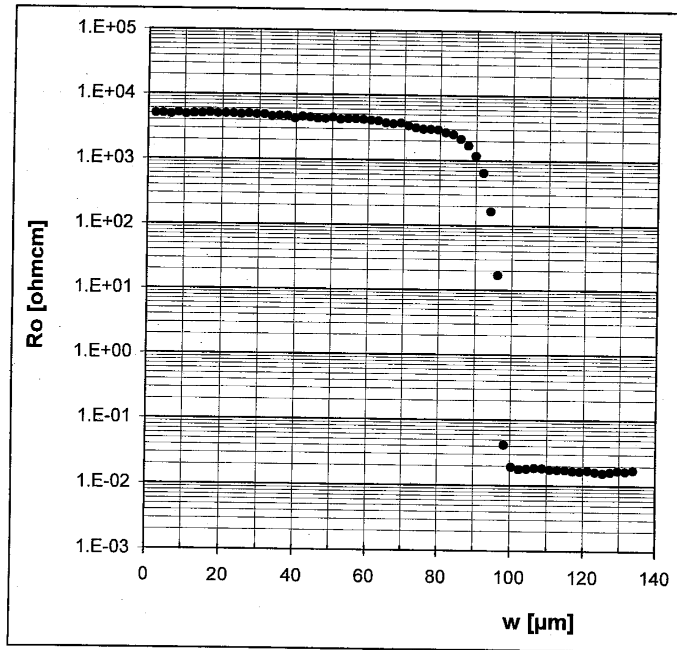
- Resistivity: 0.008 ÷ 0.02 W cm
- Thickness: 525 ± 20 mm
- Conductivity type/dopant: n^+ / Sb
- Orientation: <111> , <100>

Epitaxial layer

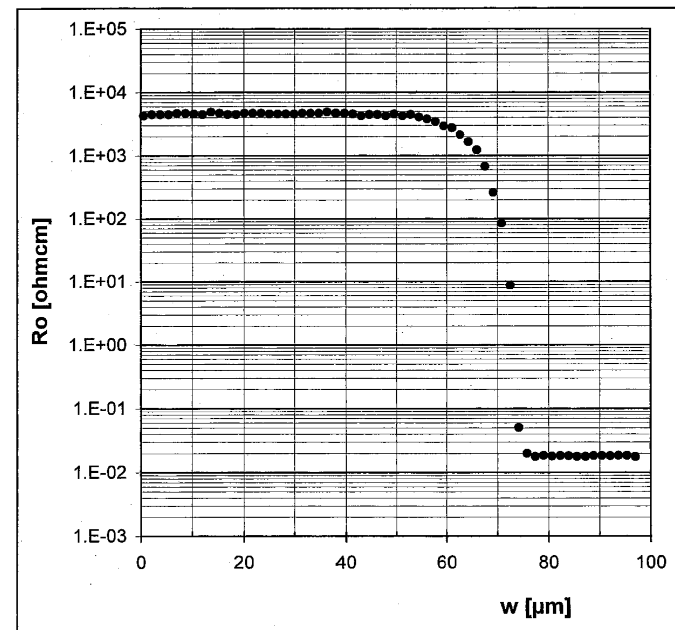
- Conductivity type/dopant: n / P
- Resistivity: 1000 ÷ 5000 W cm
- Radial resistivity variation (on the wafer): < ± 10 % (15%)
- Thickness (centre): 49.9 ± 0.5 mm, 73.5 ± 1.2 mm, 99.9 ± 0.6 mm, 150.5 ± 1.0 mm
- Radial thickness variation (on the wafer): < ± 4% (8%)

Measurements by ITME

- thickness by IR reflectance method,
- resistivity by spreading resistance method



AVERAGE (Ro) [Ohmcm] = 4.90E+03
RANGE W [µm] : 0 - 40

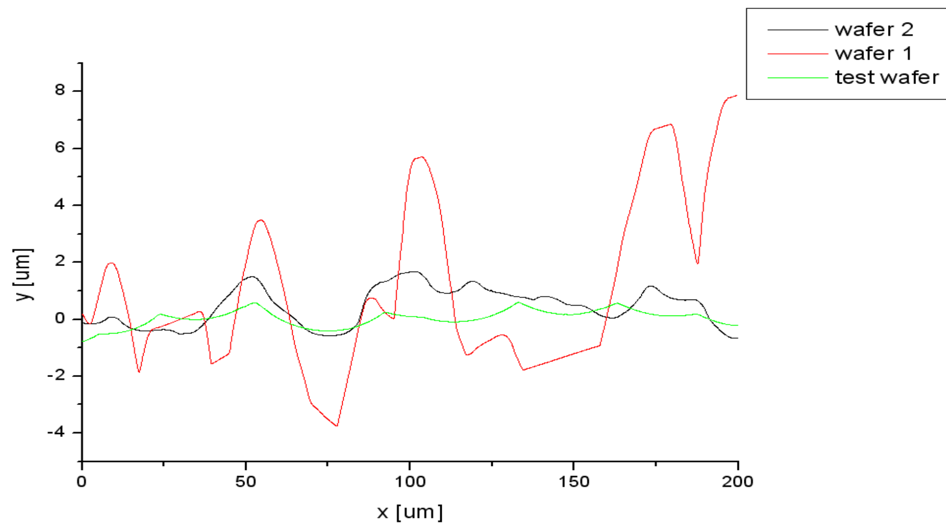


AVERAGE (Ro) [Ohmcm] = 4.57E+03
RANGE W [µm] : 0 - 30

Roughness on the wafer backside

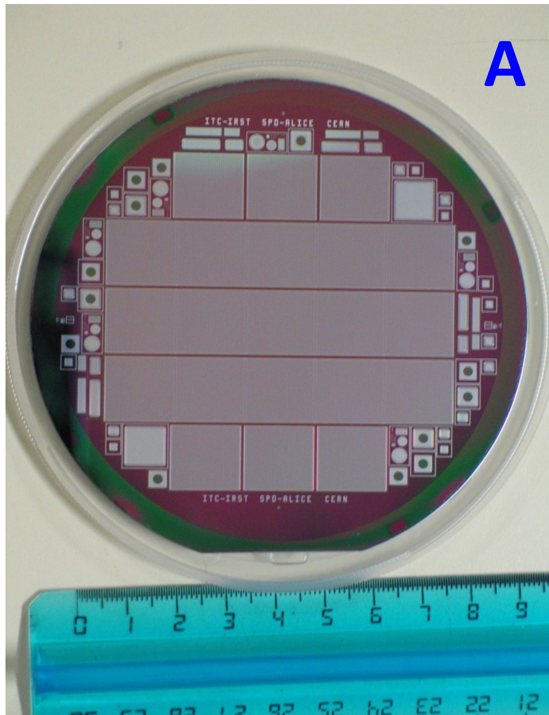
Substrate backside and epi-layers were optically inspected and they meet the SEMI Standars

Measurement perfomed at FBK
Wafer 1 shows a roughness up to 12 mm (min-max)



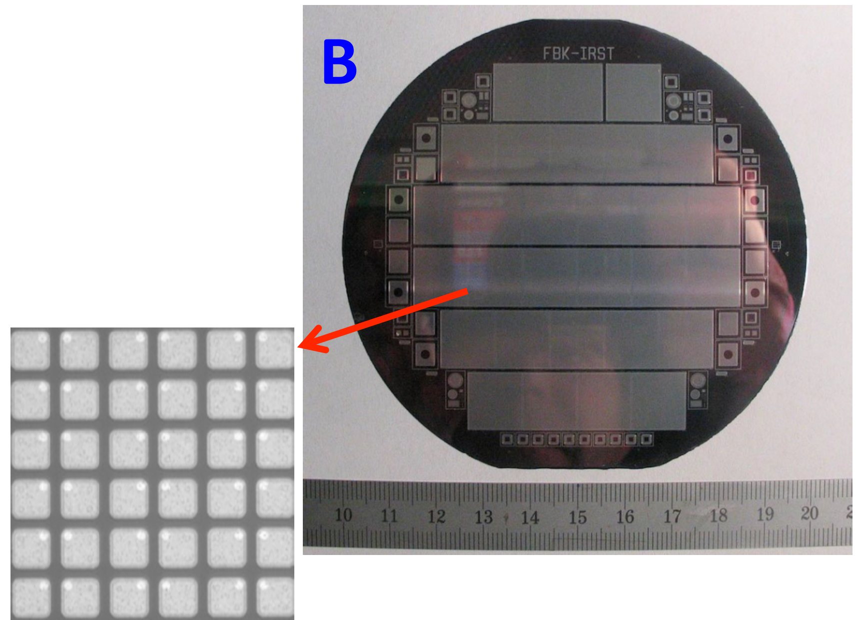
Patterned wafers

Masks of Alice sensor (from INFN-Ferrara)
Pixel: 50 mm x 425 mm



Pixel sensors of PANDA obtained using 5 masks (**Pixel: 100 mm x 100 mm):**

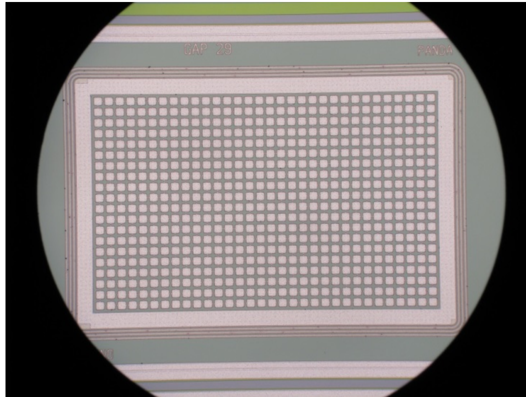
p+
n+
contact
metal
passivation

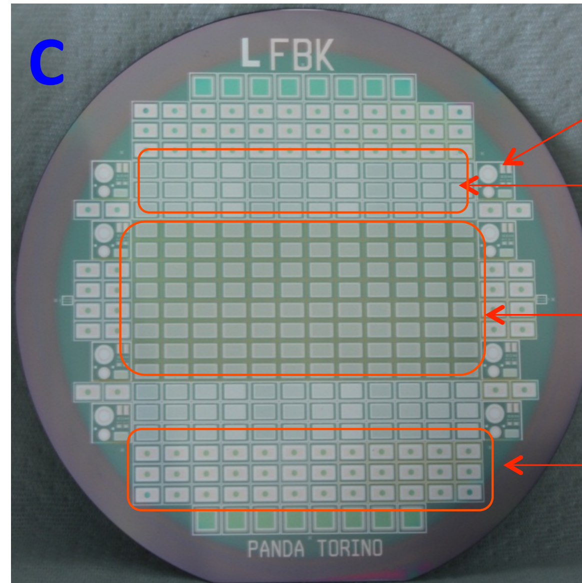


Patterned wafers

Pixel sensors of prototypes (640 cells: 32 x 20) obtained using 5 masks (**Pixel: 100 mm x 100 mm**):

p+
n+
contact
metal
passivation





Test structures

Pixel-like Test Structures

Pixel Sensors

MultiGuard Diodes

Thinning process

- Most of the CZ substrate is removed
- blank wafers, A, B, C
- Several companies: VTT (A and B), WAFER Solution (B), IZM (C)

First 6 patterned wafers (type A) (<111>) were broken during the thinning process (CMP)

Explanations

- The epi-layer is elastically accommodated to the substrate, a drastically thinning of the substrate causes cracking of the processed epi-structure due to existing strains
- In Si crystal the doping of Sb ions causes the increase of the lattice parameters and leads to increase of lattice constant difference between high resistivity Si layer and substrate: the epi-layer is in stress condition partly due to the lattice mismatch
- Alternative solutions:
  - to deposit epi-layers on substrate of <100> orientation
  - to perform the thinning in two steps: mechanical before and next chemical polishing

- The processes to obtain the wafers A were optimized for a target thickness of 200 μm (as in ALICE)
- Optimization of the passivation process for lower final thickness

- Systematic studies with blank wafers and patterned wafers with several final CZ layer thicknesses
- Measurement of the wafer profiles (x and y directions) before and after the thinning process

Thinning process – blank wafers @ VTT

<100>	blank wafer				
Wafer n./ resistivity [ohm cm]	Epi thickness [mm]	Target thickness [mm]	Max. (x/y [mm]) curvature before thinning	Max. (x/y [mm]) curvature after thinning	Wafer brocken
3/ 3139	100	130	25 / 19	138 / 134	2*
3/ 3139	100	120	26 / 17	72 / 73	1**
3/ 3139	100	110	26 / 13	76 / 51	2**

- First two wafer destroyed at CMP. The other wafers were thinned using etching technique,
- ** Wafer brocken later, ex. during tape remove.

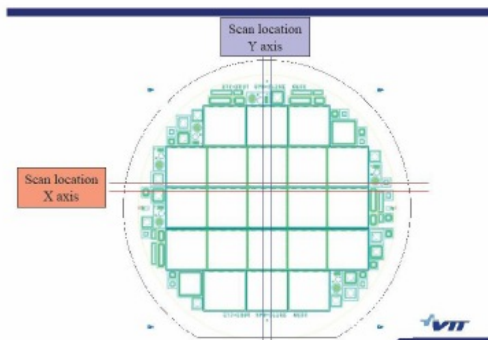
<111>	blank wafer				
Wafer n./ resistivity [ohm cm]	Epi thickness [mm]	Target thickness [10 mm]	Max. (x/y [mm]) curvature before thinning	Max. (x/y [mm]) curvature after thinning	Wafer brocken
2/ 4060	50	100	40 / 100	148 /145	0
5/ 3876	75	120	30 / 15	132 / 149	2
2/ 4570	100	150	25 / 4	114 / 116	0

Thinning process – A wafers @ VTT

<111>	A				
Wafer n./ resistivity [ohm cm]	Epi thickness [mm]	Target thickness [10 mm]	Max. (x/y [mm]) curvature before processes	Max. (x/y [mm]) curvature after processes	Wafer brocken
4/ 4060	50	200	-23 / 58	-22 / 59	0
4/ 4570	75	200	-12 / -33	27 / 57	1
4/ 4900	100	200	-18 / -40	-35 / -33	1

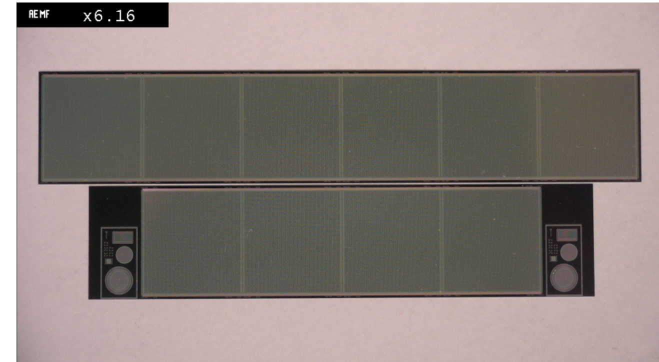
- Processes: bumping, thinning (backgrinding + CMP or etching), 1000 nm Al backside sputtering
- Breaking line observed in correspondence of wafer numbers engraved on the surface (?)

Scanning locations in X and Y direction



Thinning process – B wafers @Wafer Solution

<111>	B		
Wafer n./ resistivity [ohm cm]	Epi thickness [mm]	Target thickness [10 mm]	Wafer brocken
2/ 3100	50	100	0
4/ 448, 3200	75	100	0
2/ 3610	100	120	0



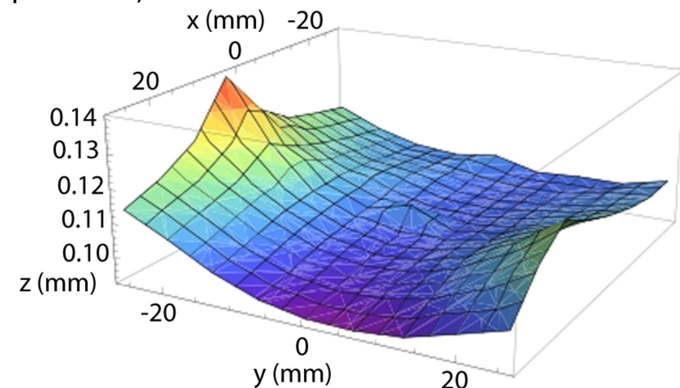
- Processes: backside grinding, polishing, de-stressing

Planarity evaluation– B wafers @INFN-Torino

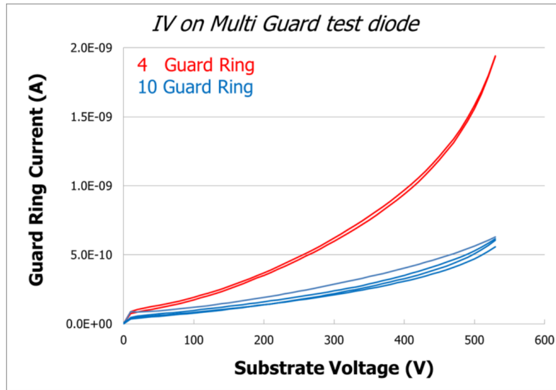
Measurement perfomed with a Mitutoyo machine

1. equipped of a precision CCD camera (magnifier 1:10)
2. and a stylus probe (3mm over 1 m precision)

1. Total non planarity of 40% by a grid of 8x9 positions and preferential cup shape observed, due to the elasticity of the wafer and light reflection on the wafer surface.
2. Elasticity of the wafer by observing the movement of the wafer under the probe pressure, without any breakage. The same previous measurement grid was used.



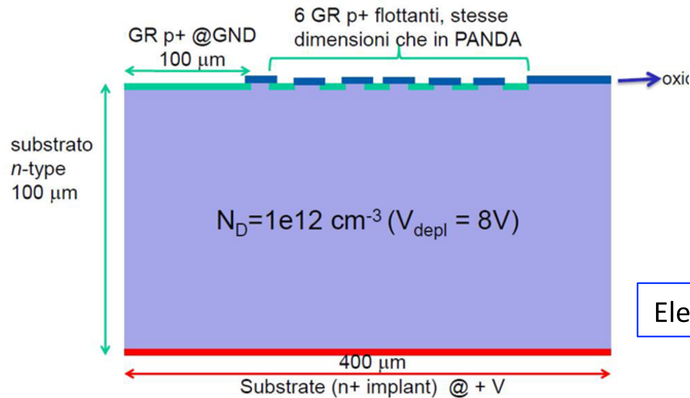
Guard rings

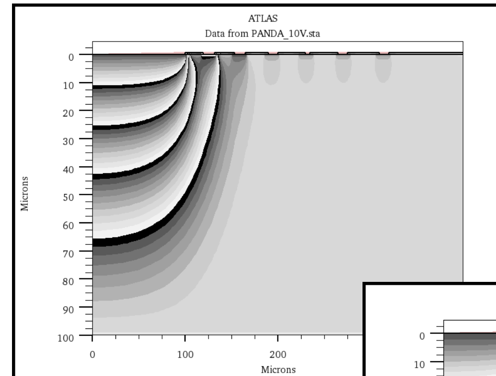


@ FBK

- Multi Guard Ring diodes of thinned wafers (epi layer of 50 mm)
- High Breakdown Voltage equal before and after thinning)

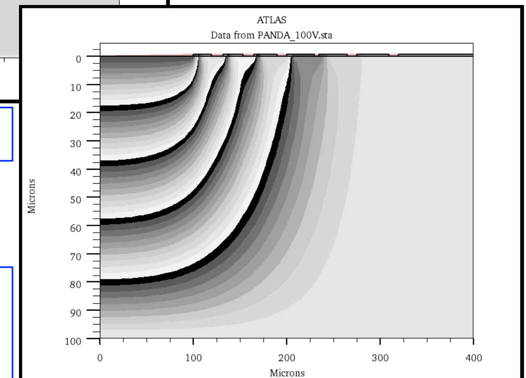
Simulations @ FBK by G. Giacomini





n-type layer @10 V
(>~ V_{dep})
GR @ GND

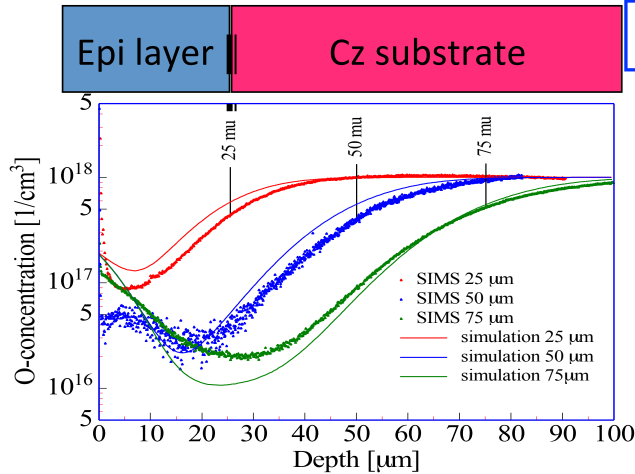
Electrostatic potential map

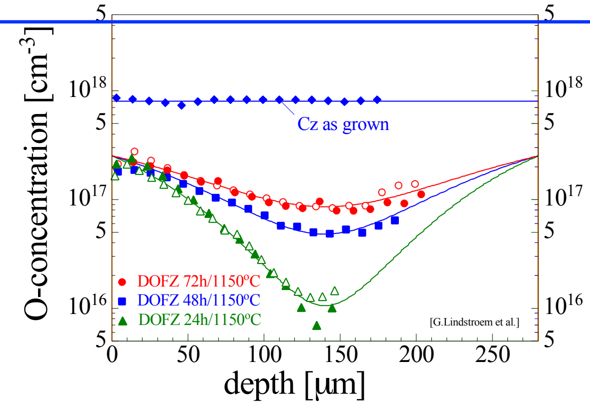


n-type layer @100 V
(>> V_{dep})
GR @ GND

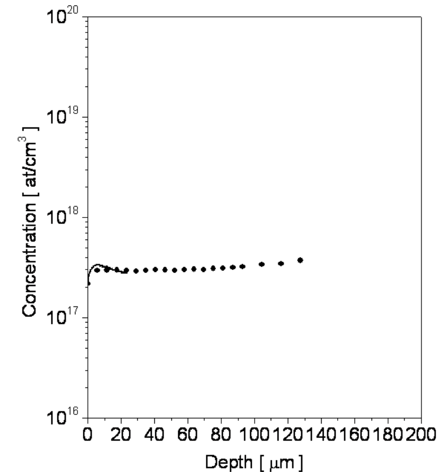
Oxygen enrichment process

G. Lindstrom et al., Nucl. Instr. Meth. A568-1:1-474,2006





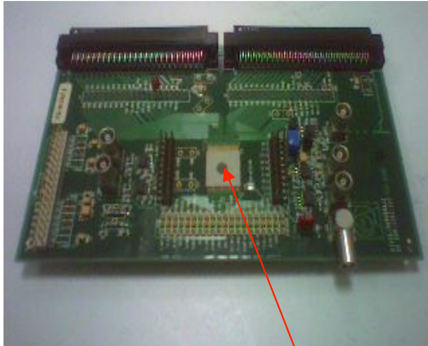
Oxygen enrichment process applied to some epitaxial Si wafers @ FBK. 12 h in oxygen atmosphere and 53 h in a nitrogen atmosphere at 1150 °C



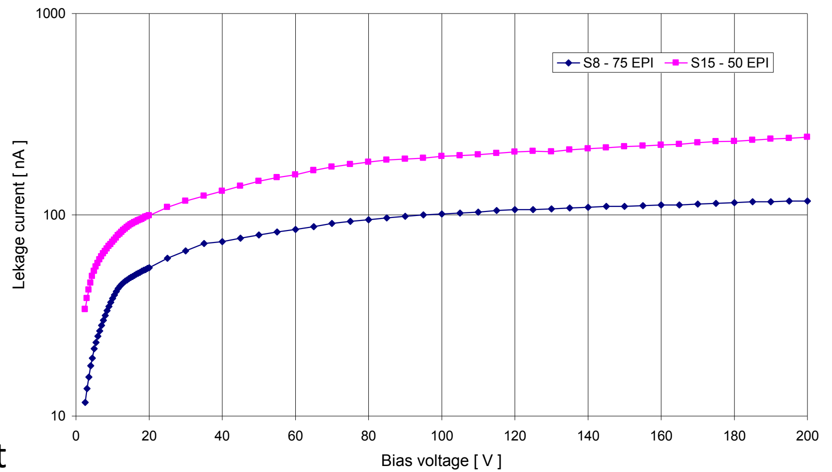
The scatter graph of the oxygen concentration measured on beveled surface.

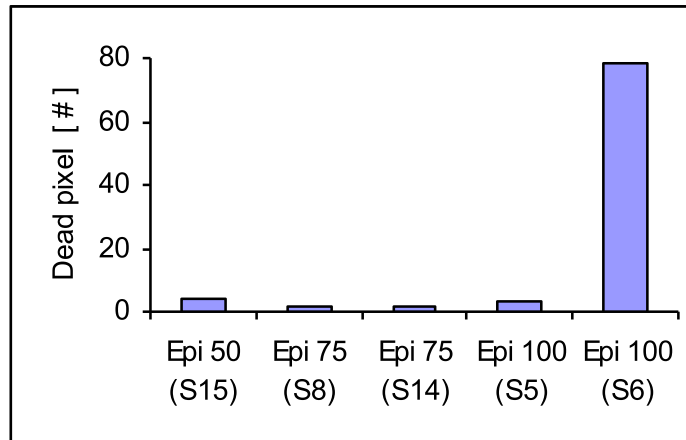
Single chip assemblies @VTT – A sensor

Sensor A + Alice readout (8192 pixels)

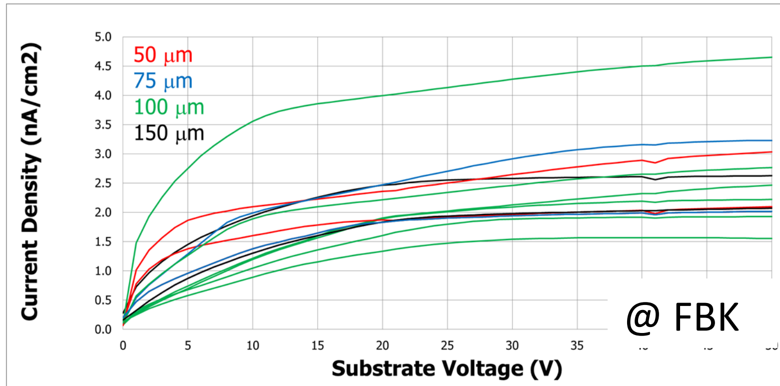


Hole on the backside for laser test

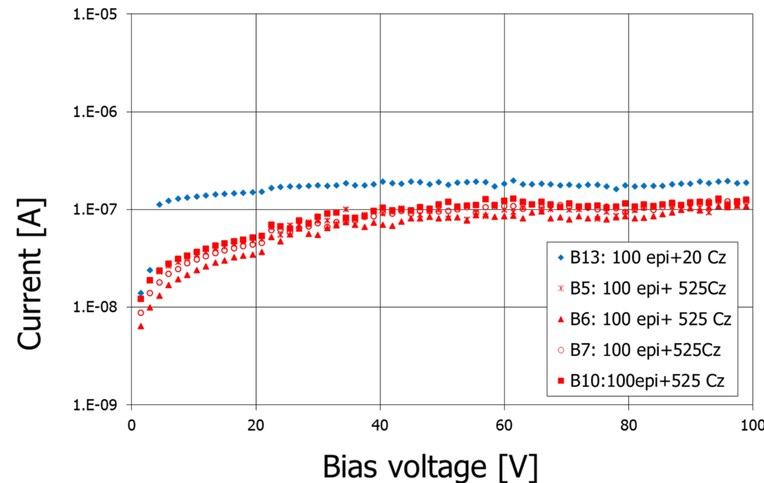




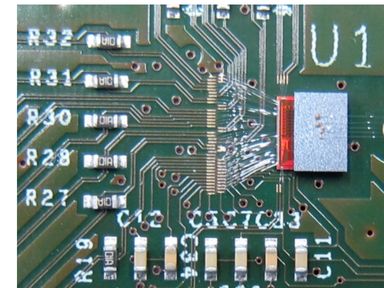
C sensors



- Tau (generation time): 3-10 ms
- Surface generation velocity: 2-4 cm/s
- Oxide charge density: 0.6-3 10^{11} cm^{-2}
- I-V of 4 mm^2 diodes from 50, 75, 100 and 150 mm epitaxial silicon wafers

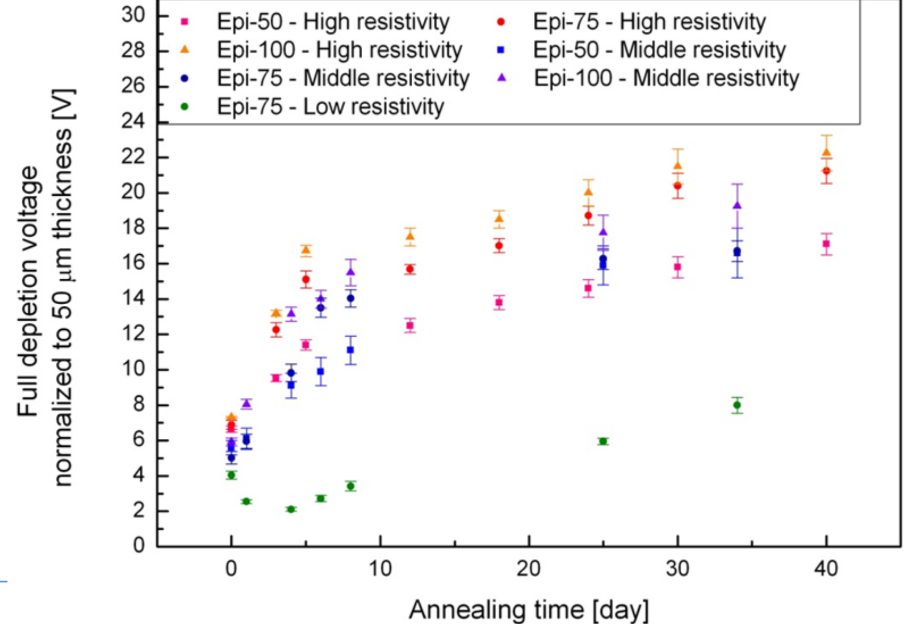


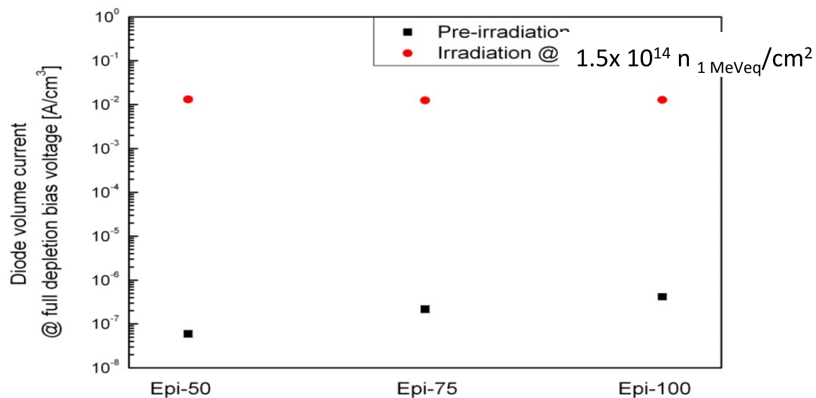
- C sensor + ToPix3 readout
- IV measurement of bump bonded sensors as obtained with (blue) and without (red) thinning process
- The difference of the two measured currents is in the range of the typical spread for test structures



Radiation damage studies

Neutron irradiation: 1.5 x 10^{14} n $_{1\ MeVeq}$/cm^2
Annealing T: 60°C



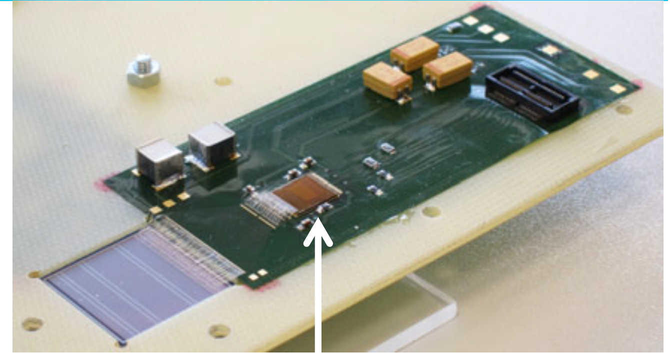


Epi-50, HR: 49 mm (4060 W·cm, n/P)
Epi-75, HR: 74 mm (4570 W·cm, n/P)
Epi-100, HR: 98 mm (4900 W·cm, n/P)
Epi-50, MR: 50 mm (3100 W·cm, n/P)
Epi-75, MR: 75 mm (3200 W·cm, n/P)
Epi-100, MR: 100 mm (3610 W·cm, n/P)
Epi-75, LR: 75 mm (460 W·cm, n/P)
+ Cz substrate (0.01-0.02 W·cm, n+/Sb)

Silicon detectors assembly in Torino

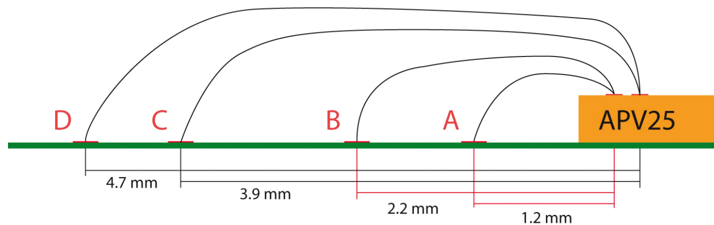
- Examples of wire bonding activities
- Examples of glue studies
- Tools and equipment
- Examples of Si device assembly with gluing and alignment phases

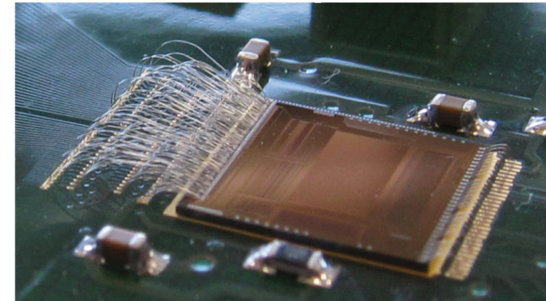
Wire bonding activities for PANDA

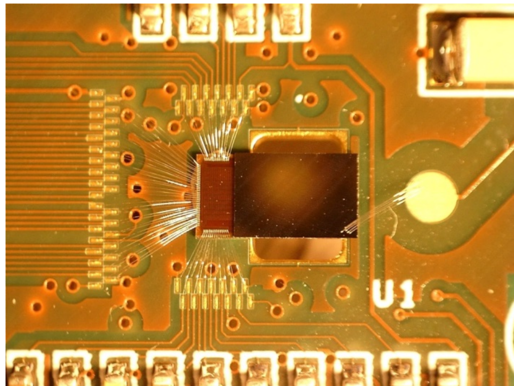


Wire bonding between a double sided strip sensor and the chip (APV25) carrier

- On the chip: two staggered rows, with 64 pads each, 88 mm pitch
- Pad size (chip): 136 mm x 58 mm,
- Wires made of Al + Si1%, 17 mm diameter





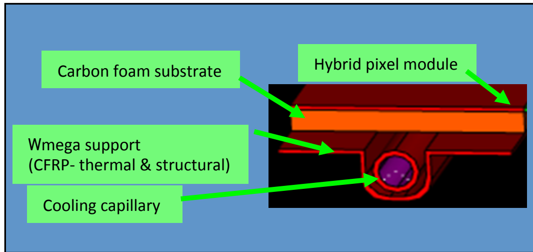


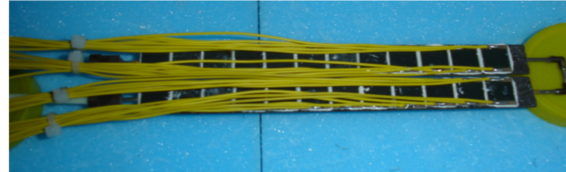
Single-chip assembly of hybrid pixel: C sensor and ToPiX4, a reduced scale prototype of the final pixel readout, connected via bump bonding

Wire bonding between the assembly and the testing PCB

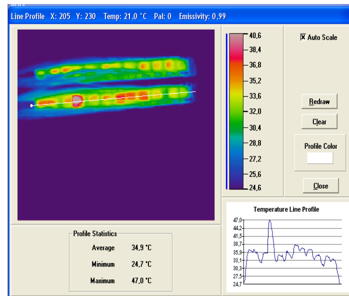
- Pad pitch on the chip: 75 mm
- Wires made of Al + Si1%, 17 mm diameter

Glue studies for PANDA

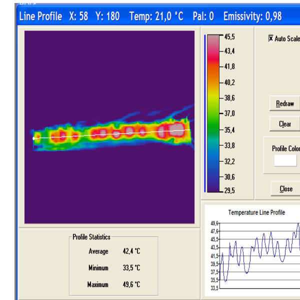




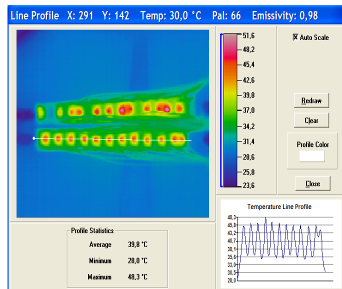
PROTOTYPE:
2 glue layers/stave
1) Between tube, omega and foam
2) Between chip and carbon foam



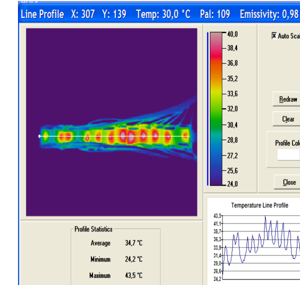
21W (1,75 W each chip, 1W/cm^2)
Flow rate: 0,3 lit/min
Inlet cooling temperature: 18°C
1ST prototype: T max around 39°C
-H70 glue between tube, omega and foam
-ARTIC ALUMINA glue (rapid) between chips and foam



21W (1,75 W each chip, 1W/cm^2)
Flow rate: 0,3 lit/min
Inlet cooling temperature: 18°C
6TH prototype: T max around 48°C
-H70 glue between tube, omega and foam
-H70 glue between chips and foam



21W (1,75 W each chip, 1W/cm^2)
Flow rate: 0,3 lit/min
Inlet cooling temperature: 18°C
2ND prototype: T max around 46°C
-MASTER BOND glue between tube, omega and foam
-MASTER BOND glue between chips and foam

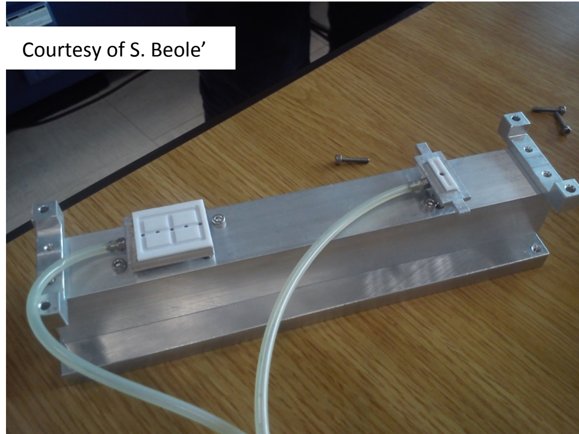


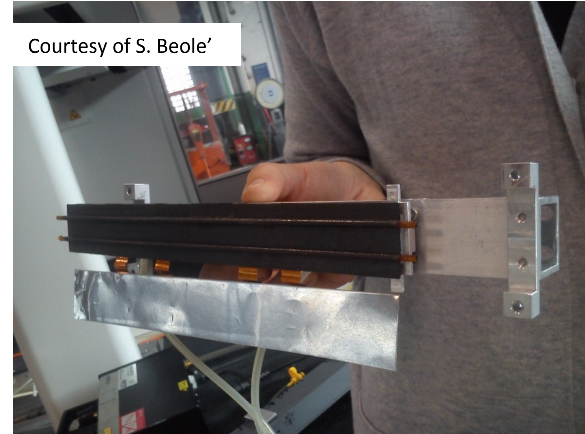
21W (1,75 W each chip, 1W/cm^2)
Flow rate: 0,3 lit/min
Inlet cooling temperature: 18°C
7TH prototype: T around 41°C
-Duralco 128 glue between tube, omega and foam
-Duralco 128 glue between chips and foam

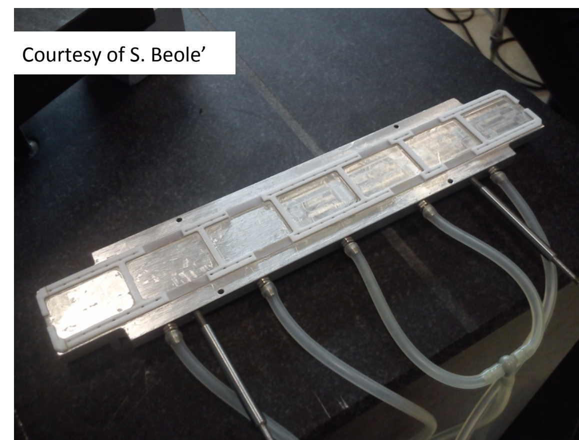
CONCLUSION:
- Best results with Arctic Alumina glue, BUT with rapid polymerization
- Acceptable results with Duralco 128 glue (ceramic glue, polymerization in 24h at AT)

Assembly jigs for Si devices assembly

- specific jig made of aluminum (stiffness) and teflon
- It uses the suction effect when handling detectors
- The hands cannot manipulate the silicon sensors due their fragility


Courtesy of S. Beole'

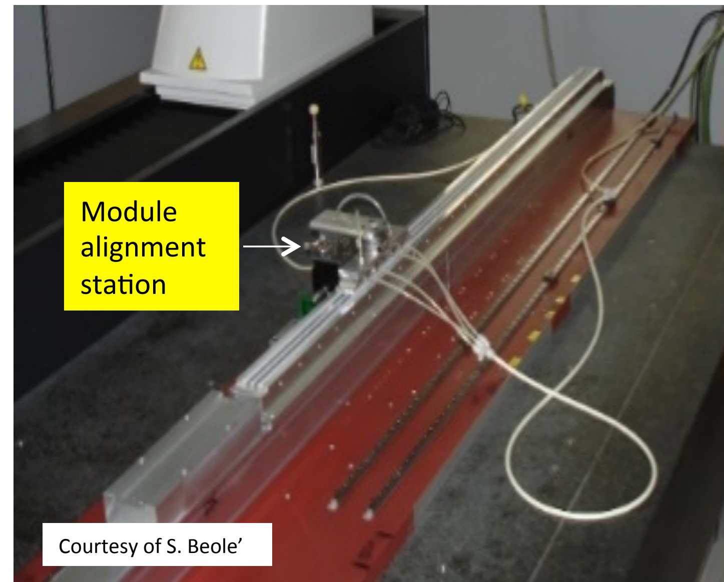

Courtesy of S. Beole'


Courtesy of S. Beole'

Courtesy of S. Beole'

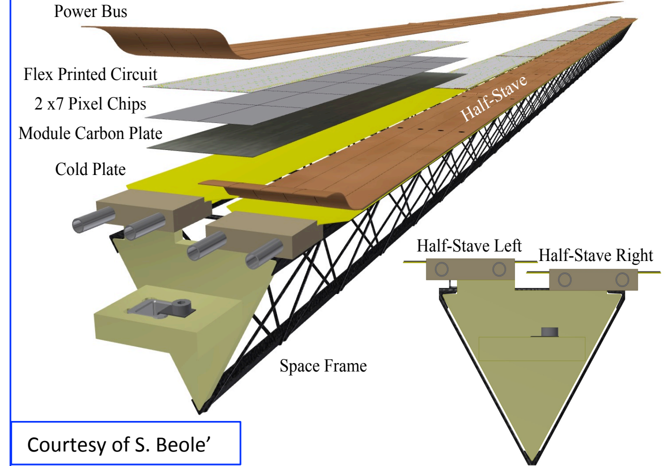
Equipment

- Coordinate measuring machine (in Torino, Mitutoyo Crysta Apex S 9206) equipped with touch probe and video camera
- Jig components

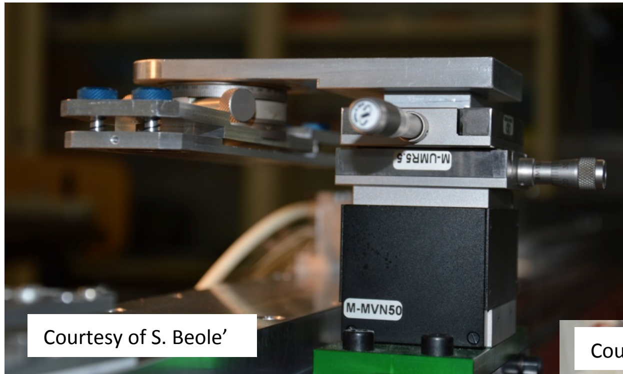


Equipment - examples

Stave for the new ITS of the ALICE experiment

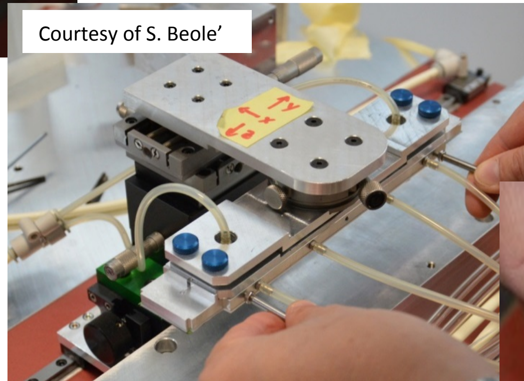


Courtesy of S. Beole'



Courtesy of S. Beole'

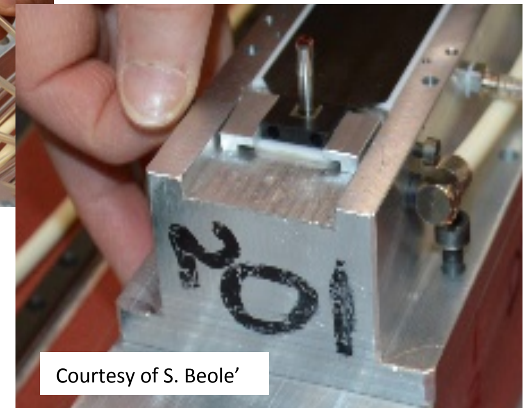
Module alignment station



Courtesy of S. Beole'

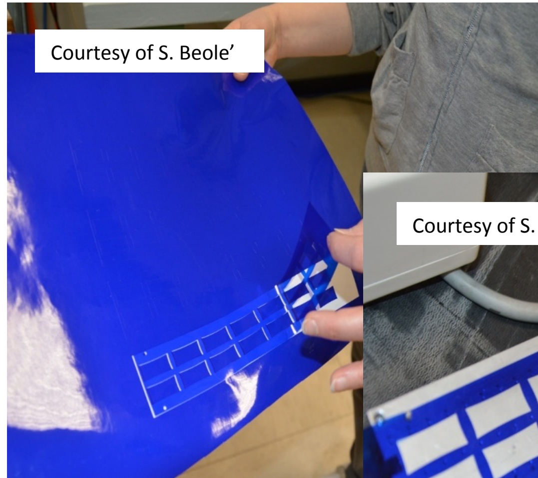
System to hang a Si module

Precision in the positioning of all the elements is mandatory, ex. dowels, reference holes, lock connectors

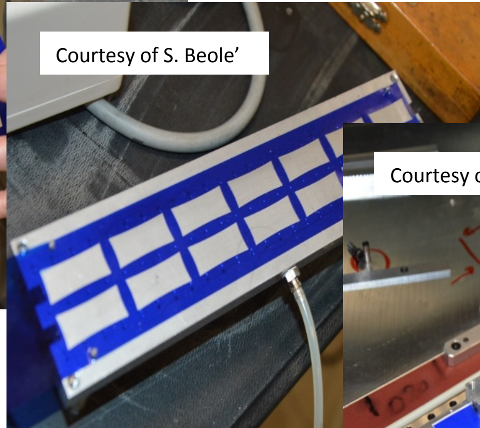


Courtesy of S. Beole'

Gluing process example

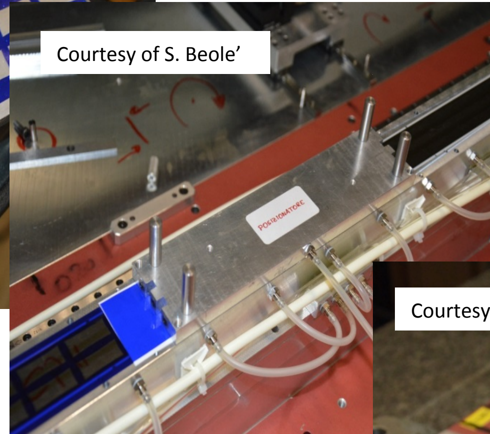


Adhesive masks

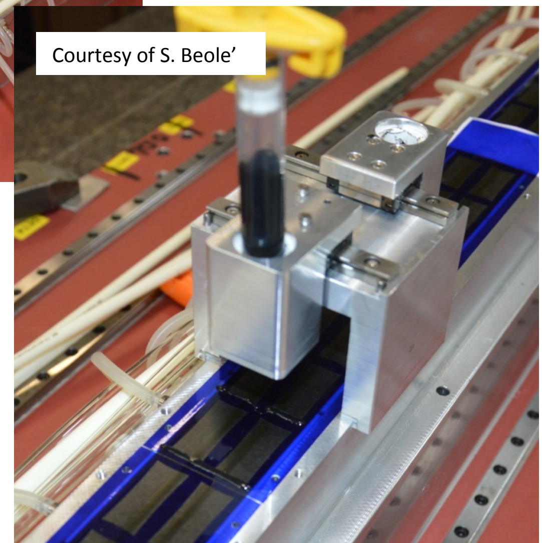


Mask kept by vacuum

Masks in position

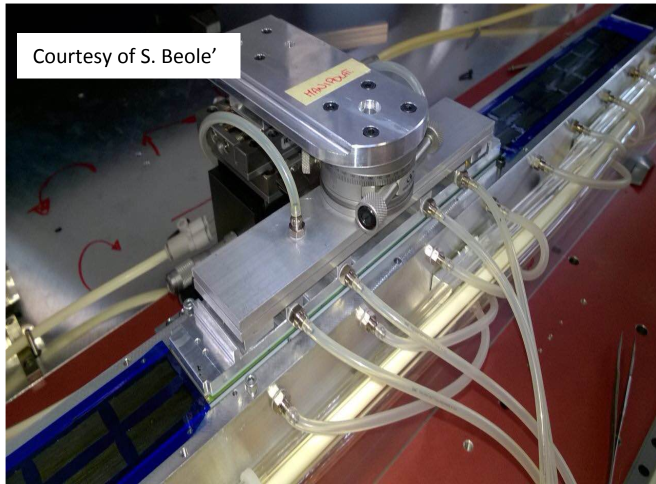


Glue deposition

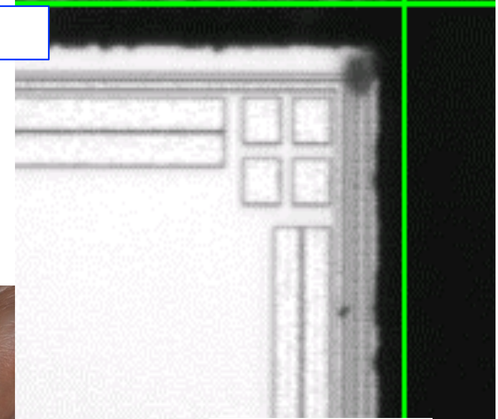


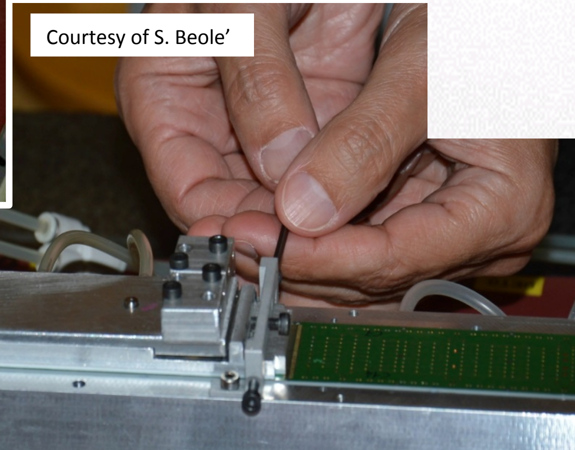
Thanks to S. Coli (INFN-Torino), the designer of all the tools and jigs for the ALICE ITS stave assembly and maker of all the procedures

Alignment and wire bonding connection

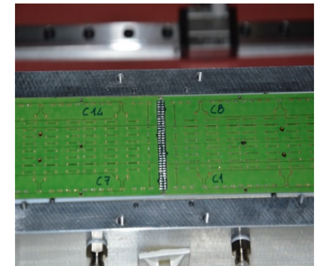


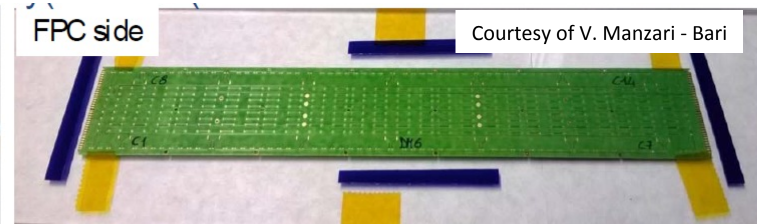
Reference makers





Courtesy of S. Beole'





Conclusion

- Sensor made of new material requires many studies and tests.
- Prototypes of each parts of a detector have to be built and tested.
- The assembly of a detector is not trivial in terms of equipment, tools and jigs. The development of this part cannot be left to the last minute because you can have sensors and electronics featuring good performance, but you might not be able to assemble all things together by guaranteeing good final performance.