



Overview on sensors design and prototyping @FBK

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Fondazione Bruno Kessler



Consistent R&D investment by Local Government (2% of Province's GDP, Gross Domestic Product)









CMM-FBK People

Research	<u>86</u>
Tech & Staff	<u>23</u>
Postdoctoral Fellows	<u>3</u>
PhD Students	<u>22</u>
All Personnel	<u>134</u>
Visiting Scientists	<u>24</u>

Annual Budget: 10.5 M€, 50% self-financing



from Silicon to SiC detectors







> R&D and technology transfer with private companies

At present we have 3 long-term contracts with multinational companies following this scheme.

Collaborative projects

with public funding (H2020, ESA...) In the past 5 years we participated to ~10 FP7/H2020 projects.

Small productions for public and private entities Mainly dealing with custom technologies both for industrial and research applications.





Research Units

The activity is carried out in two Research Units:





~20 people (electronic eng, physicists)

~40 people (physicists, chemists, technicians)



from Silicon to SiC detectors



Full Custom Silicon Technology



State-of-the art CMOS Technologies



Analog and Digital IC Design

130nm-350nm external Fab

Parametric Testing Functional Testing



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Prototyping





Infrastructures





Microfabrication Area: CMOS-like pilot line (6" wafers) with 2 Clean Rooms for device fabrication



- Testing Area: device parametric testing
- Integration Area: device packaging and microsystems assembly
- Micro-Nano Analysis: surface science analytical methodologies (SIMS, AUGER, AFM, ..)

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Infrastructures



SRSIab:

- electro-optical characterization
- tests with high-energy radiation

FunLab:

- microchip electrical characterization
- PCB and prototype assembly
- THz Test Bench

LaserLab:

- electro-optical testing,
- single-photon detectors characterisation
- image sensors testing
- M-BOSOF tests









Research topics

Two main platforms:

Single-photon light sensors



High-energy radiation detectors





R&D initiatives on:

TeraHertz detectors



Graphene-based detector



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Single-photon light sensors

Silicon photomultiplier



SiPM

array of tiny SPADs connected in parallel to give proportional information





number of activated cells equal to number of photons (PDE=1)

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Single photon @ FBK

Single-Photon Avalanche Diodes



Custom technology:

- high efficiency
- low noise
- high flexibility



Standard CMOS technology:

- smart architecture
- high-level integration





PDE vs λ



- RGB-HD 25mm
- Over-voltage = 9 V

30mm cell pitch 77% fill factor

Technologies

Silicon-based detector in full-custom technology







Low Gain Avalanche Detector (LGAD)



- APDs revisited for ionizing particles
- Aiming at low gain both before and after irradiation
- Gain vs breakdown voltage trade-off
- High sensitivity to the implant dose of the multiplication layer
- JTE to prevent from edge breakdown







Silicon Strip Detectors

AMS experiment (@ISS)



Limadou experiment (@CSES)



ALICE experiment (@LHC)

Custom productions for industry



Silicon Drift Detectors



SDD: Tiny collecting electrode for "large" sensing areas
→ minimial series noise!!!

Double-side wafer processing. Fully depleted substrate.





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3D detectors

First proposed by S. Parker et. al. in NIMA 395 (1997), 328



ADVANTAGES:

- Electrode distance and substrate thickness decoupled:

- low depletion voltage
- high speed
- good charge collection efficiency
 → High radiation hardness

-Active edges:

- Dead area reduced up to few microns from the edge

DISADVANTAGES:

- Non uniform response due to electrodes
- Complicated technology
- Higher capacitance with respect to planar



3D pixels @ FBK



- FZ material
- Double side technology
- Columns are passing and empty
- No support wafers
- Surface isolation with p_spray on both side
- 200micron slim edge

FBK Si-3D for IBL ATLAS



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G. Darbo, PIXEL 2014 FBK Wafer Test

<u>Method</u>: temporary metal layer – pixel \rightarrow strips – 80 strips / wafer - IV measured individually (strip to V_{bias} on back side)

- 50 wafer completed and tested, 33 selected
 (≥ 3 good tiles): yield 57% on selected wafers
- Good correlation between wafer and module measurements.







Leakage Current [- nA]

IBL 3D Performance – FC J. Lange, PIXEL 2015 Radiation Hardness

Sub-Pixel Efficiency at 5x10¹⁵ n_{eg}/cm² CNM 3D Sensors (230 µm), Thr. 1500 e p-type Blas Electrodes n-type read-out Electrodes 0.98 8.66 100 160 V. 1.24 80 60 0.32 o. 40 97.5% 8.9 20 00 8.88 100 200 300 (µm) 100 1.10 160 V, 80 60 1.64 40 1,42 99.0% 20 0 100 300 200 400 (um) Planar Sensors (200 µm), Thr. 1400-1600 e , 0 and the local division of 0.98 30.0 1000 V 1.94 0.37 150

96.9% (µm) 600 V. 15, 50 86.4% 140 400 (µm ATLAS IBL Coll., JINST 7 (2012) P11010

- 3D sensors
 - Fully efficient at 160 V and 15° angle
 - Mean efficiency 1-2% lower at normal incidence due to columns

Radiation hardness tested up to 5x10¹⁵ n_{ea}/cm²

- Power dissipation <15 mW/cm² at T=-15° C
- Planar sensors

0.9

3.88

0.86

3.34

9.82

- Need 1000 V for similar efficiency
- Power dissipation ~90 mW/cm² at T=-15° C

→ operational advantage for 3D sensors



100



Are thin 3D feasible ?

Thin wafers

- at 6-inch not thinned that 200um
- double sided process
- bow ?

Local thinning

- Single side
- Processing thicker wafers with local thinning of sensor active areas by DRIE (1) or TMAH (2) could be done

G. Pellegrini et al., NIMA 604 (2009) 115

Back end process: thinning the processed wafers

- Single side
- "special" wafers: Epi, SOI, ...
- After bump





Thin 3D pixels @ FBK



Realizzato un lotto planare su SI-SI

- SI-SI or SOI
- Single Side Technology
- Ohmic columns depth > active layer
- Junction columns depth < active layer
- Holes partially filled with poly-Si
- Slim edge





Thanks to G-F Dalla Betta Univ TN



A few pictures

- Wafers with temporary metal
- Good lithographical quality





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SEM Pictures



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Ohmic & Junction Column

Filled (partially) with polysilicon SEM HV: 30.0 kV WD: 19.30 mm **VEGA3 TESCAN** View field: 50.0 µm Det: SE 10 µm SEM MAG: 5.53 kx Date(m/d/y): 02/18/16 Performance in nanospace

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FBK edgless technology

Support wafers SOI wafers, epi, ... Si-Si

DRIE etched trench and doping

- Trench definition and etching (DRIE)
- Doping using gas source technology
- Trench filling with polysilicon



Trench filled with polisilicon







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• Hit-efficiency above 90% up to 40 µm away from the last pixel

No good tracks beyond -50 μm due to quality cuts

M. Bomben et al. Nucl. Instrum. Meth. A 712 (2013) 41 Thanks to Marco Bomben



Anisotropic TMAH Etching tetramethylammonium hydroxide





Silicon buried channels for detector cooling

Channels made with individual holes:

The section is determined by the DRIE process, the length by the layout





Channels realized as a sum of individual holes: The section is determined by the process and by layout, the length by the geometry Experimental results made in the lab TFD INFN of Pisa show a general compliance of the temperature of the sample to the specific fixed at least up to a power of about 2.5 W/cm².







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grazie