ATLAS Pixel R&D Projects Meeting
Bologna 14th-15th March

HVR_CCPD: Hybridization

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(Summary of the work done in Genova, Milano and Trento)

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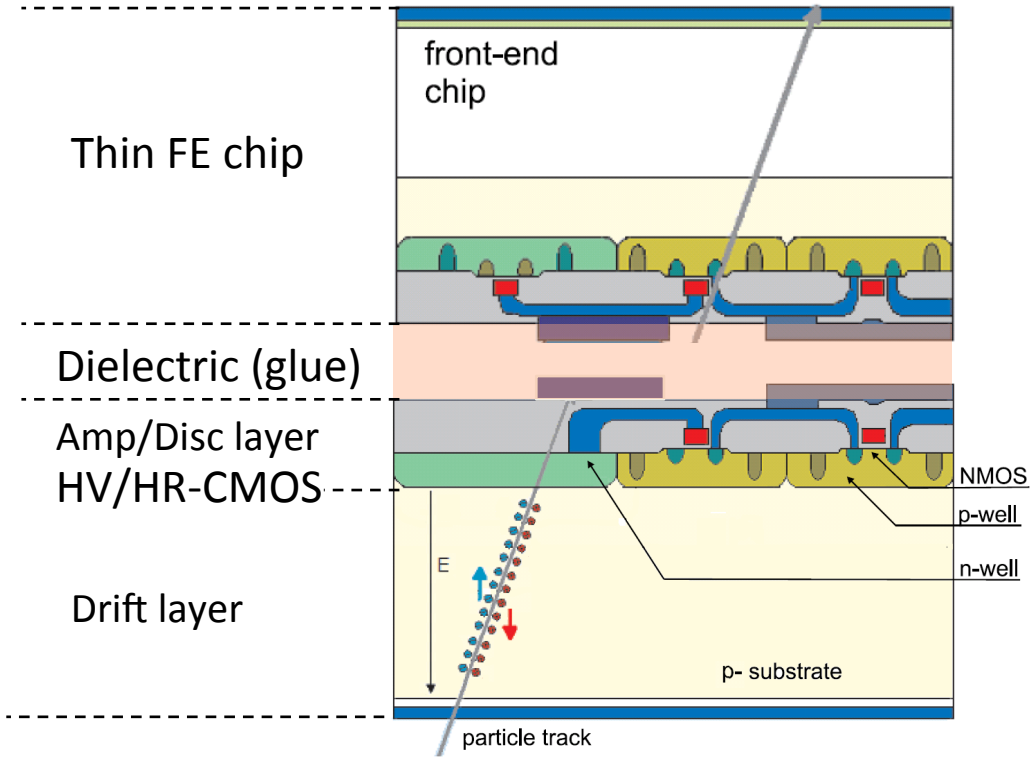
Studies on Capacitive Couplings

The new 65 nm front-end chip, being developed by RD53 Collaboration, will be compatible with **50 × 50 µm² or 25 × 100 µm² pixel size sensors.**

The smaller pixel sizes imply up to five times the bump density used in the current ATLAS Insertable B-Layer modules and consequently an order of **120 k pixels per chip.**

In next slides will be shown some studies done on:

- **capacitive coupling for CMOS**



Studies on Capacitive Couplings

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

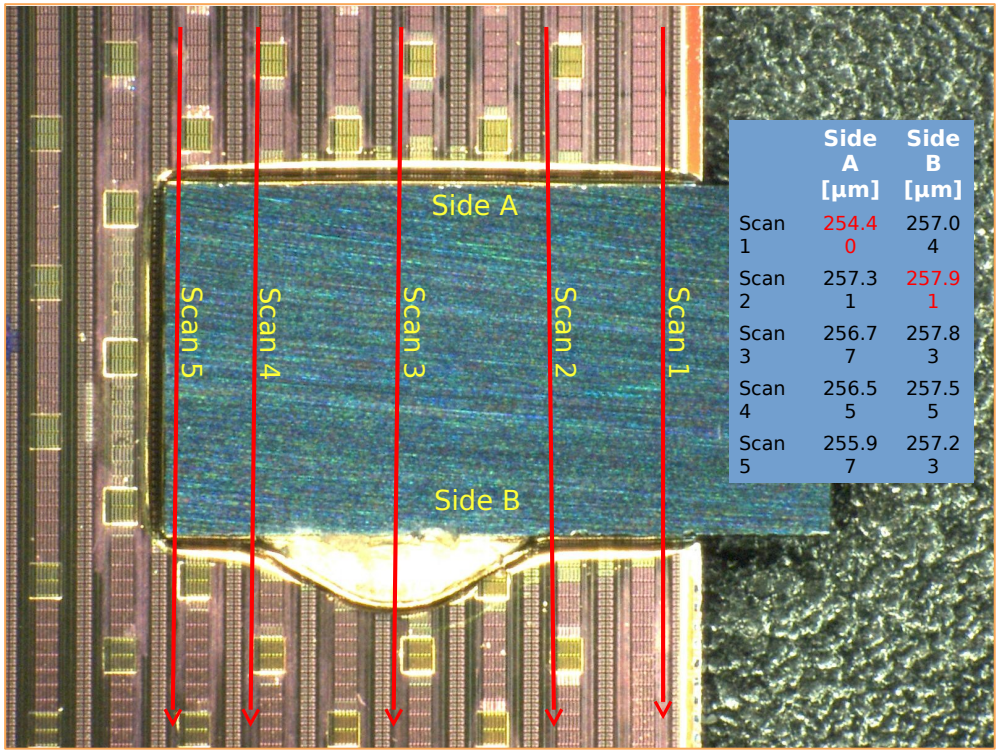
Align & pressure

Deposition of SU8 photoresist by spinning

Credits: Giovanni Darbo

In 2014 and mid 2015 test on “in-house” hybridization

➘ Successful single chip assemblies and learnt on glue and SU8 deposition (spacers)



	Side A [µm]	Side B [µm]
Scan 1	254.40	257.04
Scan 2	257.31	257.91
Scan 3	256.77	257.83
Scan 4	256.55	257.55
Scan 5	255.97	257.23

In picture: HV2FE-I

Now systematic test on large chips (FE-I4 size) and wafer process for pillars

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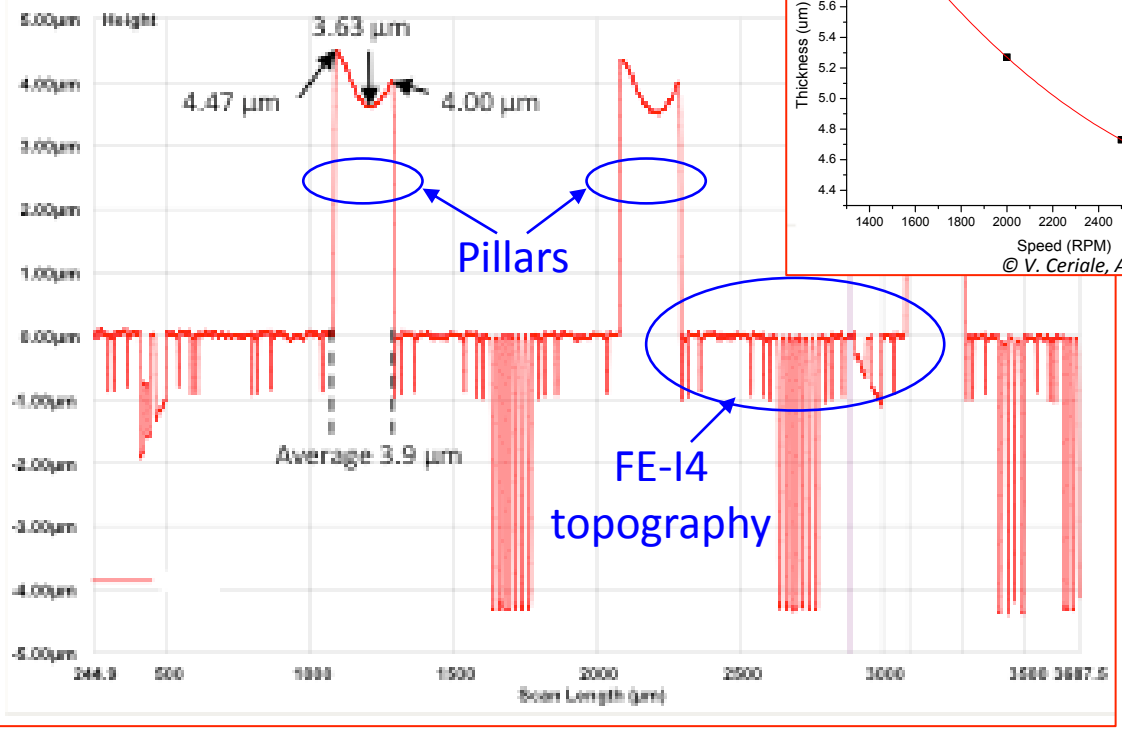
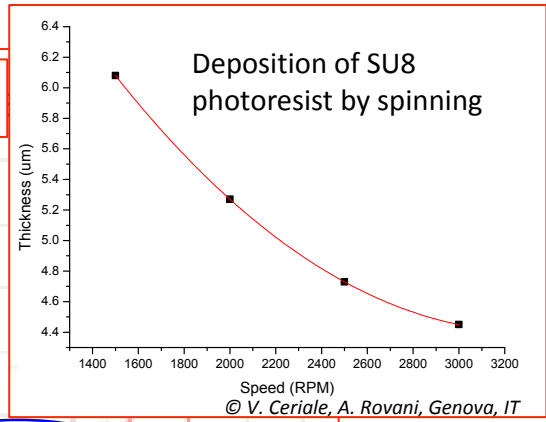
Procedure for Controlled Glue Thickness

- Deposit uniform layer of SU8 photoresist on R/O chip wafer (or single chip) by spinning – tune for 5 µm layer by controlling RPM speed
- Pattern pillars using lithographic process

Profile of pillars on top of a FE-I4 chip





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A batch of dummy wafer produces at FBK (Trento) with capacitive structures to test uniformity of glue thickness layer 6-inch wafers, 24-32 capacitors (3-7 pF) per chip

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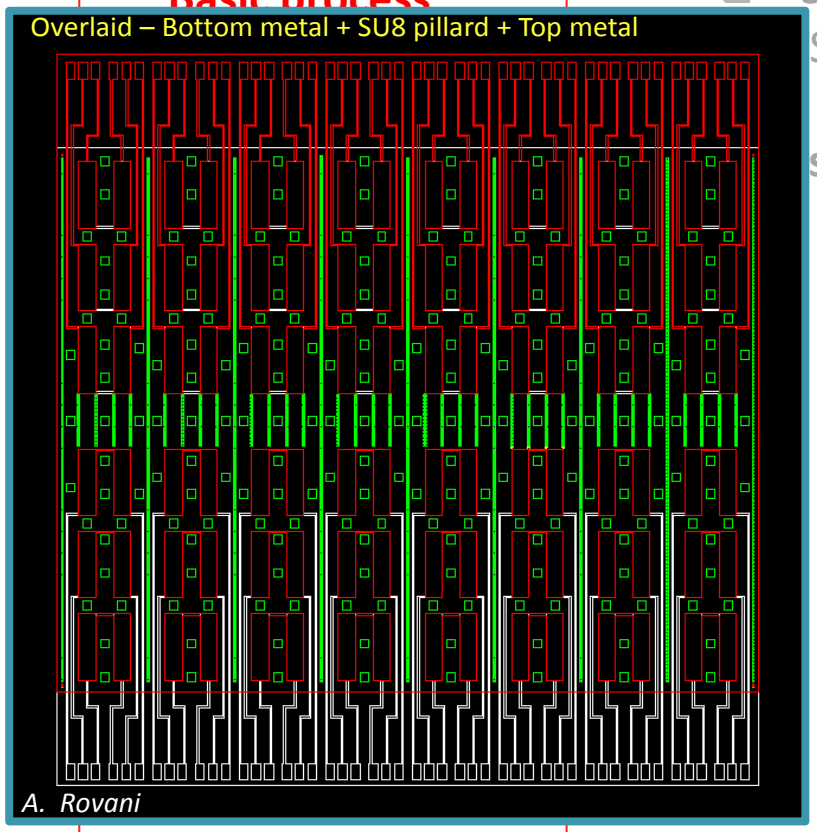

photoresist by spinning

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A batch of dummy wafer produces at FBK (Trento) with capacitive structures to test uniformity of glue thickness layer **6-inch wafers, 24-32 capacitors (3-7 pF) per chip**

The 6 wafers are at Selex together with pillar deposition mask – also 10 blank wafer provided to Selex to test SU8 spinning and photolithography – measurements of pillar uniformity will be done in Genova

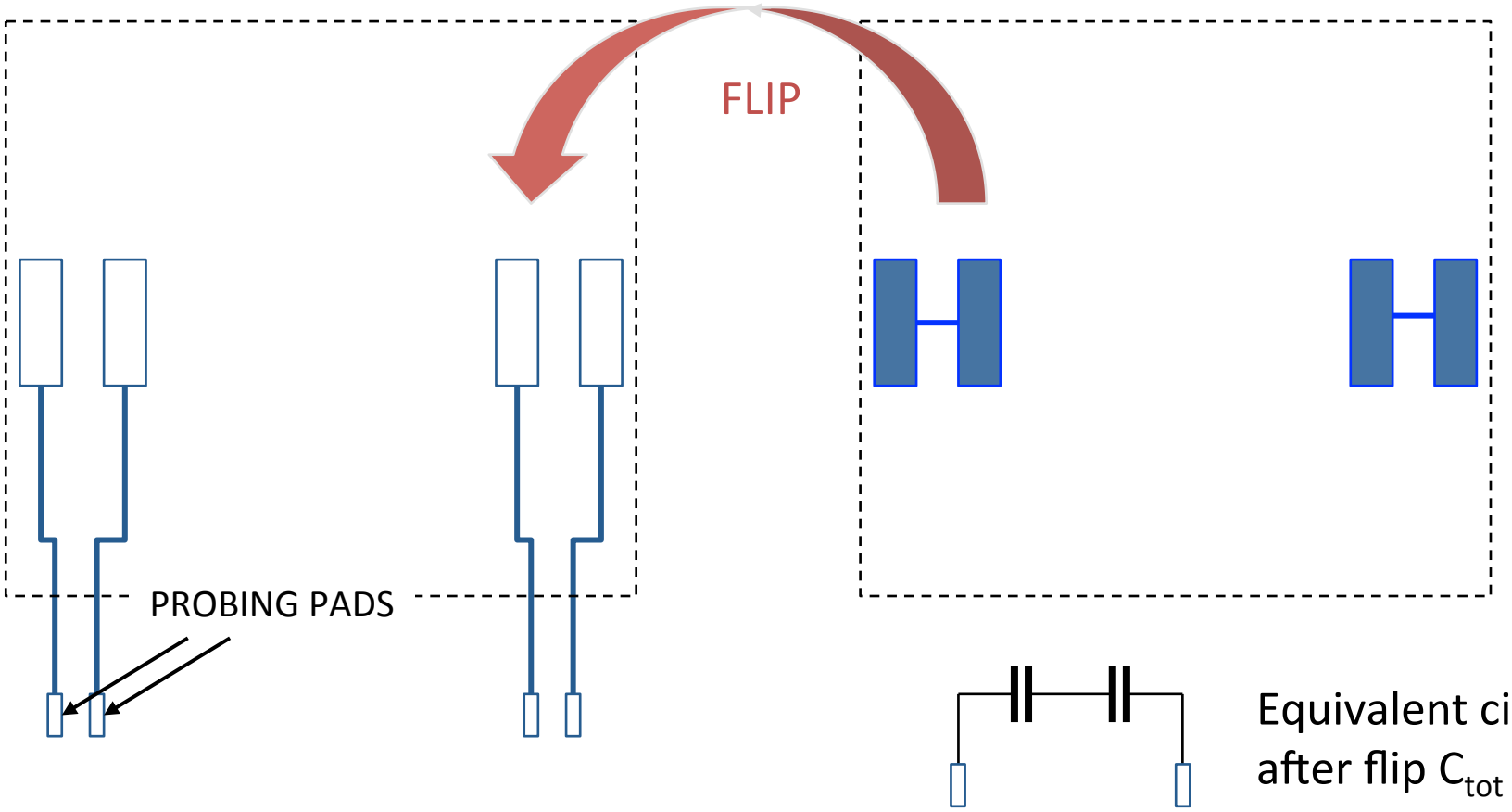
PTA in Grenoble has been contacted for pillar deposition

Flip-chip at Genova and other labs – thermal/UV glue curing (preliminary studies done)

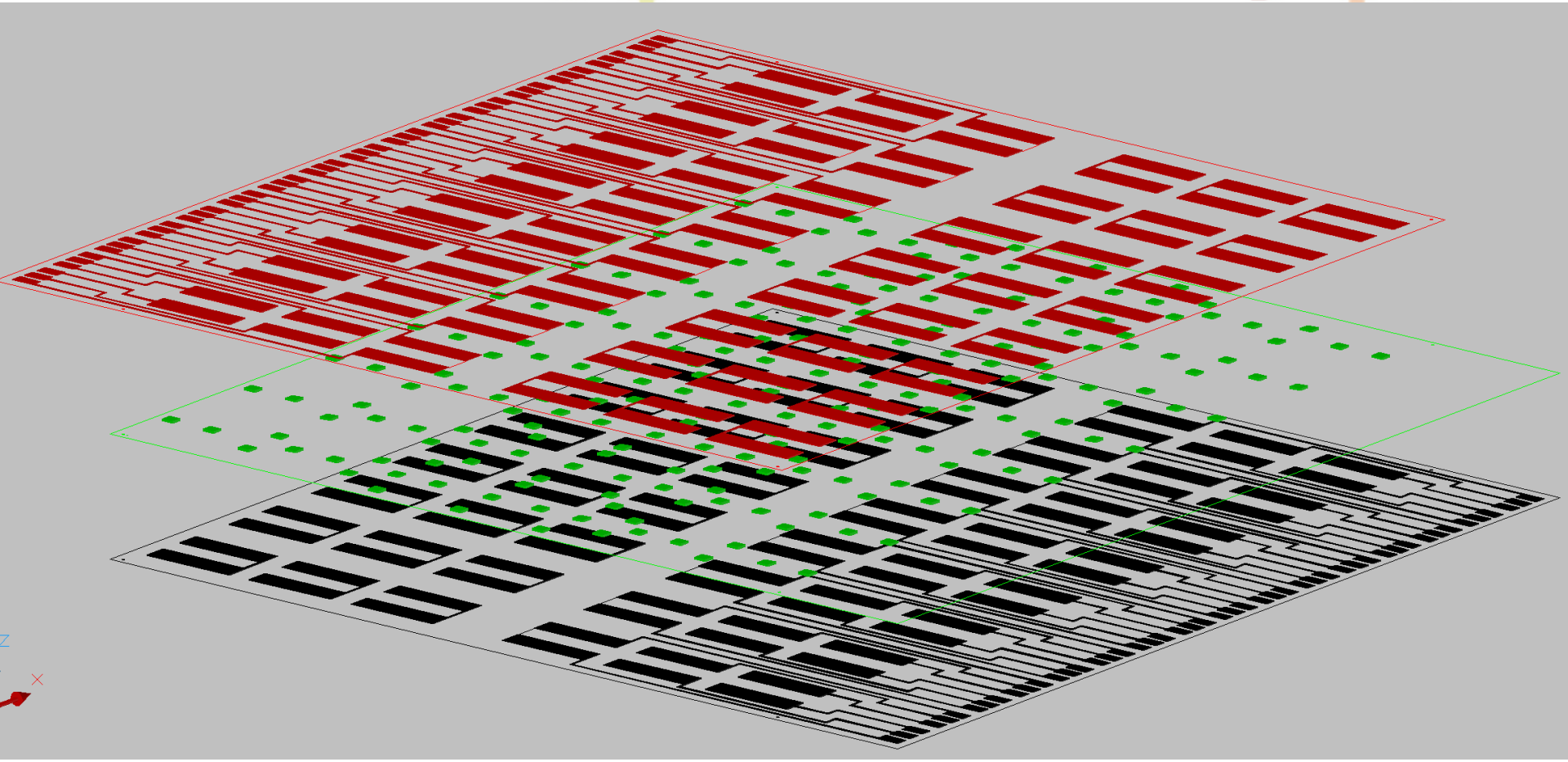
Dummy Assembly

Test pillar and glue process on dummy wafers/chips

Design a 6-inch wafer with FE-I4 size dummies – place 32 (24) capacitors of 1 (2) mm^2 to test glue thickness uniformity over all surface

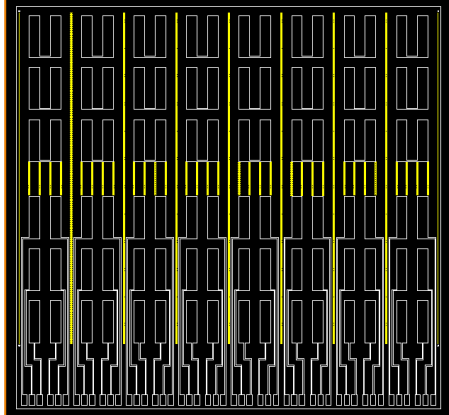


Dummy Assembly

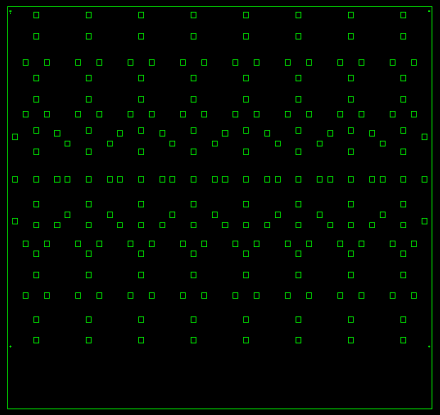


Dummy Assembly

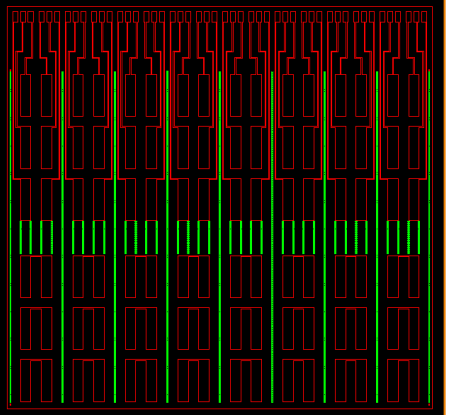
Bottom metal

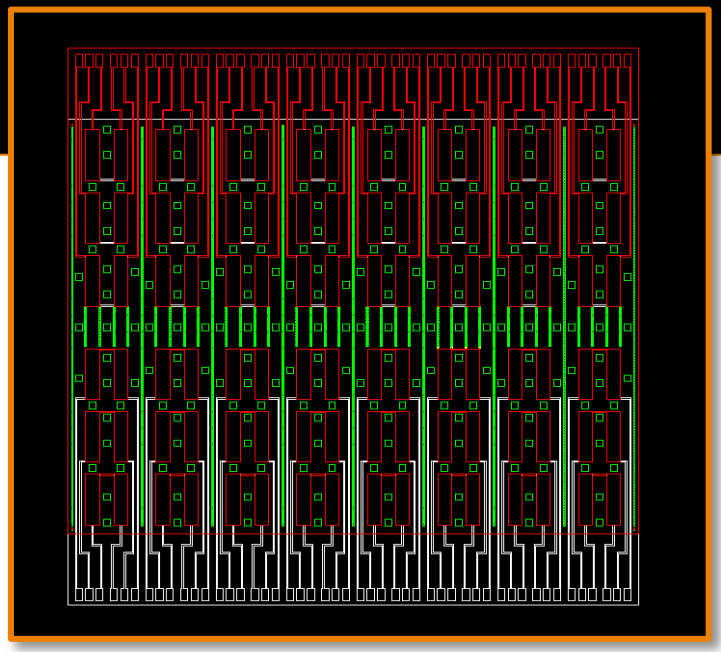


SU8 pillars Mask



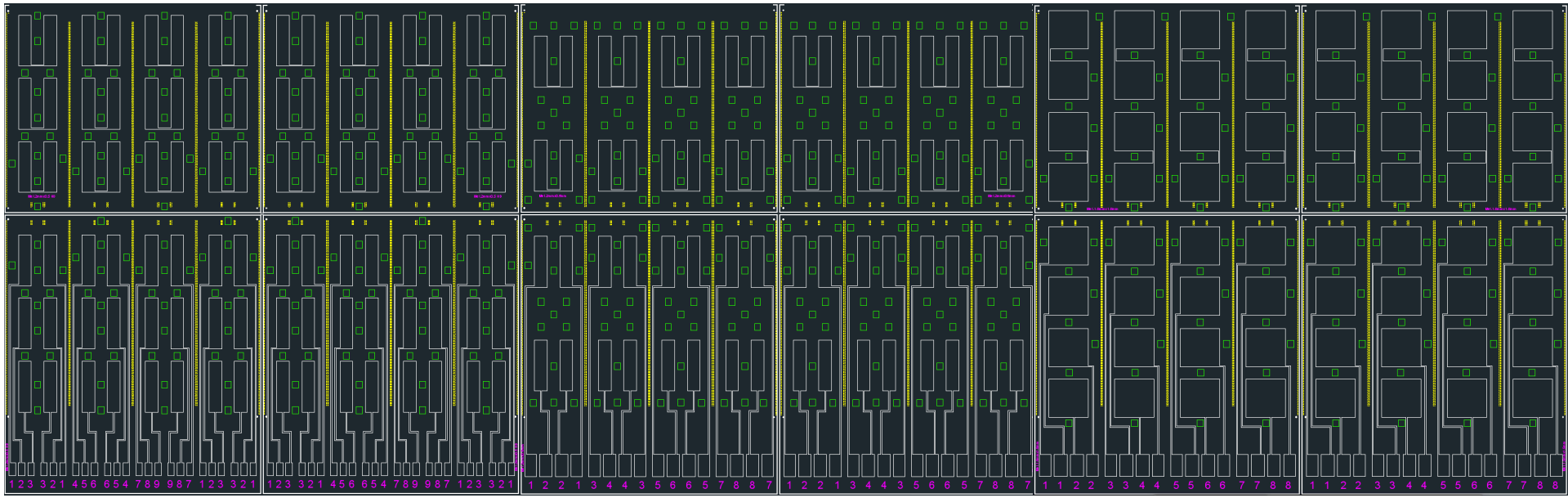
Top metal





Dummy Assembly

Different Layouts



DESIGN 1
48 capacitors
3.6 fF @ 5µ dielectric (ε_r = 3.8)

DESIGN 2
32 capacitors
3.6 fF @ 5µ dielectric (ε_r = 3.8)

DESIGN 3
24 capacitors
~7 fF @ 5µ dielectric (ε_r = 3.8)

Conclusions

Capacitive Couplings:

- ✓ Good results of tests done on first lab prototypes
- ✓ **Dummy wafers for FE-I4 size tests produced**
  - ✓ **Measurements will start as soon as the dummies will return from Selex**