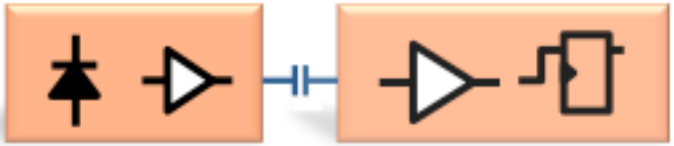


HVR - CCPD

STMicroelectronics chips

ATLAS ITK Italy meeting, 14/03/2016

Attilio Andreazza, M. Citterio, V. Liberali, C. Meroni, F. Ragusa, E. Zaffaroni - INFN Milano

M. Biasotti, G. Darbo, G. Gariano, A. Gaudiello, C. Gemme, P. Morettini, L. Rossi, E. Ruscino, M. Sannino – INFN Genova

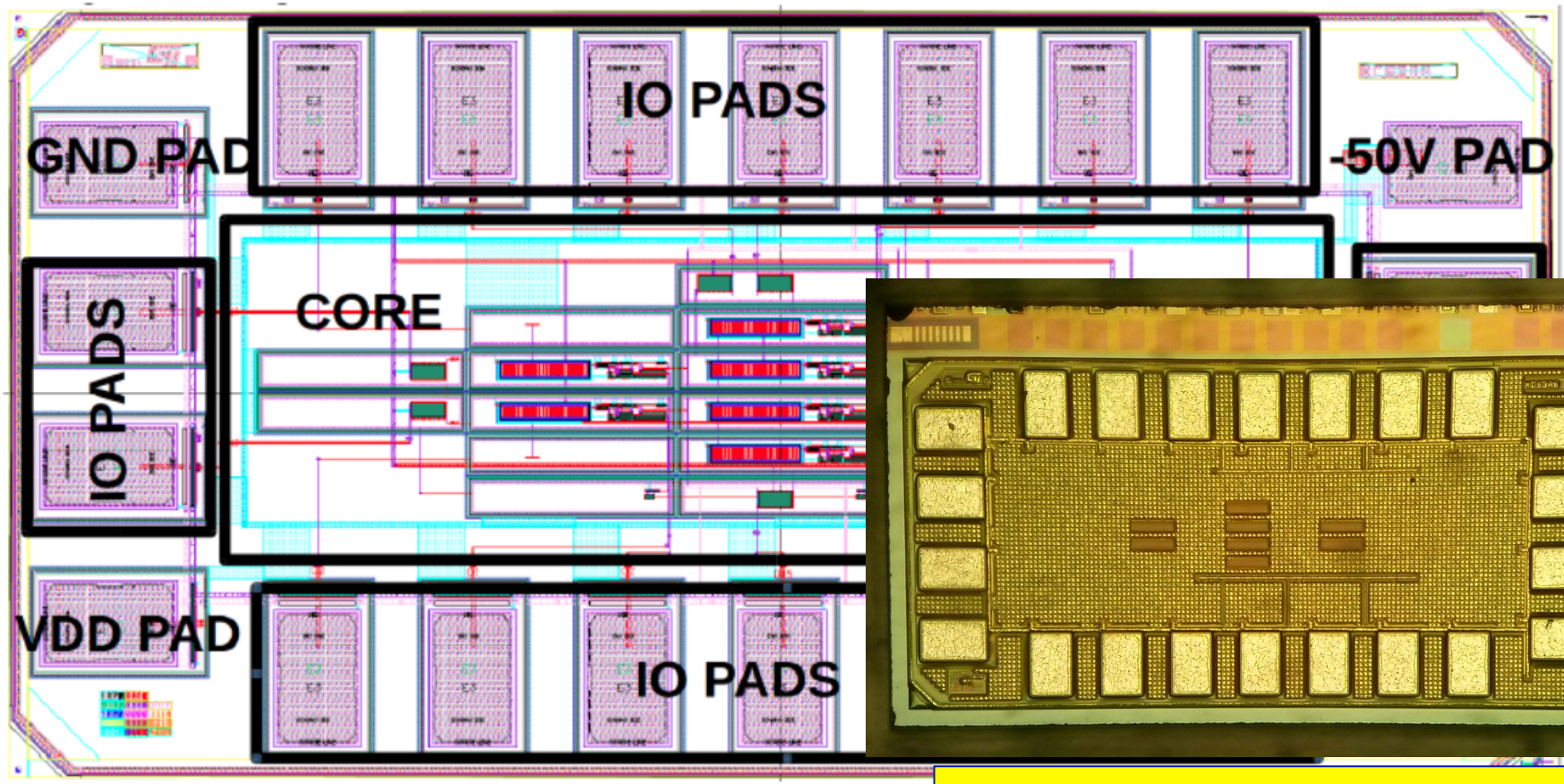
C. Sbarra, A. Sidoti, F. Fabbri – INFN Bologna

H. Shrimali, I. Yadav, A. Yoshi – IIT Mandi

Overview

- Reminder of passive diode performance
- Test of active pixels
  - amplifier design
  - injection circuitry
  - performance
- Submission of 3×4 mm^2 array
  - STM postponed submission time to 22nd April
  - **Hybridization in Andrea's talk today**
  - **Simulation covered in Federica's talk tomorrow**

KC35A



Layout of the STM test chip (KC53A):

- *22 I/O and VDD/GND pads*
- *8 pixels (50 x 250 µm²): Collecting diode + Amp.*
- *4 pixels (50 x 250 µm²): Collecting diode only*

First version delivered July 2015:

- shorts between power lines and ground

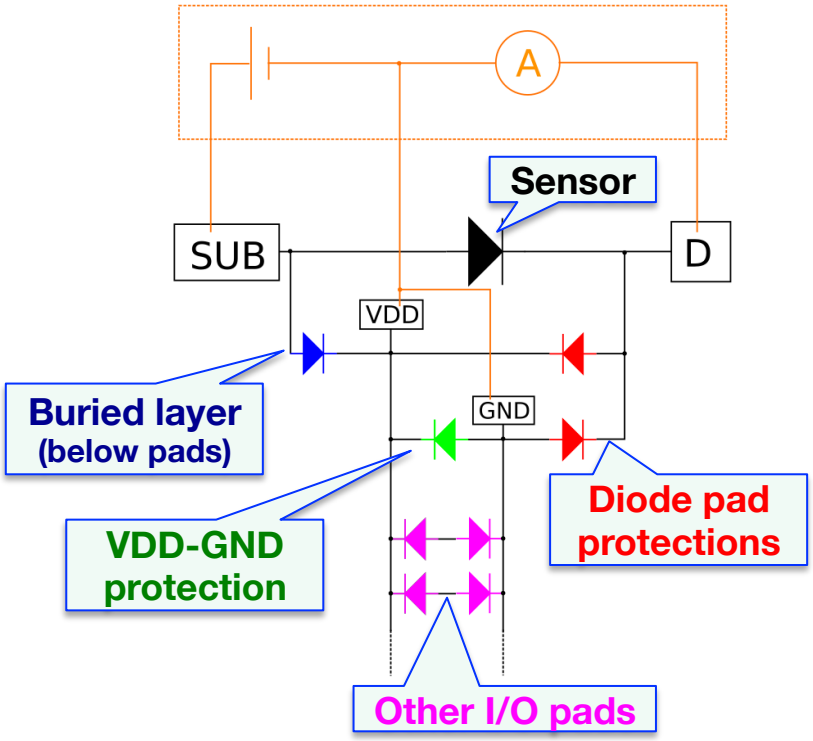
Fixed version delivered 29 Jan. 16

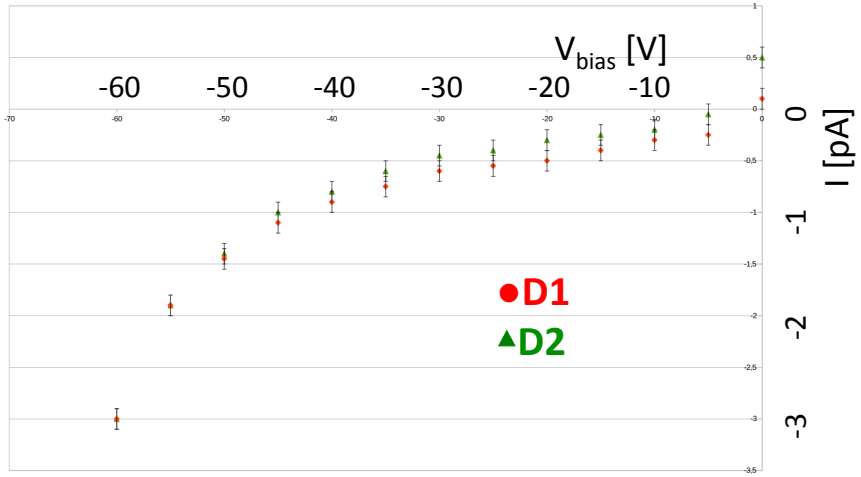
Design and layout by:

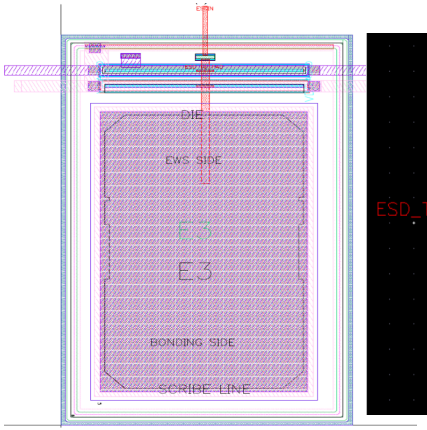
- *H. Shrimali and V. Liberali (MI)*

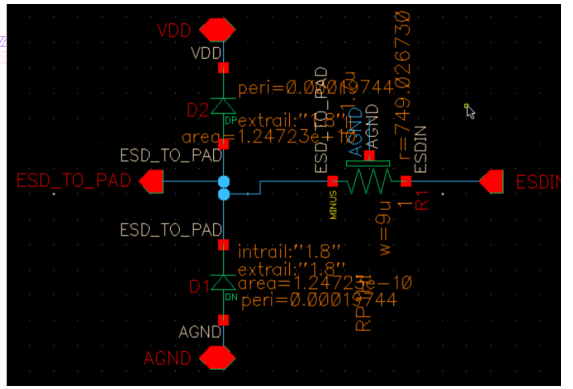
Passive diodes: I-V

- I-V measurements (and C-V as well) need to keep into account ESD protection diodes:
  - 0.8-1.4 pA leakage current @ 50 V on 50×250 µm^2 pixels
  - whole chip leakage current, dominated by buried layer below I/O pads
- "Programmed" break-down at 70 V.
- STM would like us to set also protections between SUB and GND (multiple 7V breakdown structures)









Passive diodes: C-V

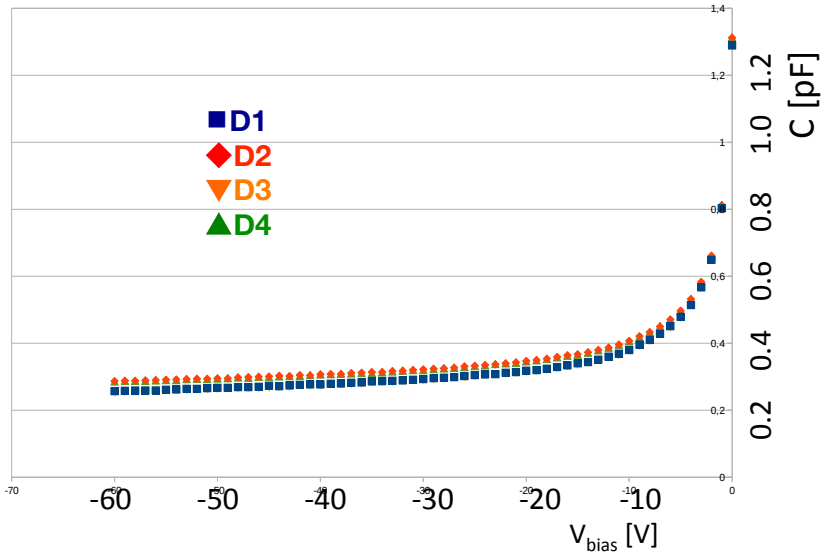
- Measured capacitance parameterized as:

$$C = C_P + \frac{1}{\sqrt{k(V+V_o)}}$$

  - C_P : parasitic capacitance
  - V_o: built-in voltage
  - $k = \frac{\mu\rho}{2\epsilon A^2}$

$\mu(holes) = 450\,cm^2\,V^{-1}$
$\rho = 125\,\Omega\,cm$
$\epsilon = 1\,pF/cm$
$A = 250 \cdot 50\,\mu\,m^2$

Substrate datasheet: 100-150 Ωcm



- Measurement compatible with expectation: k=1.8 $V^{-1}pF^{-2}$
- Corresponding depletion is 22-24 µm at 50 V

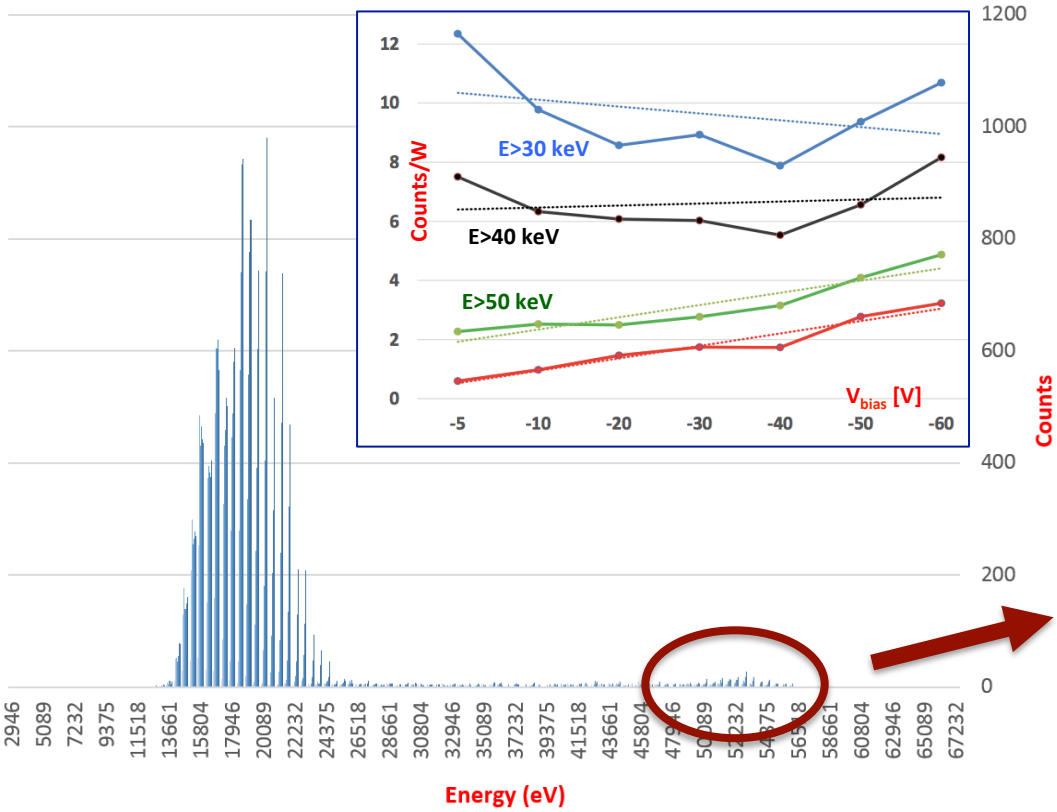
$$Q = eAdN_A$$
$$V = eN_A d^2 / 2\varepsilon$$
$$C = \frac{Q}{V} = \frac{2\varepsilon A}{d}$$

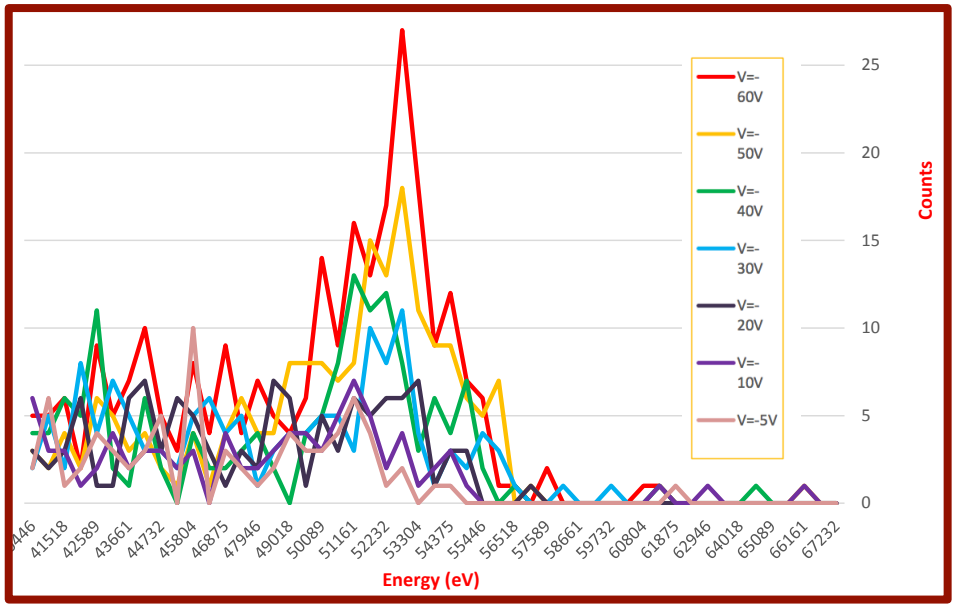
	D1	D2	D3	D4
Cp (pF)	0,156	0,191	0,153	0,191
k	1,76	1,95	1,75	1,94
Vo (V)	0,439	0,407	0,442	0,406
C-Cp@-50V (pF)	0,111	0,104	0,110	0,104

Output pads 0.12-0.15 pF

Passive diodes: source tests

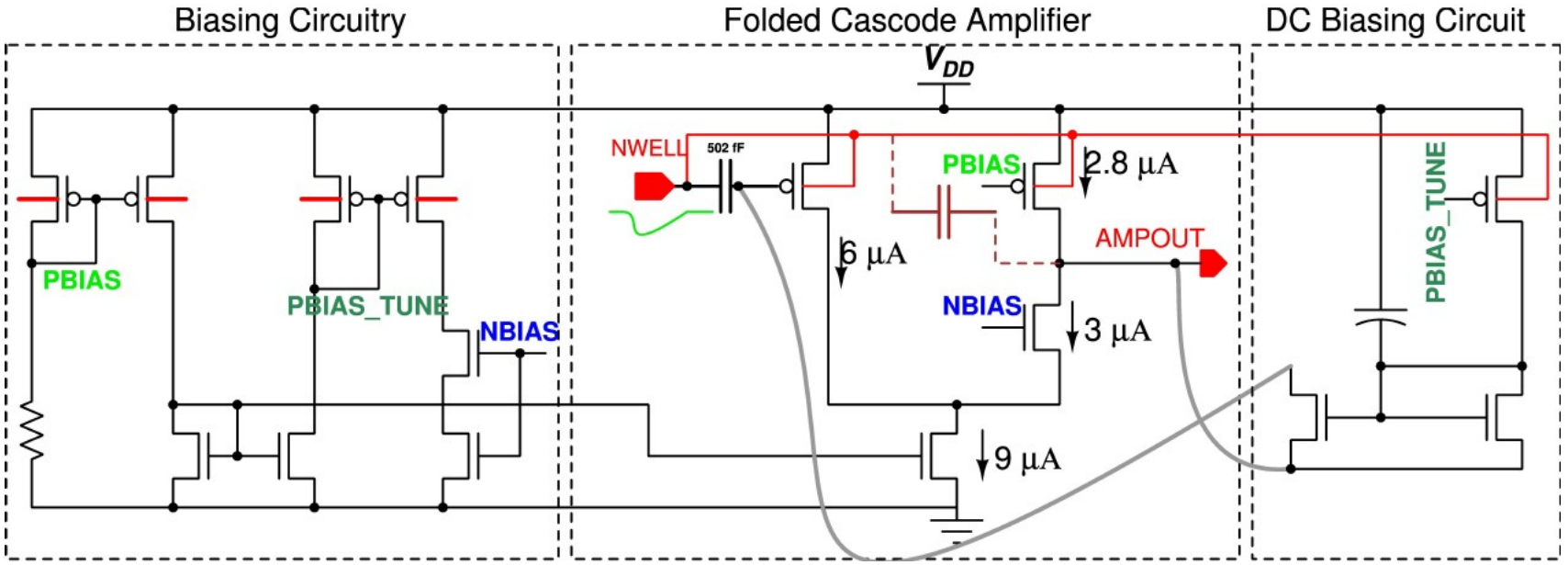
- Cross check rate with ^{241}Am source
- Low rate due to small active volume
  - photoelectric peak at ~0.1 Hz rate with 1 mCi source
  - rate proportional to depletion (as expected)
  - peak shape dependent on depletion (range of 60 keV electron in Si ~33 µm)



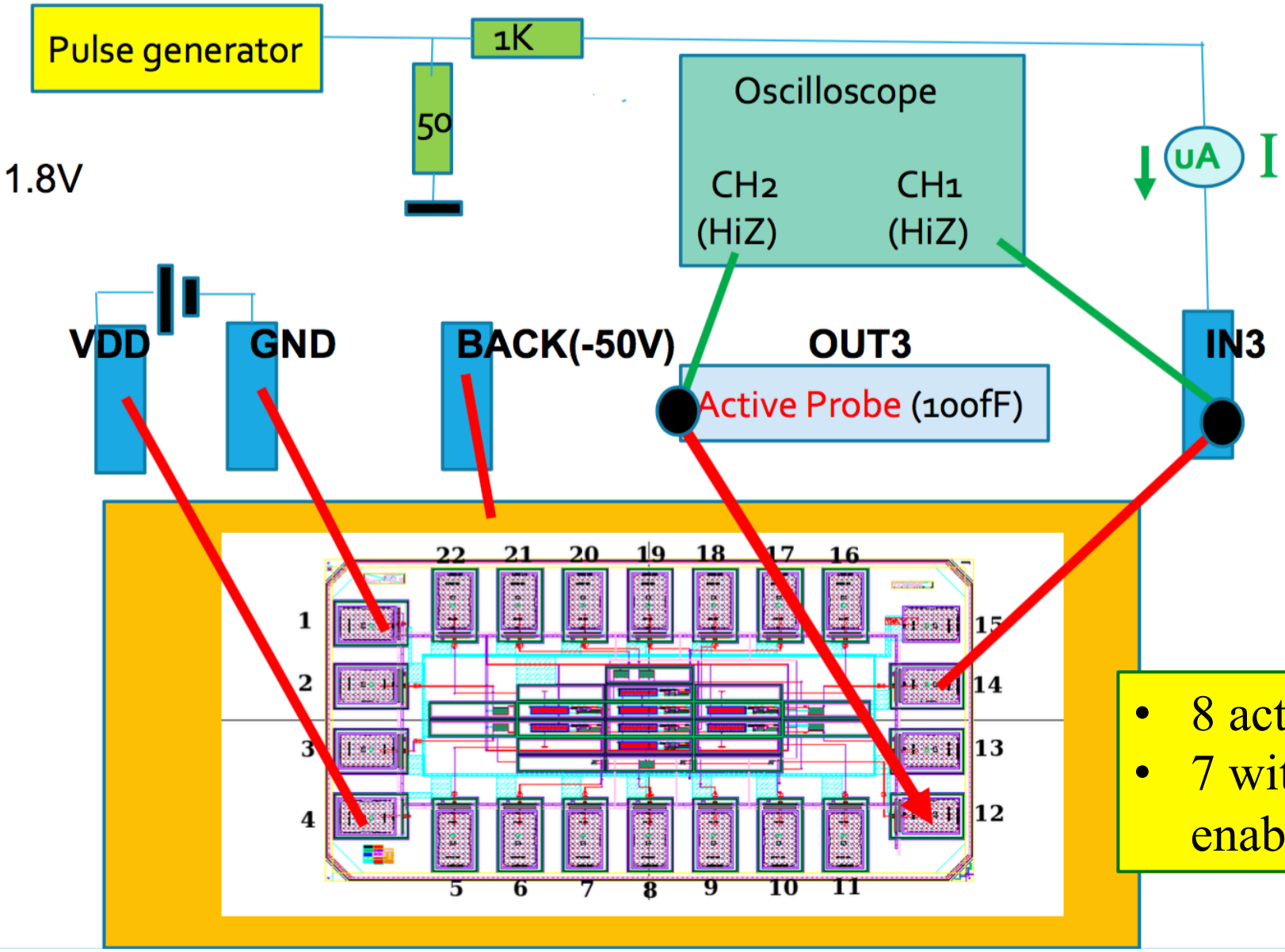


Active pixels: power consumption

- Current absorption: 0.28 mA (VDD=1.8 V)
- corresponds to 35 µA pixel
- in agreement with expectation from the device simulation:
  - 9 µA for the amplifier
  - 25 µA for the biasing circuitry



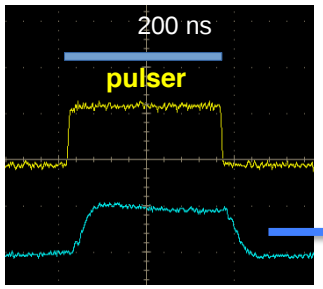
Active pixels: test setup

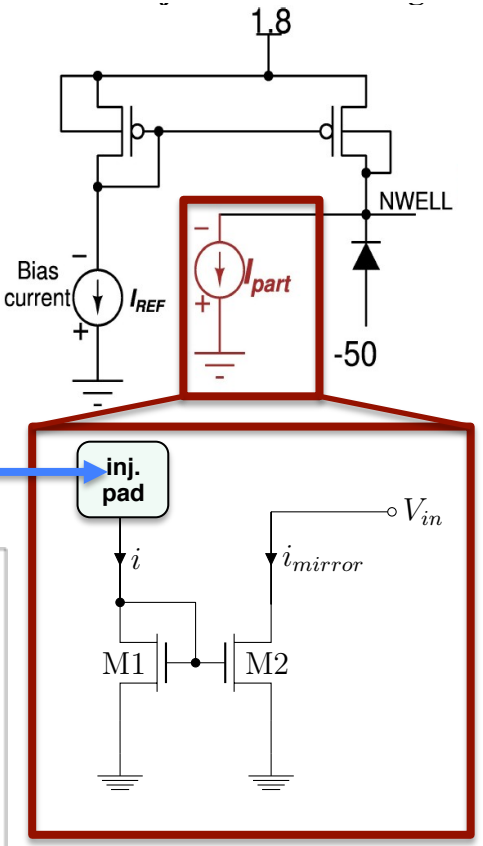


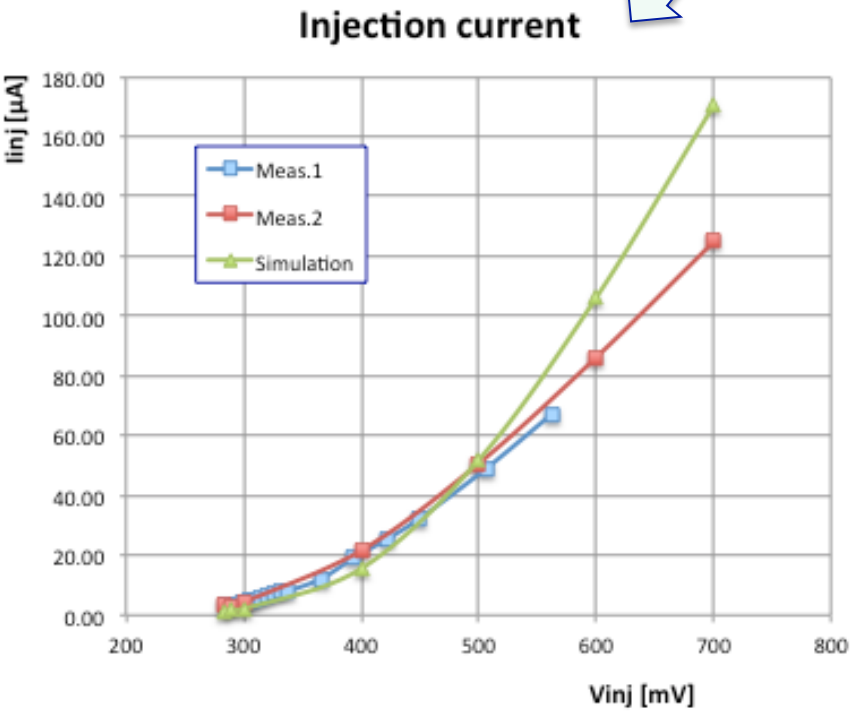
- 8 active pixels
- 7 with injection enabled

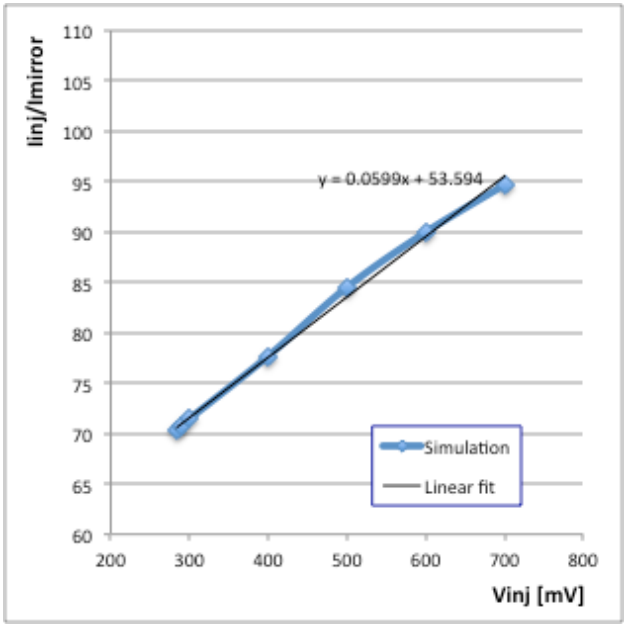
Active pixels: injection

- Injection through a current mirror
  - nominal 1/103 reduction factor
  - operating below saturation: 1/70-1/94
  - not too different from simulation…

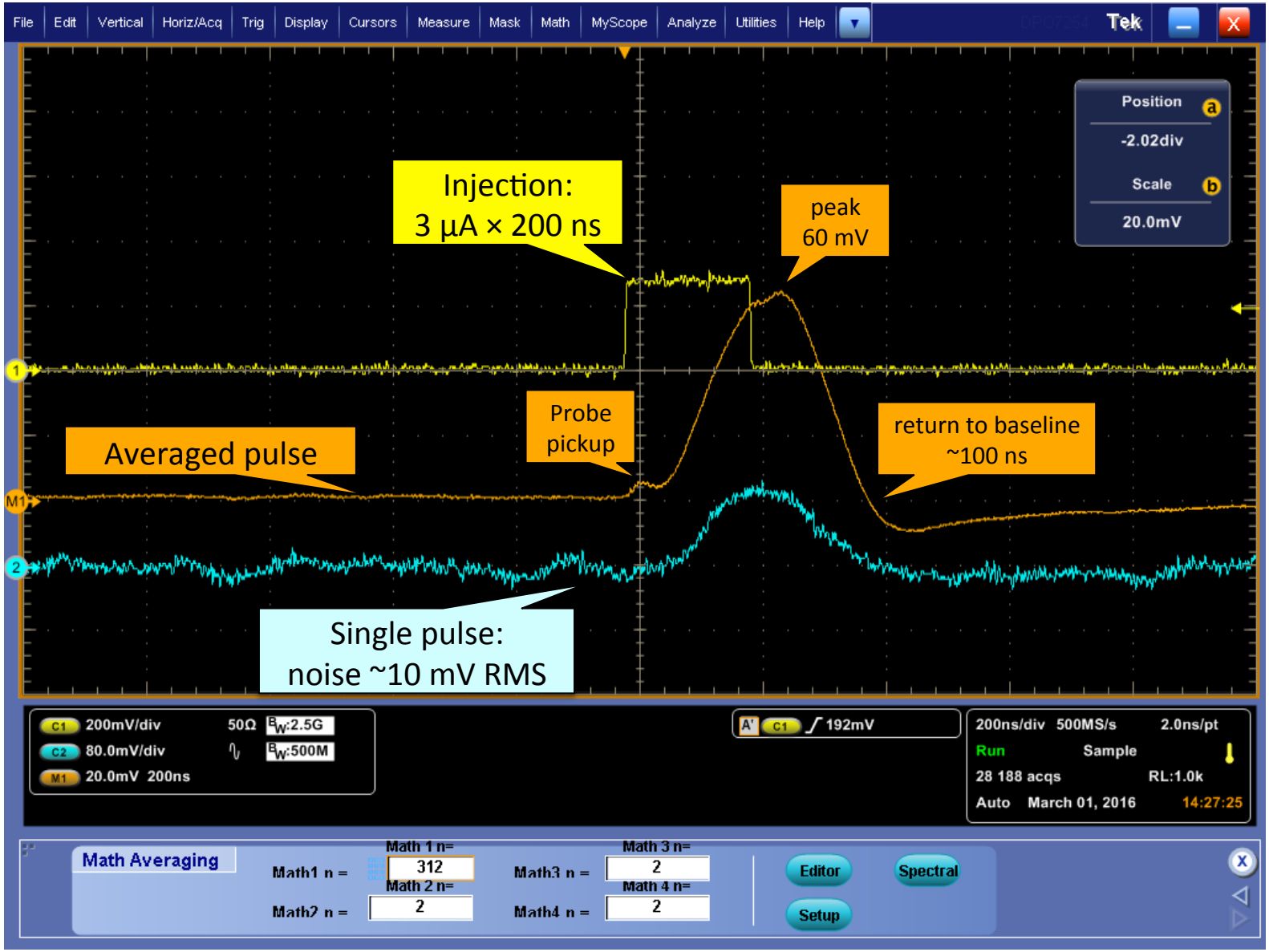




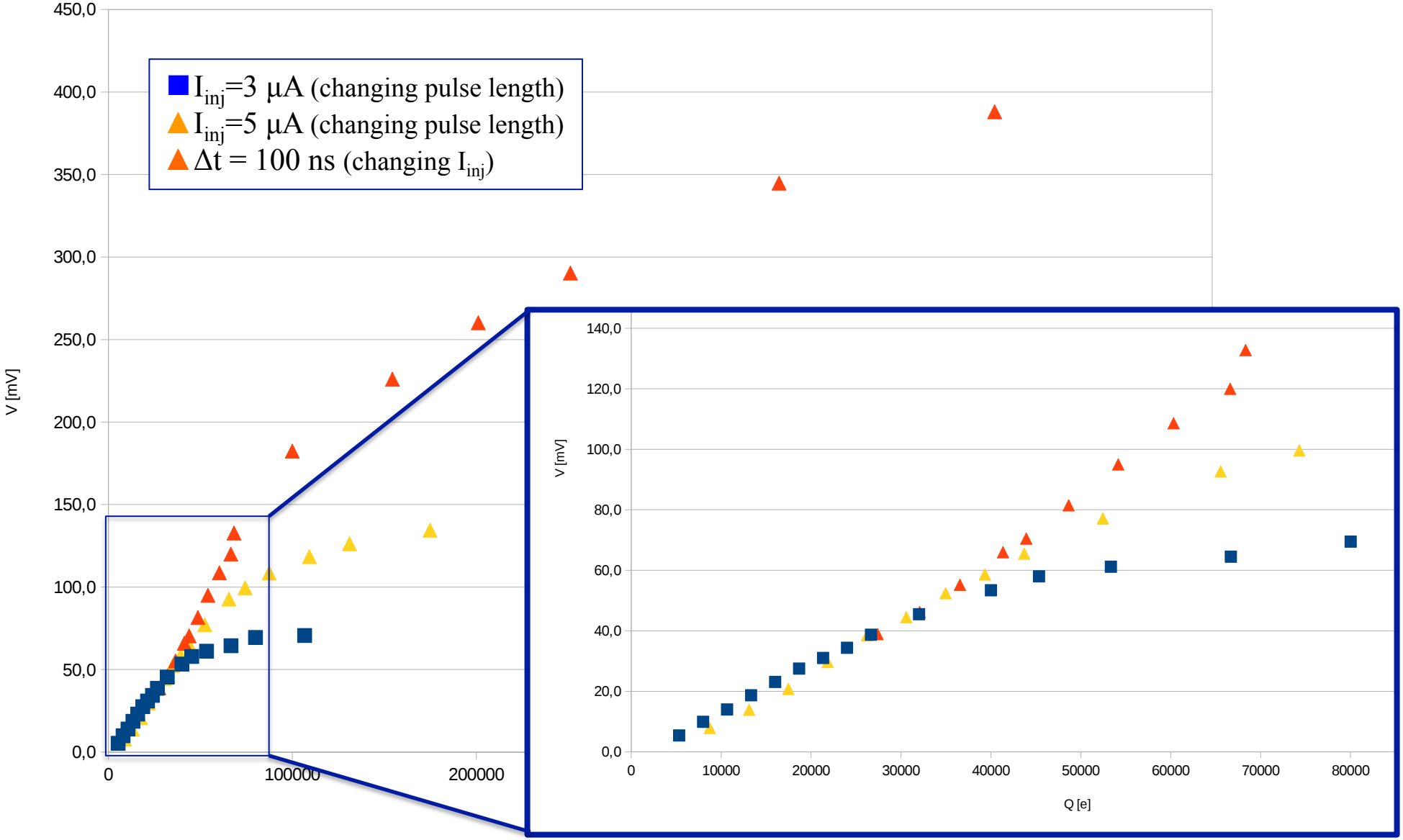




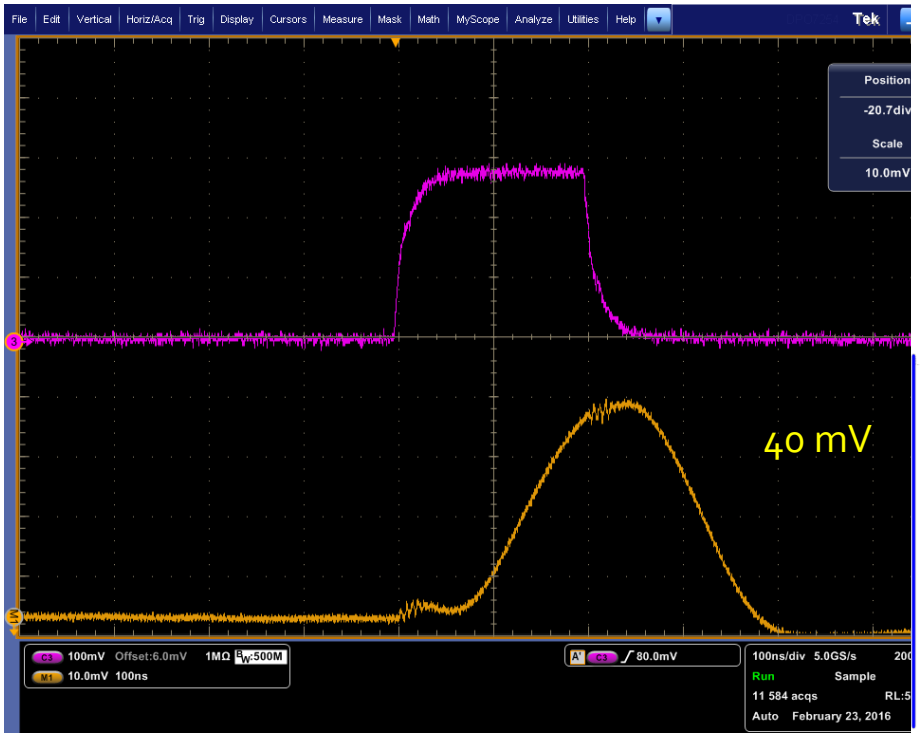
Active pixels: pulse shape

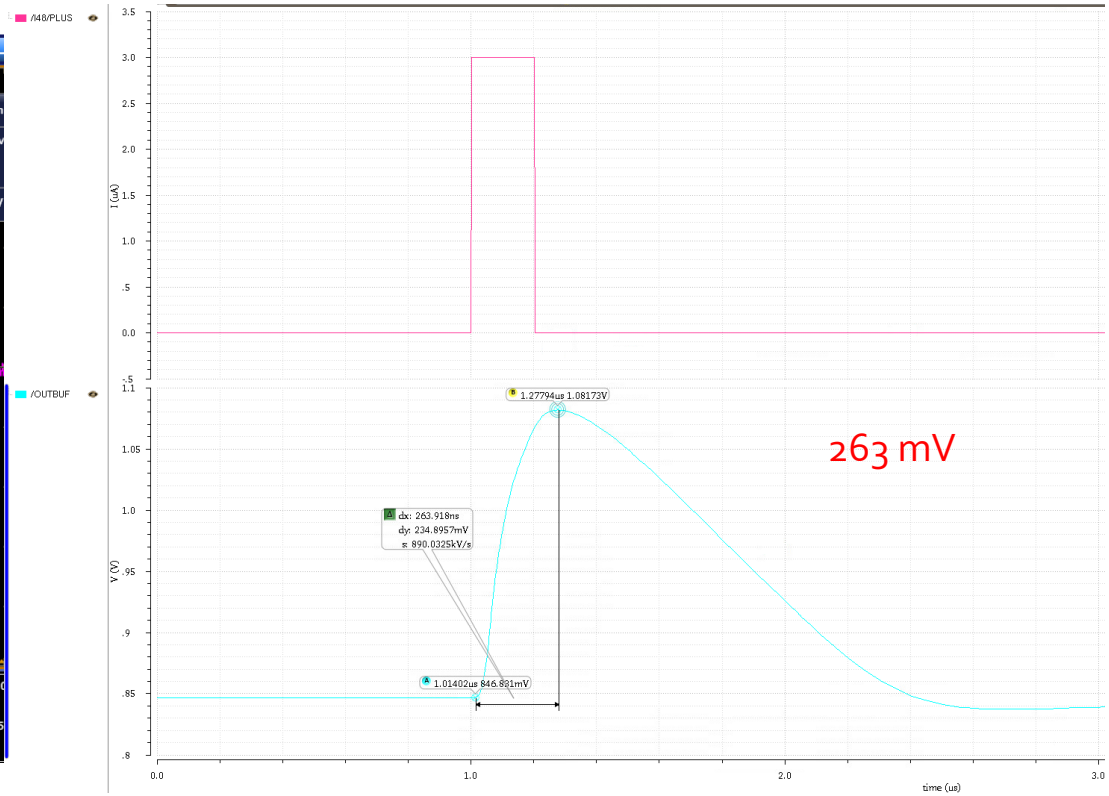


Active pixels: linearity

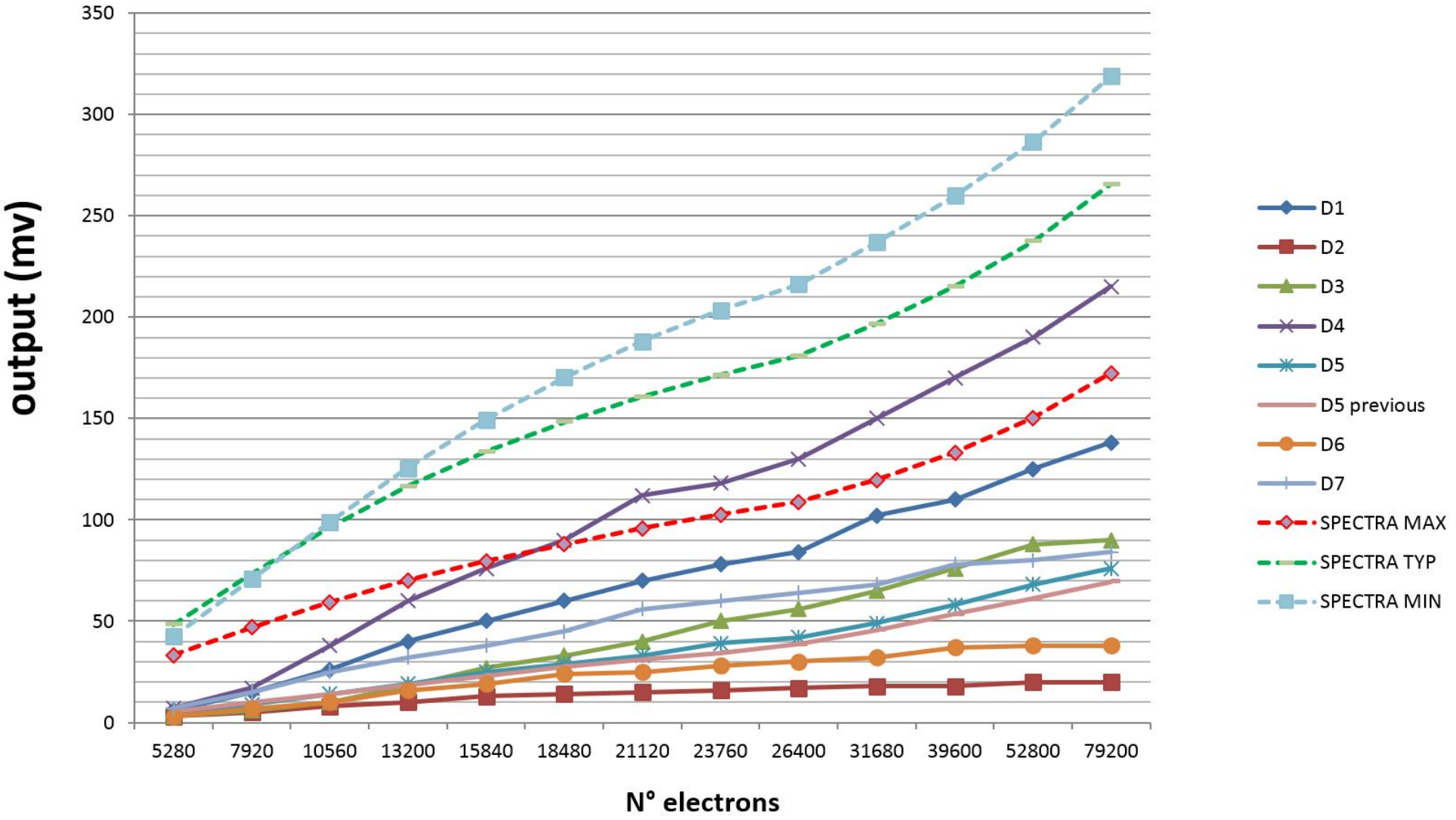


Active pixels: comparison with simulation





Active pixels: comparison with simulation



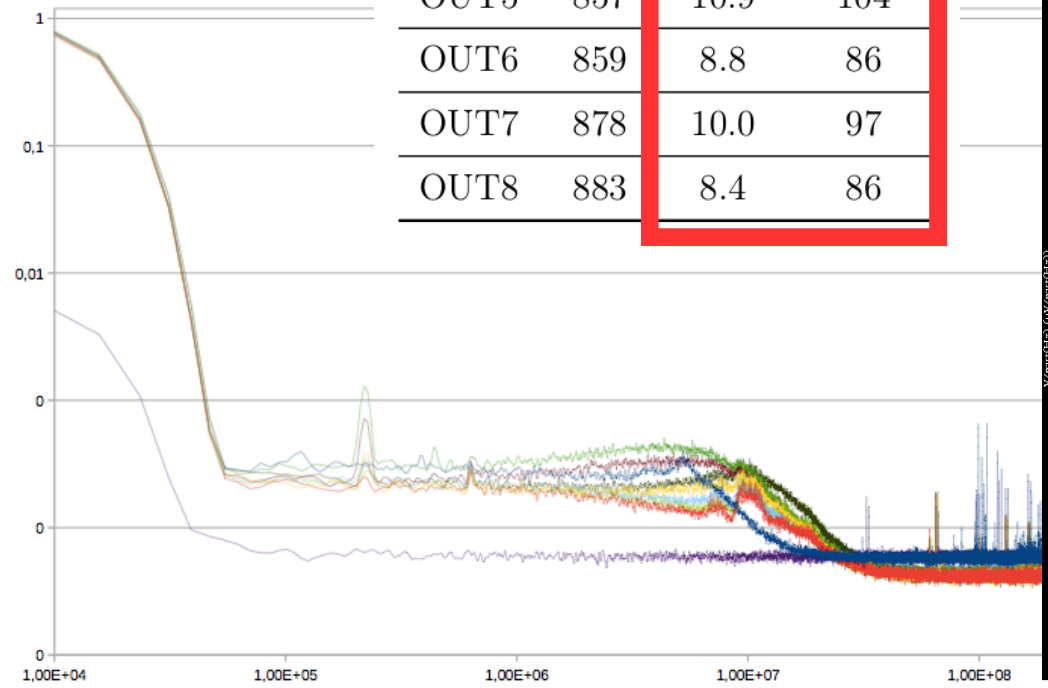
Active pixel: noise

	DC (mV)	RMS (mV)	PK-PK (mV)
OUT1	847	8.5	102
OUT2	795	8.6	83
OUT3	840	8.9	91
OUT4	855	12.1	116
OUT5	857	10.9	104
OUT6	859	8.8	86
OUT7	878	10.0	97
OUT8	883	8.4	86

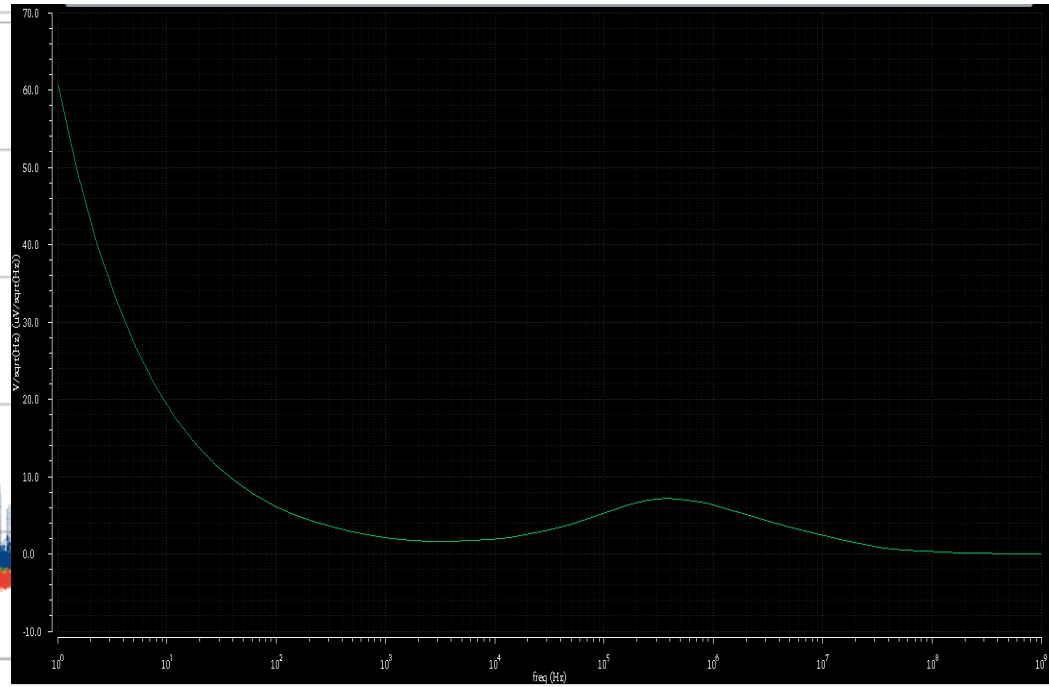
OutBuf Noise (6.6 mV rms)

Device	Param	Noise Contribution	% Of Total
I8.M4.m1	id	0.00306388	21.02
I0.M17.m1	fn	0.00303263	20.60
I0.M0.m1	fn	0.0027767	17.27

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00668221
Total Input Referred Noise = 5.26717e-08
The above noise summary info is for noise data



10 kHz 1 MHz 100 MHz



10 kHz 1 MHz 100 MHz

TPM1 layout

- Inspired from demonstrator layout (picture below)
- Lateral space to be tuned to match alignment with FE-I4
- Leftover space ad bottom of pixel region is only 20 µm, may be increased in multiple of the 50 µm pixel size.

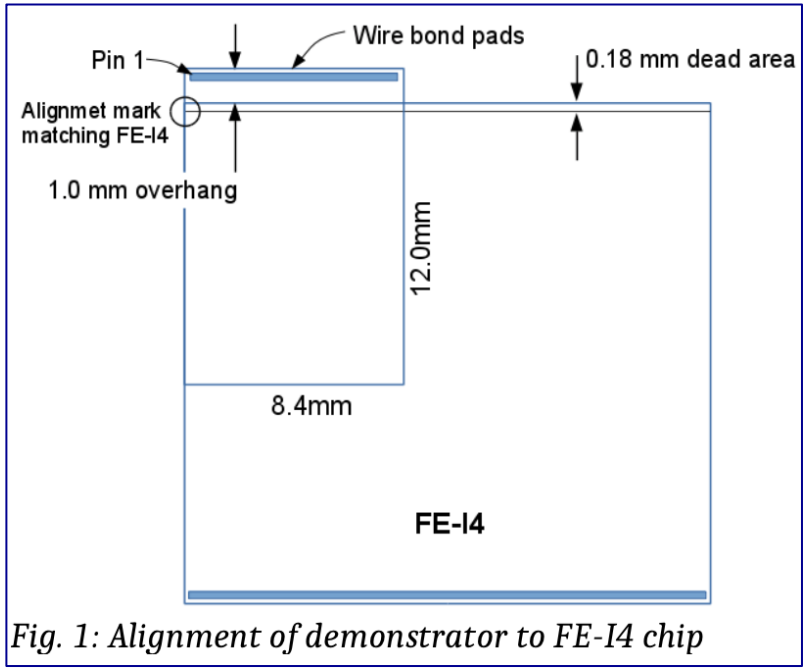
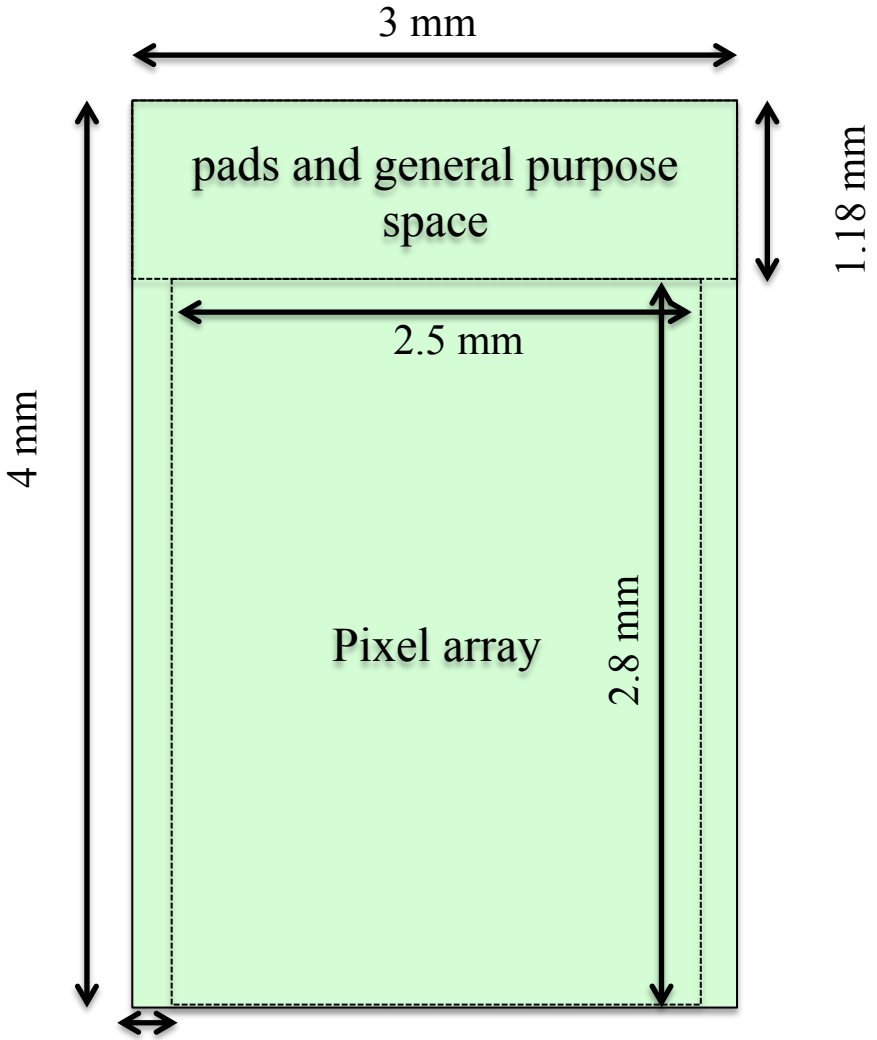
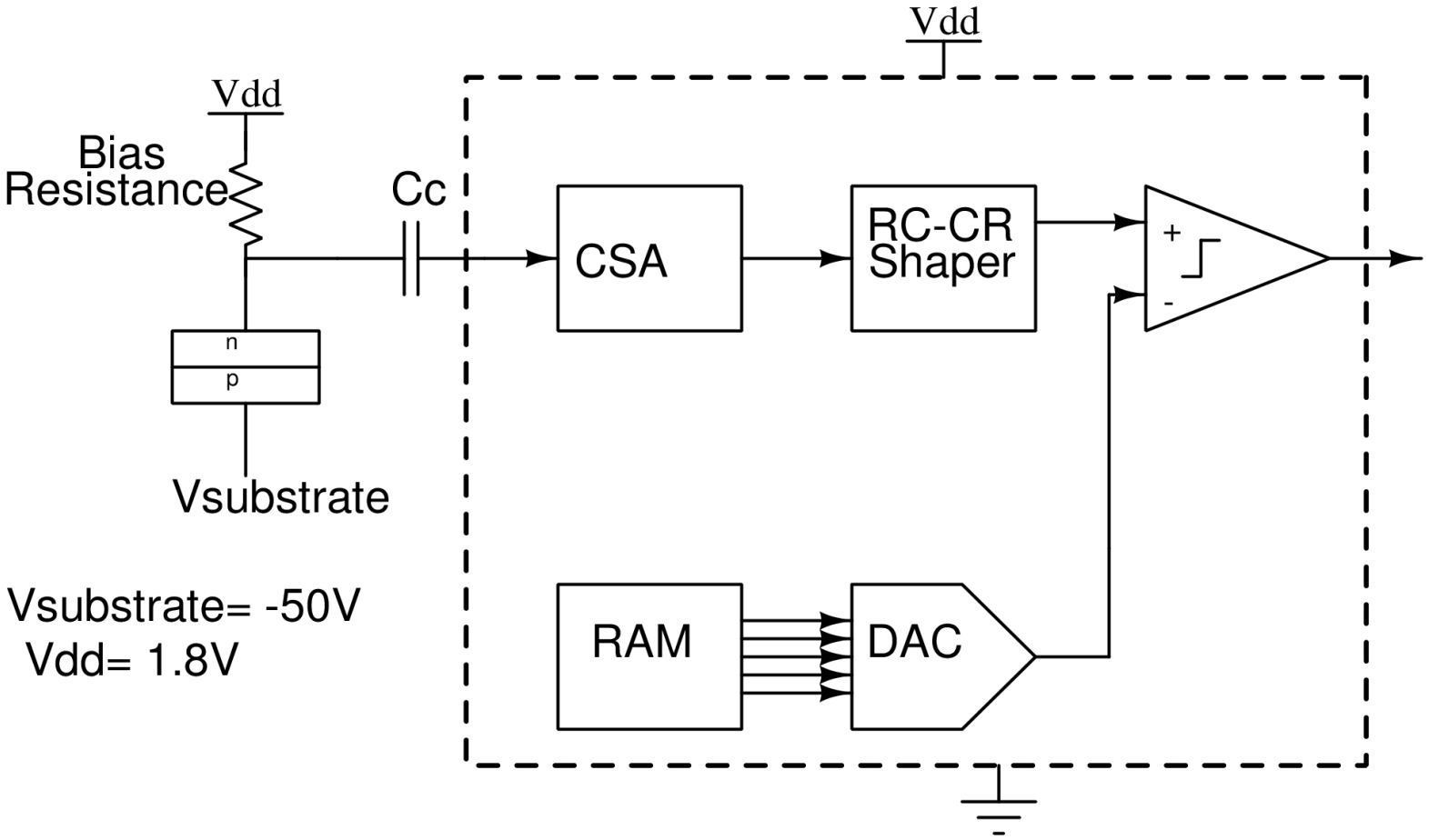


Fig. 1: Alignment of demonstrator to FE-I4 chip



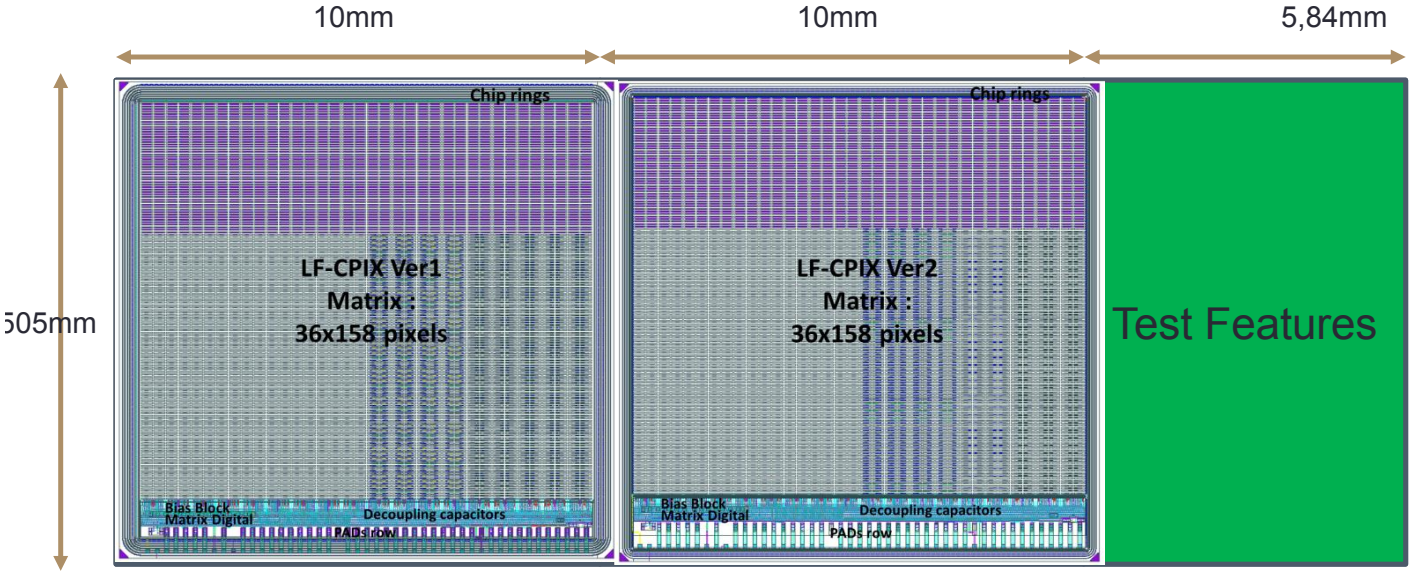
Pixel cell



Genova + Mandi + Milano

HV-CMOS in ATLAS

- Two large size demonstrators:
  - AMS 180 nm (Genève-Karlsruhe), available
  - LFoundry (CPPM-Bonn), submitted



Other technologies being tested:

- XFAB (SOI)
- TowerJazz

- Seat 1 : LF-CPIX (see details)
- Seat 2 : LF-CPIX with new guards rings strategy
- Seat 3 : test features

Testbeams

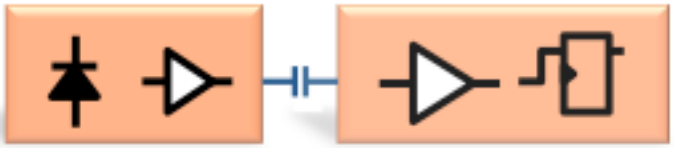

Mon 2 Mai | Tue 3 Mai | Wed 4 Mai | Thu 5 Mai | Fri 6 Mai | Sat 7 Mai | Sun 8 Mai | Mon 9 Mai | Tue 10 Mai | Wed 11 Mai | Thu 12 Mai | Fri 13 Mai | Sat 14 Mai | Sun 15 Mai | Mon 16 Mai | Tue 17 Mai | Wed 18 Mai | Thu 19 Mai | Fri 20 Mai | Sat 21 Mai | Sun 22 Mai | Mon 23 Mai | Tue 24 Mai | Wed 25 Mai | Thu 26 Mai | Fri 27 Mai | Sat 28 Mai | Sun 29 Mai | Mon 30 Mai | Tue 31 Mai | Wed 1 Jun | Thu 2 Jun | Fri 3 Jun | Sat 4 Jun | Sun 5 Jun
Week 18 19 20 21 22
Area T4 - H6
ATLAS AFP H. Kagan
RD42 CMS Outer Tracker D. Lazic
M. Silari
CERF S. Vlachos
ATLAS ITK
Mon 30 Mai | Tue 31 Mai | Wed 1 Jun | Thu 2 Jun | Fri 3 Jun | Sat 4 Jun | Sun 5 Jun | Mon 6 Jun | Tue 7 Jun | Wed 8 Jun | Thu 9 Jun | Fri 10 Jun | Sat 11 Jun | Sun 12 Jun | Mon 13 Jun | Tue 14 Jun | Wed 15 Jun | Thu 16 Jun | Fri 17 Jun | Sat 18 Jun | Sun 19 Jun | Mon 20 Jun | Tue 21 Jun | Wed 22 Jun | Thu 23 Jun | Fri 24 Jun | Sat 25 Jun | Sun 26 Jun | Mon 27 Jun | Tue 28 Jun | Wed 29 Jun | Thu 30 Jun | Fri 1 Jul | Sat 2 Jul | Sun 3 Jul
Week 22 23 24 25 26
Area T4 - H6
S. Vlachos
ATLAS ITK
S. Vlachos
ATLAS BCM/ITK
H. Kagan
RD42
D. Dannheim
Clic pix
ATLAS AFP
Mon 1 Aug | Tue 2 Aug | Wed 3 Aug | Thu 4 Aug | Fri 5 Aug | Sat 6 Aug | Sun 7 Aug | Mon 8 Aug | Tue 9 Aug | Wed 10 Aug | Thu 11 Aug | Fri 12 Aug | Sat 13 Aug | Sun 14 Aug | Mon 15 Aug | Tue 16 Aug | Wed 17 Aug | Thu 18 Aug | Fri 19 Aug | Sat 20 Aug | Sun 21 Aug | Mon 22 Aug | Tue 23 Aug | Wed 24 Aug | Thu 25 Aug | Fri 26 Aug | Sat 27 Aug | Sun 28 Aug | Mon 29 Aug | Tue 30 Aug | Wed 31 Aug | Thu 1 Sep | Fri 2 Sep | Sat 3 Sep | Sun 4 Sep
Week 31 32 33 34 35
Area T4 - H6
AIDA WP7
S. Vlachos
ATLAS ITK
S. Vlachos
ATLAS BCM/ITK
D. Dannheim
Clic pix
RD42 & Monopix
Mon 26 Sep | Tue 27 Sep | Wed 28 Sep | Thu 29 Sep | Fri 30 Sep | Sat 1 Oct | Sun 2 Oct | Mon 3 Oct | Tue 4 Oct | Wed 5 Oct | Thu 6 Oct | Fri 7 Oct | Sat 8 Oct | Sun 9 Oct | Mon 10 Oct | Tue 11 Oct | Wed 12 Oct | Thu 13 Oct | Fri 14 Oct | Sat 15 Oct | Sun 16 Oct | Mon 17 Oct | Tue 18 Oct | Wed 19 Oct | Thu 20 Oct | Fri 21 Oct | Sat 22 Oct | Sun 23 Oct | Mon 24 Oct | Tue 25 Oct | Wed 26 Oct | Thu 27 Oct | Fri 28 Oct | Sat 29 Oct | Sun 30 Oct
Week 39 40 41 42 43
Area T4 - H6
ATLAS AFP
CMS Outer Tracker D. Lazic
D. Dannheim
Clic pix
V. Manko
ALICE PHOS
A. Tauro, S. Vlachos
ALICE & ATLAS muons
ATLAS ITK
Mon 31 Oct | Tue 1 Nov | Wed 2 Nov | Thu 3 Nov | Fri 4 Nov | Sat 5 Nov | Sun 6 Nov | Mon 7 Nov | Tue 8 Nov | Wed 9 Nov | Thu 10 Nov | Fri 11 Nov | Sat 12 Nov | Sun 13 Nov | Mon 14 Nov | Tue 15 Nov | Wed 16 Nov | Thu 17 Nov | Fri 18 Nov | Sat 19 Nov | Sun 20 Nov | Mon 21 Nov | Tue 22 Nov | Wed 23 Nov | Thu 24 Nov | Fri 25 Nov | Sat 26 Nov | Sun 27 Nov | Mon 28 Nov | Tue 29 Nov | Wed 30 Nov | Thu 1 Dec | Fri 2 Dec | Sat 3 Dec | Sun 4 Dec
Week 44 45 46 47 48
Area T4 - H6
S. Vlachos
ATLAS ITK
M. Silari
XSEC

Summary and short-term plans

- Detected signal from passive diodes
  - still to fully understand depletion depth and rate
  - TCAD / Geant4 simulations (help welcome)
  - trying to organize irradiation tests (setup in development with Politecnico)

ATLAS TCAD workshop
CPPM, 11-12 May.

- Fixed KC53AB received:
  - all components are operational
  - gain lower than expected and large dispersion
  - still to understand mismatch between measurements and simulation
- Large pixel matrix to be submitted by mid-April
  - can be matched to FE-I4 chips
  - possibly also to RD53 prototype

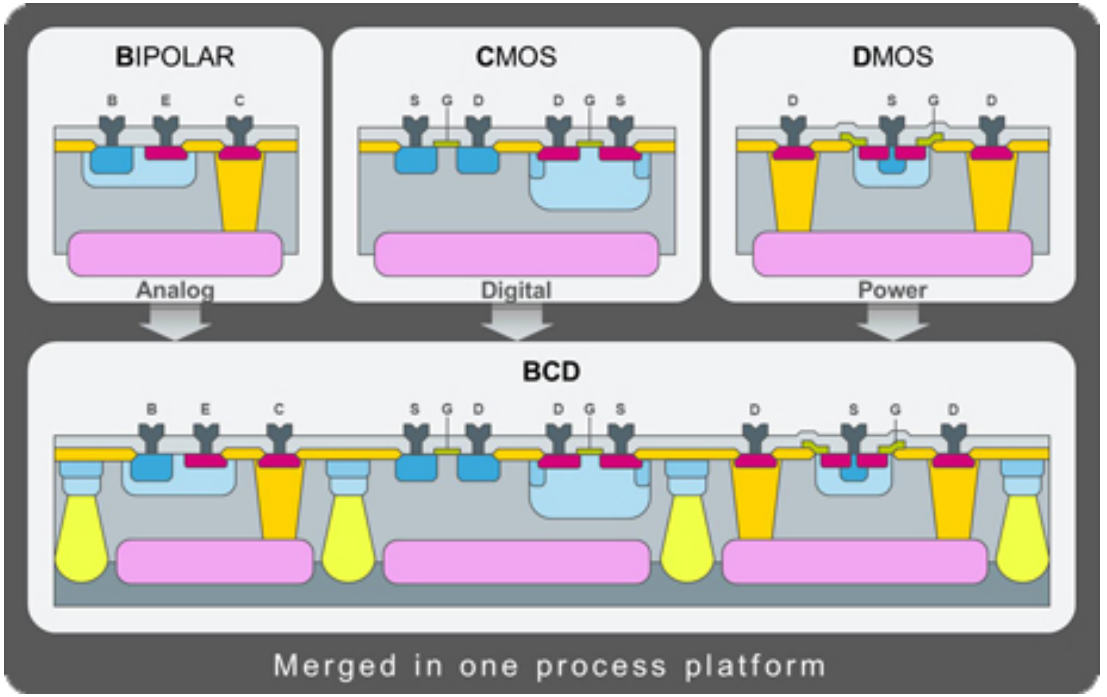


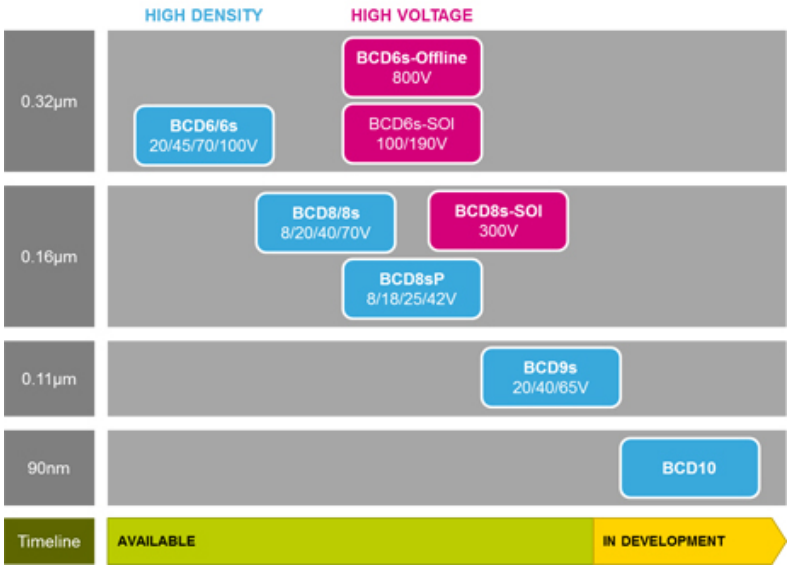
HVR - CCPD

BACKUP

BCD8 Technology STMicroelectronics

BCD = Bipolar + CMOS + DMOS





http://www.st.com/web/en/about_st/bcd.html

- Among the competing technologies BCD8 has several appealing features:
  - availability of different devices integrated in the same process
  - **epitaxial process**: can easily grow on different substrates.
  - possible to reach thick depletion layers: 30 µm looks an optimal compromise between signal and material thickness of the detector
  - **long-term availability**: it is one of the major production line for ST automotive products.

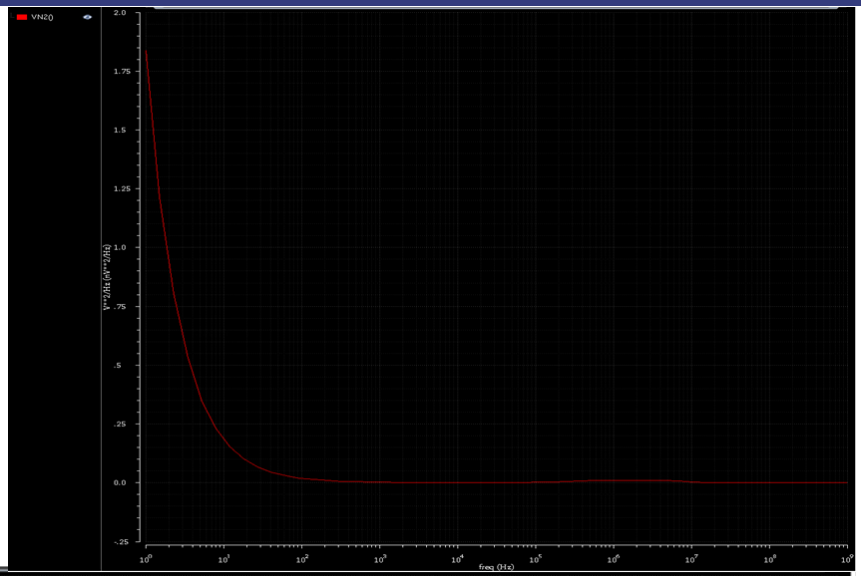
Noise performance

Device	Param	Noise Contribution	% Of Total
M30.m1	fn	0.00689093	26.71
M30.m1	id	0.00646208	23.48
M5.m1	id	0.00420071	9.92
M5.m1	fn	0.0036419	7.46
M41.m1	id	0.00333666	6.26
M41.m1	fn	0.00273693	4.21
M2.m1	fn	0.00238552	3.20
M1.m1	id	0.00235236	3.11
M3.m1	fn	0.0021559	2.61
M21.m1	id	0.00191197	2.06

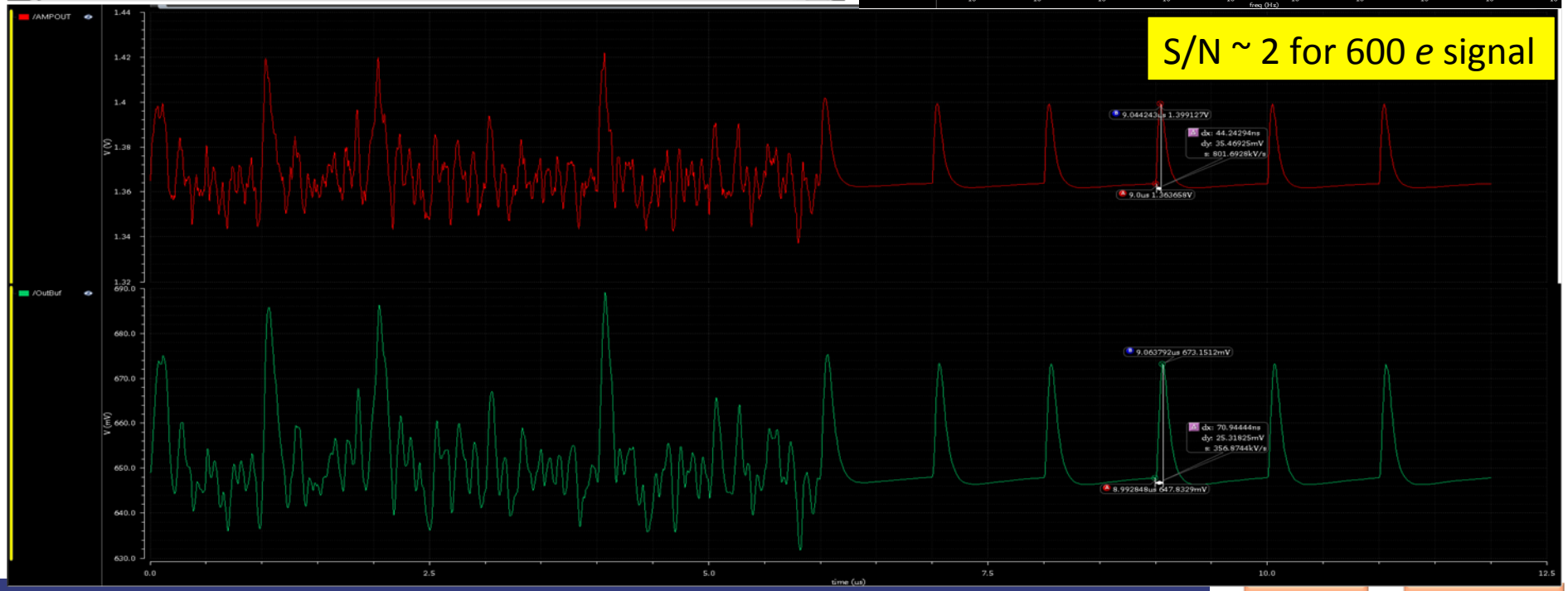
Integrated Noise Summary (in V) Sorted By Noise Contributors

Total Summarized Noise = 0.0133346

Total Input Referred Noise = 0.000239562 ⇐ =239uV ~ VIN



S/N ~ 2 for 600 *e* signal



CMP

- BCD8 now available also through CMP
  - easier to get new people started
  - increase of costs with respect to initial informal contacts:
    - 2600 Euro/mm^2 if Area ≤ 5 mm^2
    - 13000 Euro + [(Area-5) * 2100 Euro] if 5 mm^2 < Area < 15 mm^2