High density Indium bumps interconnection

ITK

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Current R&D with FBK/Selex

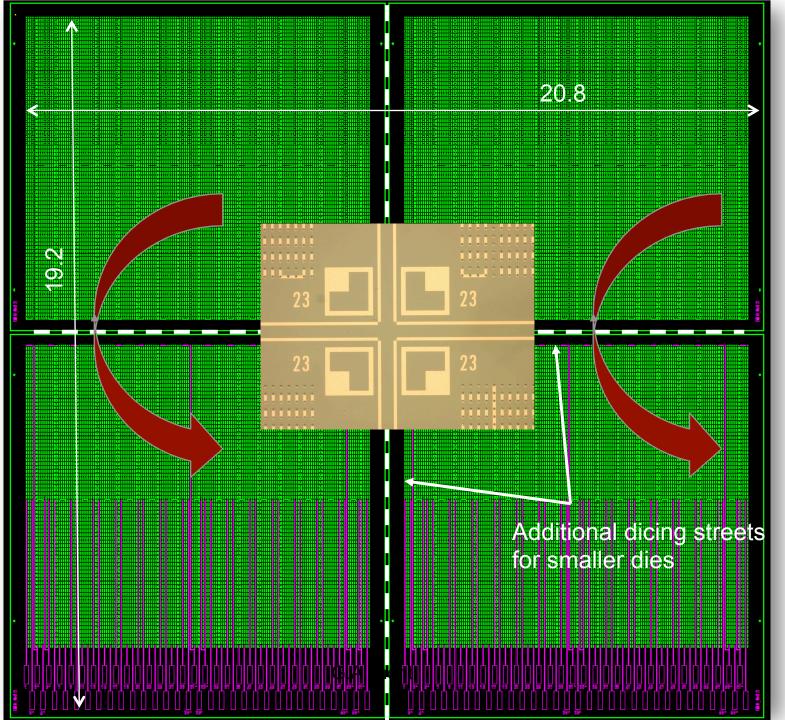
High density – High number of bumps

- 5x bump number of FE-I4 → 120 k-bumps/chip FE-I4 size
- Optimize process on dummies: bump height, bump size, pad and overglass opening geometry, temperature and pressure with resistive chains.
- Mechanical / electrical test on assemblies

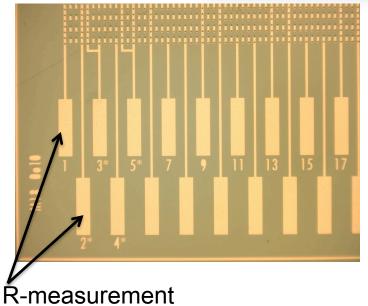
Bump deposition on 12-inch wafers

- wafers & deposition mask already procured
- test uniformity of vacuum deposition of bumps

FBK dummy wafers with resistive chains: 6-inch, 640μm thick wafers with 30 FE-I4 size dummy chips (or x4 10x10 mm) Metal pad: 18 and 20 µm Passivation open: 10 and 12 µm Indium bump size: 12 and 16 µm 120 k-bumps/chip, 21k bumps tested (124 chains with 172 bumps uniformly distributed over the chip surface) 16 μm diameter bumps 12 μm diameter bumps Credits: Alessandro Rovani INFN / Genova



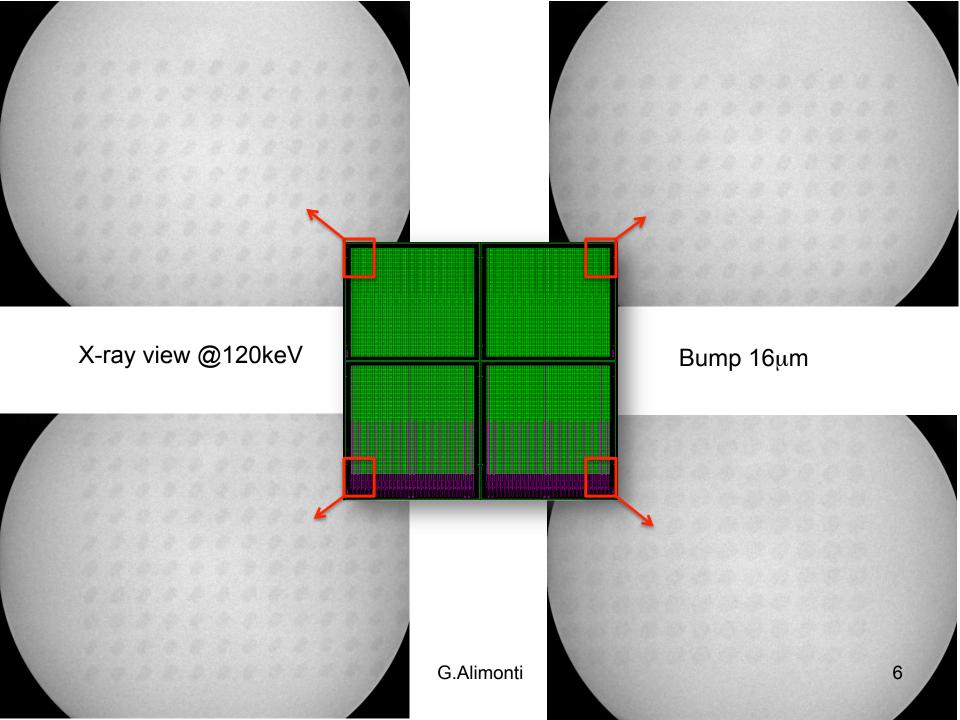
Front view before flipping

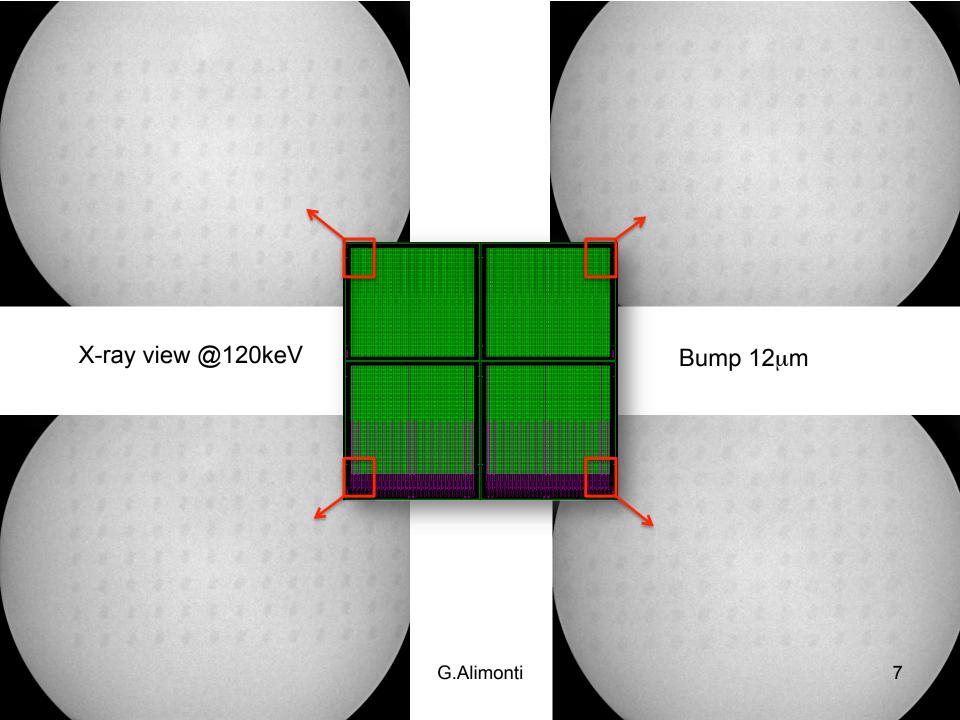


- Test 124 chains with 172 bumps in series.
- Must apply 150V (I_{max}=100μA) to break
 Indium oxide before R-measurement

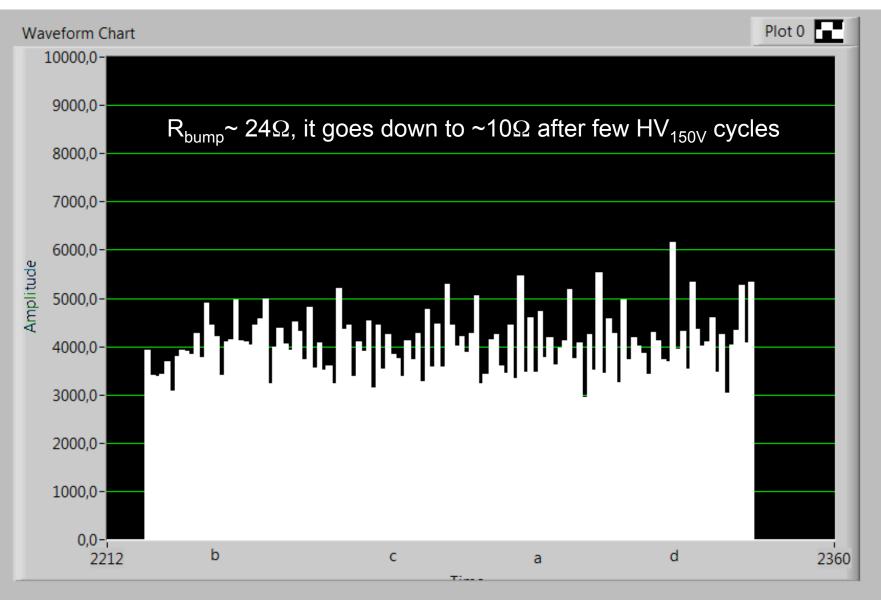
Mesurement pads here

Side view after flipping



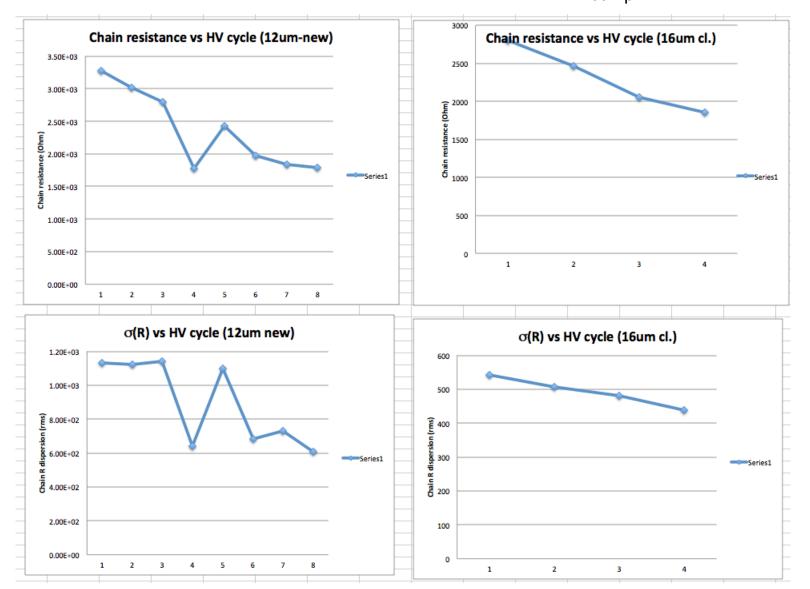


Resistance across each chain of 172 bumps (124 chains)



Indium oxide breaking done with 150V through the chain.

Repeated measurements optimize oxide breaking: $R_{\text{bump}} \text{~-} 10\Omega,\, \sigma(R)$ few Ω



Conclusions and next steps

Very promising results from first resistive chain tests:

- No open among 64k bumps (3 chips)
- No indication of shorts (either by x-ray or resistance measurements)
- Flip-chip planarity needs to be improved

More studies on:

- More modules planned with adjusted planarity
- Mechanical stress tests
- Bump deposition on 12" wafer ongoing now (to check bump uniformity)

Past experience with In BB at Selex

Selex assembled more than half of ATLAS Pixel detectors with Indium BB.

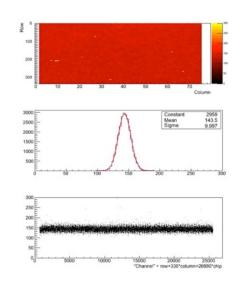
IBL did not use Indium bump modules, but:

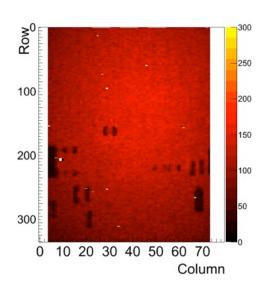
 A few modules have been successfully assembled with single chip planar and 3D sensors and 100 μm and 150 μm thick FE-I4 chip

ATLAS Insertable B-Layer (IBL), JINST 8 (2013), P01024.

Process uses low temperature (90°C vs 250°C) and chip support already provided by the pick-up tool (as glass substrate used by IZM)
 <u>Ref.</u>: G. Alimonti et al., Development of Indium bump bonding for the

32,00,1138.0





Americium source

