RD_FASE2: INFN-FBK Sensors

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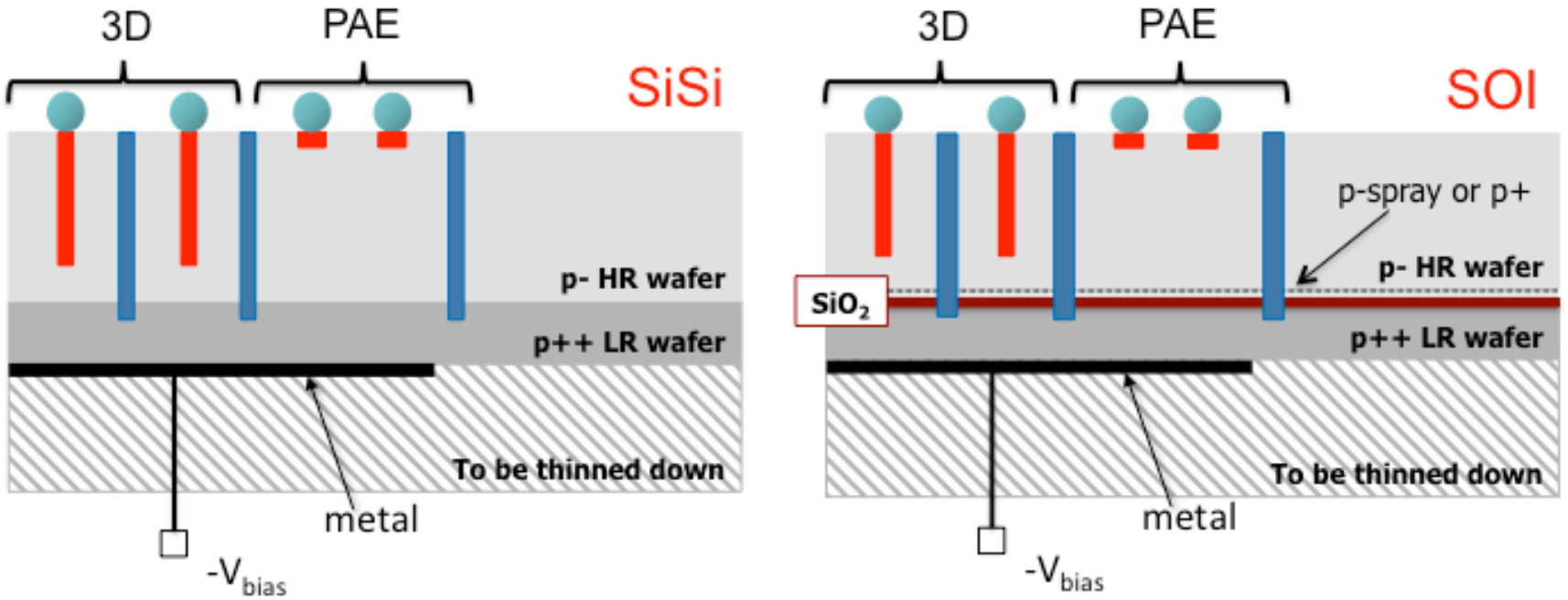
GOAL: development of new thin 3D and Planar Active Edge (PAE) pixel sensors on 6" p-type wafers at FBK:

- Technology and design to be optimized and qualified for extreme radiation hardness ($2x10^{16}$ n_{eq} cm^{-2})
- Pixel layouts compatible with present (for testing) and future (RD53 65nm) FE chips of ATLAS and CMS

Strong sinergy with WP7 of AIDA2020

New single-side approach to 3D/PAE



- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~5 um
- Holes (at least partially) filled with poly-Si

Process Tests

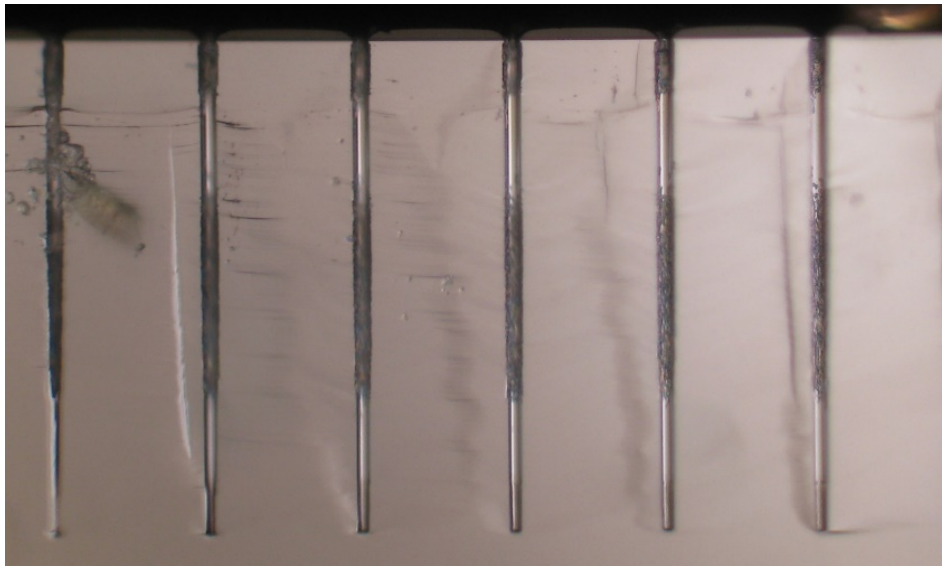
Etching test p-columns

S. Ronchin, FBK

p-holes > 130 µm

70’ SDE+10’ HER

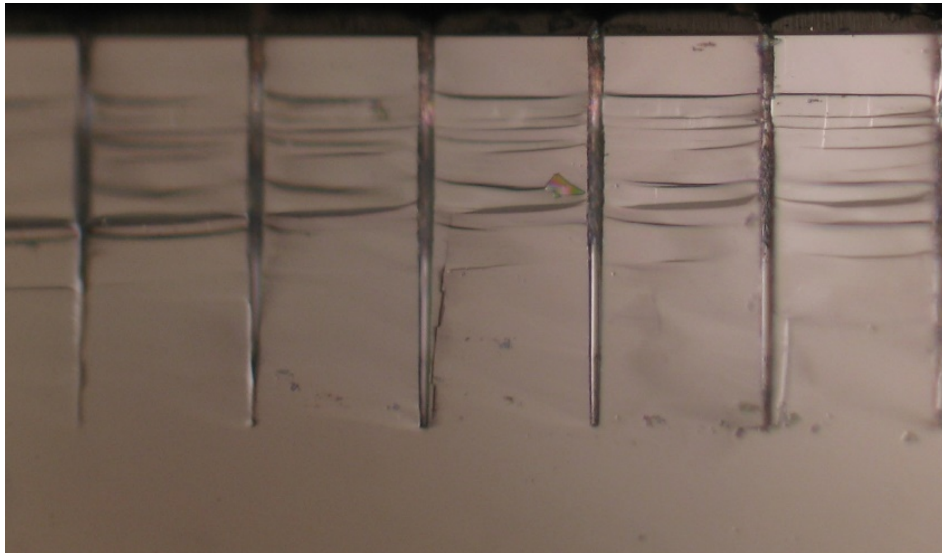
Position	depth (um)	Width at top	Width at bottom
c	**160**	5.3	4.0
t	159	5,5	2.25
f	156	5,8	3.2
dx	157	5, 5?	2.9
sx	**155**	4.85	2.6



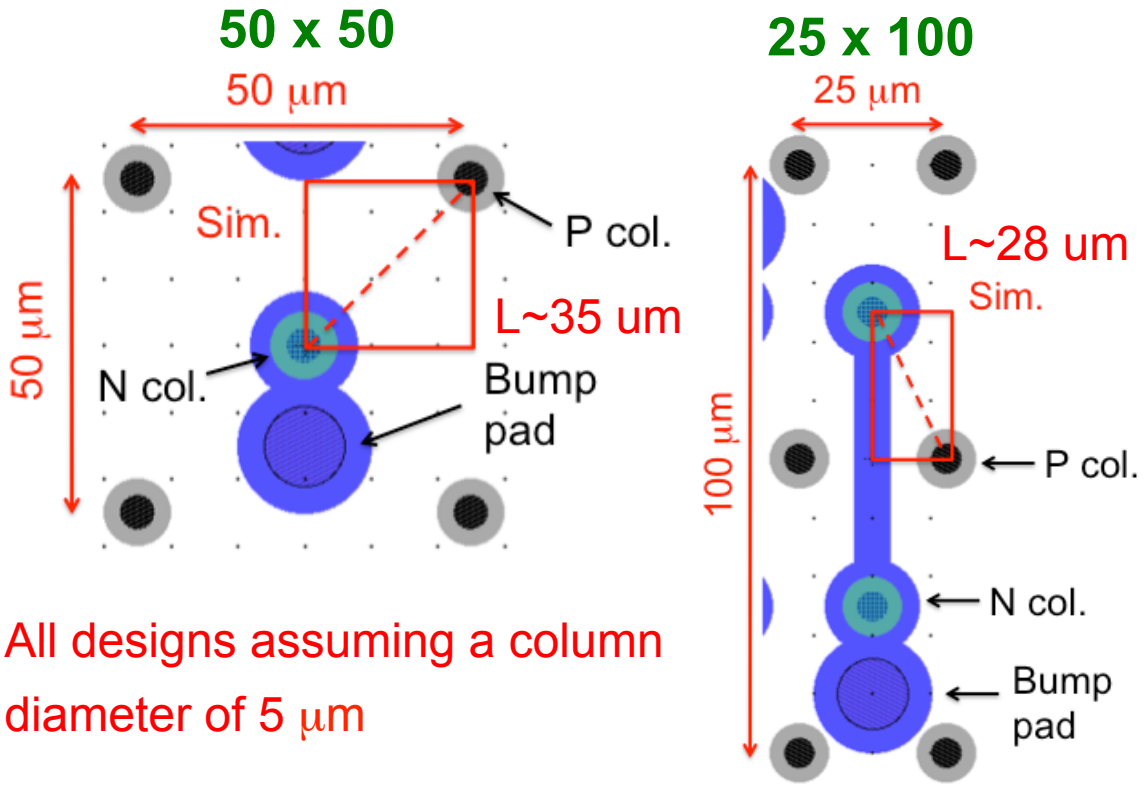
p-holes > 100 µm

43’ SDE + 10’HER

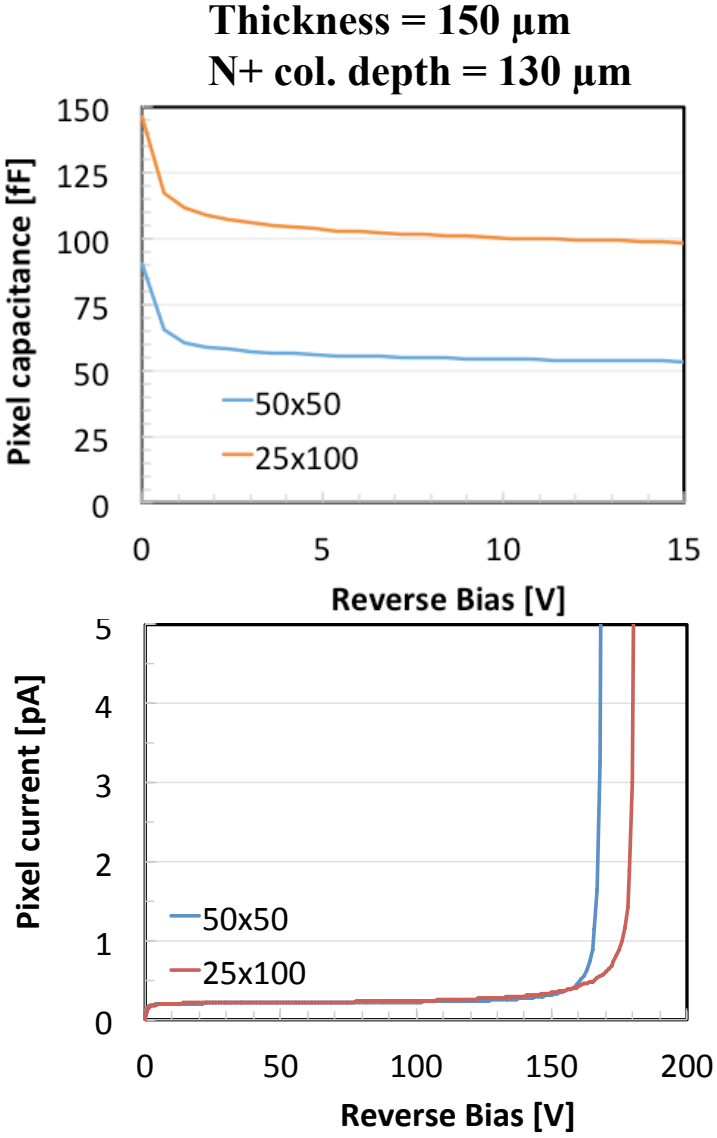
Position	depth (um)	Width at top	Width at bottom
c	**117**	4,7	3,2
t	117	4,4	3,2
f	114	4,7	3,2
Dx	115	5,2	3,2
Sx	**114**	4,8	2.4



New 3D pixels: design and simulations



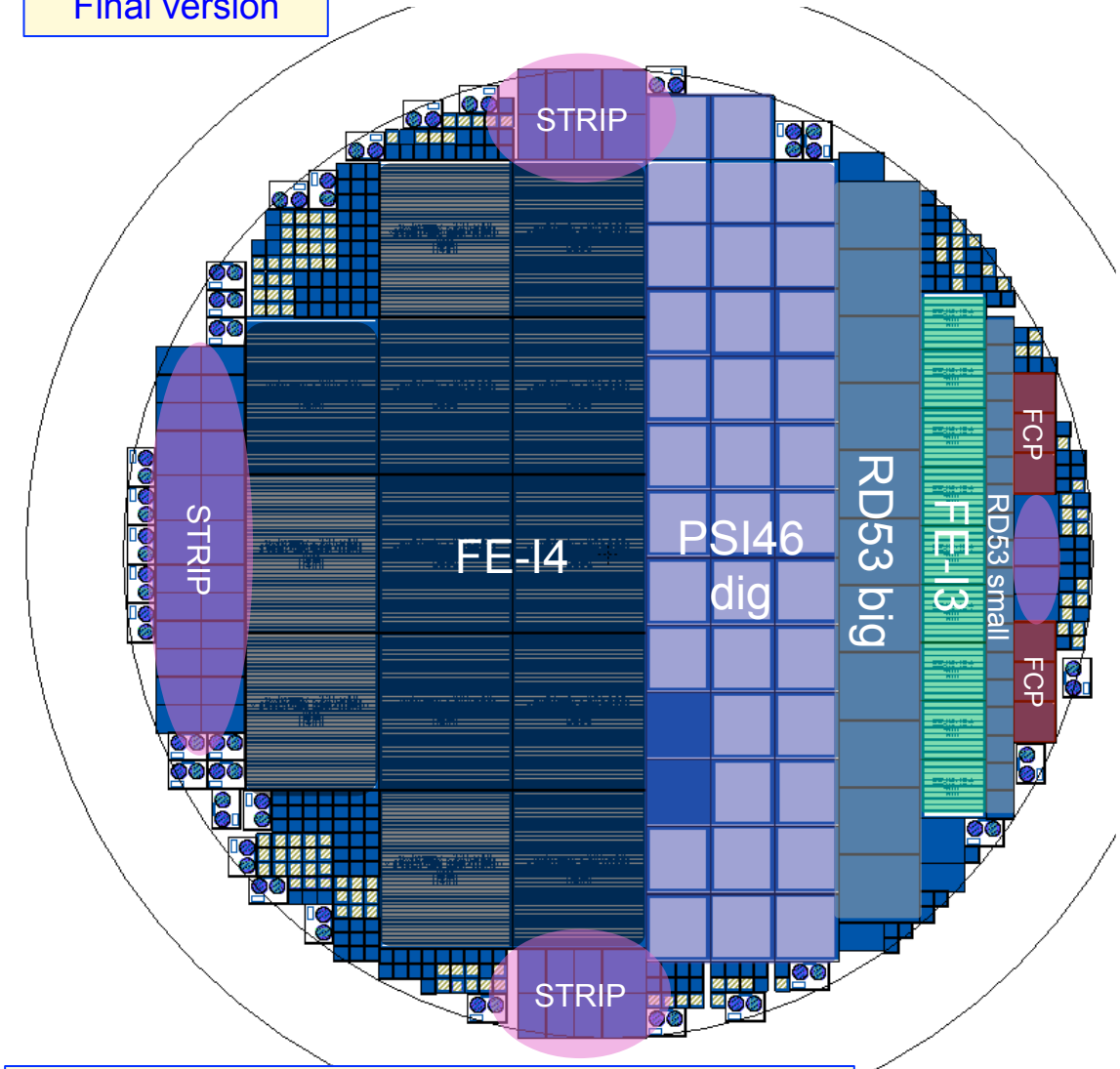
All designs assuming a column diameter of 5 µm



- 50x50 design safe, 25x100 is difficult … too little clearances (new ideas for bump pad to be tested)
- Capacitance compatible with RD53 specs
- Initial breakdown voltage high enough

3D Pixel Wafer Layout

Final version



+ Test structures (strip, diodes, etc)

Many different pixel geometries and pitch variations:

- FE-I4
  - 50 x 250 (2E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
  - 25 x 500 (1E)
- FE-I3
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- PSI46dig
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E and 2E)
  - 50 x 100, 100 x 100 (2E + 4E)
  - 50 x 100, 100 X 150 (2E + 6E)
  - 25 x 100 (1E and 2E)
- FCP
  - 30 x 100 (1E)
- RD53
  - 50 x 50 (1E)
  - 25 x 100 (1E)
  - 25 x 100 (2E)

Fabrication status at FBK

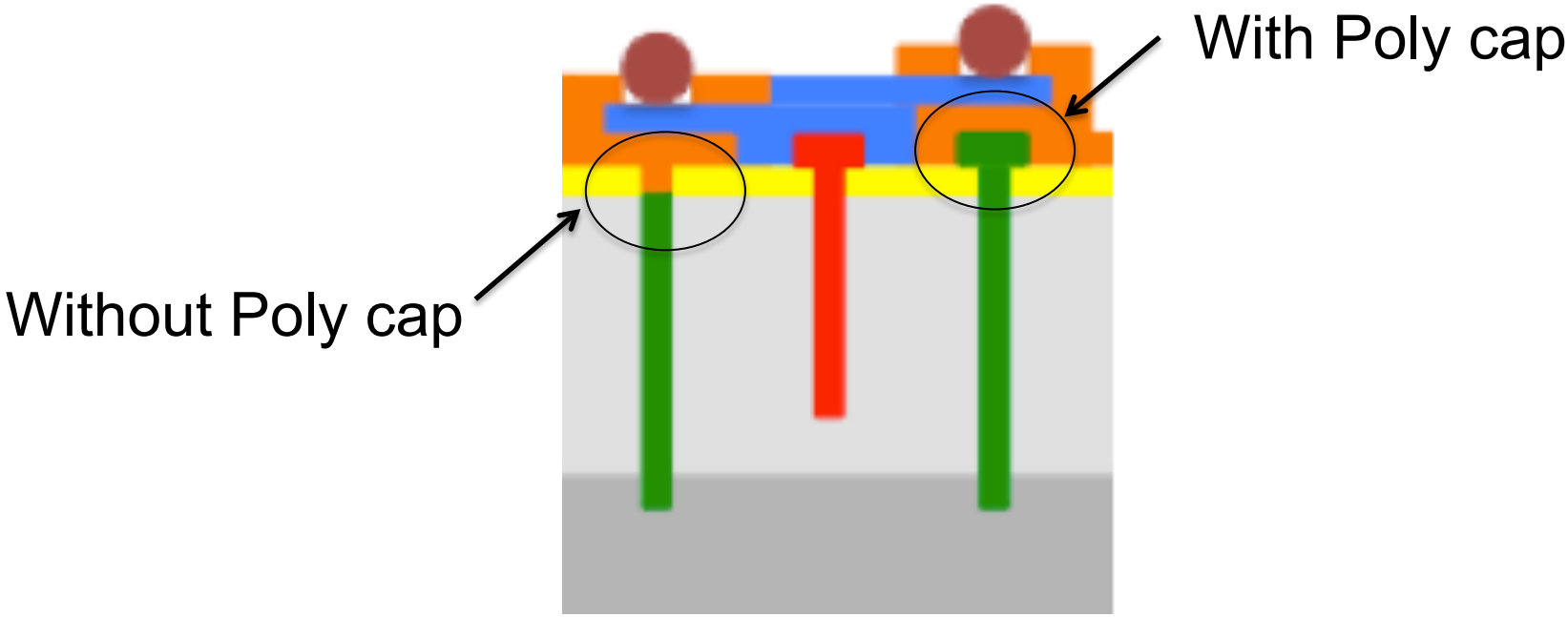
- First 3D batch (15 SiSi DWB wafers) aborted at the end of October 2015 due to problem with Boron doping of ohmic columns
- Four wafers (3D_rec) completed anyway to check all relevant process steps
- A new 3D batch (10 SiSi DWB wafers) re-launched in November 2015, now completed
- First electrical measurements performed on three wafers, results promising
- Now waiting for automatic I-V testing on all sensors

Process splits

Two active thicknesses, w. and w/o poly "cap"

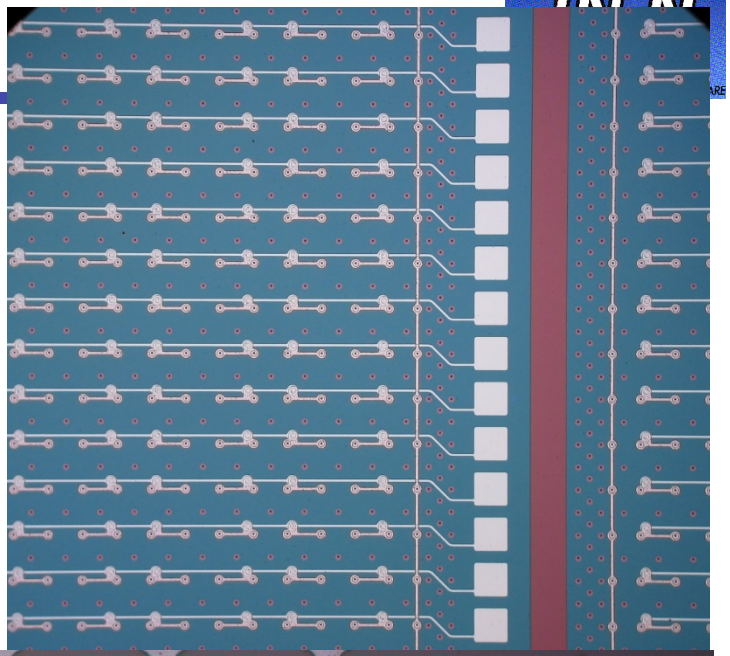
- 3 wafers 100μm thick, p-columns with poly "cap"
- 2 wafers 100μm thick, p-columns without poly "cap"
- 3 wafers 130μm thick, p-columns with poly "cap"
- 2 wafers 130μm thick, p-columns without poly "cap"

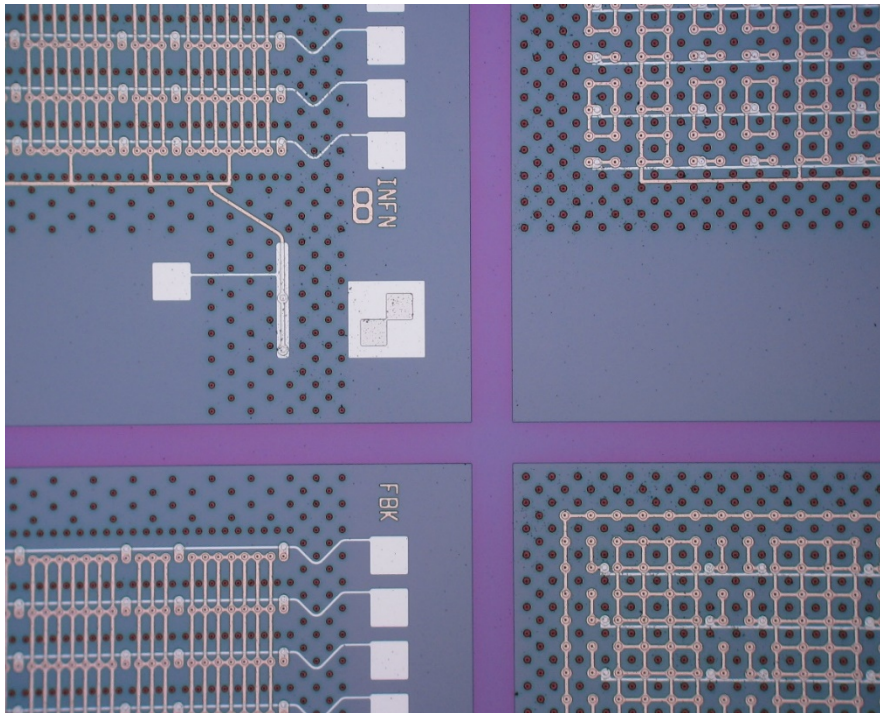
  (one broken at the end!)

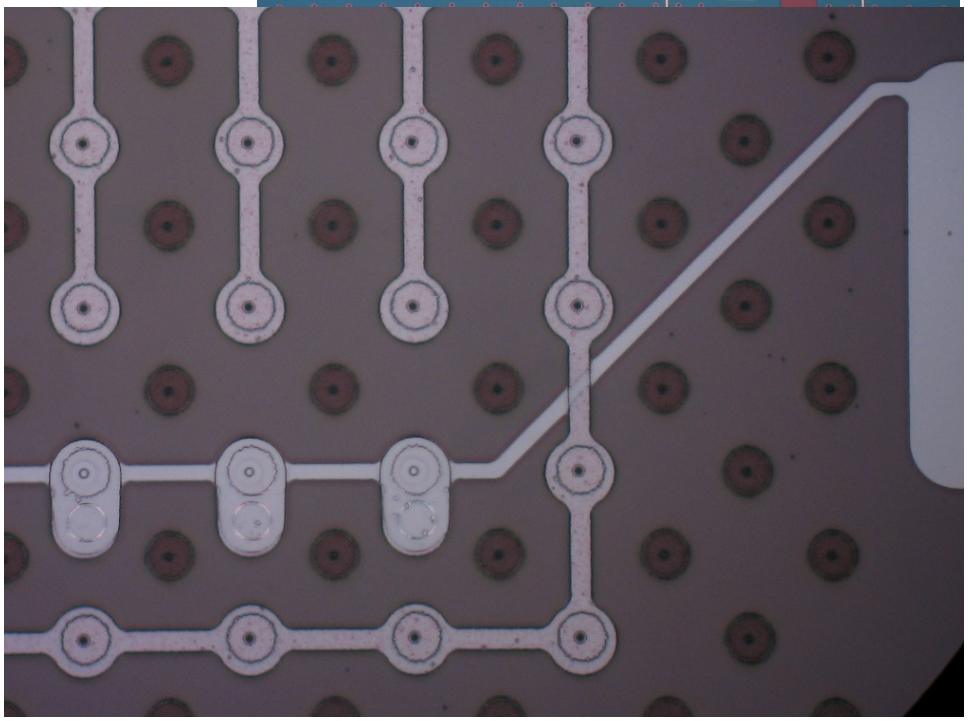


A few pictures

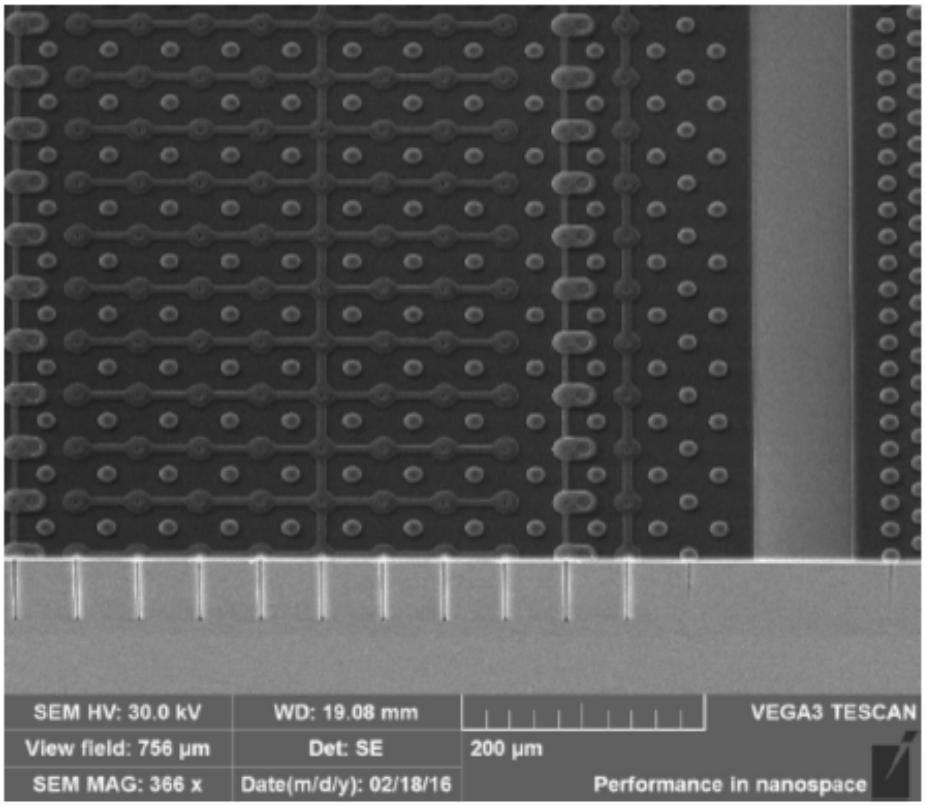
- Wafers with temporary metal
- Good lithographical quality

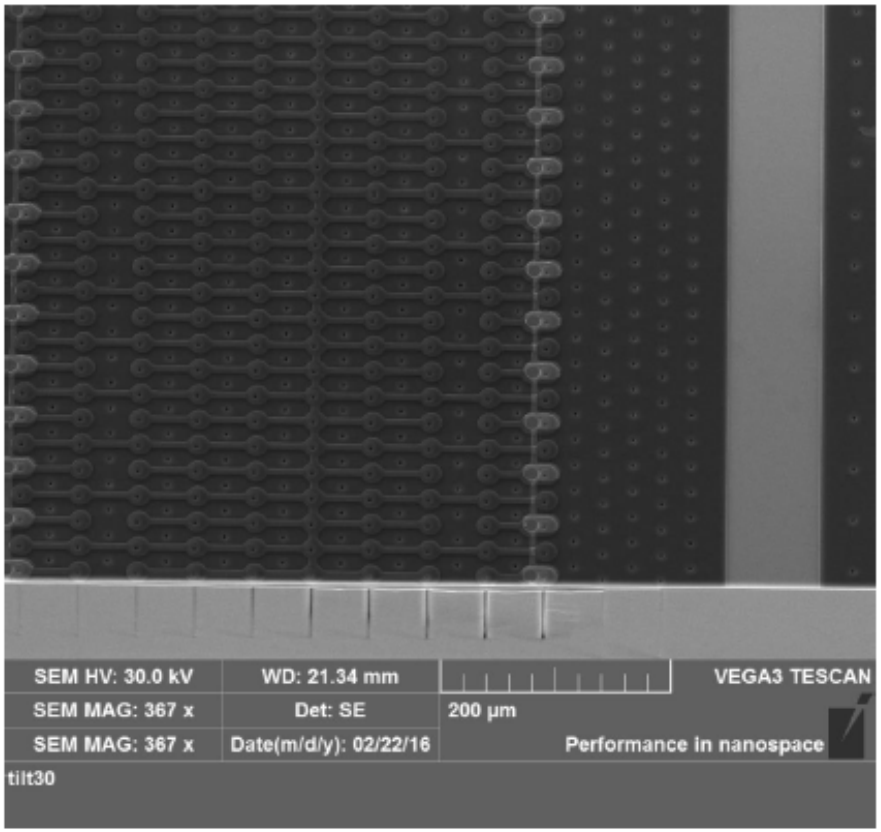




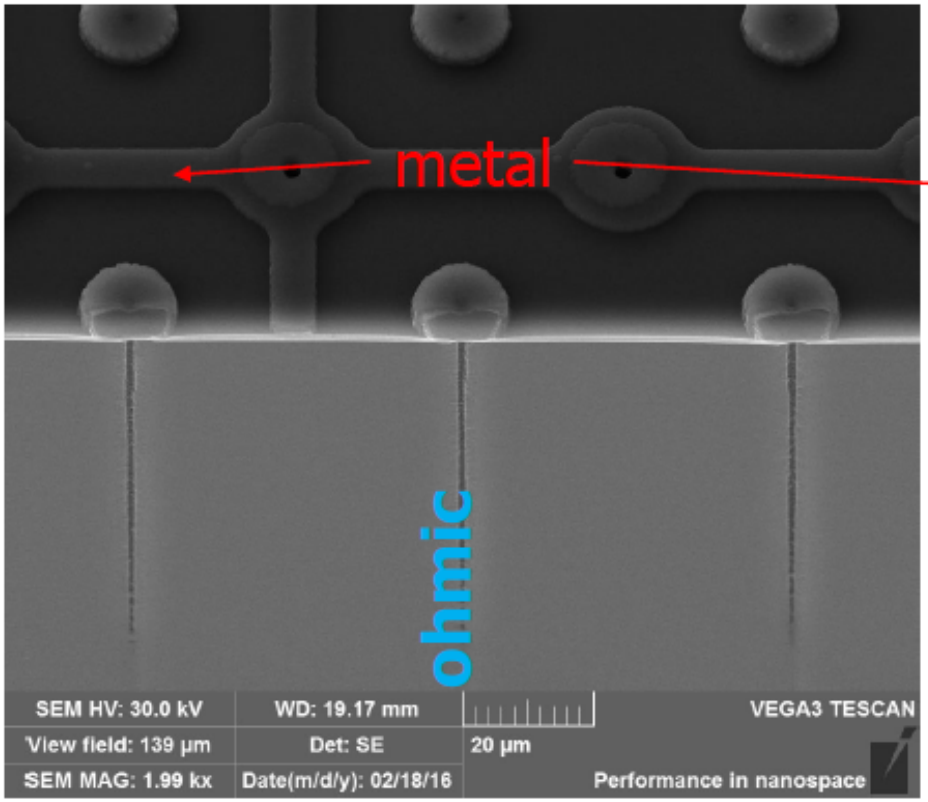


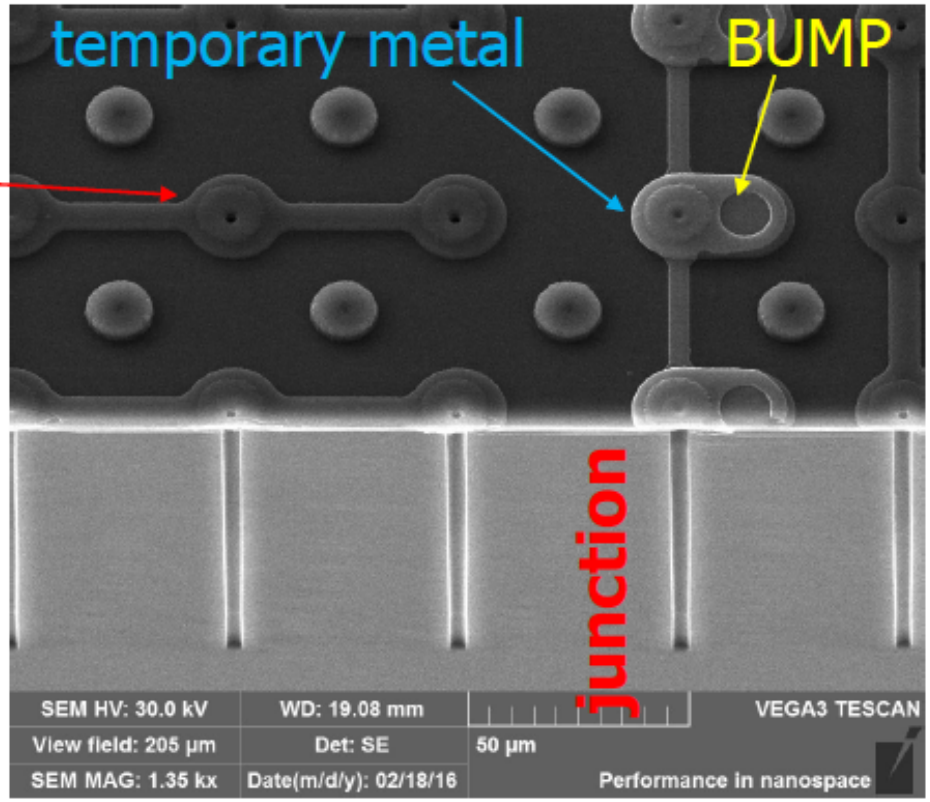
SEM pictures (1)



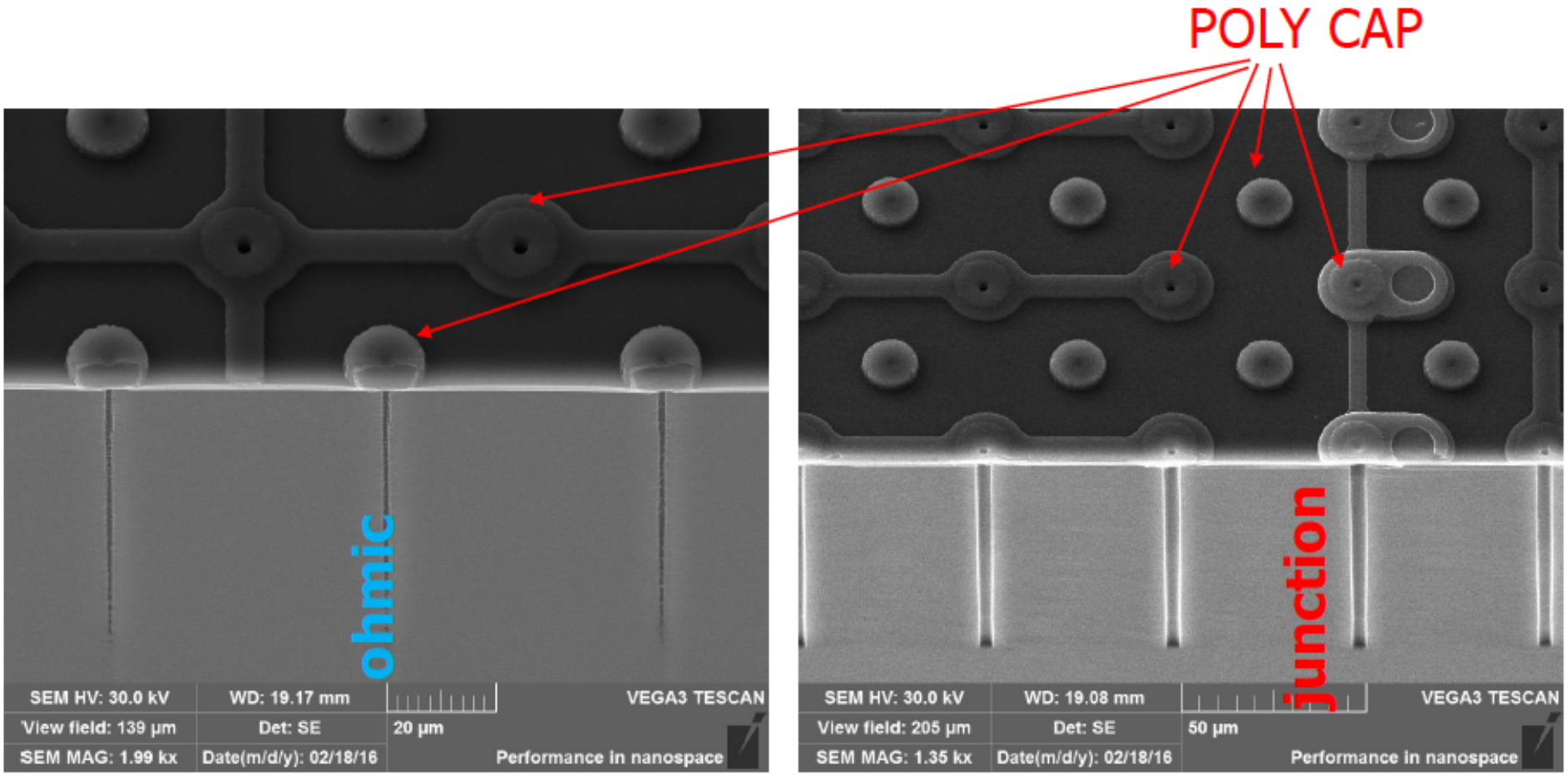


SEM pictures (2)

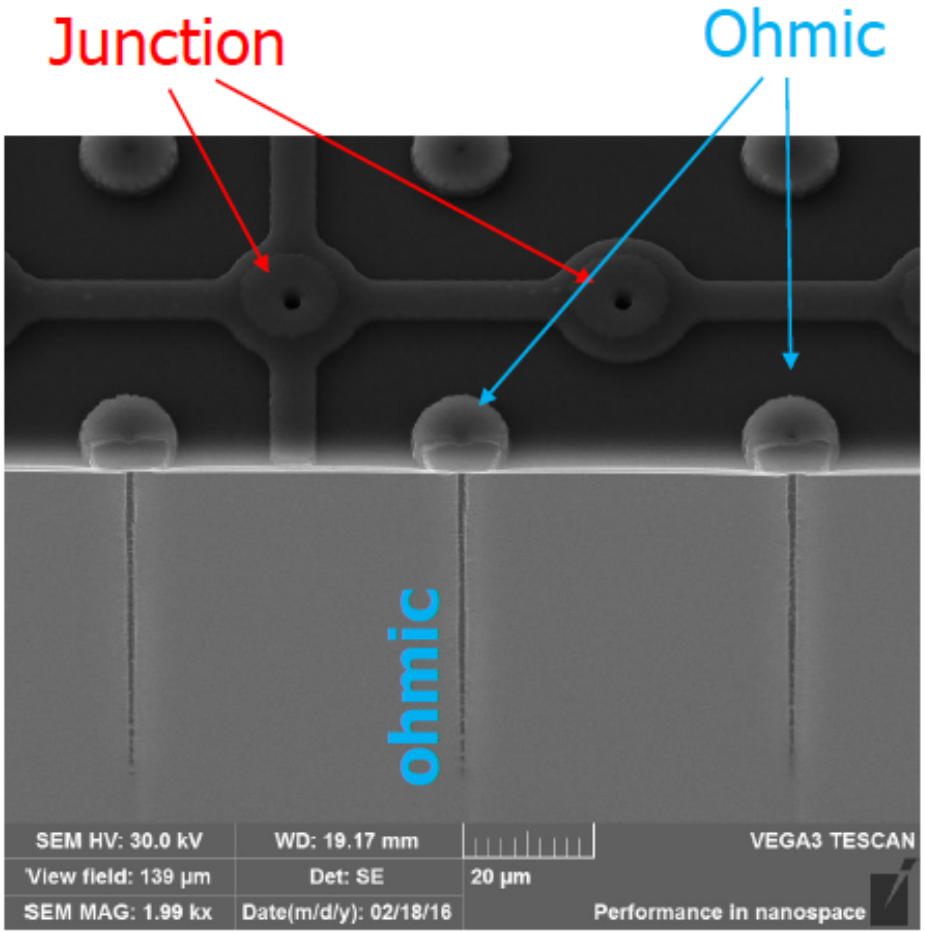


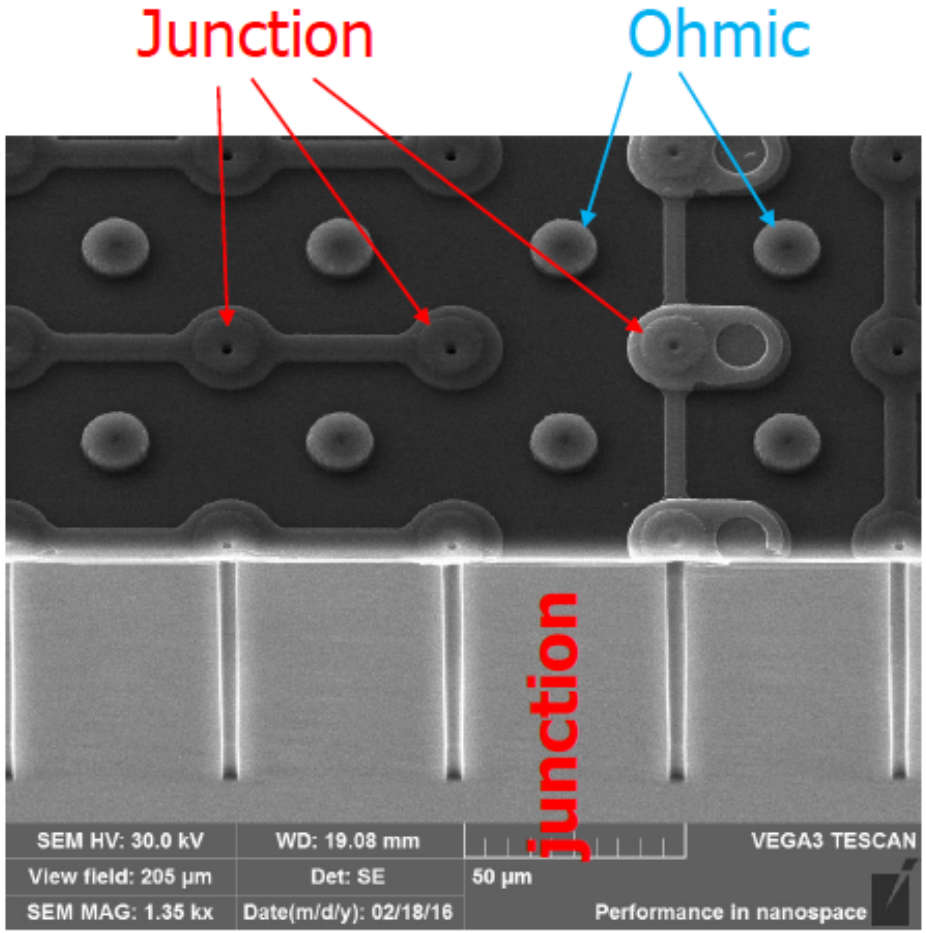


SEM pictures (3)



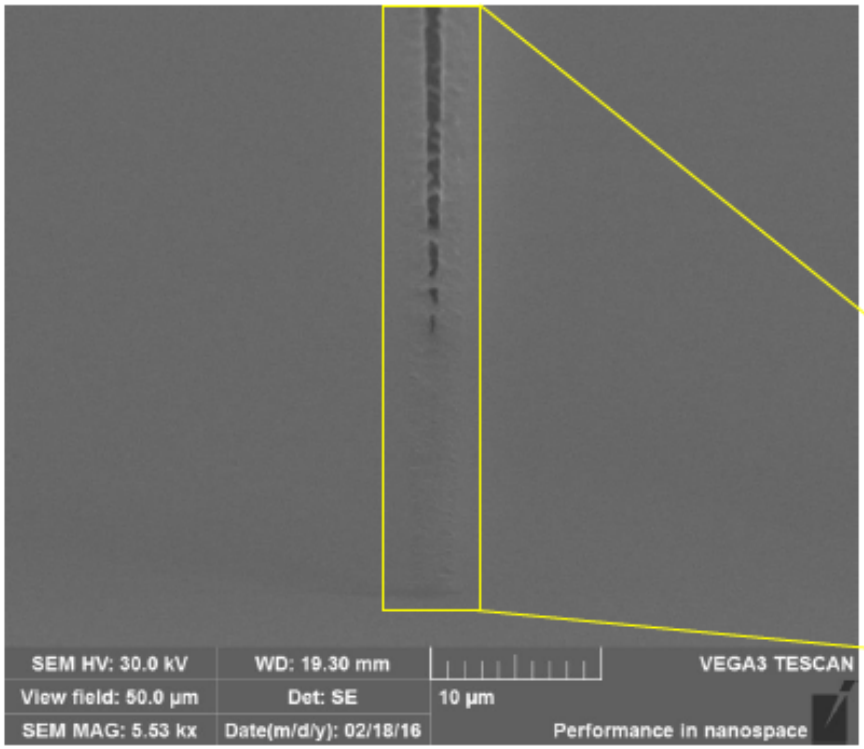
SEM pictures (4)

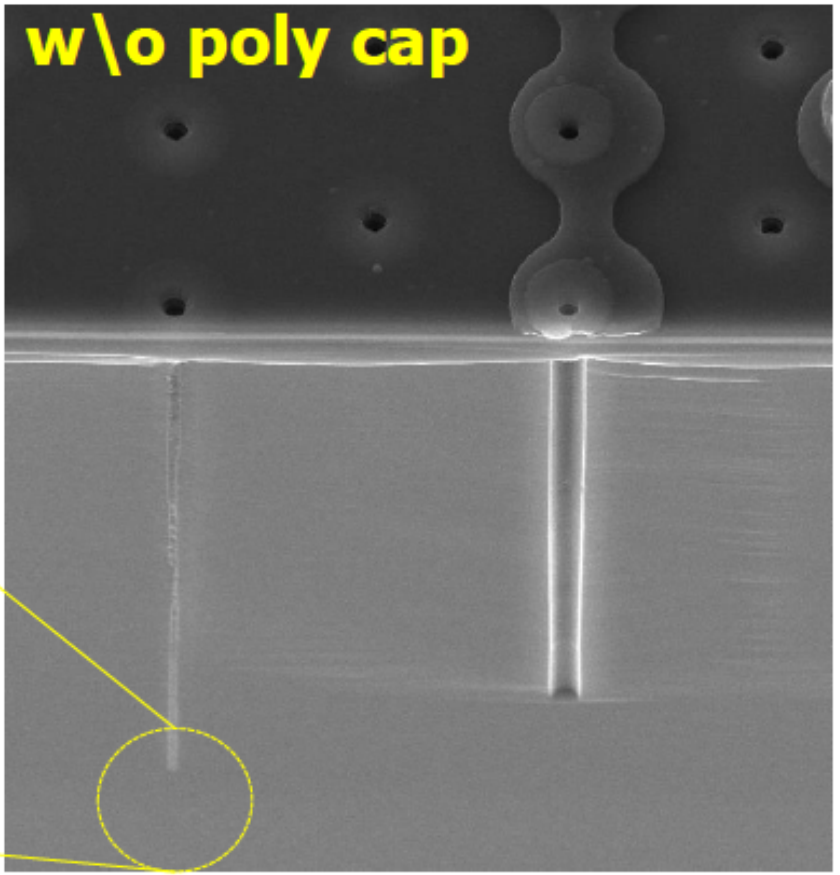




SEM pictures (5)

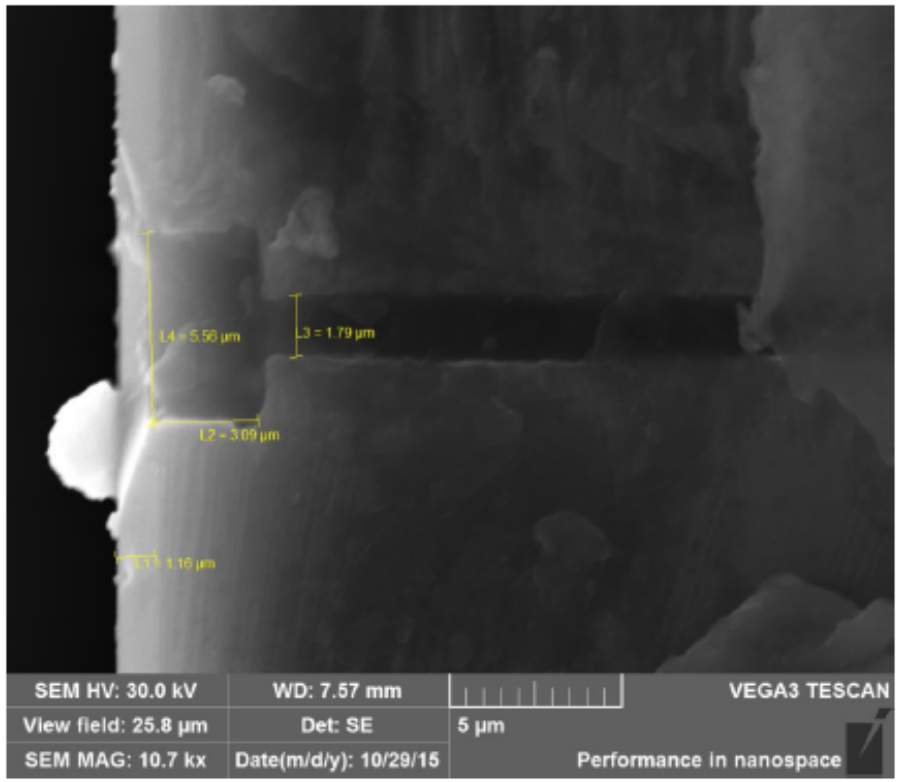
Filled (partially) with polysilicon



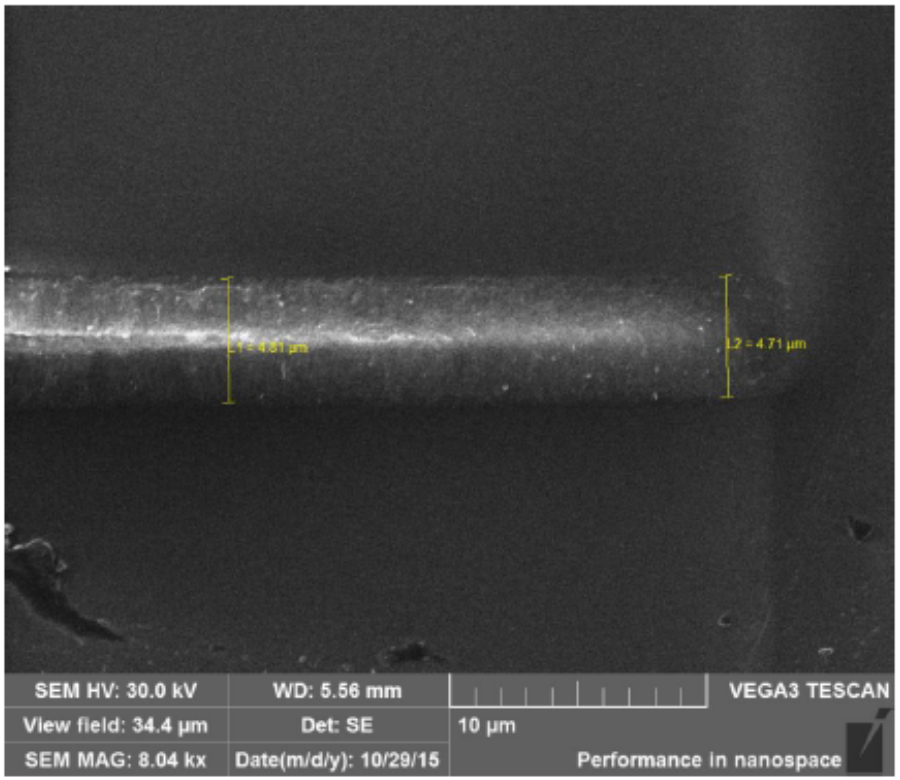


SEM pictures (6)

w/o poly cap



Column opening

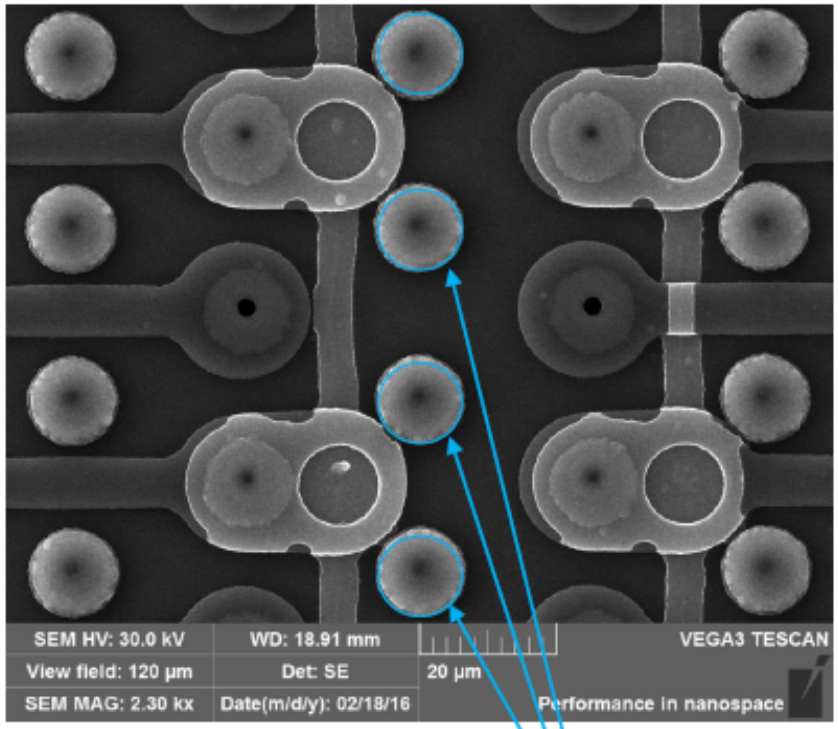


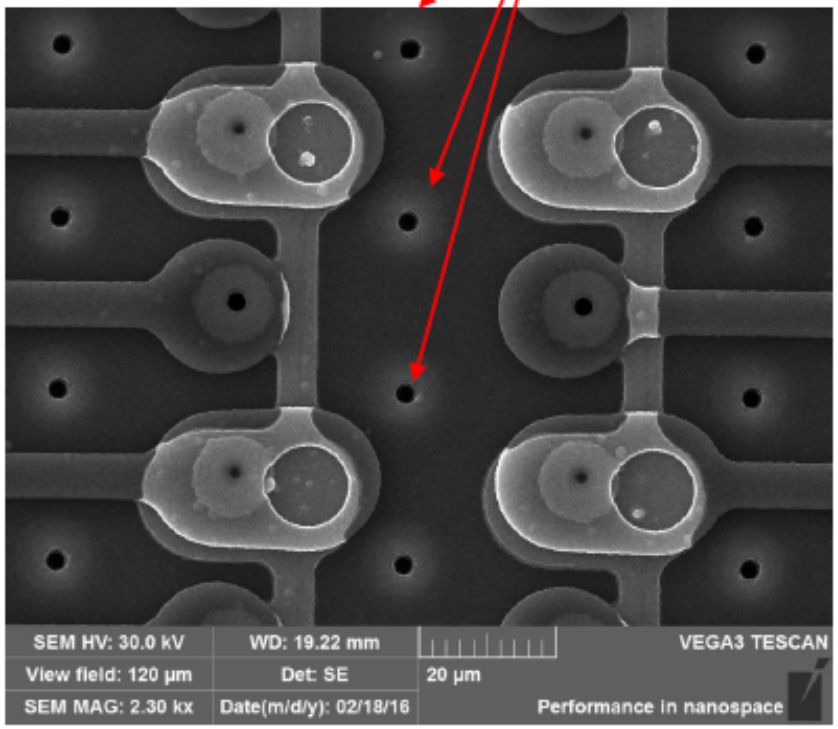
Column end

SEM pictures (7)

On test wafer: bad alignment

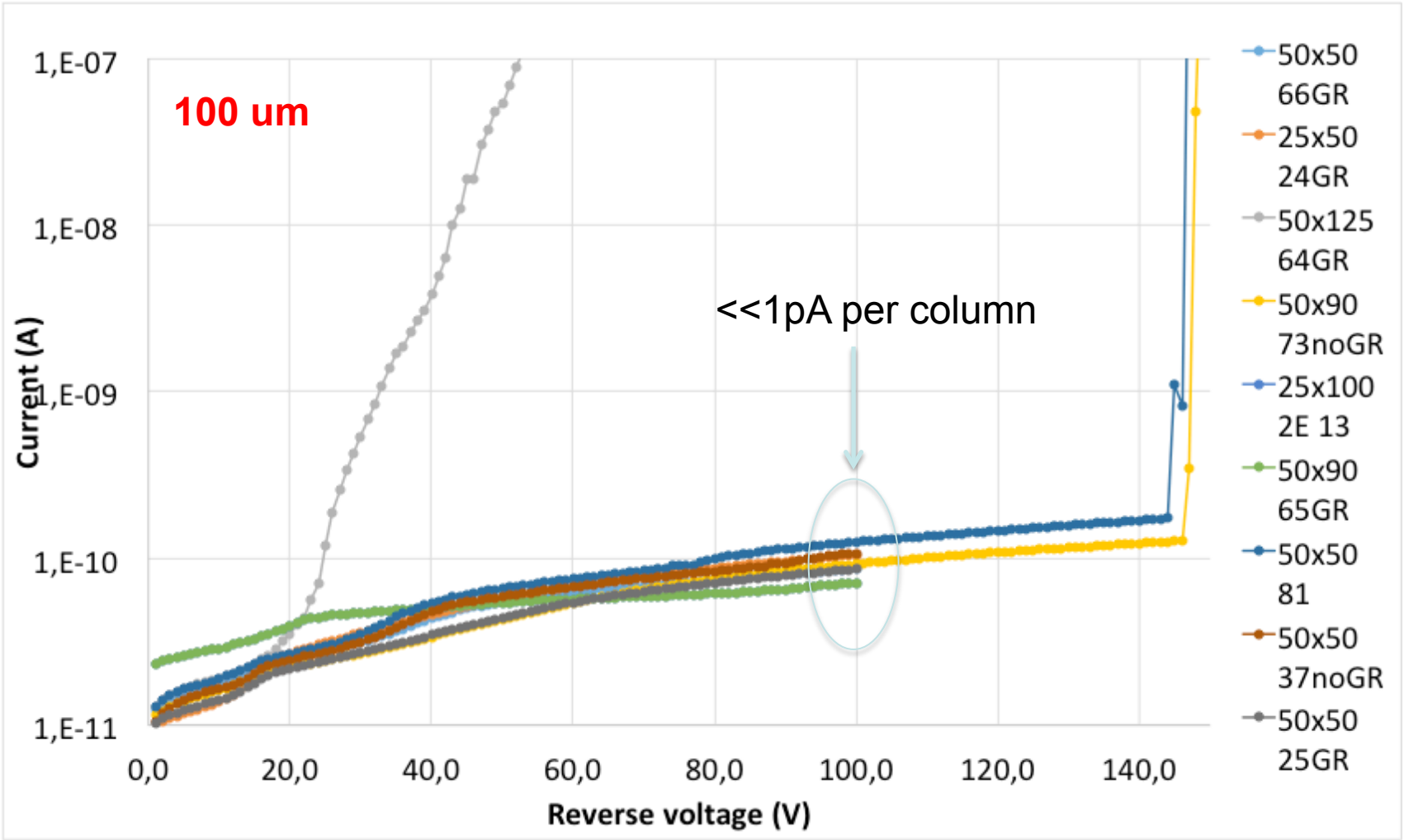
without poly cap



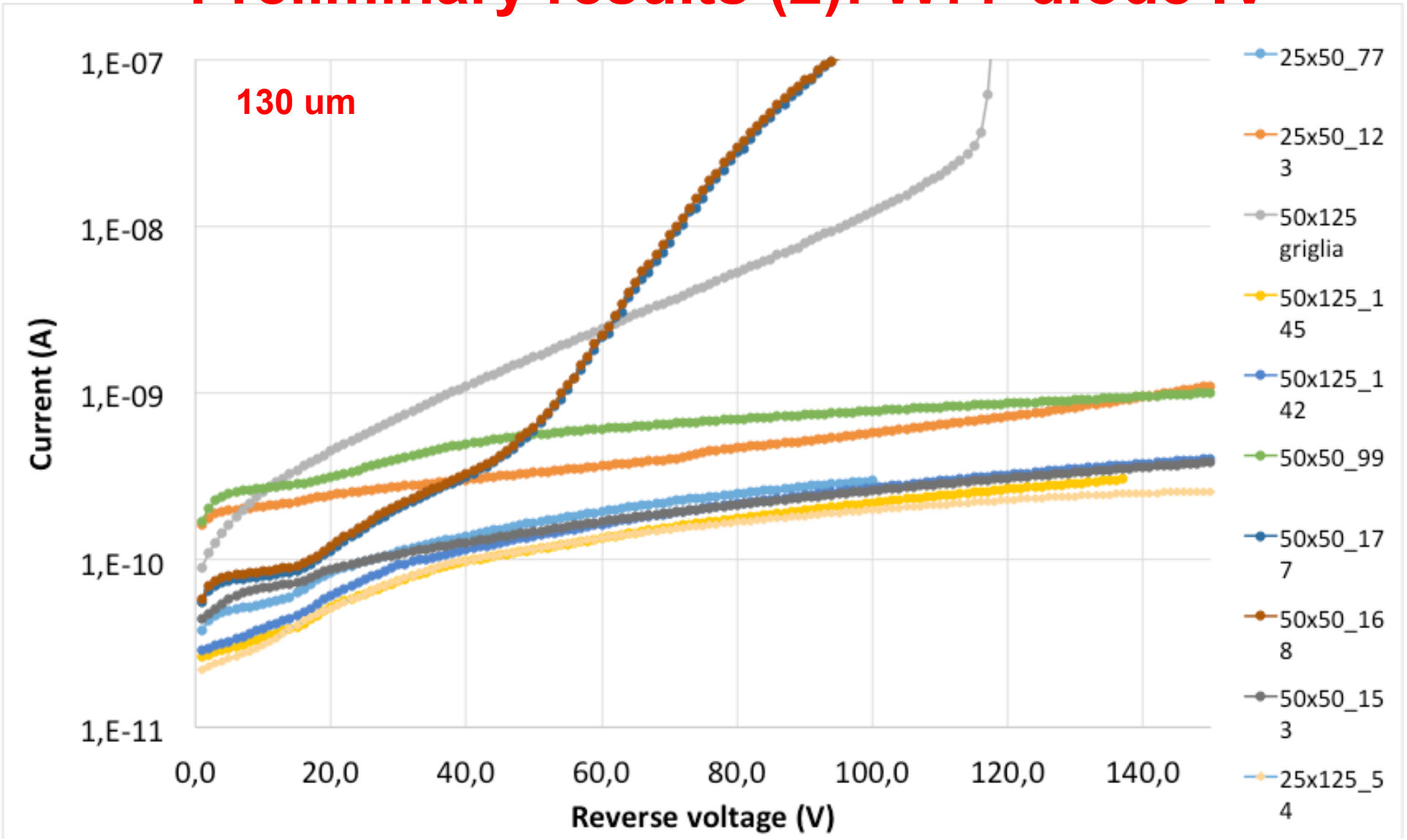


with poly cap

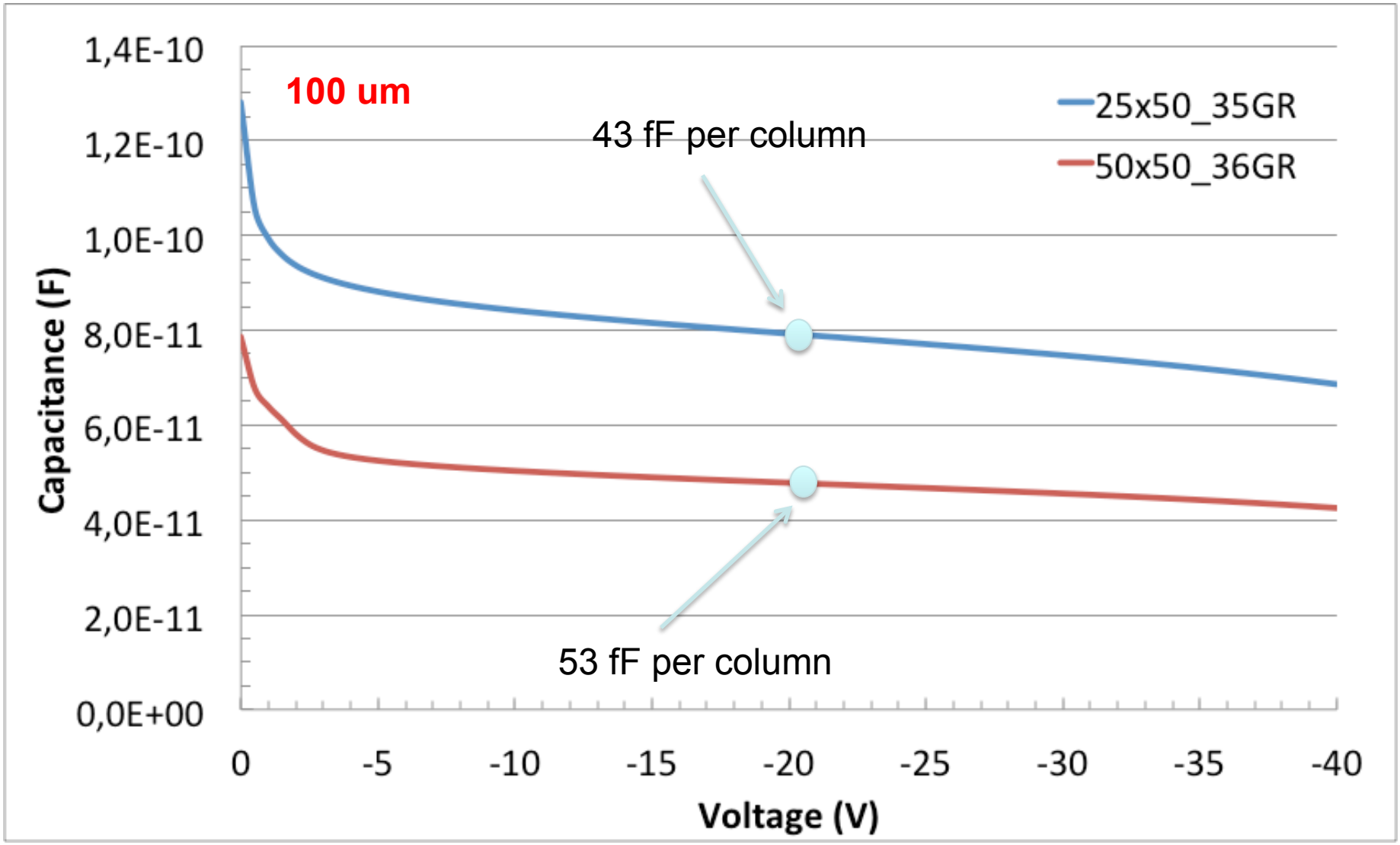
Preliminary results (1): W48 diode IV



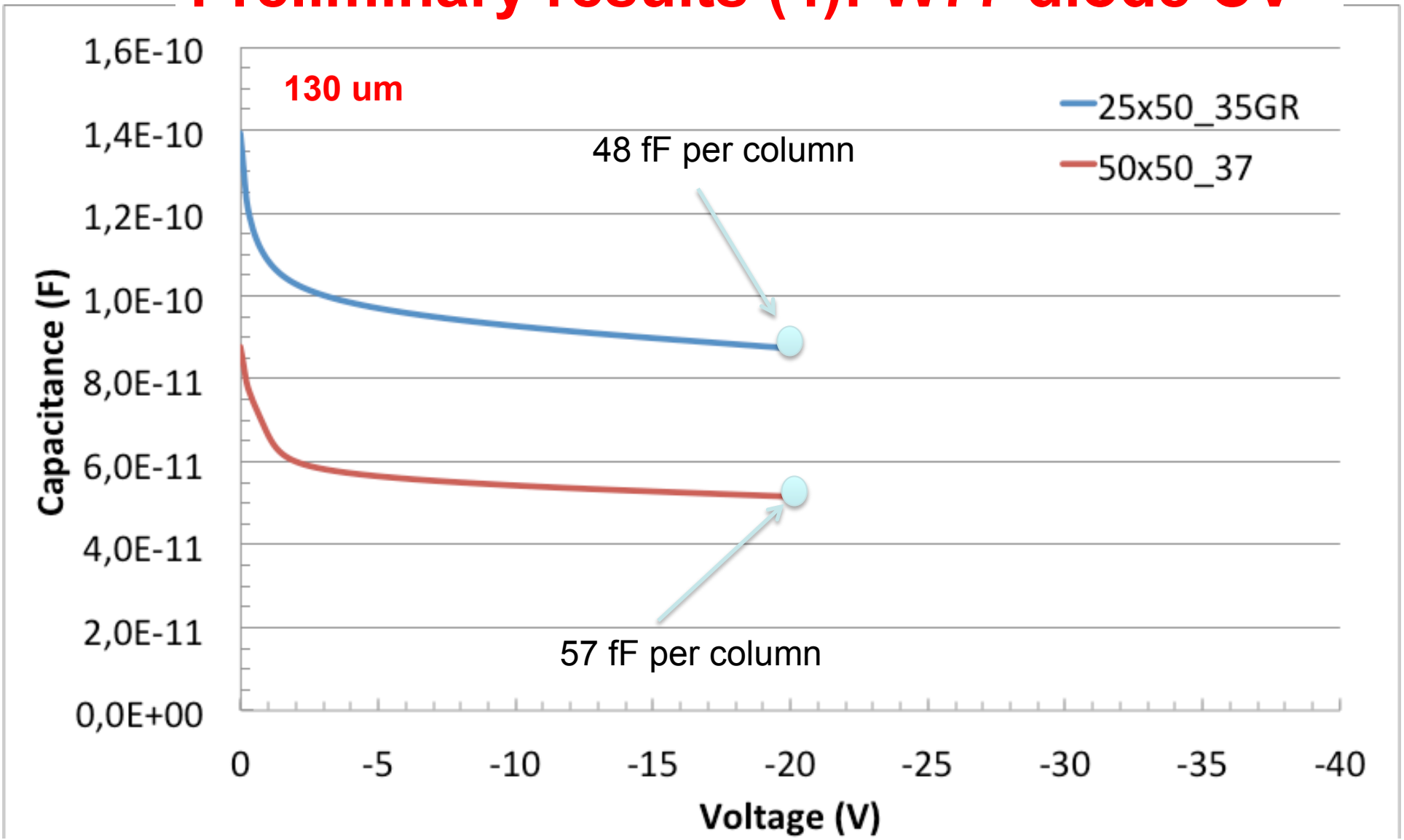
Preliminary results (2): W77 diode IV



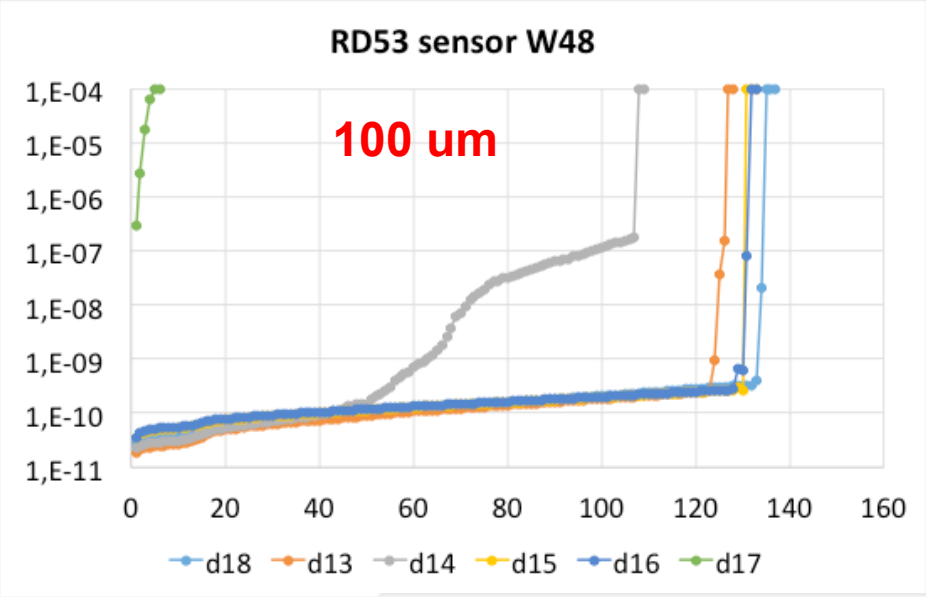
Preliminary results (3): W48 diode CV

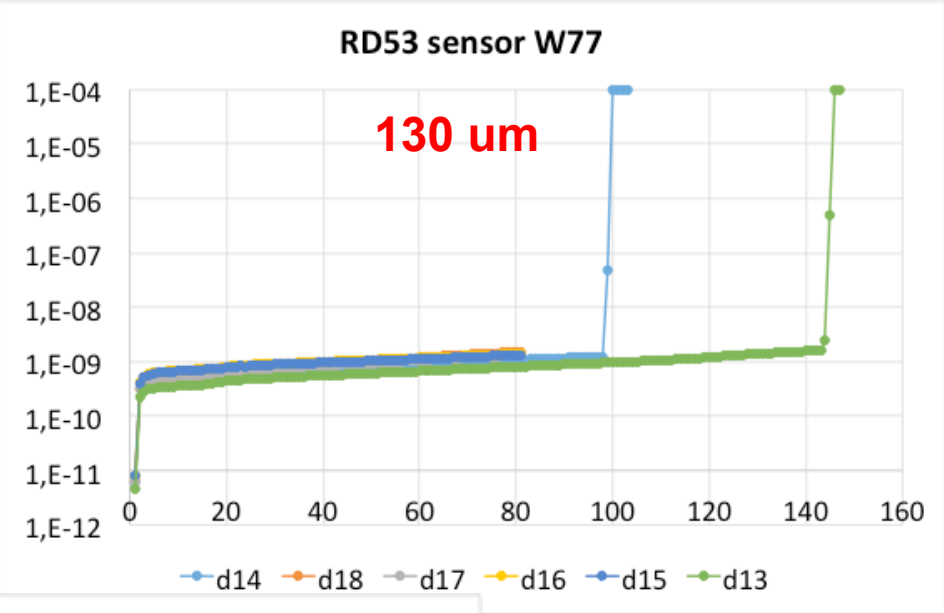


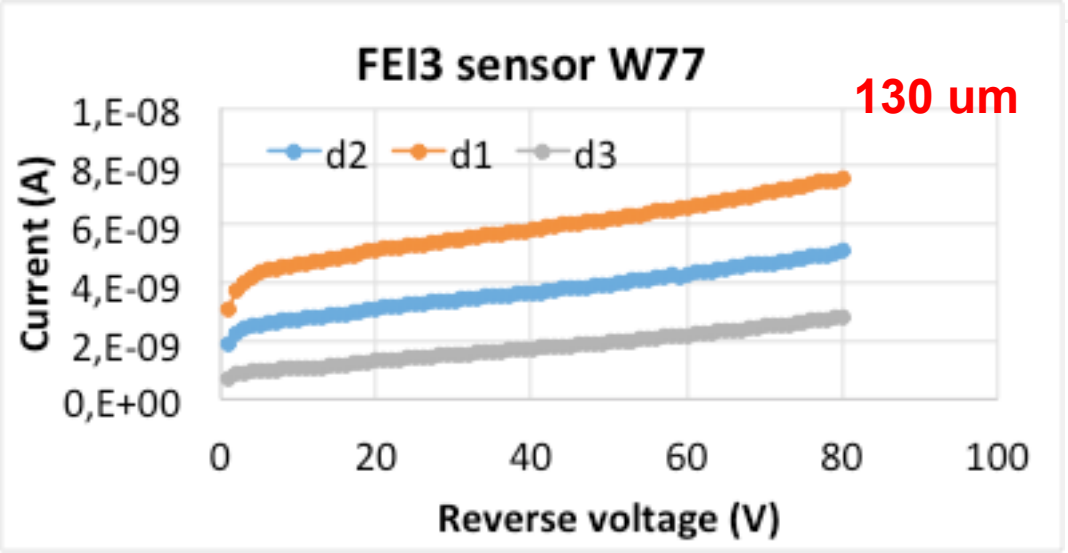
Preliminary results (4): W77 diode CV



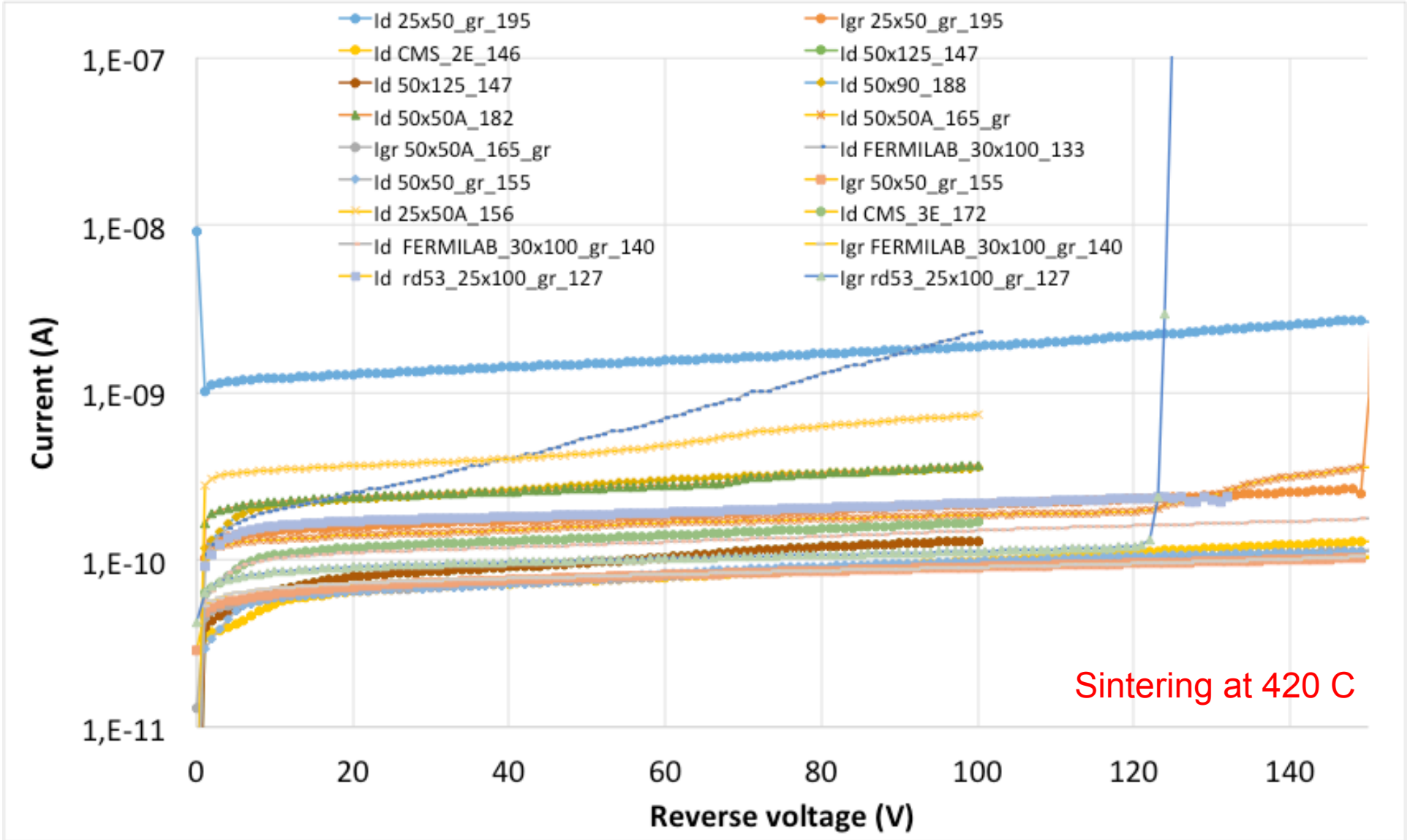
Preliminary test results (5): sensor IV







Preliminary results (6): Wxx diode IV



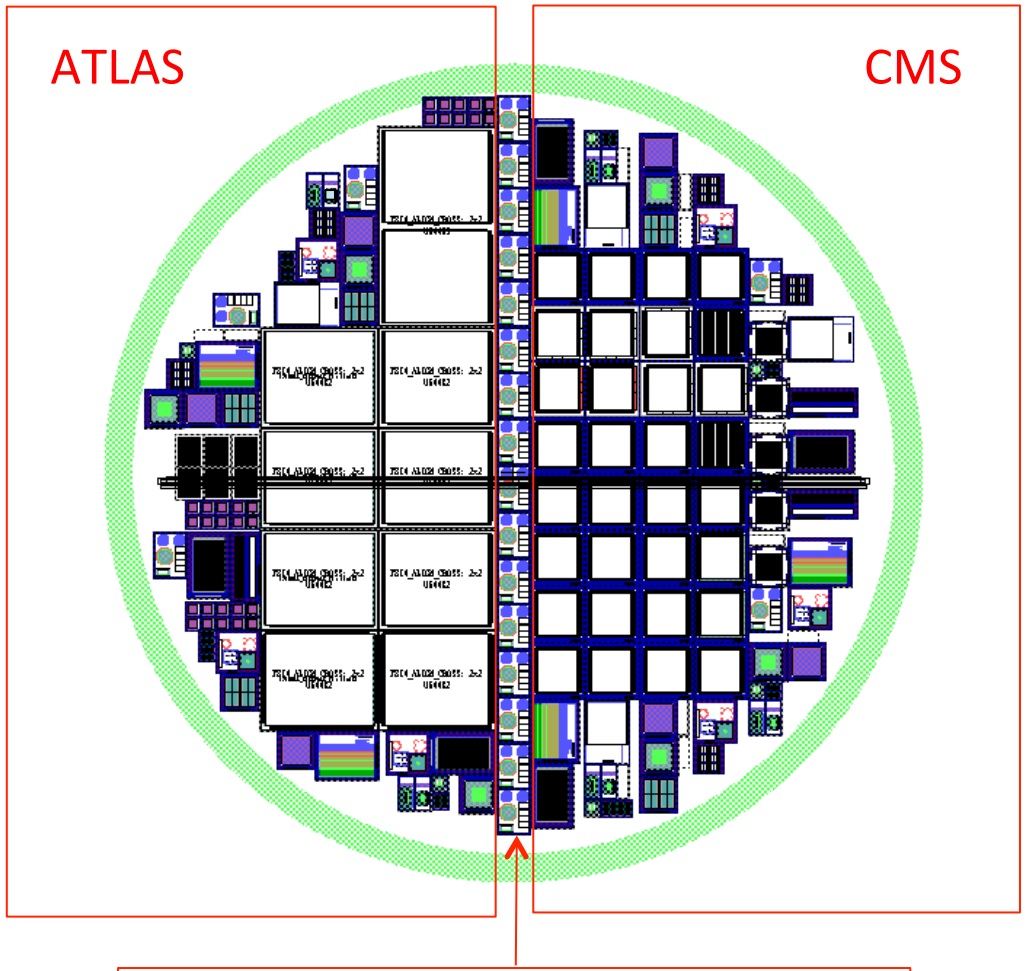
Conclusion and next steps

- From initial electrical tests, good sensor quality observed:
  - low depletion voltage
  - low leakage current
  - high breakdown voltage

  } Good agreement with simulations
- 25x100 pixel layout confirmed to be critical (metal misalignment, low oxide thickness, …)
- Automatic tests under way to check I-V curves of all sensors
- Quality permitting, pixel sensors from a few wafers to be bump bonded for functional tests

Back-Up slides

Planar test batch



Test structures for SiSi DWB substrate qualification

Wafers

6” Si-Si silicon wafers (ICEMOS), 100±2μm and 130±2μm sensor layer thickness with ρ>3000 Ωcm (+500±10μm support wafer)

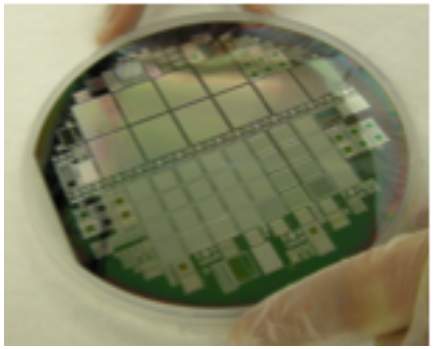
Process

- n-on-p planar process
- three different p-spray doses

Layout

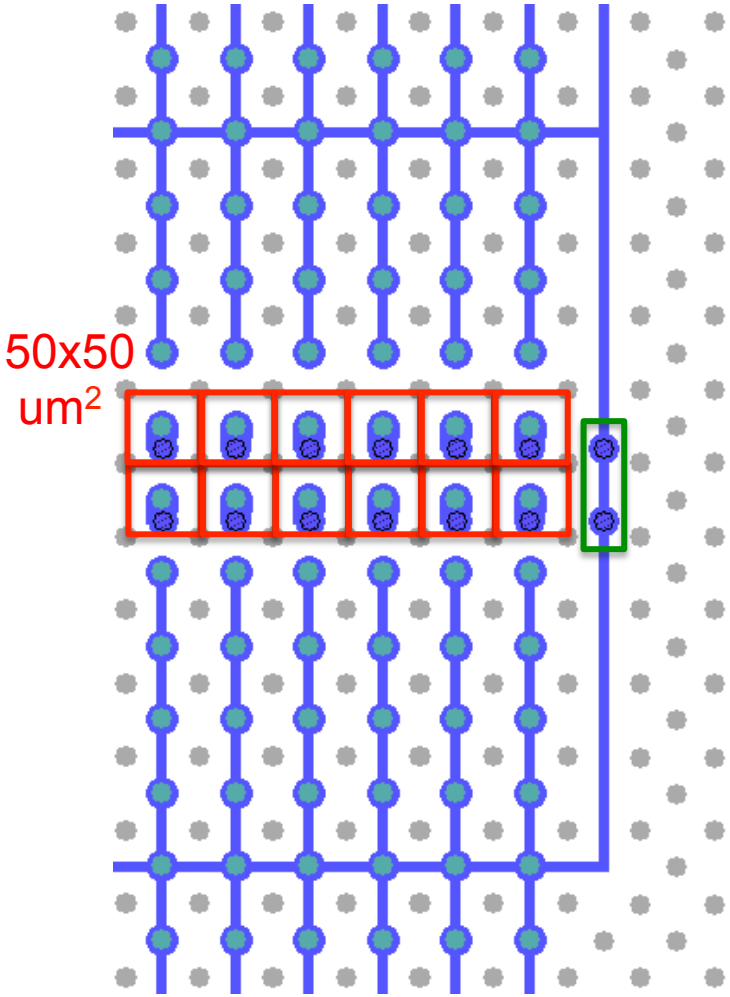
- 10 ATLAS pixels (FEI4)
- 32 CMS pixels (PSI46)
- Many test structures

Batch completed at FBK in Dec. 2014

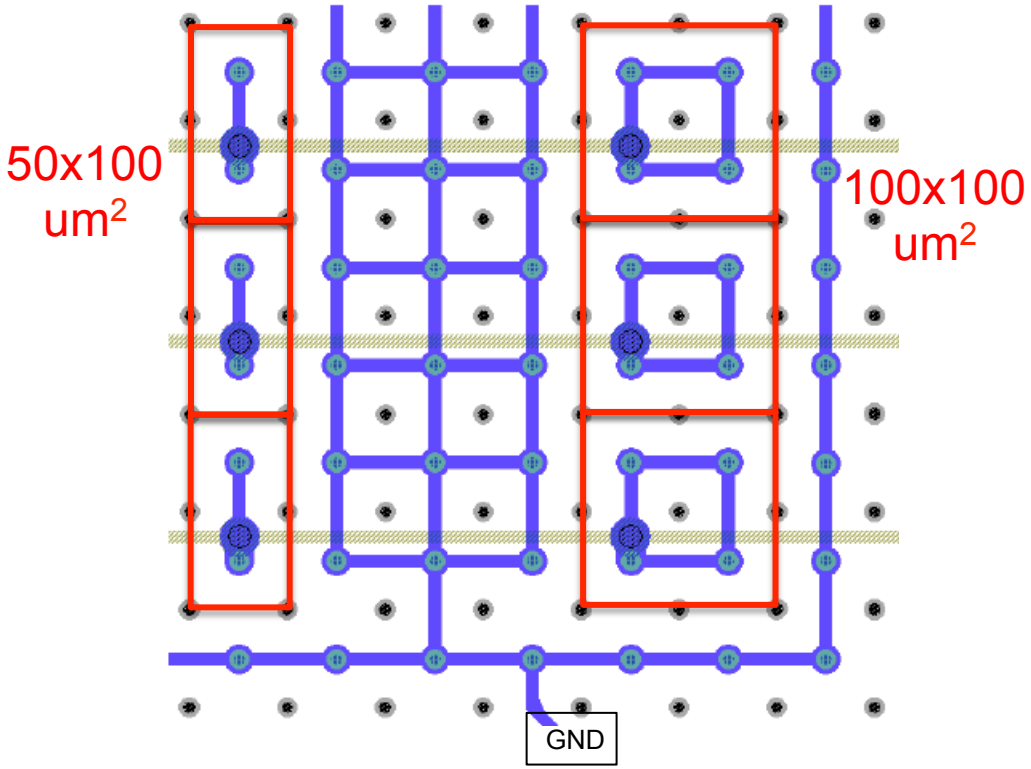


New pixels with existing ROCs ?

ATLAS FE-I4 50x50 (1E) + grid

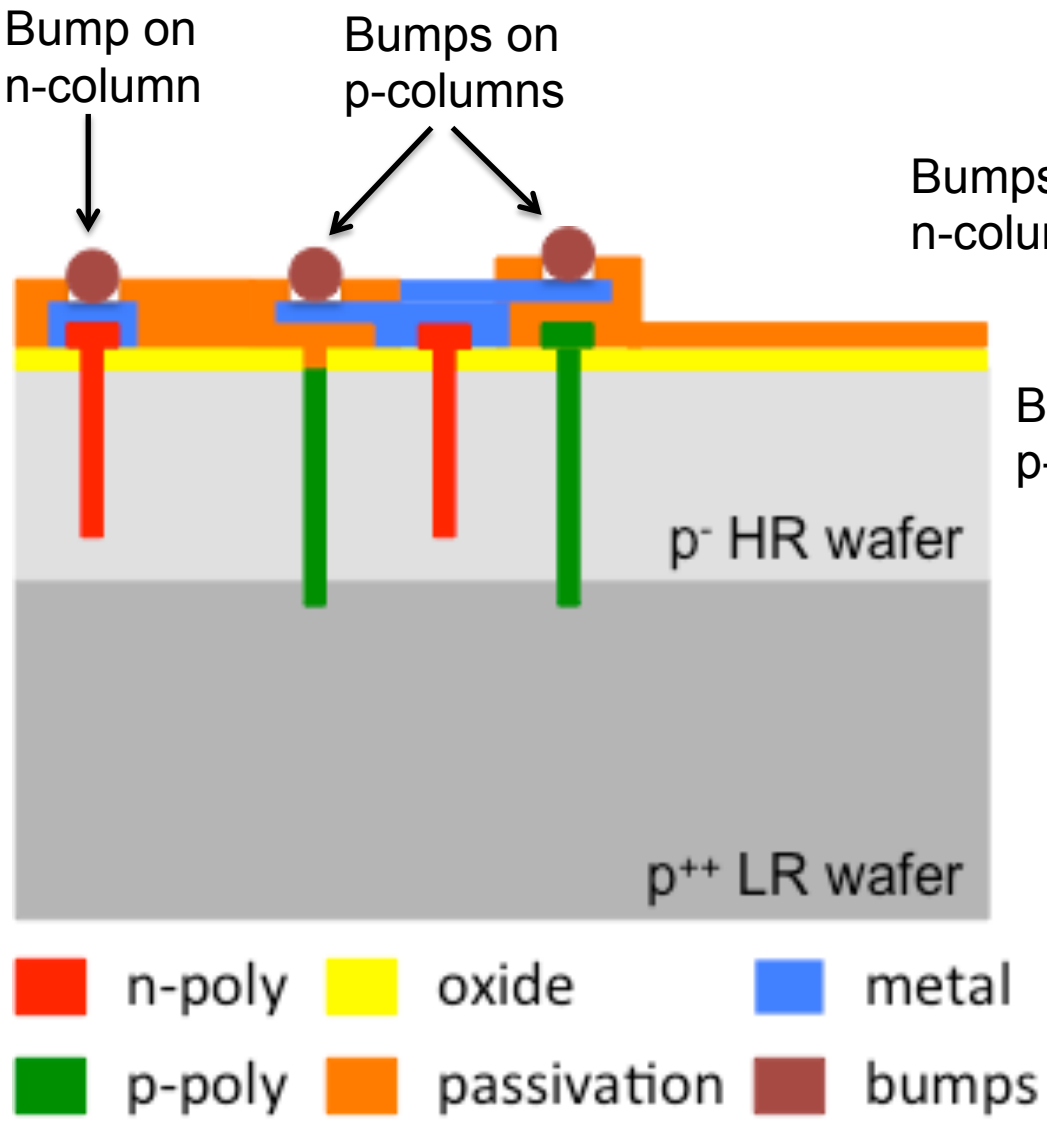


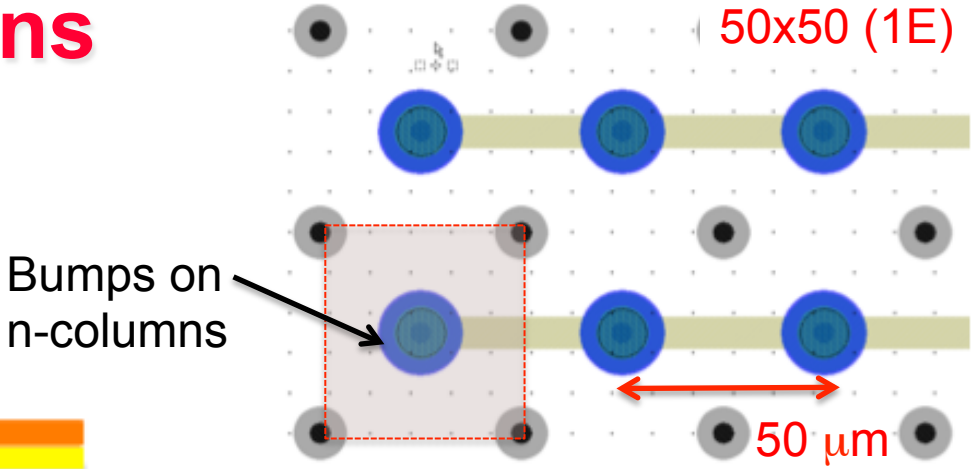
CMS PSI46: 50x50 (2E+4E) + grid

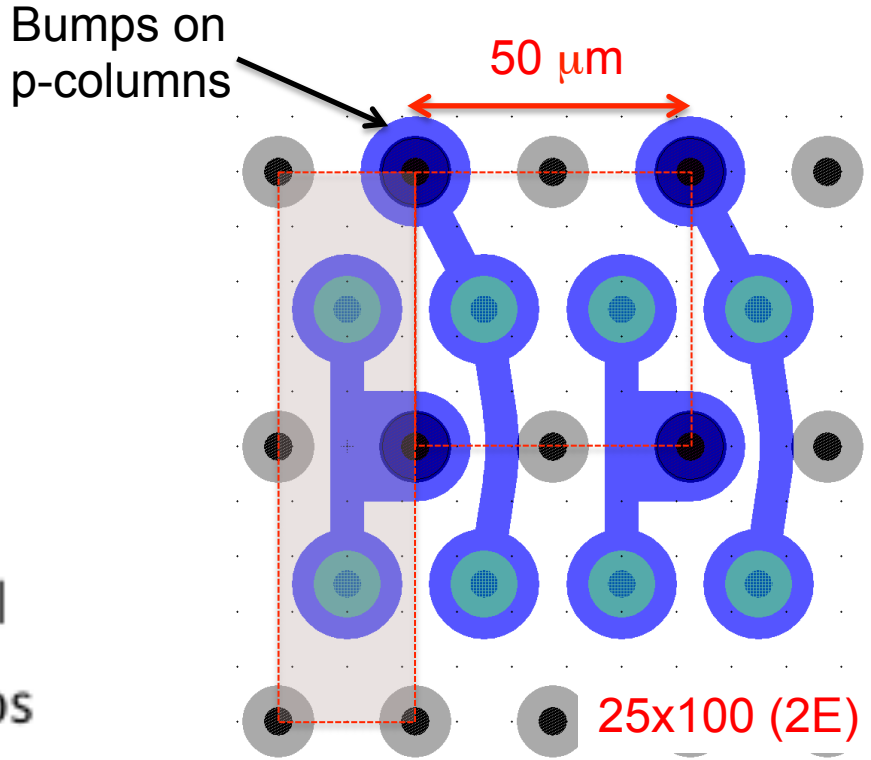


Small pixels take all bonding pads
+ rest of pixels at GND using a metal grid and extra-pads at the periphery

Bumps on columns







Slim edges

- Slim edge concept based on multiple ohmic columns termination developed for IBL (~200 μm) M. Povoli et al., JINST 7 (2012) C01015
- It can be made slimmer by reduced inter-electrode spacing (safely 75 - 100 μm, more aggressively down to ~50 μm)
- 3D guard rings also possible with similar dead area