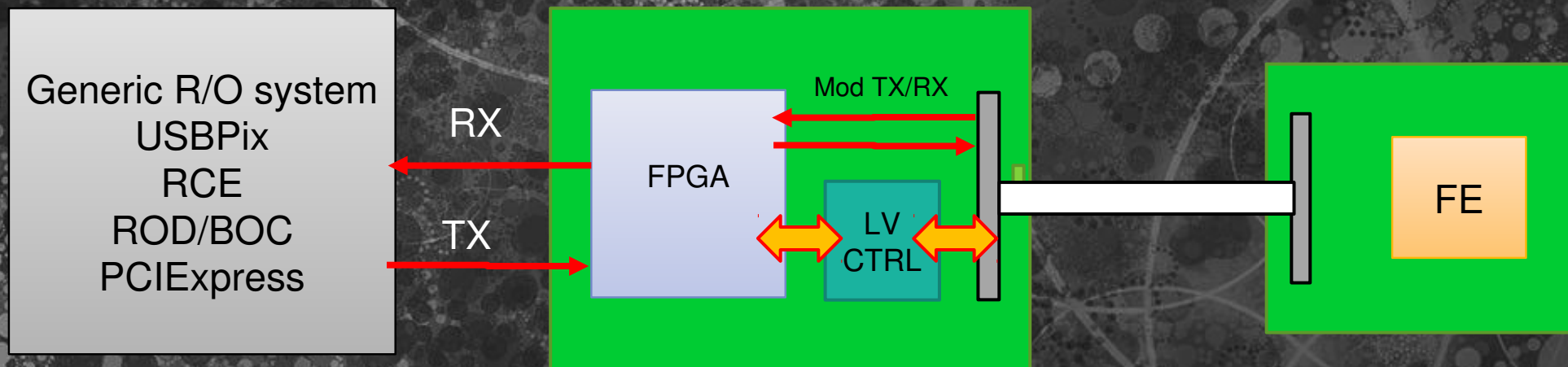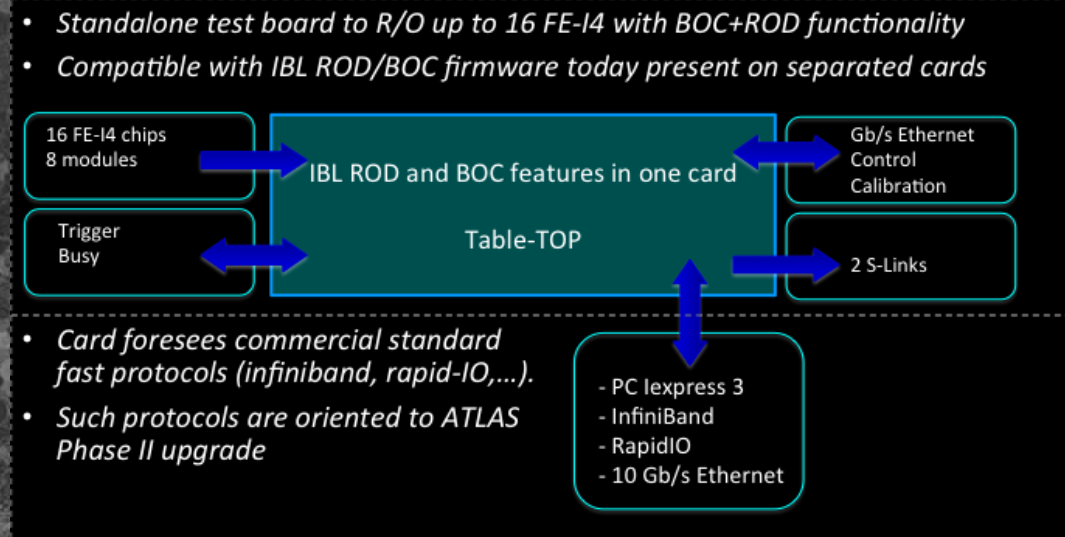# BladeBoard v1.0

INFN Bologna

G. Balbi, D. Falchieri, A. Gabrielli, **L. Lama**, G. Pellegrini, C. Preti
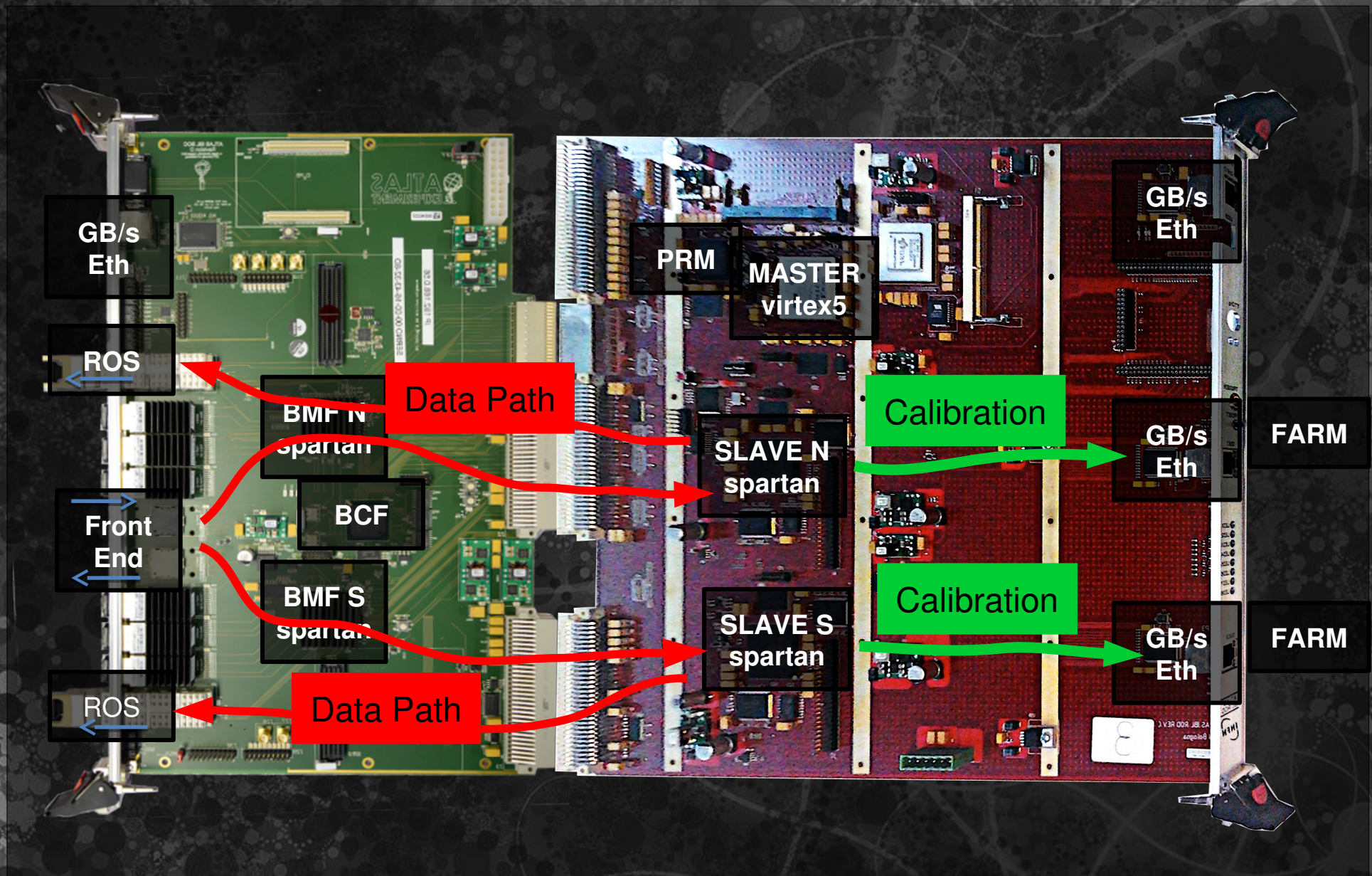
Overview

- State of the project

  - Schematic nearly done

- Main Features

  - GBT

  - PCIE

  - Back Compatibility through FMC

  - Ethernet spare connector for differential generic readout

Table Top proposal

- Table-top ROD/BOC version (BO)
- Use expertise on IBL ROD, no VME needs
- **Full SW/FW compatibility with PIT cards**
- Half ROD, up to 16 FE
- Financed by INFN
- Possible activities on read-out
- Expand existing FE-I4 R/O systems to HV/HR-CMOS
- Common HW/FW/SW interface definition
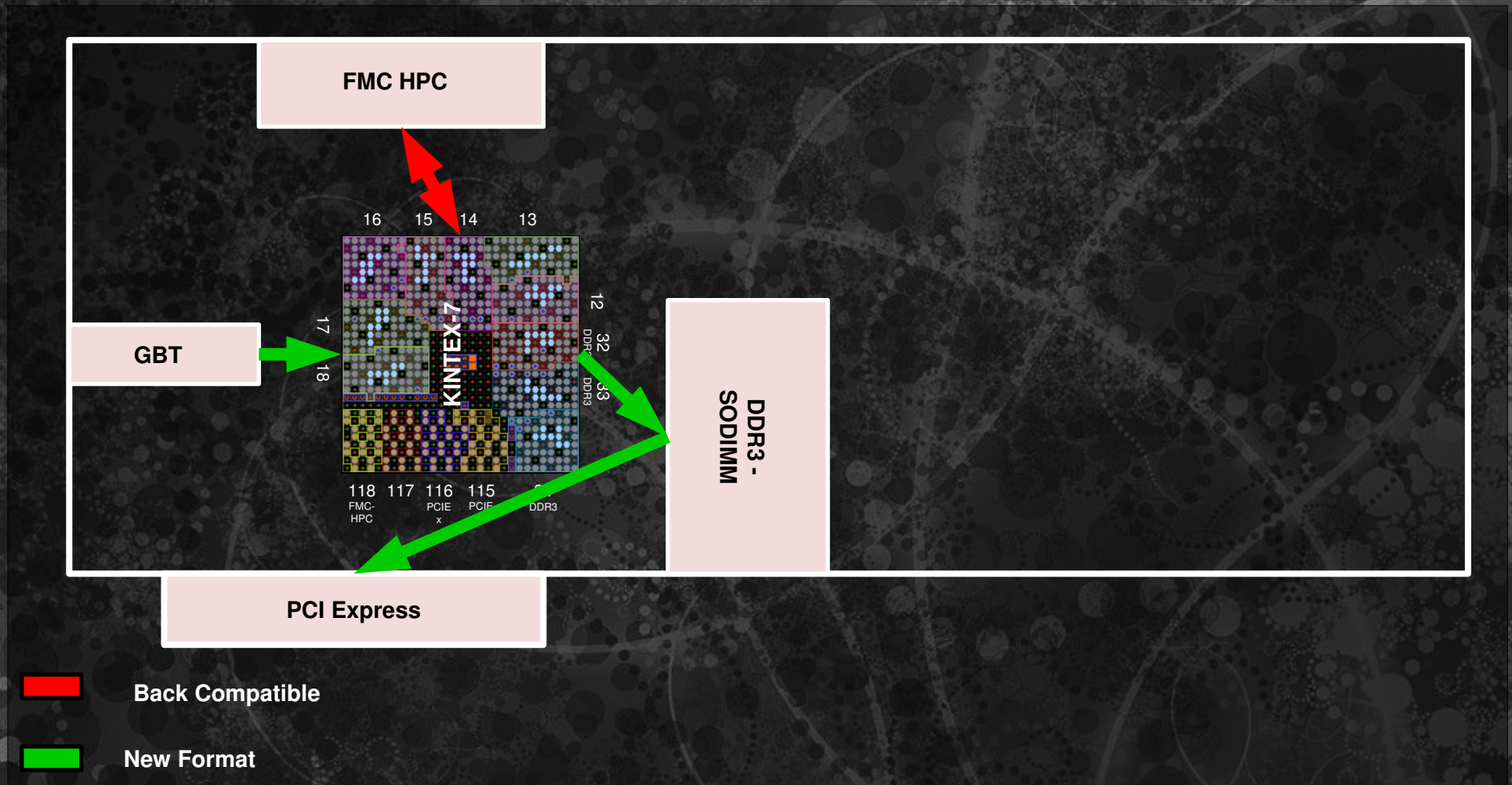- Integrate mini-DCS in the read-out
- GBT concentrator

- Standalone test board to R/O up to 16 FE-I4 with BOC+ROD functionality
- Compatible with IBL ROD/BOC firmware today present on separated cards

16 FE-I4 chips 8 modules → IBL ROD and BOC features in one card ↔ Gb/s Ethernet Control Calibration

Trigger Busy ↔ Table-TOP → 2 S-Links

- Card foresees commercial standard fast protocols (infiniband, rapid-IO,...).
- Such protocols are oriented to ATLAS Phase II upgrade

- PC Iexpress 3
- InfiniBand
- RapidIO
- 10 Gb/s Ethernet

Generic R/O system
USBPix
RCE
ROD/BOC
PCIExpress

RX

TX

FPGA

Mod TX/RX

LV CTRL

FE

3

History

Data Taking

- Three possible input paths

  - GBT

  - FMC (Snap 12)

  - Spare pins within an ethernet connector

- Two possible output paths

  - PCIE

  - FMC (QSFP)

- Depending on the firmware each combination is possible

Data Taking Paths

FMC HPC

GBT

KINTEX-7

16 15 14 13

17
18

12
32 DDR3
33 DDR3

DDR3 - SODIMM

118 117 116 115
FMC-   PCIE PCIF
HPC   x   DDR3

PCI Express

■ **Back Compatible**

■ **New Format**

Every combination of the two is possible depending on the firmware

Control & Clock

- Architecture of these features changed dramatically from IBL ROD design:

  - Main Clock is fed directly to the Kintex

  - The Zynq is taking care of both programming and control tasks

  - JTAG chain can be split so the Kintex can be configured by the Zynq

  - FMC LPC connector is compliant with CERN TTCRQ FMC mezzanine

  - Calibration path is there to keep compatibility

Control Features
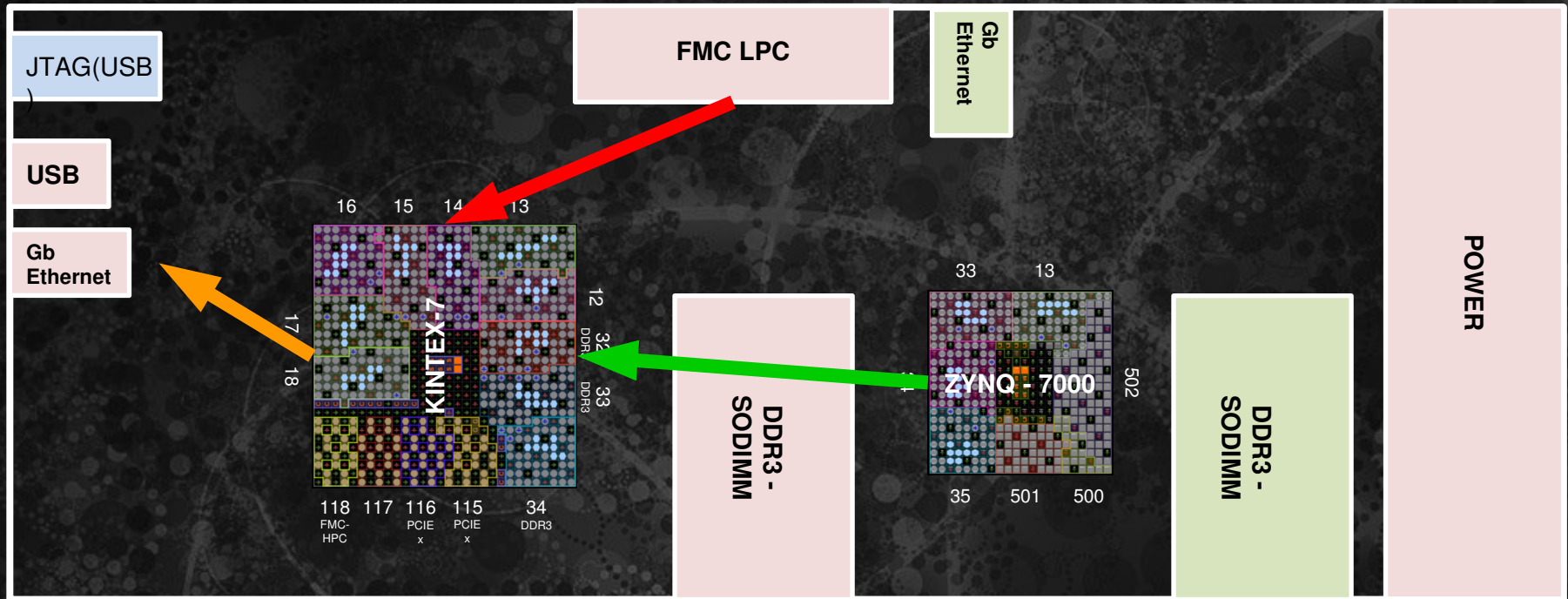
Legend:
- **Clock (Can be back compatible with mezzanine)** (red)
- **Maintaining Compatibility with calibration path** (orange)
- **Changing from PPC to ARM** (green)

This Change will affect the C++ Code only a little and the main access through EPC will remain nearly the same
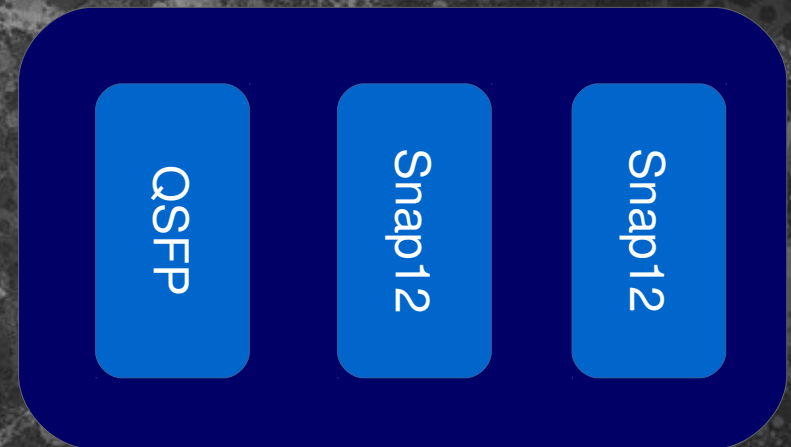
Expansions

- TTCRx LPC expansion board from CERN

  - The board is already prototyped and has only one clock line incompatible with the LPC connector specifics.
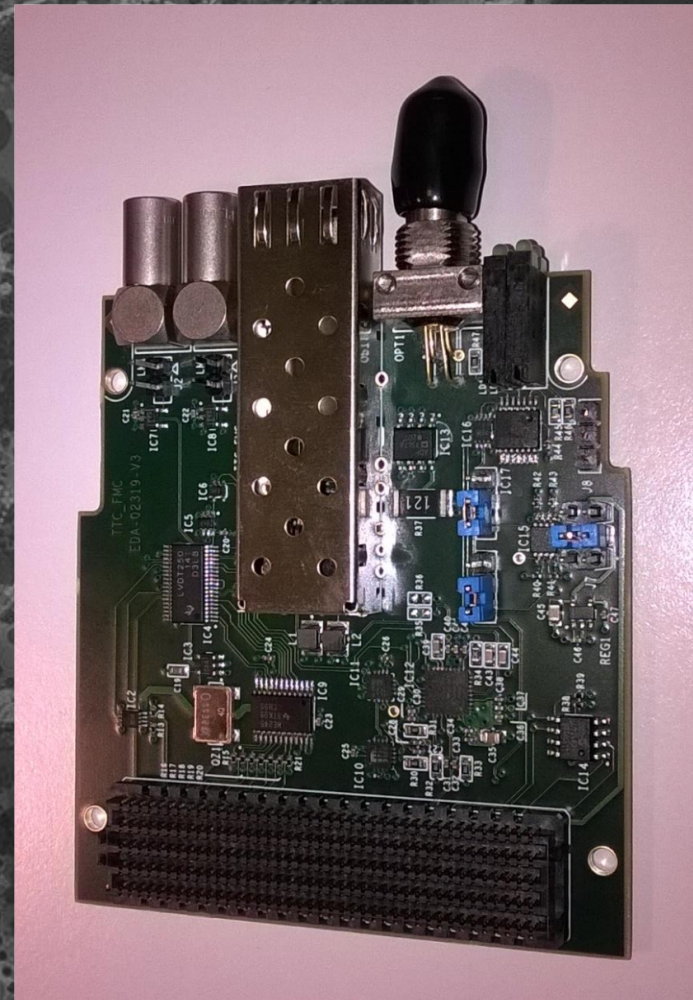
Expansions

- Snap12 and QSFP HPC expansion board

  - Since for these components we don't need fast IOs we can keep them on the FMC

QSFP

Snap12

Snap12

Production Plans

- The schematic development should end soon.

- We should expect one month for the layout because it needs some simulations.

- For the time being the requests will be taken into consideration only for another release.