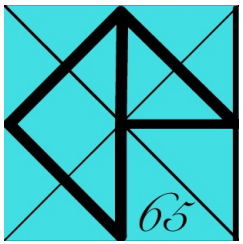
CHIPIX65: Sviluppo di un pixel chip innovativo in tecnologia CMOS 65 nm per altissimi flussi di particelle e radiazione agli esperimenti di HL_LHC e futuri collider di nuova generazione

Valentino Liberali (Milano)

on behalf of the CHIPIX65 project



Marzo 2016

Scopo e partecipanti

Scopo: Lo sviluppo di un pixel chip innovativo in tecnologia CMOS 65nm (TSMC) resistente a altissimi flussi di particelle e radiazione si inserisce nella partecipazione italiana al progetto CERN RD53, di cui CHIPIX65 è parte.

Coordinatore: **N. Demaria (Torino)**
Unità partecipanti: **Bari**, **Bergamo + Pavia**, **Milano**, **Padova**, **Perugia**, **Pisa**, **Torino**, **Lecce** (dal 2016)

Persone:
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Attività in corso: IP blocks

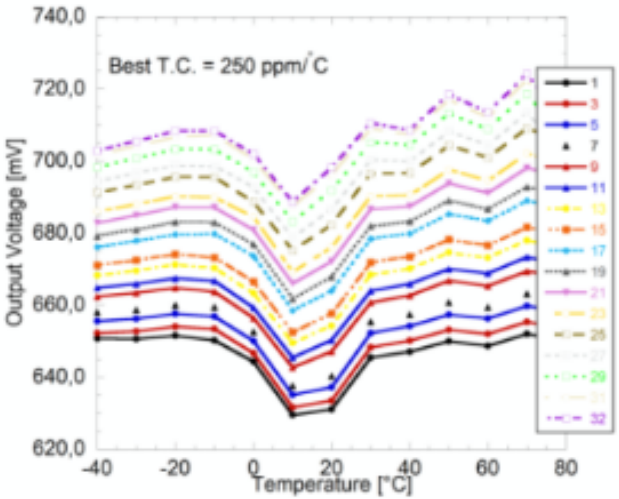
BandGap: Pavia
ADC: Bari
DAC: Bari
SER/DES: Pisa
s-LVDS: Pavia, Pisa
DICE SRAM: Milano

BLOCK	DIMENSIONS	POWER	Performance / Main-Characteristics
Band-Gap	$100\times270\ \mu m^2$	65 μW	based on MOS only
10-bit DAC	$140\times240\ \mu m^2$	150 μW	DNL $<$ 0.4 LSB, INL $<$ 1LSB
12-bit ADC	$308\times535\ \mu m^2$		1V, 16-ch, 5kSample/s
SER	$100\times56\ \mu m^2$	2.3 mW	2 Gbps
DES	$180\times56\ \mu m^2$	17.8 mW	2 Gbps
sLVDS-TX	$160\times160\ \mu m^2$	2 mW	1.2 Gbps
sLVDS-RX	$70\times80\ \mu m^2$	0.2 mW	1.2 Gbps
Dice S-RAM	$1.8\times3.3\ \mu m^2$		SEE recover in 2.5ns

BandGap

Il BandGap è un blocco importante perché deve fornire un riferimento indipendente da T e dalle radiazioni

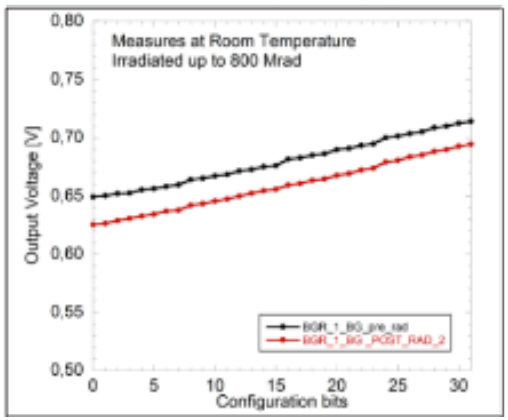
Pavia / Bg



- Temperature range: from -40°C to 80°C
- Trimming resistor with 5 bits resolution
- Power Supply: 1.2V
- Power Consumption: 50 uW

•Irradiated up to 800 Mrad (Si) with protons at 10 MeV

•The reference output voltage has a limited shift under irradiation around 4 %



New version designed and submitted in May 2015, now starting test:

- mismatch variations < 2%, process ~4%
- trimming can correct process, radiation variations, leaving at max mism@2%

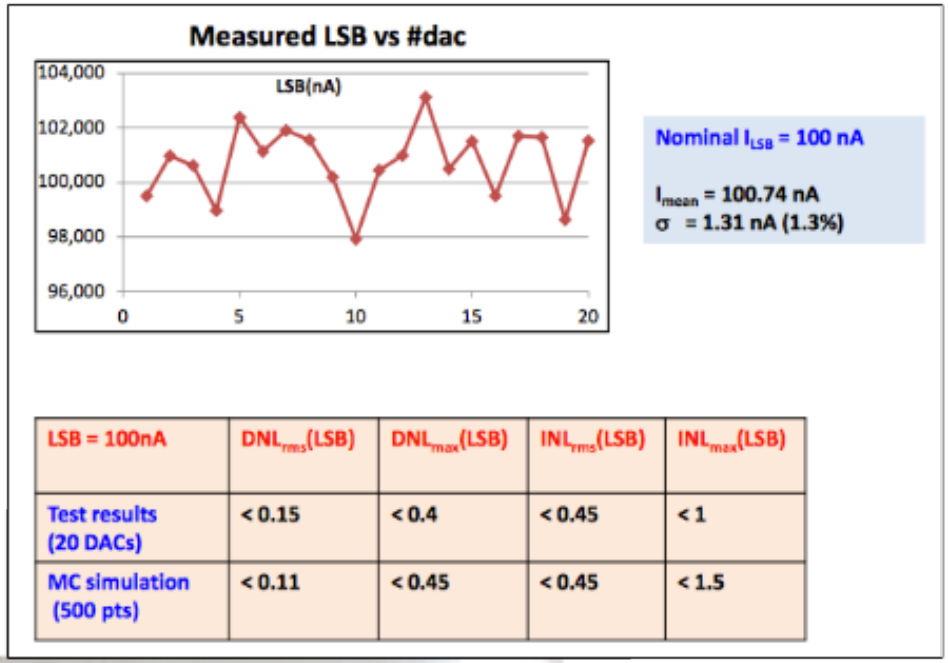
DAC

- Important for ASIC biasing

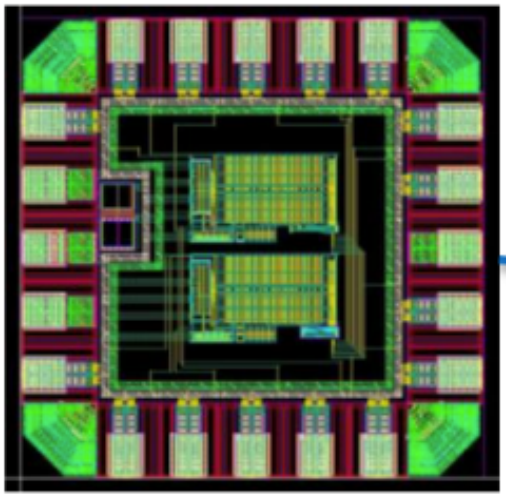
Bari

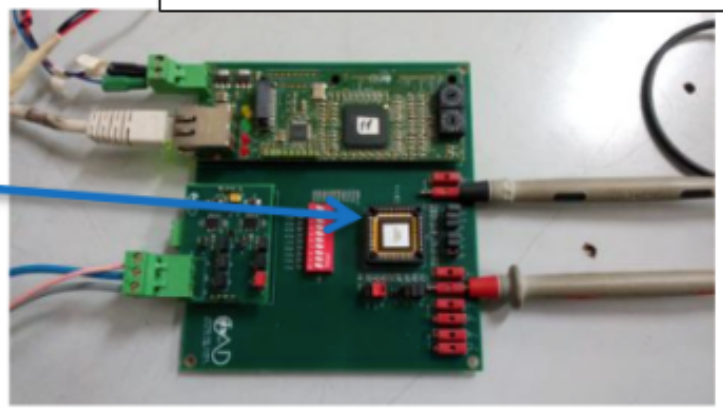
- 10-bit **current-steering** Digital-to-Analog converter; LSB = 100nA (nominal)
  -Architecture: 8+2 segmented DAC (2 binary weighted + 8 unitary decoded cells)

- Characterised in Lab
- Now under radiation test at Padova x-ray machine

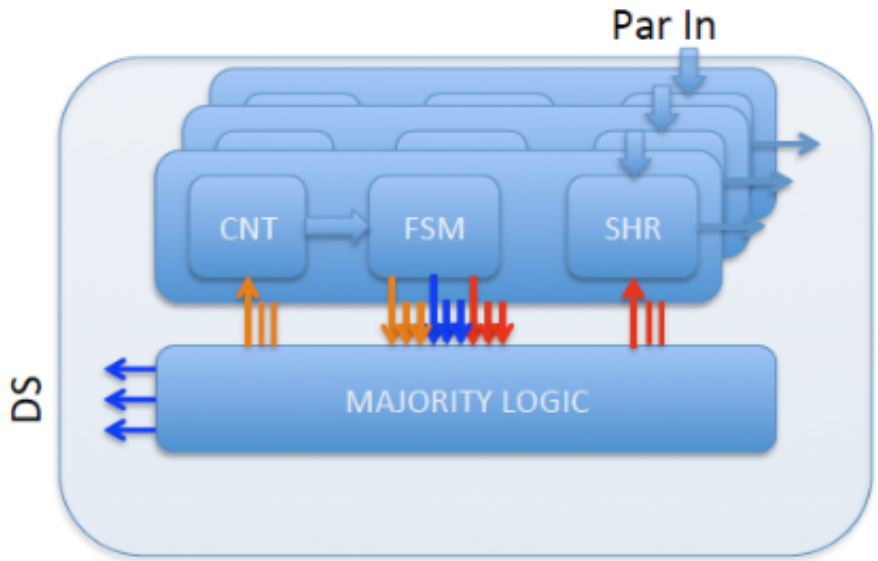


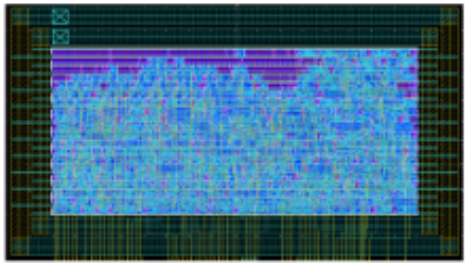
LSB = 100nA	DNL_{rms}(LSB)	DNL_{max}(LSB)	INL_{rms}(LSB)	INL_{max}(LSB)
Test results (20 DACs)	< 0.15	< 0.4	< 0.45	< 1
MC simulation (500 pts)	< 0.11	< 0.45	< 0.45	< 1.5





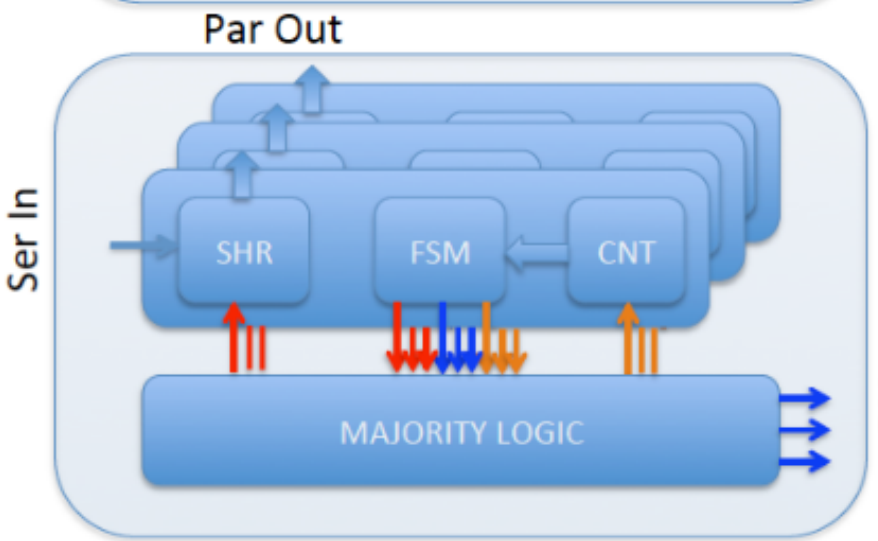
SER / DES

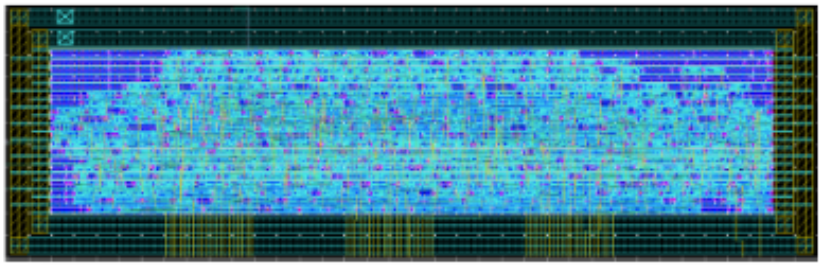




Pisa

- 20 bits – 2Gbps
- Standard Cells + TMR
- FSM => Counter Reset, Load, Data Strobe (DS)
- H = 56um – W = 100um (299 cells)
- Power = 2.35 mW (max)





- 20 bits – 2Gbps
- Standard Cells + TMR
- FSM => Counter Reset, Data Valid (DV)
- H = 56um – W = 180um (556 cells)
- Power = 17.85mW (max)

5

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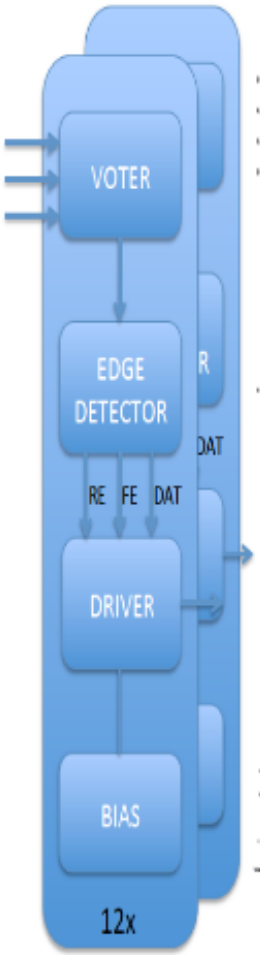
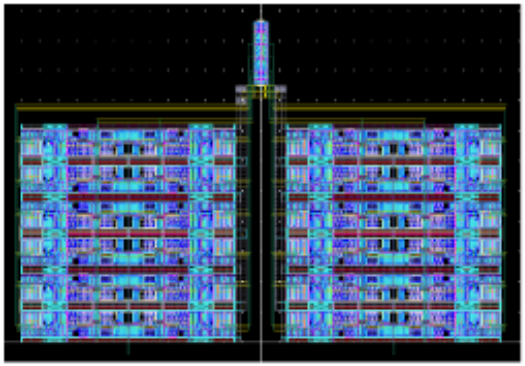
s-LVDS

TX





- Target frequency = 3GHz
- Modular Redundancy (12x)
- Edge detection for Pre-Emphasis
- W = 130um – H = 36um
- I= 5.4 mA (typ)

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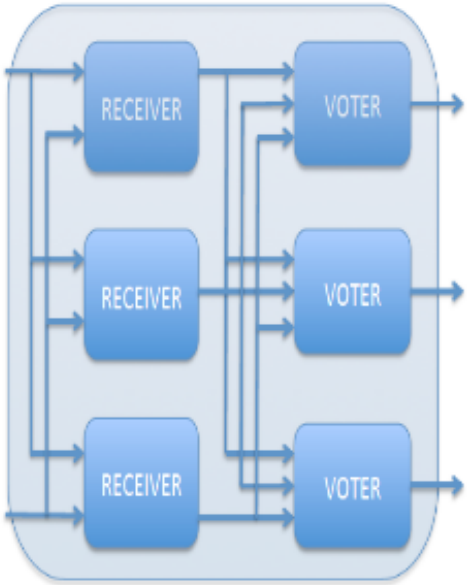
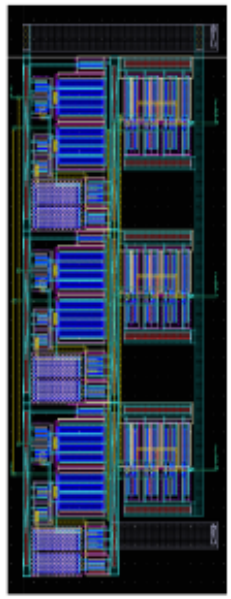
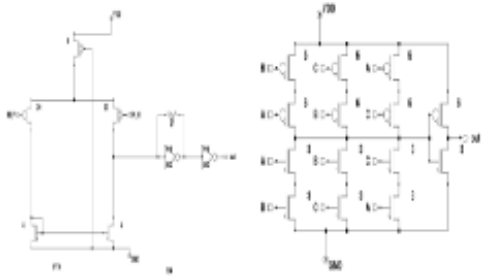
Pisa

RX







Target frequency = 3GHz
Triple Redundancy
Two-stages OTA+TIA
W = 30um – H = 16um
I = 1.3mA (typ)

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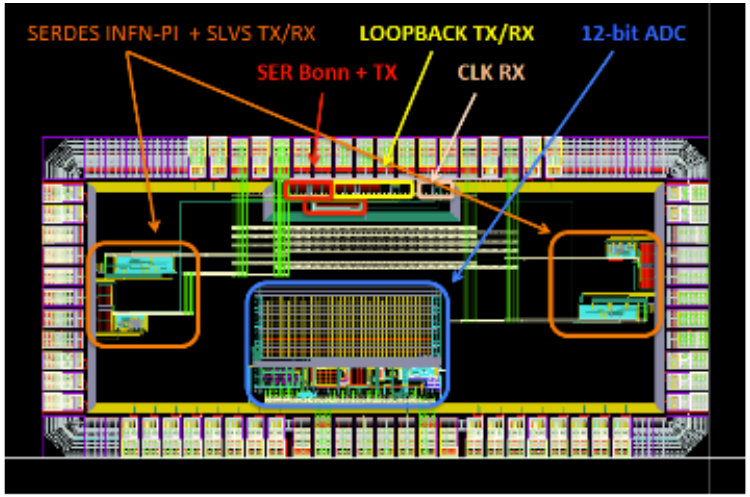
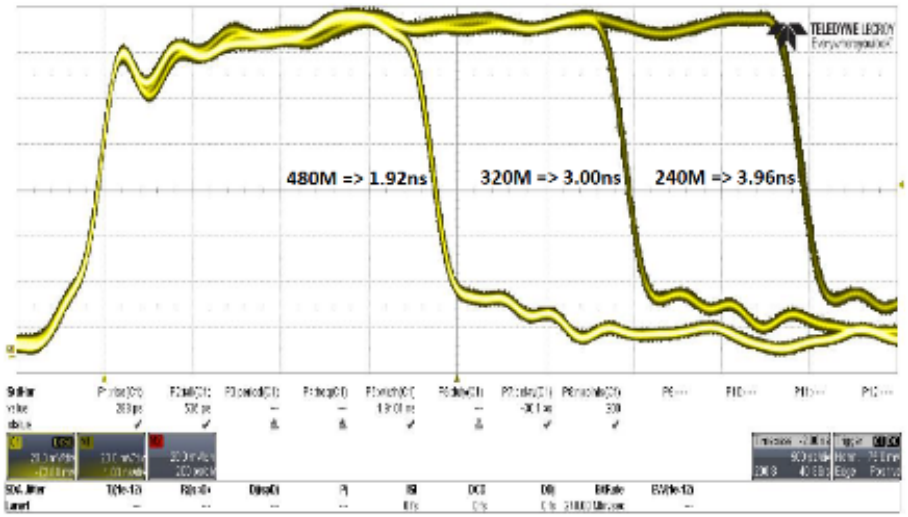
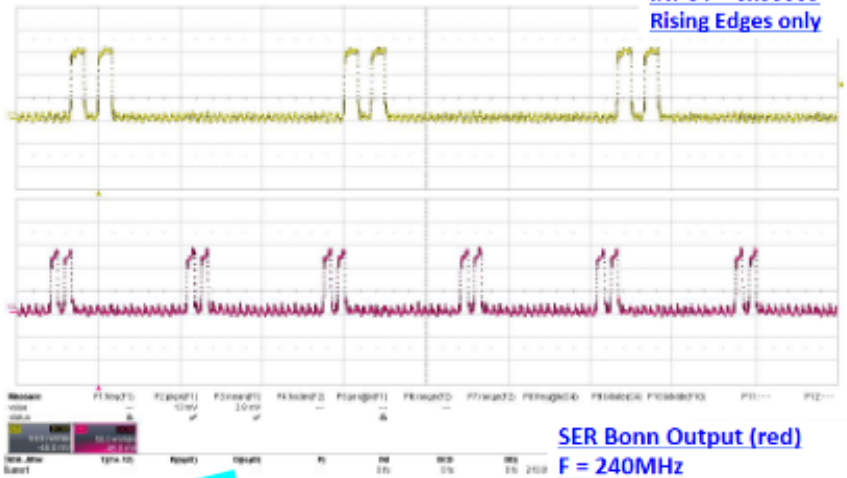
SER / DES v. 2





SER INFN-PI Output (yellow)
F = 240MHz - Pre-Emphasis off
INPUT = 0x00005
Rising Edges only



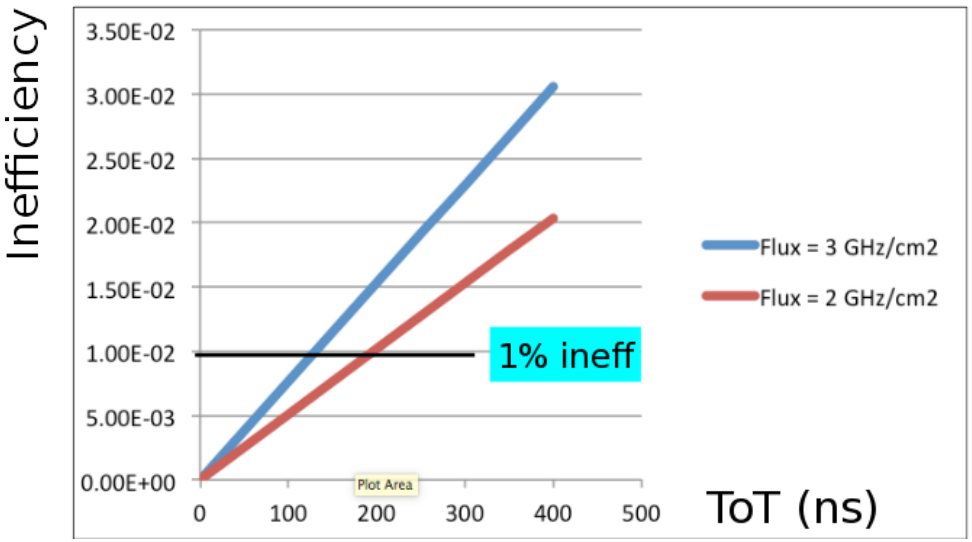
SER Bonn Output (red)
F = 240MHz
INPUT = 0x00005
Both Rising and Falling Edges

Pisa

AFE

Requirements:

- Compact: $\approx 50\,\%$ of $(50 \times 50\ \mu m^2)$; $25 \times 50\ \mu m^2$ or $35 \times 35\ \mu m^2$
- Low power: $< 4\ \mu A$ (or $5\ \mu W$)
- Low threshold: $< 1000\ e^-$
- Dead-time inefficiency $\ll 1\,\%$ @ 3 GHz/cm (200 PU)
- Digitization: desired at least 4-bits



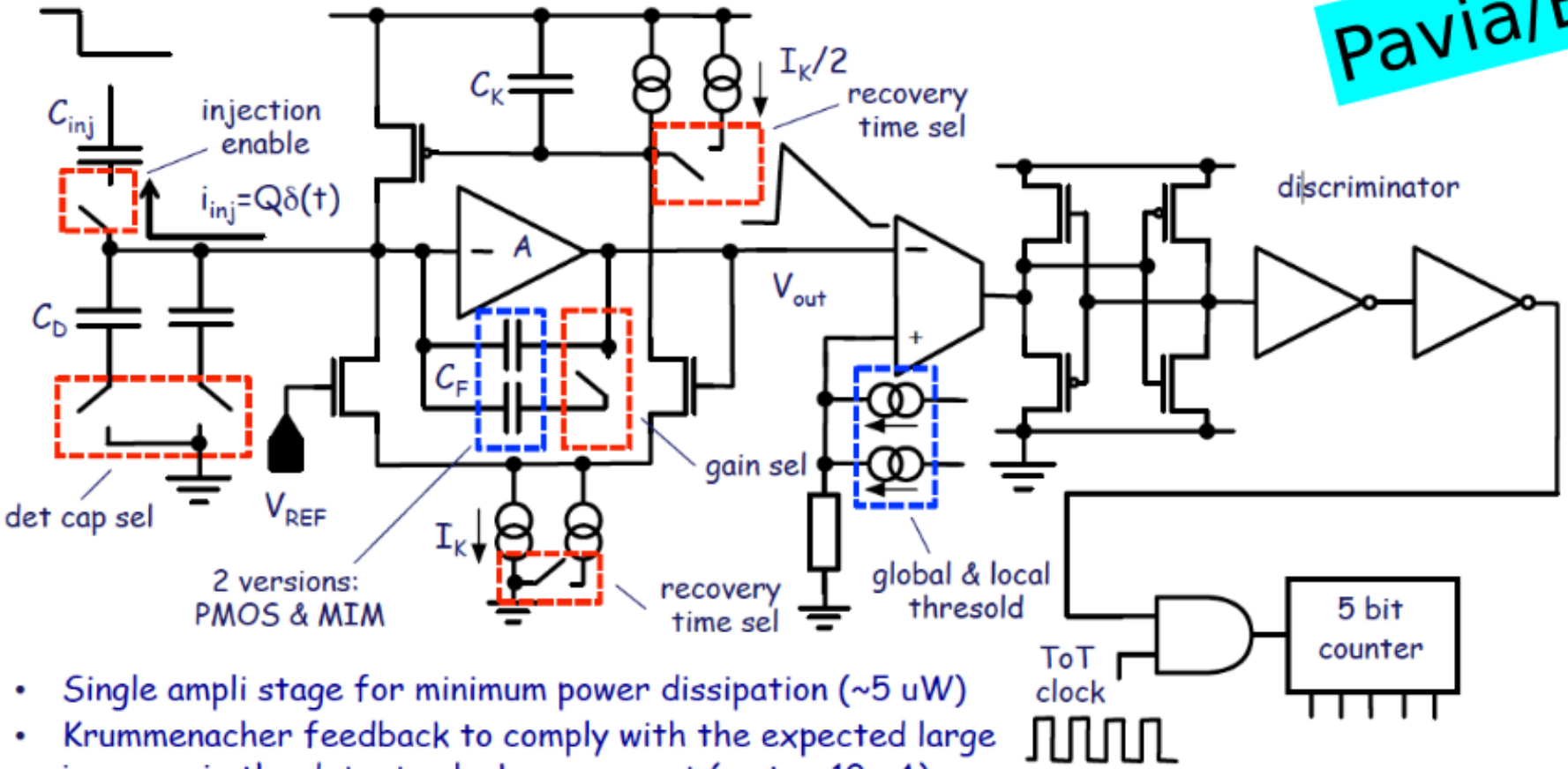
CONSEQUENCES

1.<ToT> should be < 150ns (200PU)
2.<ToT> should be < 200ns (140 PU)

3. For 4-bit (600e-) ToT freq > 100 MHz
4. For 5-bit (300e-) ToT freq > 200 MHz

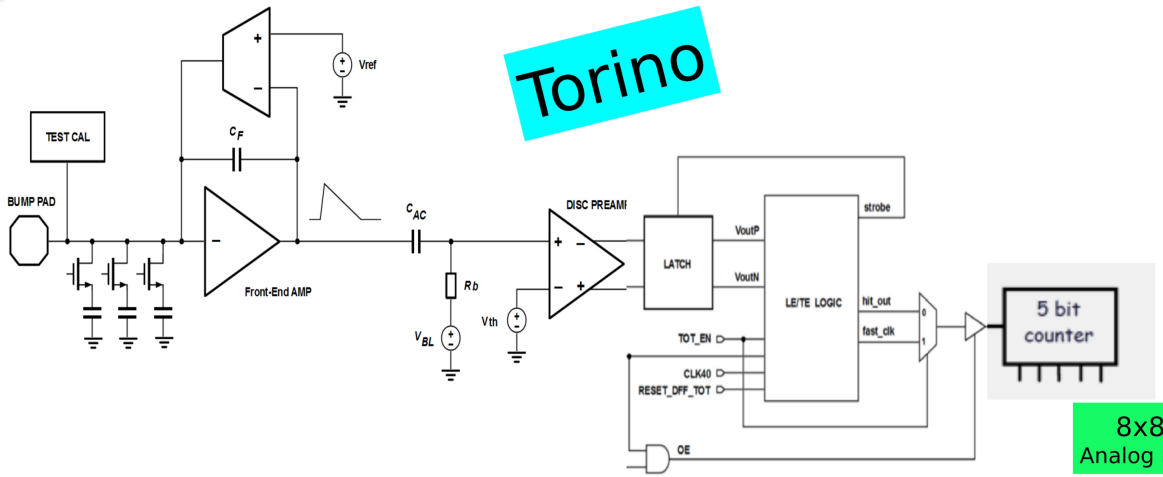
Asynchronous AFE

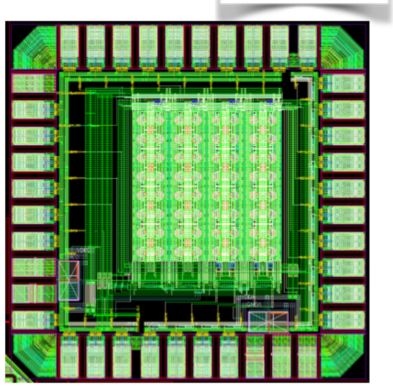
Pavia/Bg



- Single ampli stage for minimum power dissipation (~5 uW)
- Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to ~10 nA)
- 30000 electron maximum input charge expected, ~450 mV preampli output dynamic range
- Selectable gain, recovery current and detector emulating capacitance
- 40 MHz clock, 5 bit dual edge counter, 400 ns maximum ToT

Synchronous Analog FE





8x8 pixel matrix submitted and tested
Analog readout of CSA and Discriminator (via buffers)

- **PREAMPLIFIER**
  - One stage CSA with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - (AC coupled to CSA)
  - off-set compensated diff.amplif. + latch;
  - **FAST Time-over-Threshold**
    - Local oscillator strobing Latch (to 800MHz
- **Calibration circuit**
  - digital signal + DC calibration leve

Performance SUMMARY
- Compact: ~25um x 40 um
- Low power: < 5.5 uW (with ToT logic)
- Low noise: ENC=100e- @C_{det}=100 fF
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 10 ke- in : 90 / 180 / 360 ns (Fast/Medium/Low recovery current)
  - up to 7-8bit (125-250e-/ADC) - no ext clock
- NO Threshold-Trimming:
  - autozeroing made by hardware

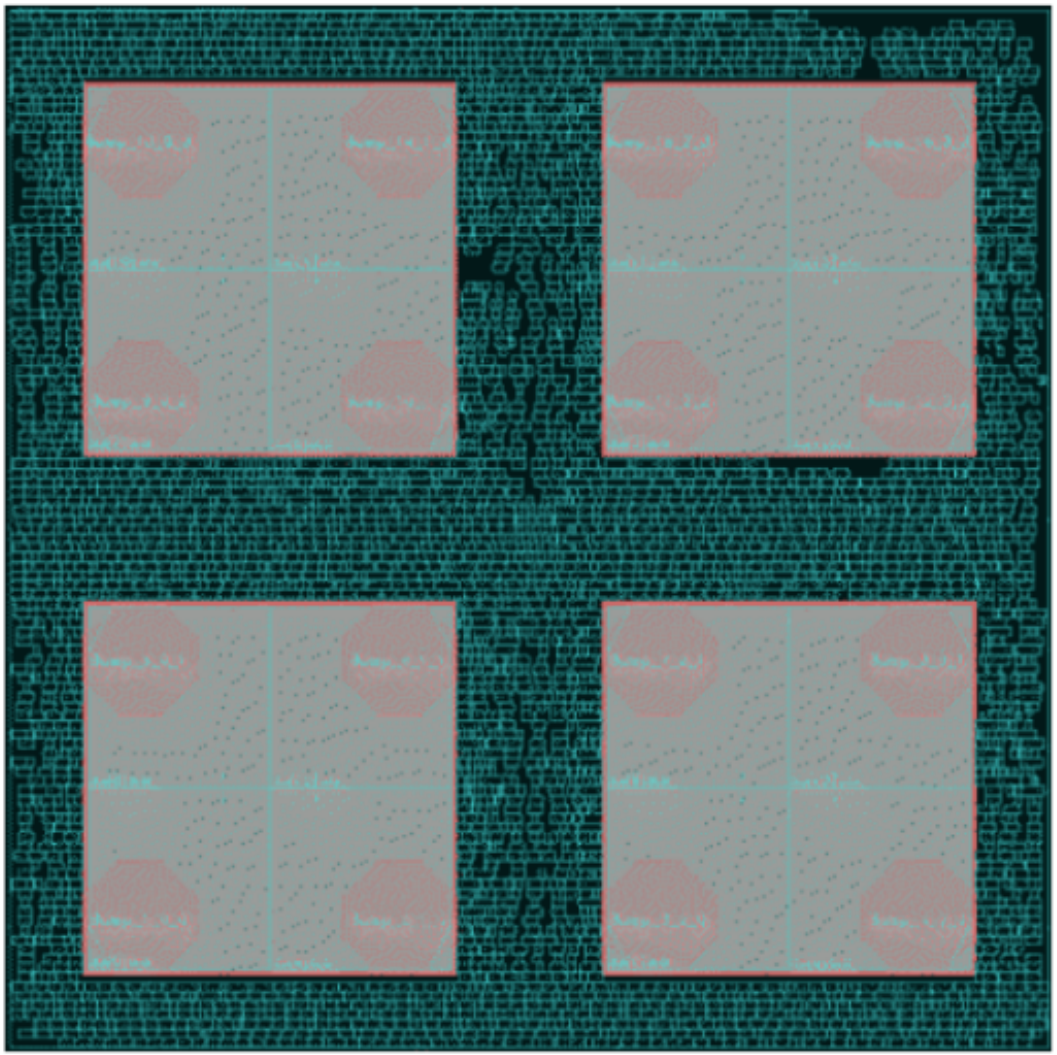
CHIPIX65 Demonstrator: Motivation (1)

- design a small yet fairly complex pixel array demonstrator in 65nm CMOS technology (intermediate step before full-scale RD53 prototype)
  - **64×64** pixels with **50um×50um** pixel size
  - independent development from FE65_P2
- integration of **two different flavours of analogue front-end** into the same digital readout/configuration architecture
  - asynchronous front-end chain (Pavia)
  - synchronous design (Torino)
- design and implementation of a **realistic and new region-based digital architecture**
  - usage of the **RD53 SystemVerilog/UVM verification environment** from the beginning
  - digital architecture studies performed with hits and trigger patterns provided by the verification environment
  - baseline choice of a **4×4 pixel-region**

CHIPIX65 Demonstrator: Motivation (2)

- **no ambition** to extend the exercise to complex digital readout/slow control
  - SPI-based chip configuration
  - simple column arbitering with RAM-based FIFO derandomizer and serializer
- integration of available **silicon-proved RD53 IP blocks**
  - biasing DAC and monitoring ADC (Bari), bandgap (Bergamo/Pavia)
  - sLVDS TX/RX (Bergamo/Pavia), serializer (Pisa)
  - others if available and successfully tested
- usage of the **modified CERN I/O library**
- core design-team based on INFN/CHIPIX65 groups
  - gain expertise and promote among INFN units the **digital-on-top (DoT) design methodology**
  - **ClioSoft-based** distributed design environment
  - periodic and detailed design reviews among designers
- **Multi-Project Wafer (MPW) run** submission planned for **Q1/2016**

CHIPIX65 Demonstrator: 4 x 4 pixel array



- Exercise with 'brute-force' :
  - with 20us the digital area is very full (>80%)
- With second iteration (signal-only) promising early results
  - area@ 60%, low power (<4uW/px)
  - **working on it**

RD53A Demonstrator

- **2016 : RD53 Design of RD53A prototype**
  - 2-3 cm^2 prototype
  - Joined effort of the **whole RD53 collaboration**
  - Now definition / discussions o:
    - Technical Specs, Funding,
    - Milestone, Design team organization
  - submission end-2016
  - THIS WILL BE THE OUTPUT of RD53 Collaboration, closing the major part of R&D, communities will concentrate more into the chip for the experiments then.

- **CHIPIX65 contributions**
  - Provide Analog Front End(s)
  - Provide IP-blocks
  - Digital architectures (shared work)
  - CHIP integration (shared work)
  - IP-block whould be in a stable 'final' version by middle/end of 2016
  - Finance contribution:

    about 1/5 of cost

    cost ~ 500ke- 600ke

CHIPIX65 providing ~5 FTE out of 10 (50%) - covering all aspects

Contributo CHIPIX65
PV/BG: Gaioni, De Canio; TO: Monteil, Pacher, Paternò;
PG: Marconi; PI: Beccherle

Conclusione

CHIPIX65 activities

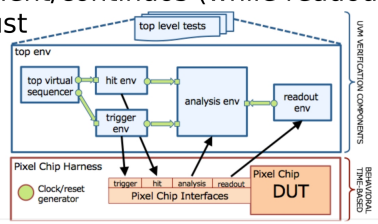
...at a glance

Radiation characterisation

- x-ray machine at LNL / Pd-INFN
  - Total Ionising Dose (TID)
  - 1 GRad in ~ 2 weeks
- Low-p at CN accelerator LNL
  - TID and Total Displacement damage
- TANDEM / SIRAD
  - Single Event Effects - with Heavy Ion
- Studies on n-MOS, p-MOS
- Irradiation of IP-block, Noise-measurements vs Irradiation

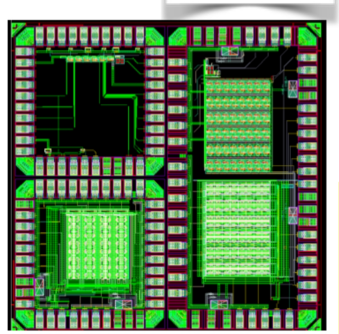
Digital Electronics:

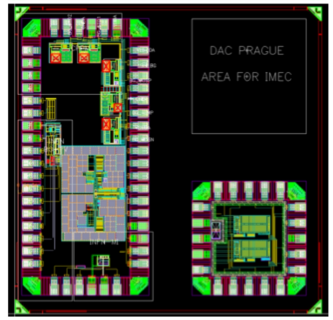
- Simulation Framework
  - System-Verilog-UVM (VEPIX53)
- Digital Architecture Studies
- Input protocols definition
  - fast/efficient/continuos (while readout)
  - SEE robust

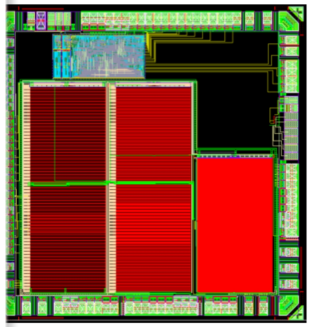


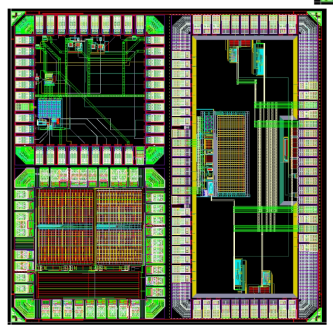
Design in 65nm

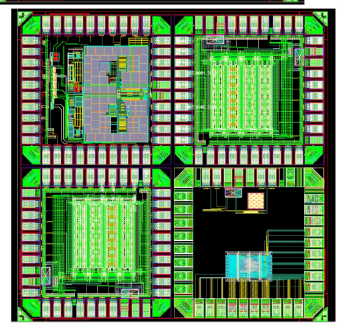
- 6 silicon dies 2x2mm2 submitted
- CHIPIX65 IP-blocks
  - DAC-curr, ADC, SRAM,
  - SER/DES, sLVDS(TX/RX)
  - BandGap, D2RA digital cells
  - JTAG
- CHIPIX65 Analog Very Front End
  - Synchronous chain
  - Asynchronous chain
- Integration of other RD53 IPs
  - DAC-volt (Prague)
  - SER (Bonn), BandGap (CPPM, CERN)











CHIPIX_SRAM, CHIPIX_IP_3, CHIPIX_VFE_2