

HVR - CCPD

HVR_CCPD

ATLAS ITK Italy meeting, 02/02/2016

**Attilio Andreazza, M. Citterio, V. Liberali, C. Meroni, F. Ragusa, E.
Zaffaroni - INFN Milano**

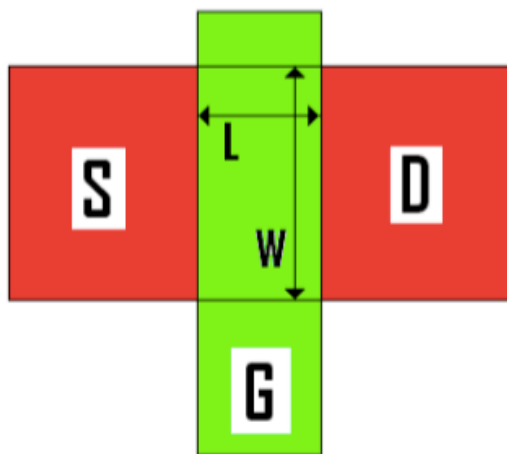
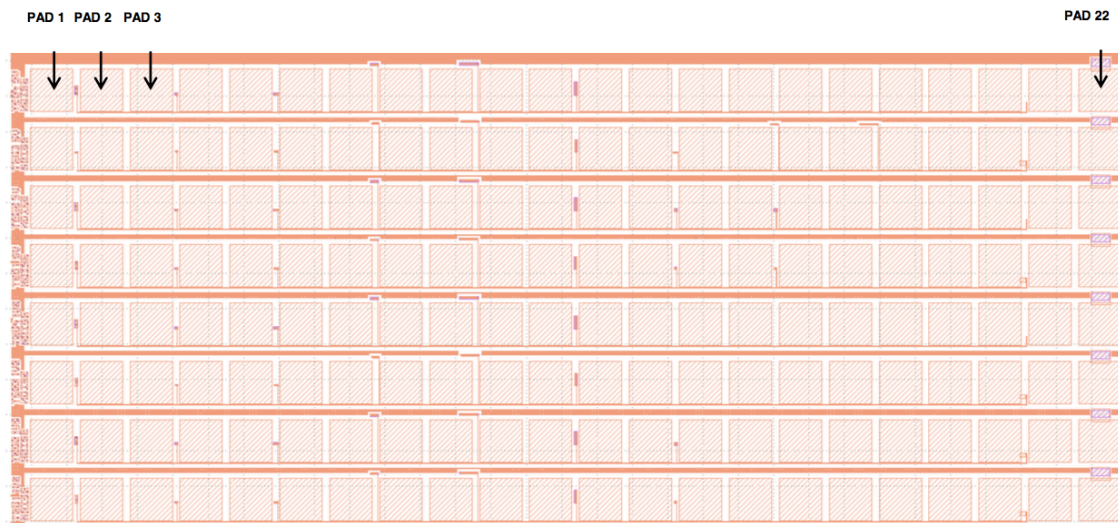
**M. Biasotti, G. Darbo, G. Gariano, A. Gaudiello, C. Gemme, P.
Morettini, L. Rossi, E. Ruscino, M. Sannino - INFN Genova**

C. Sbarra, A. Sidoti, F. Fabbri – INFN Bologna

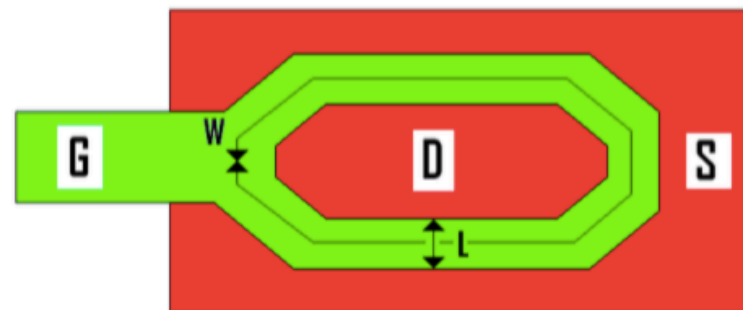
H. Shrimali, IIT Mandi

- Summary of irradiation tests
- Passive diode performance
- Hybridization
- Submission of $3 \times 4 \text{ mm}^2$ array
 - tape out 18th March
 - **Simulation covered in Federica's talk**

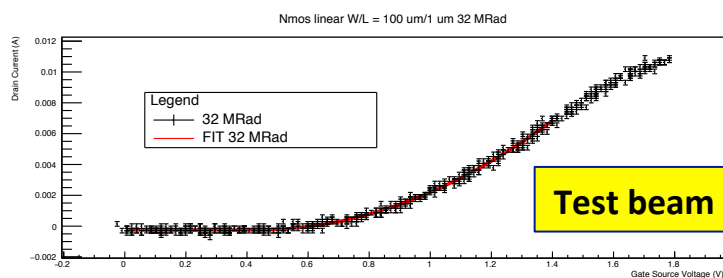
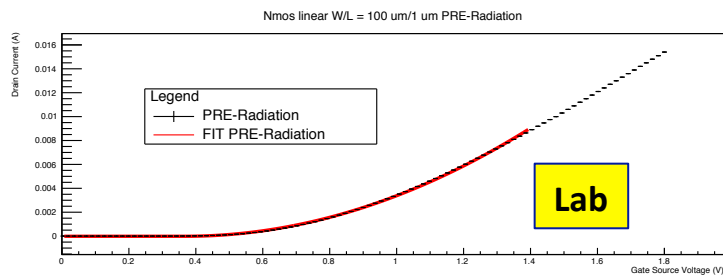
- STM designed test chip
- array of transistors with different W/L (see backup)
- **Linear** and **Enclosed Layout** designs



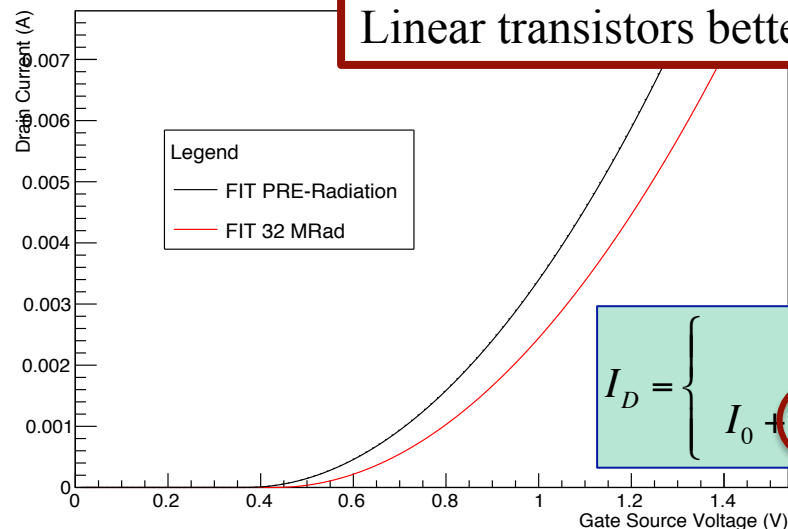
Linear Transistor



Enclosed Layout Transistor (ELT)



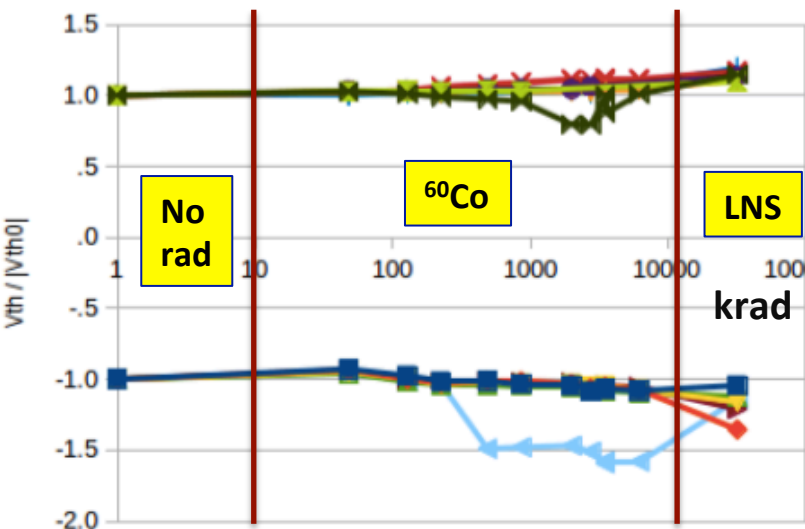
Nmos linear W/L = 100 um



No significant damage up to 32 MRad
Linear transistors better behaving than ECL

$$I_D = \begin{cases} I_0 & V_{GS} < V_{th} \\ I_0 + K(V_{GS} - V_{th})^2 & V_{GS} > V_{th} \end{cases}$$

Threshold Voltage (linear)

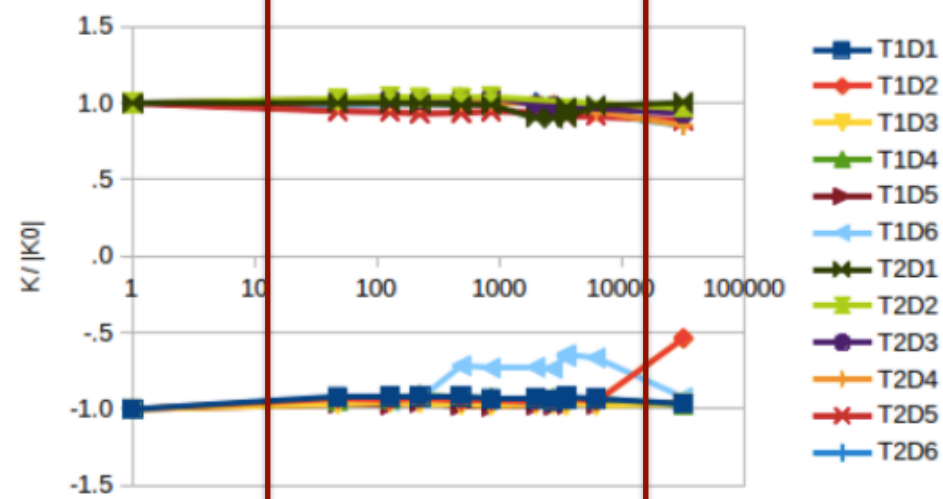


T1D1
T1D2
T1D3
T1D4
T1D5
T1D6
T2D1
T2D2
T2D3
T2D4
T2D5
T2D6

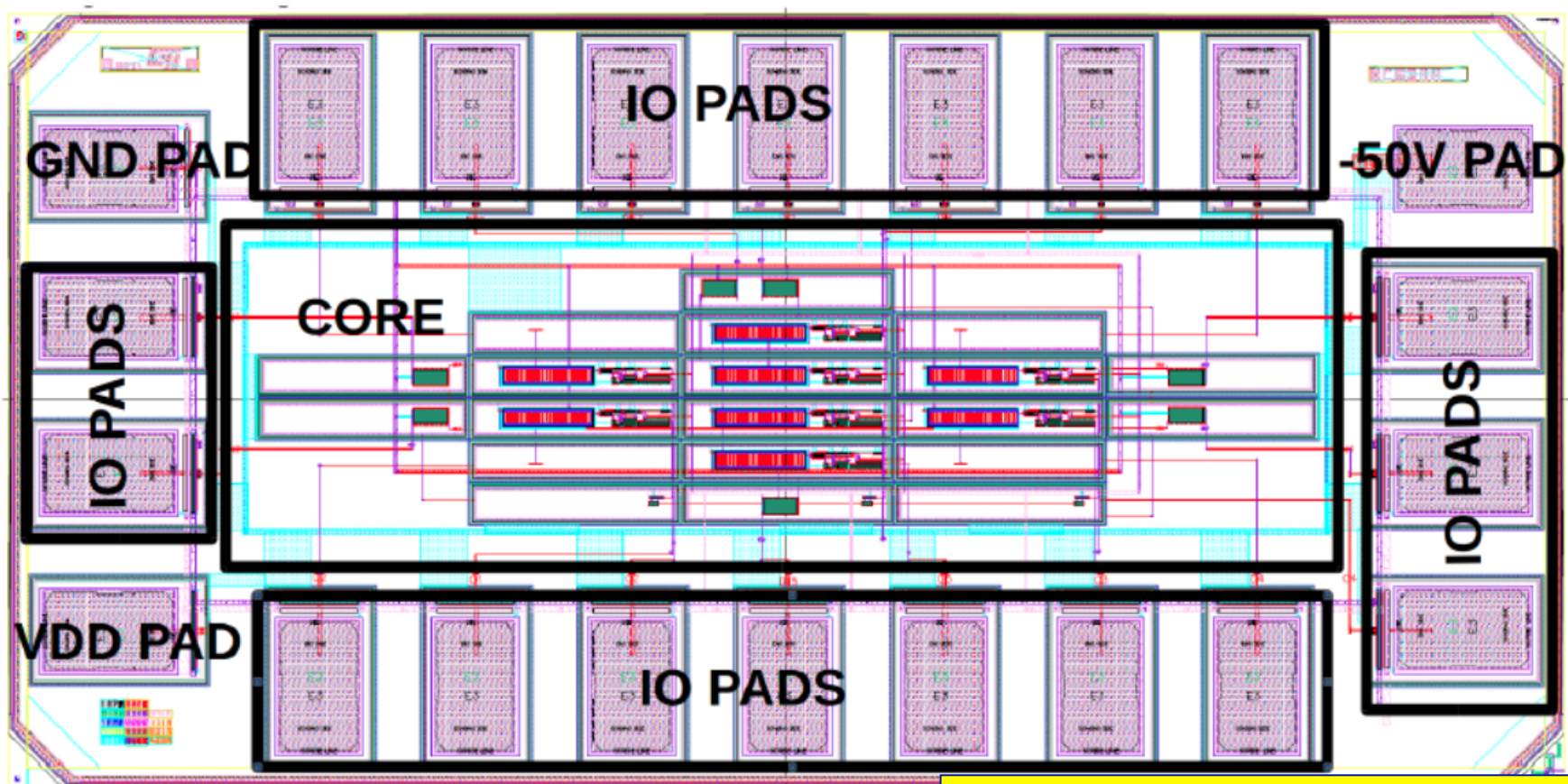
nmos

pmos

Transconductance (linear)



T1D1
T1D2
T1D3
T1D4
T1D5
T1D6
T2D1
T2D2
T2D3
T2D4
T2D5
T2D6



Layout of the STM test chip (KC53A):

- 22 I/O and VDD/GND pads
- 8 pixels ($50 \times 250 \mu\text{m}^2$): Collecting diode + Amp.
- 4 pixels ($50 \times 250 \mu\text{m}^2$): Collecting diode only

First version delivered July 2015:

- shorts between power lines and ground

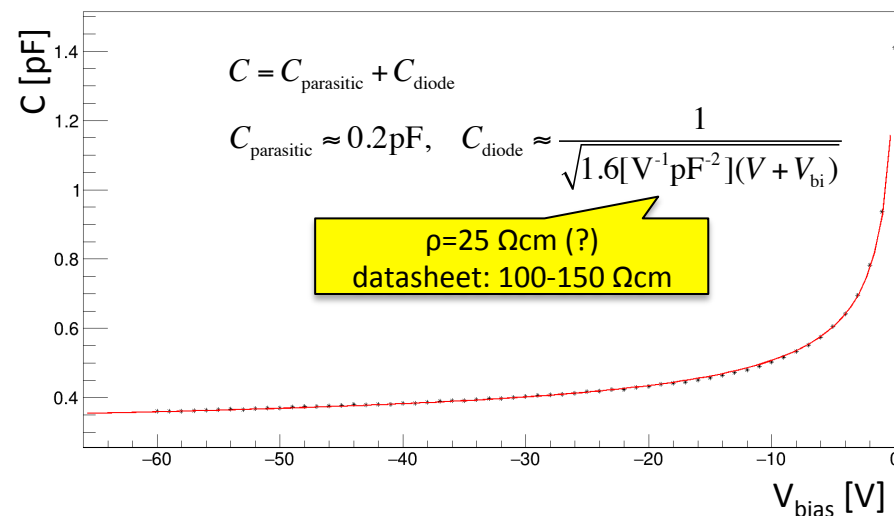
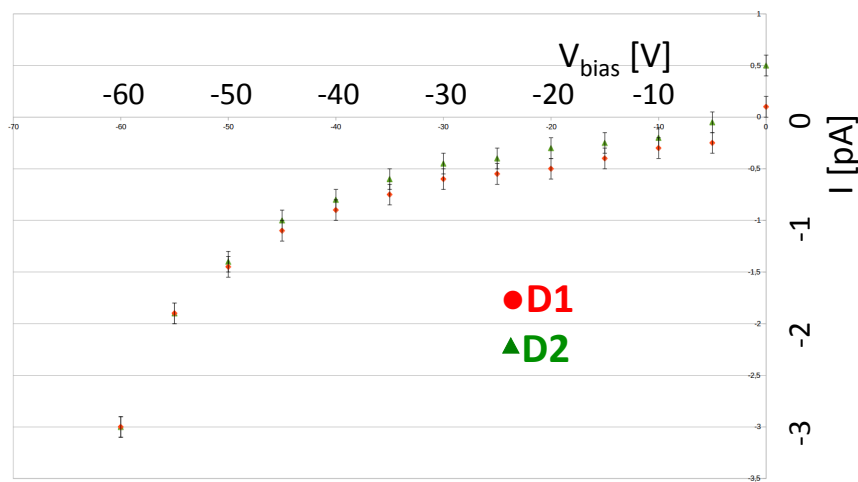
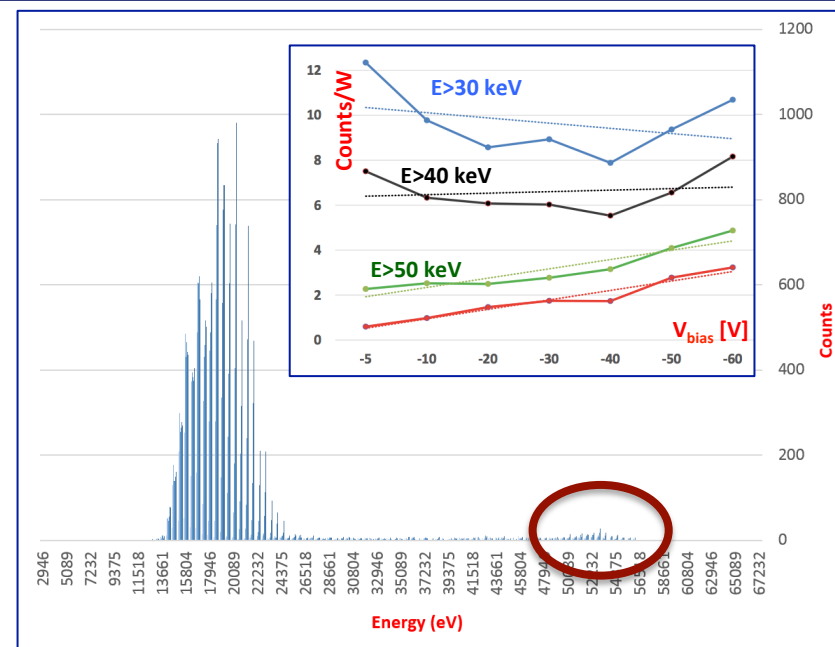
Fixed version delivered 29 Jan. 16

Design and layout by:

➤ H. Shrimali and V. Liberali (MI)

KC53A: diode characterization

- Only two passive diodes usable for tests:
 - I-V curve with backplane or front pad biasing
 - C-V characterization
 - Source measurement
 - low rate $O(10^{-2} \text{ Hz})$ due to small active region
 - in qualitative agreement with $W = 0.3 \mu\text{m} \sqrt{\rho(V + V_{bi})}$



Basic process

Spin SU-8 photoresist
Pattern pillars by mask



Glue deposition



Align & pressure

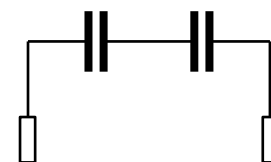
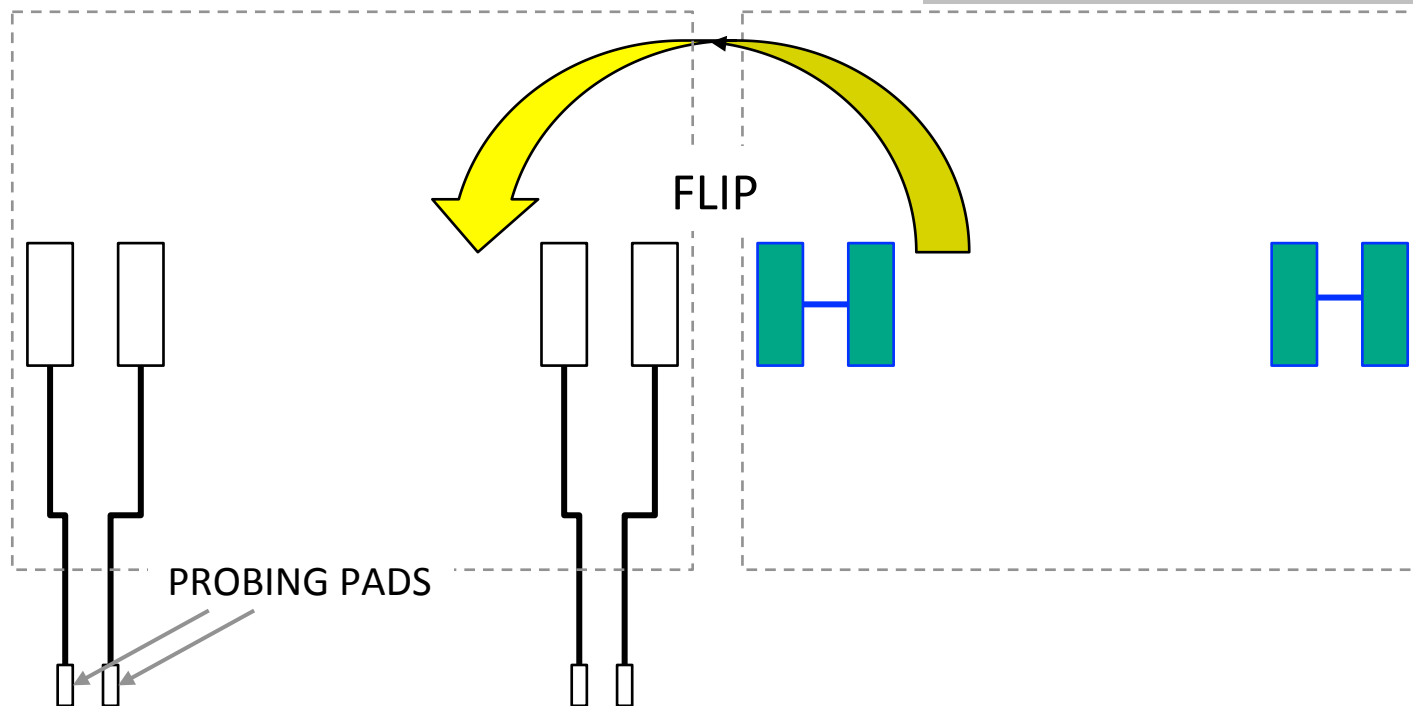
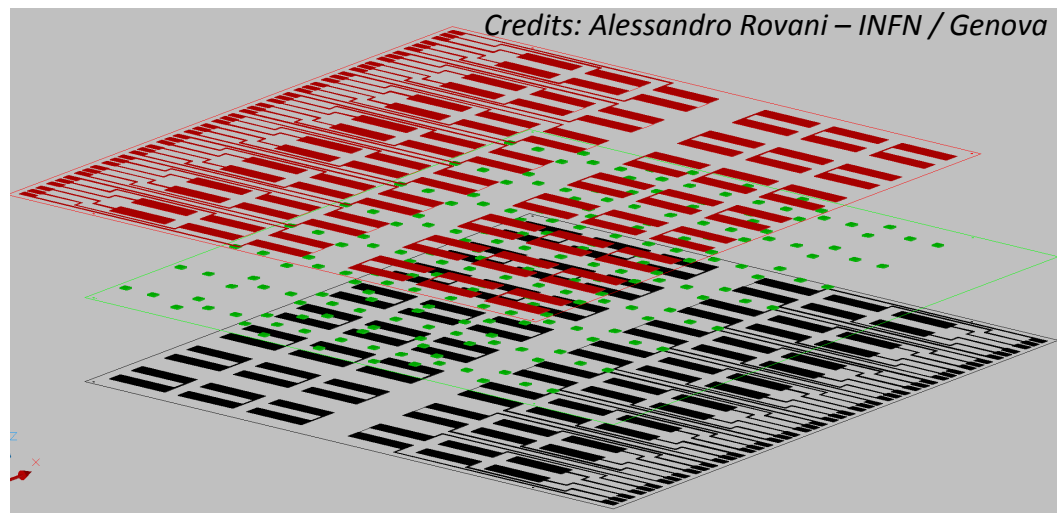


Deposition of SU8
photoresist by spinning

- In 2014 and mid 2015 test on “in-house” hybridization
 - Successful single chip assemblies and learnt on glue and SU8 deposition (spacers)
- Mid 2015 decided systematic tests on dummies
- Now systematic test on large chips (FE-I4 size) and wafer process for pillars
 - A batch of dummy wafer produces at FBK (Trento) with capacitive structures to test uniformity of glue thickness layer – **6-inch wafers, 24-32 capacitors (3-7 pF) per chip.**
 - **Wafers: CW silicon + 1 μm Oxide + 1.2 Al 1%Si (no passivation)**
 - The 6 wafers are at Selex together with pillar deposition mask – also 10 blank CW wafer provided to Selex to test SU8 spinning and photolithography – measurements of pillar uniformity will be done in Genova
 - PTA in Grenoble has been contacted for pillar deposition
 - Flip-chip at Genova and other labs – thermal/UV glue curing (preliminary studies done)
 - Electro-mechanical test, glue qualification planned on next months also in the framework of AIDA-2020 WP6.4
 - After successful testing plan to work on FE-I4 wafer (already available)

Test pillar and glue process on dummy wafers/chips

- 6-inch wafer with FE-I4 size dummies
- 32 (24) capacitors of 1 (2) mm²
- test glue thickness uniformity



Equivalent circuit
after flip $C_{\text{tot}} = \frac{1}{2} C$

- Inspired from demonstrator layout (picture below)
- Lateral space to be tuned to match alignment with FE-I4
- Leftover space at bottom of pixel region is only 20 μm , may be increased in multiple of the 50 μm pixel size.

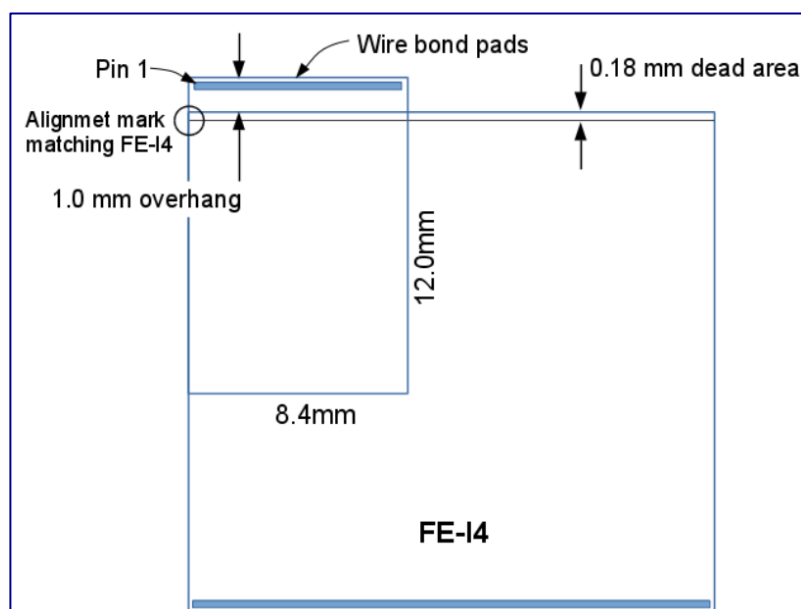
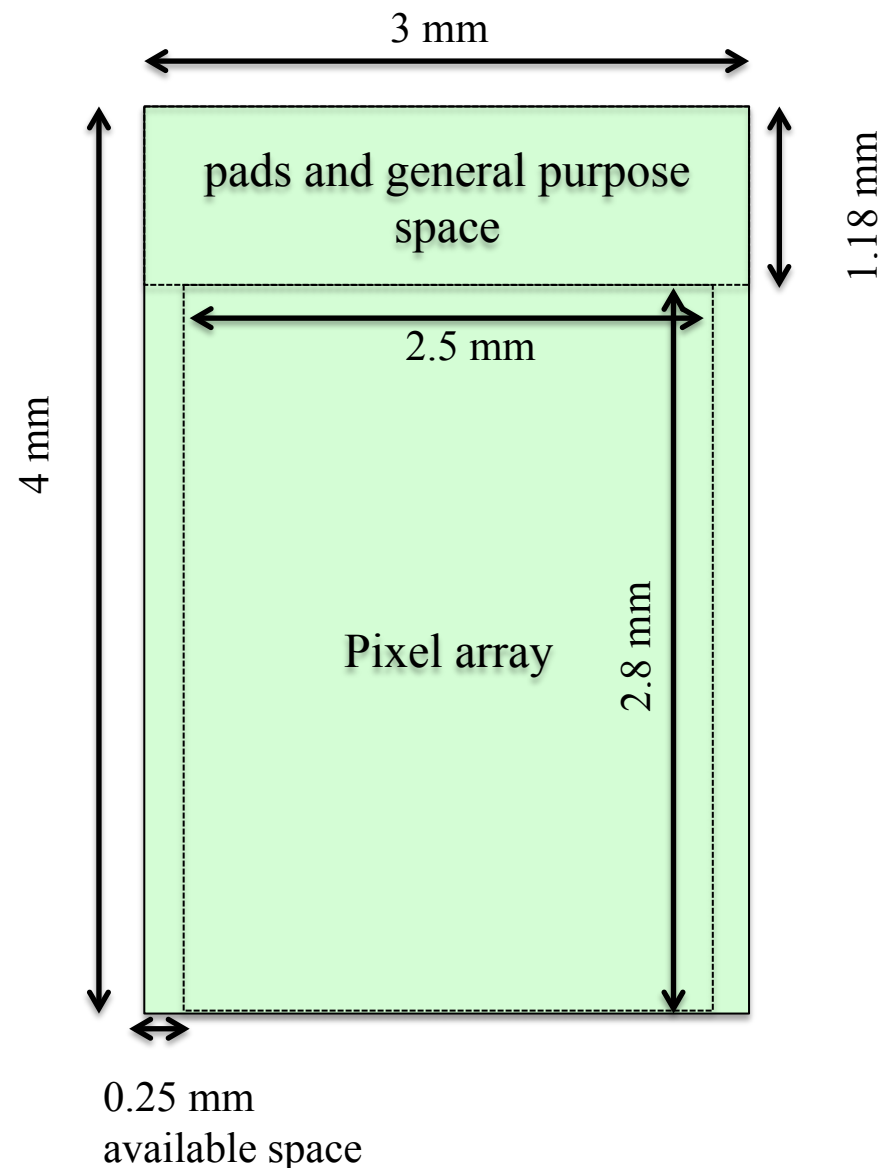
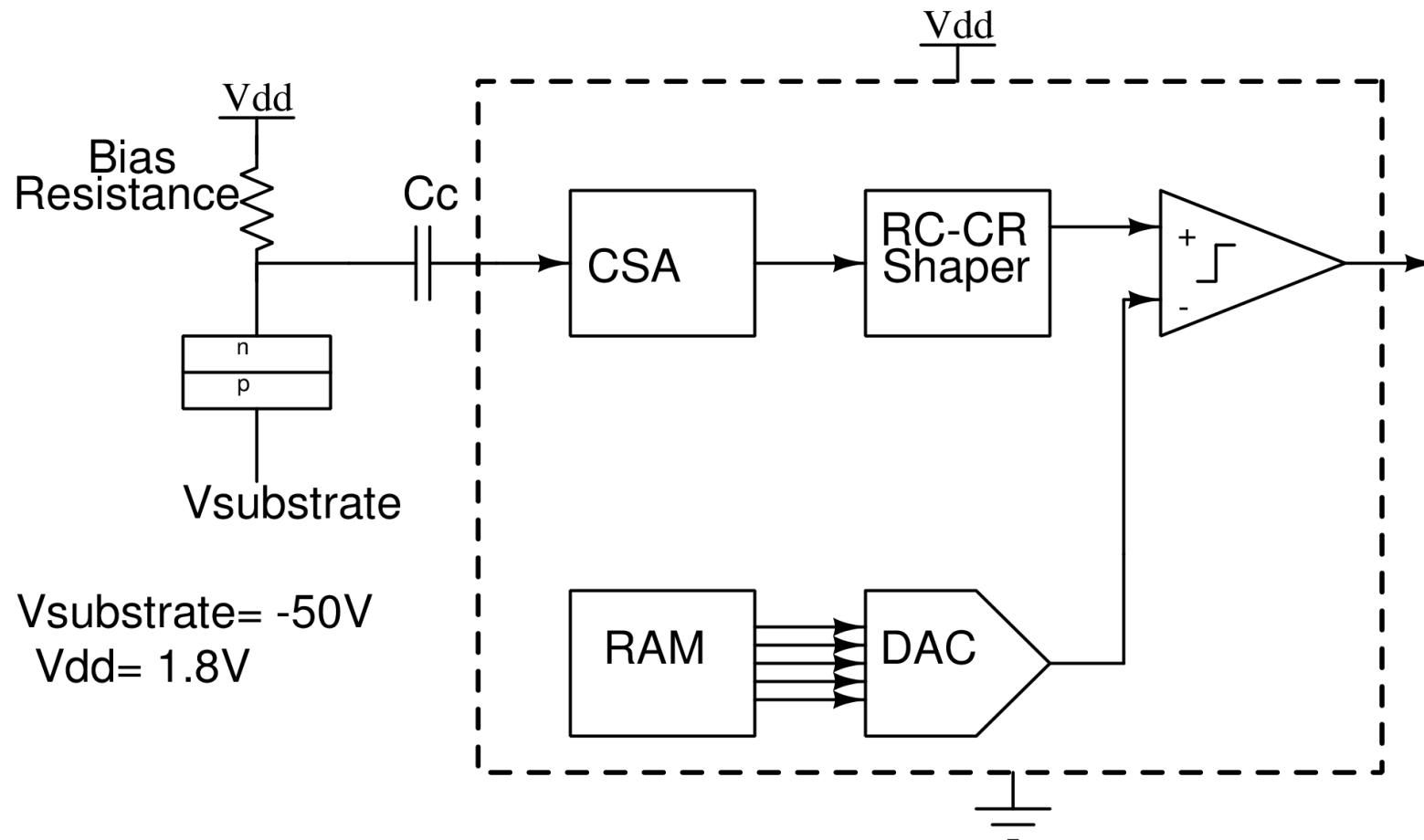


Fig. 1: Alignment of demonstrator to FE-I4 chip





Genova + Mandi + Milano

Device	Param	Noise Contribution	% Of Total
M30.m1	fn	0.00689093	26.71
M30.m1	id	0.00646208	23.48
M5.m1	id	0.00420071	9.92
M5.m1	fn	0.0036419	7.46
M41.m1	id	0.00333666	6.26
M41.m1	fn	0.00273693	4.21
M2.m1	fn	0.00238552	3.20
M1.m1	id	0.00235236	3.11
M3.m1	fn	0.0021559	2.61
M21.m1	id	0.00191197	2.06

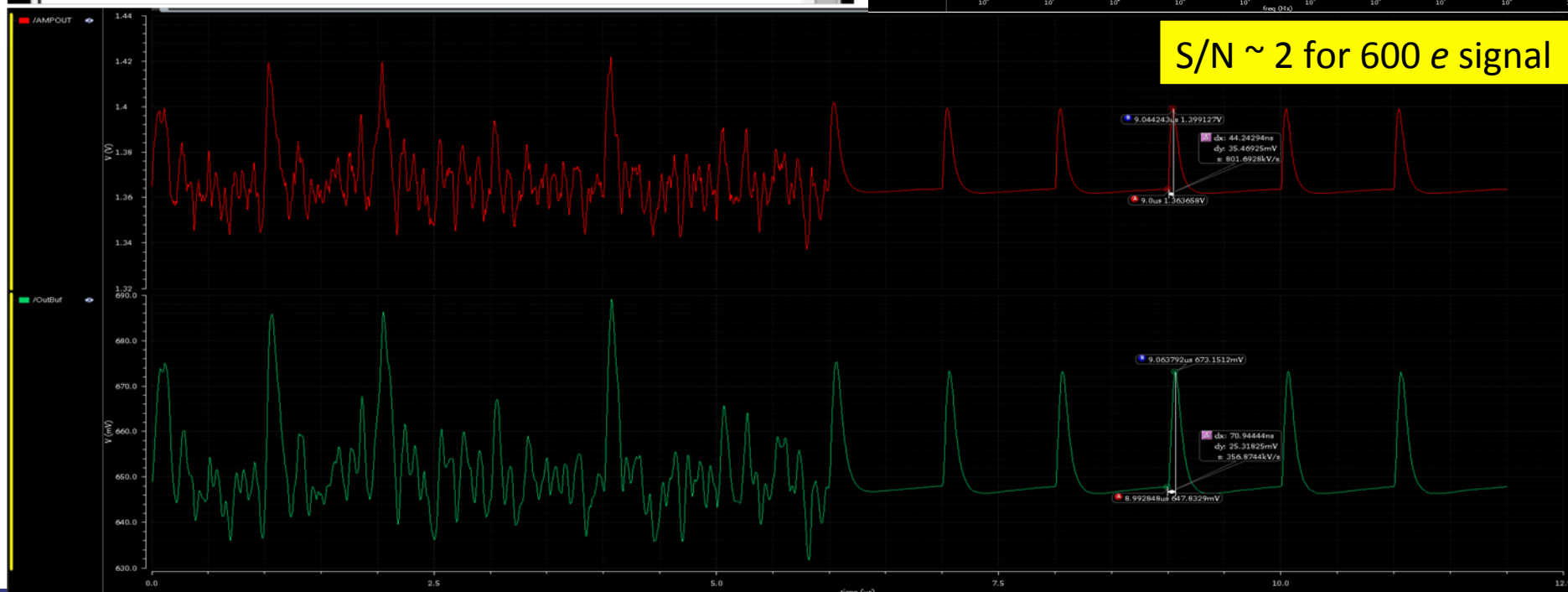
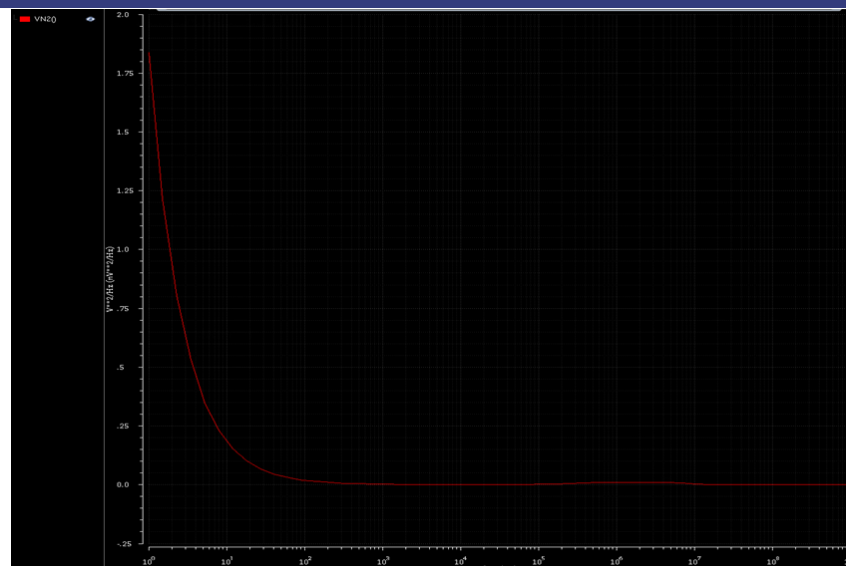
Integrated Noise Summary (in V) Sorted By Noise Contributors

Total Summarized Noise = 0.0133346

Total Input Referred Noise = 0.000239562

line above noise summary info is for noise data


← =239uV ~ VIN



- BCD8 now available also through CMP

- easier to get new people started
- increase of costs with respect to initial informal contacts:

- 2600 Euro/mm²
if Area ≤ 5 mm²
- 13000 Euro
+ [(Area-5) * 2100 Euro]
if 5 mm² < Area < 15 mm²



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CMP is a service organization in ICs and MEMS for prototyping and low volume production. Circuits are fabricated for Universities, Research Laboratories and Industrial companies.

Advanced industrial technologies are available in CMOS, SiGe BiCMOS, HV-CMOS, SOI, MEMS, 3D-IC, etc. CMP distributes and supports several CAD software tools for both Industrial Companies and Universities.

Since 1981, more than 1000 Institutions from 71 countries have been served, more than 7275 projects have been prototyped through 952 runs, and 60 different technologies have been interfaced.

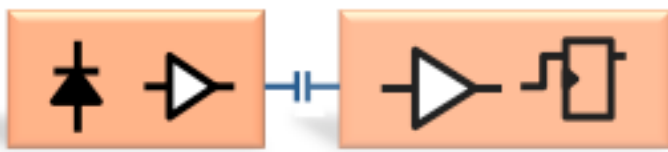


2016

MPW runs schedule

tech	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
CMOS												
C180A 0.18 µm CMOS	18		17		16		15		14		13	
N180A 0.18 µm HV-CMOS	19		18		17		16		15		14	
C170A 0.17 µm CMOS	25		24		23		22		21		20	
C170A01 0.17 µm CMOS 0.018	25		24		23		22		21		20	
C160A 0.16 µm CMOS	29		28		27		26		25		24	
C160A01 0.16 µm CMOS 0.018	29		28		27		26		25		24	
C150A 0.15 µm CMOS	29		28		27		26		25		24	
C150A01 0.15 µm CMOS 0.018	29		28		27		26		25		24	
C140A 0.14 µm CMOS	29		28		27		26		25		24	
C140A01 0.14 µm CMOS 0.018	29		28		27		26		25		24	
C130A 0.13 µm CMOS	29		28		27		26		25		24	
C130A01 0.13 µm CMOS 0.018	29		28		27		26		25		24	
C120A 0.12 µm CMOS	29		28		27		26		25		24	
C120A01 0.12 µm CMOS 0.018	29		28		27		26		25		24	
C110A 0.11 µm CMOS	29		28		27		26		25		24	
C110A01 0.11 µm CMOS 0.018	29		28		27		26		25		24	
C100A 0.10 µm CMOS	29		28		27		26		25		24	
C100A01 0.10 µm CMOS 0.018	29		28		27		26		25		24	
C90A 0.09 µm CMOS	29		28		27		26		25		24	
C90A01 0.09 µm CMOS 0.018	29		28		27		26		25		24	
C80A 0.08 µm CMOS	29		28		27		26		25		24	
C80A01 0.08 µm CMOS 0.018	29		28		27		26		25		24	
C70A 0.07 µm CMOS	29		28		27		26		25		24	
C70A01 0.07 µm CMOS 0.018	29		28		27		26		25		24	
C60A 0.06 µm CMOS	29		28		27		26		25		24	
C60A01 0.06 µm CMOS 0.018	29		28		27		26		25		24	
C50A 0.05 µm CMOS	29		28		27		26		25		24	
C50A01 0.05 µm CMOS 0.018	29		28		27		26		25		24	
C40A 0.04 µm CMOS	29		28		27		26		25		24	
C40A01 0.04 µm CMOS 0.018	29		28		27		26		25		24	
C30A 0.03 µm CMOS	29		28		27		26		25		24	
C30A01 0.03 µm CMOS 0.018	29		28		27		26		25		24	
C20A 0.02 µm CMOS	29</											

- No problems observed in first irradiation tests
- Detected signal from passive diodes
 - still to fully understand depletion depth and rate
 - TCAD / Geant4 simulations (help welcome)
- In-house hybridization test satisfactory,
 - dummy wafers for FE-I4 size tests produced
- Fixed KC53AB received:
 - need to test if working properly
 - compare performance to Cadence simulation
 - plan complete set of irradiation tests
- Large pixel matrix to be submitted by mid-March
 - can be matched to FE-I4 chips



HVR - CCPD

INFN

BACKUP

High Voltage and High Resistivity CMOS Capacitively Coupled Pixel Detector

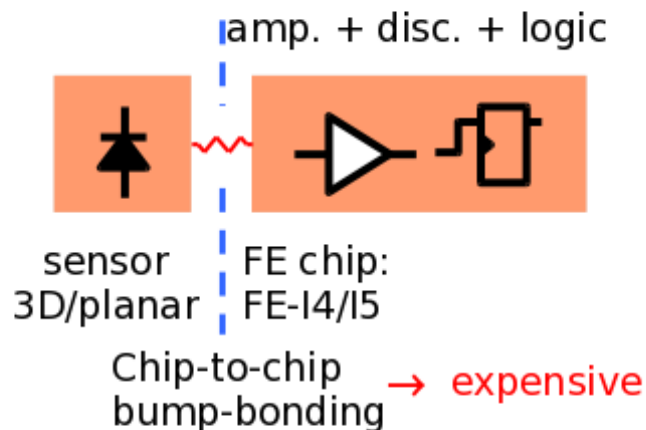
INFN CSN5 project, 2015-2017

INFN branches: Bologna, Genova, Milano

Purpose:

- To prototype an active CCPD (Capacitive Coupled Pixel Detector) by developing, testing and characterizing an **HV/HR-CMOS design** and its **integration** with a pixel detector chip for R/O. Initially the R/O chip will be the ATLAS FE-I4 and will be then moved to the RD53 (CHIPIX65) design, when this will become available.
- Aiming to large area, high rate, **high radiation environment** applications (High-Luminosity LHC as a reference benchmark)

Standard hybrid pixels



Pro's

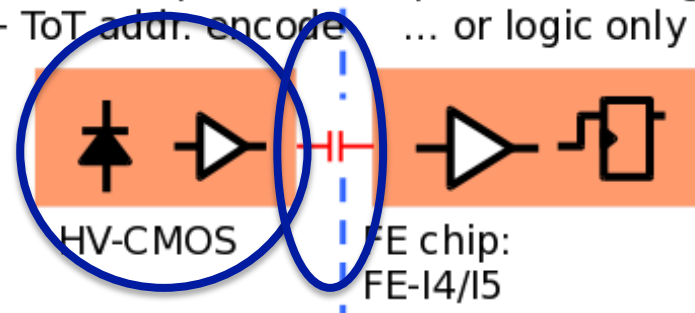
Mature technology
Radiation hard
Multi-chip modules

Con's

Sensor/bump cost
4" ÷ 6" sensor wafer
Spatial resolution
Cost/yield of BB

HV-CMOS hybrid pixels

diode + amp. + disc. + logic
+ ToT addr. encode ... or logic only



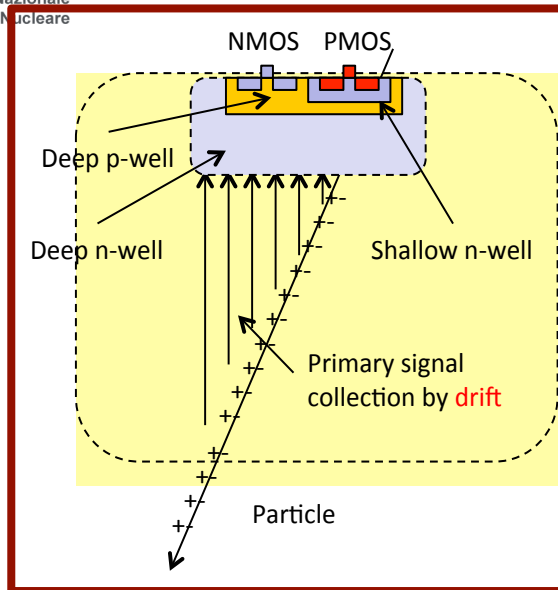
Wafer-to-wafer
gluing
... or chip-to-chip → simpler/cheaper ?

Pro's

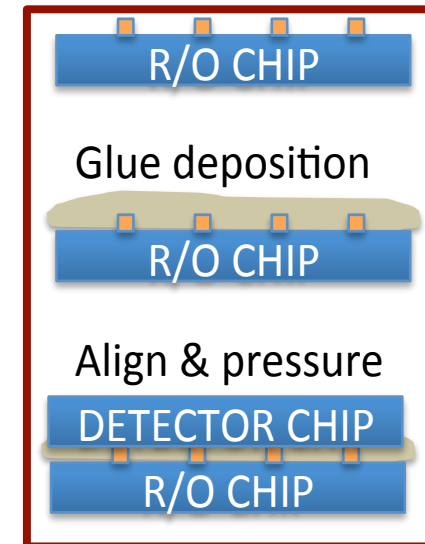
8" (or 12") HV-CMOS wafers
"Standard" IC process
Cheap BB (to demonstrate)
Small pixel → resolution

Con's

Novel technology
Small charge (800 ÷ 1500 e)
Extreme radiation ?
Single chip
(multi-chip difficult)

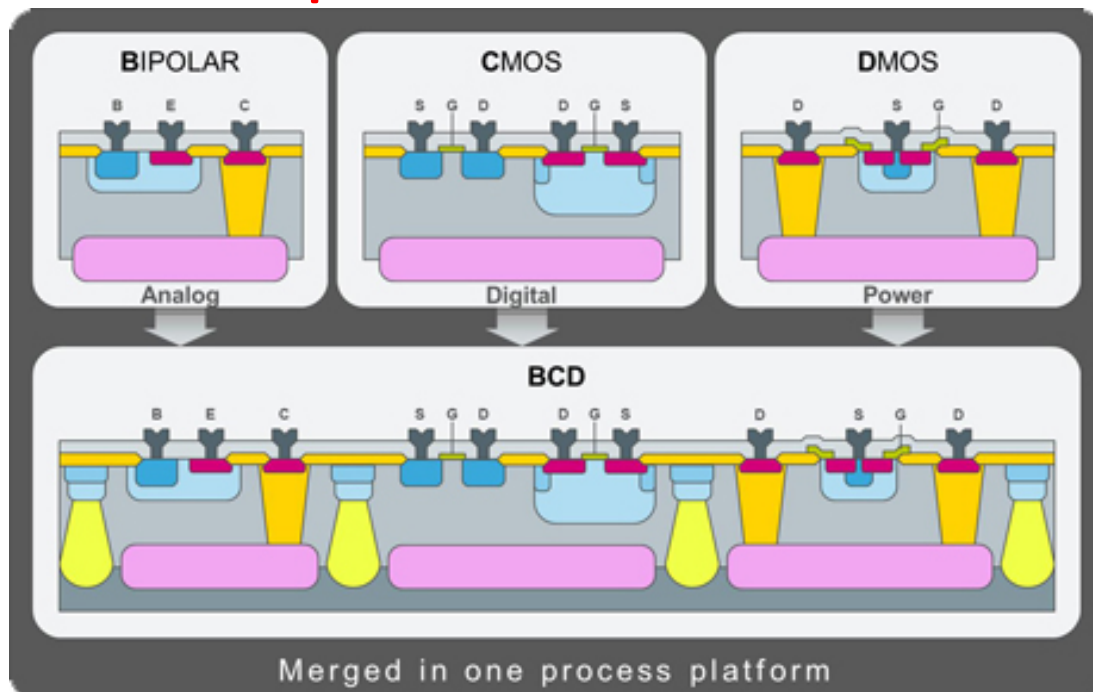


- In standard CMOS detectors charge generated by energy deposition is collected by **diffusion**.
- Combining commercial technologies sustaining HV (50-70 V) with high resistivity substrates results in a depleted (15-30 μm) region, where charge is collected by **drift**.
- Same advantages of CMOS detectors (*cheap, thin*)
- In addition: **larger and faster signals** and **better radiation tolerance**.



- Signal amplification on CMOS detectors allows **AC coupling** between the sensor and the readout chip:
 - **simpler** and **cheaper** than bump-bonding
 - **independent from density of pixels**
- Controlled flip-chip process:
 - growing of spacers in epoxy material (SU8) to control glue (dielectric) thickness
 - characterization of coupling, uniformity, radiation tolerance in single dies
 - **wafer level processing in external firms.**

BCD = Bipolar + CMOS + DMOS



	HIGH DENSITY	HIGH VOLTAGE
0.32μm	BCD6/6s 20/45/70/100V	BCD6s-Offline 800V BCD6s-SOI 100/190V
0.16μm	BCD8/8s 8/20/40/70V	BCD8s-SOI 300V BCD8sP 8/18/25/42V
0.11μm		BCD9s 20/40/65V
90nm		BCD10
Timeline	AVAILABLE	
	IN DEVELOPMENT	

http://www.st.com/web/en/about_st/bcd.html

- Among the competing technologies BCD8 has several appealing features:
 - availability of different devices integrated in the same process
 - epitaxial process:** can easily grow on different substrates.
 - possible to reach thick depletion layers: 30 μm looks an optimal compromise between signal and material thickness of the detector
 - long-term availability:** it is one of the major production line for ST automotive products.