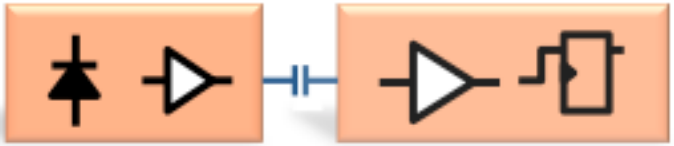


HVR - CCPD

HVR_CCPD

ATLAS ITK Italy meeting, 02/02/2016

Attilio Andreazza, M. Citterio, V. Liberali, C. Meroni, F. Ragusa, E. Zaffaroni - INFN Milano

M. Biasotti, G. Darbo, G. Gariano, A. Gaudiello, C. Gemme, P. Morettini, L. Rossi, E. Ruscino, M. Sannino - INFN Genova

C. Sbarra, A. Sidoti, F. Fabbri – INFN Bologna

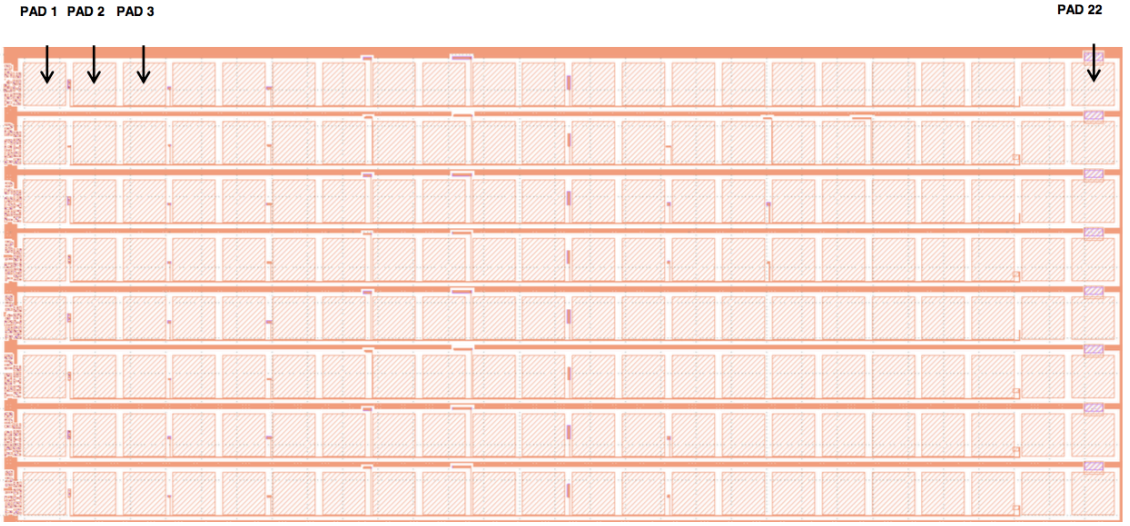
H. Shrimali, IIT Mandi

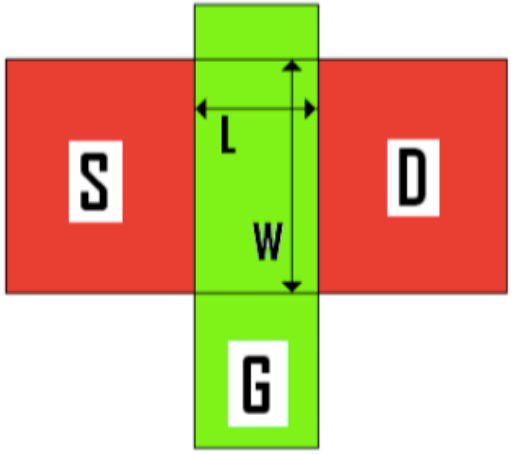
Overview

- Summary of irradiation tests
- Passive diode performance
- Hybridization
- Submission of 3×4 mm^2 array
  - tape out 18th March
  - **Simulation covered in Federica's talk**

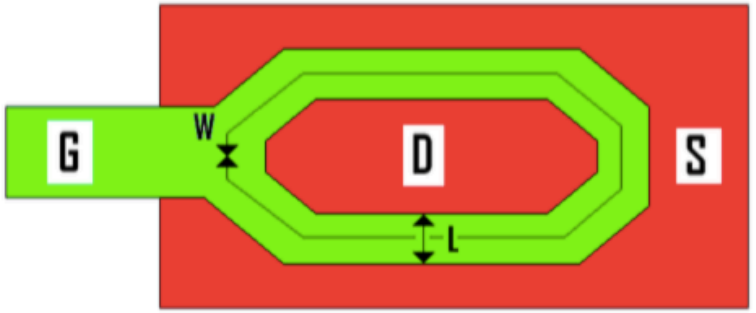
STMicroelectronics KC01

- STM designed test chip
- array of transistors with different W/L
  (see backup)
- **Linear** and **Enclosed Layout** designs





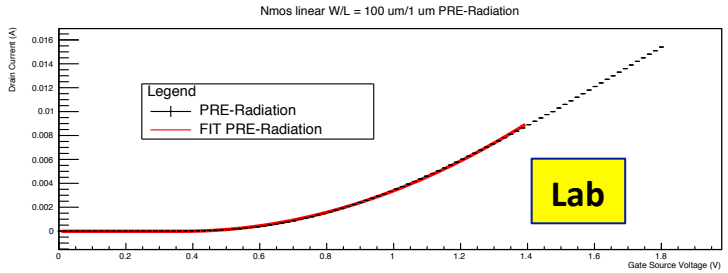
Linear Transistor

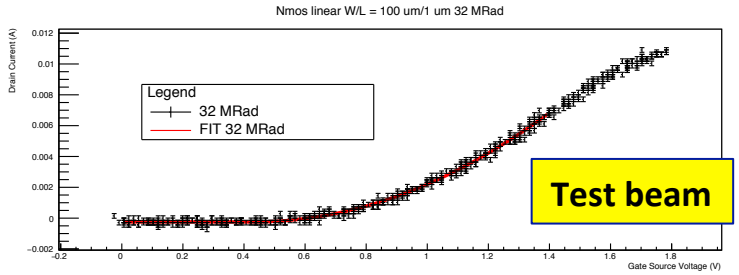


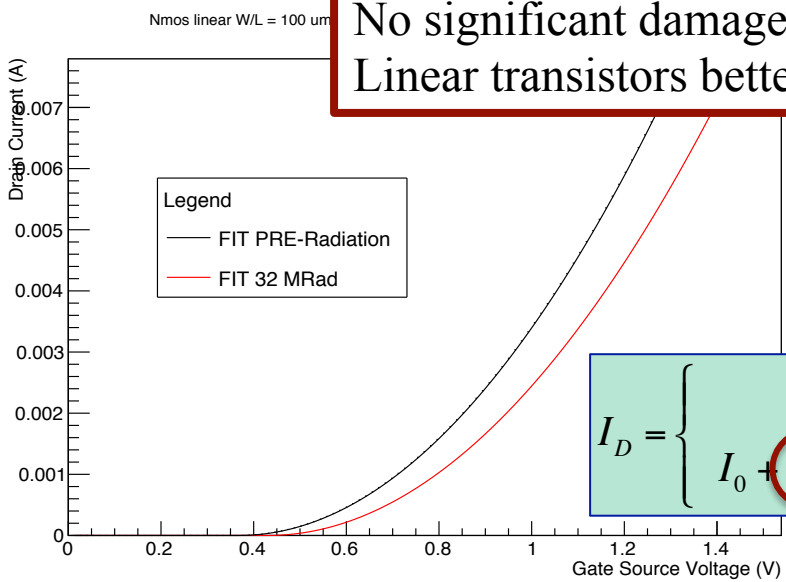
Enclosed Layout Transistor (ELT)

Irradiation 2015

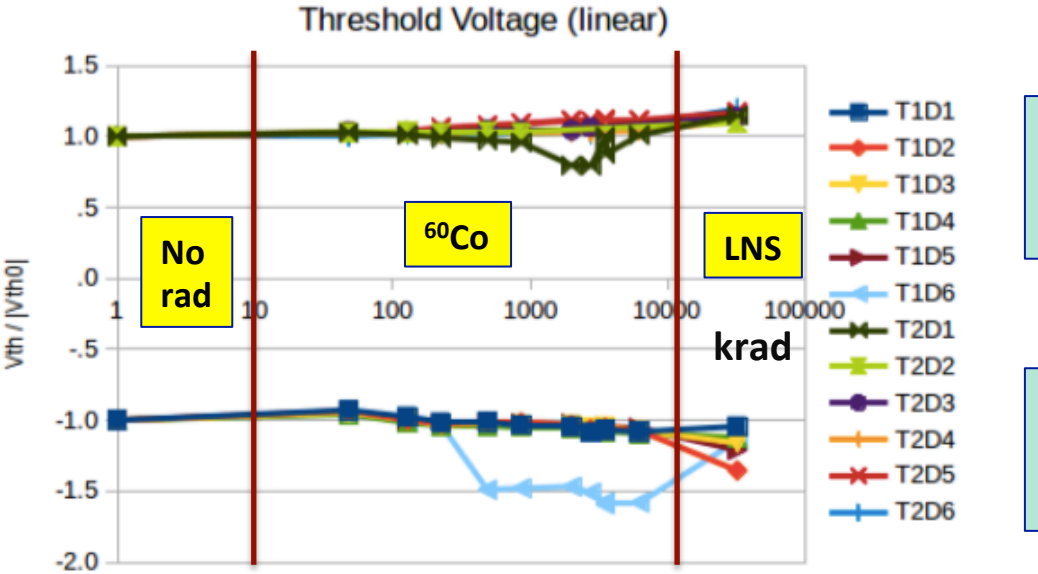
No significant damage up to 32 MRad
Linear transistors better behaving than ECL





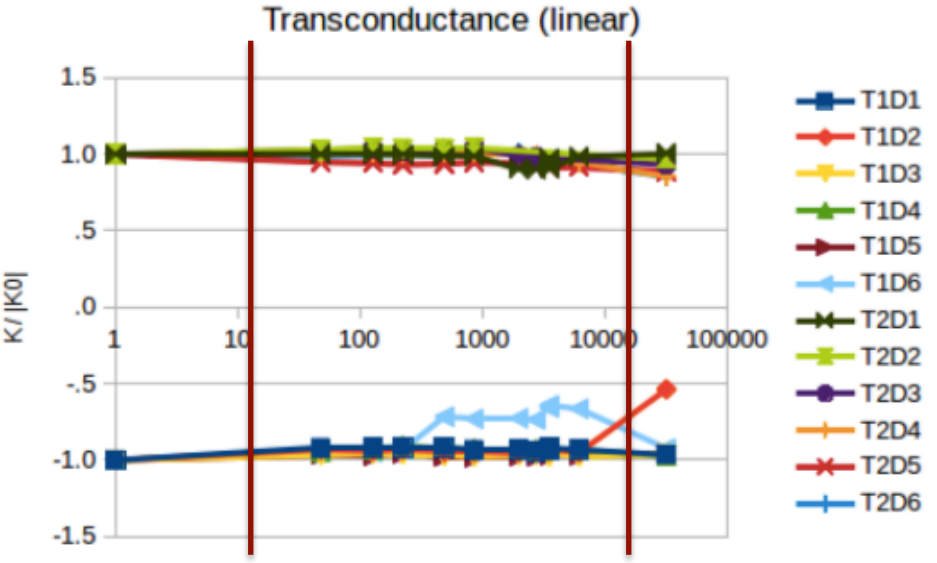


$$I_D = \begin{cases} I_0 & V_{GS} < V_{th} \\ I_0 + K(V_{GS} - V_{th})^2 & V_{GS} > V_{th} \end{cases}$$

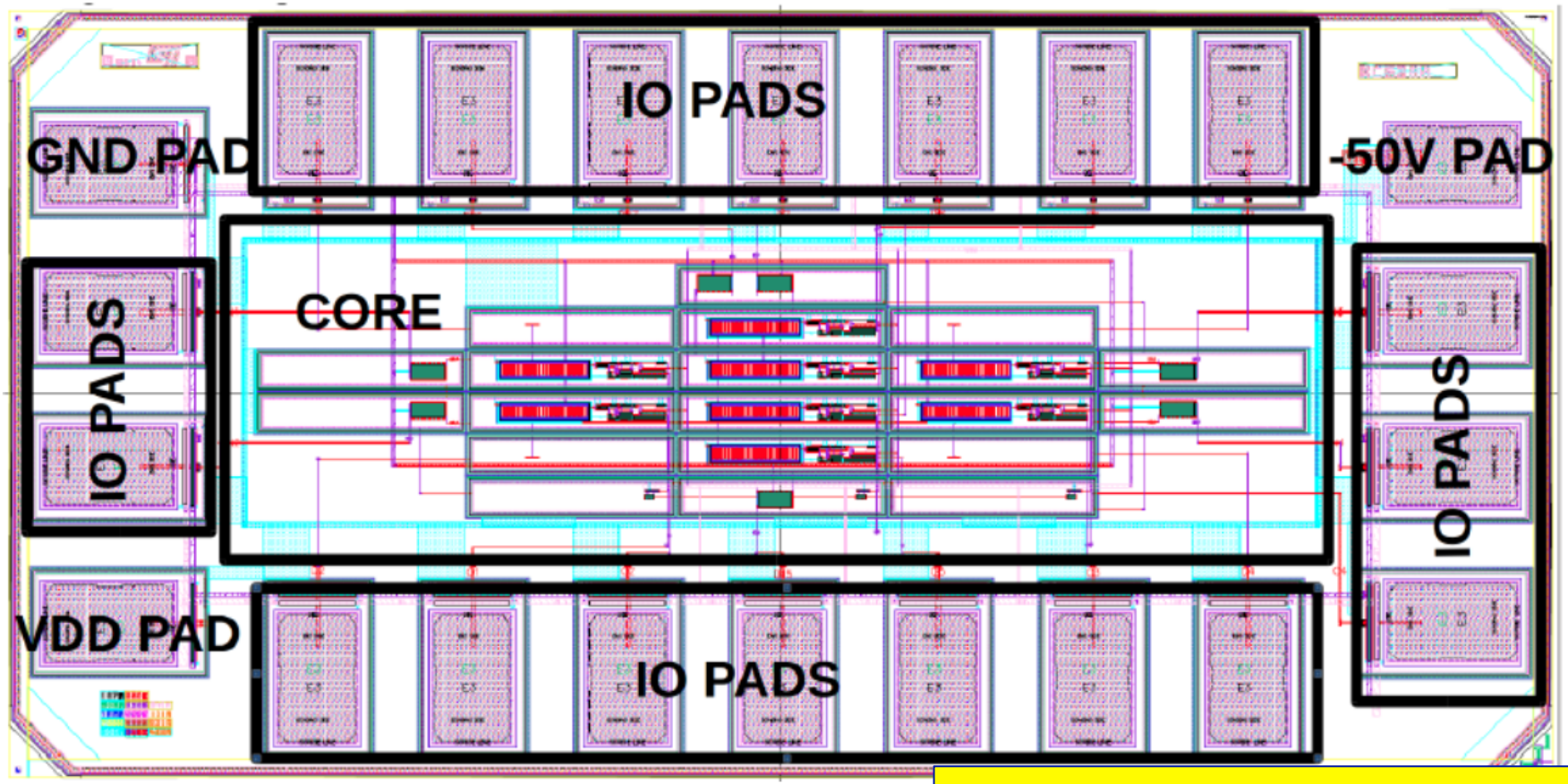


nmos

pmos



KC35A



Layout of the STM test chip (KC53A):

- *22 I/O and VDD/GND pads*
- *8 pixels (50 x 250 μm²): Collecting diode + Amp.*
- *4 pixels (50 x 250 μm²): Collecting diode only*

First version delivered July 2015:

- shorts between power lines and ground

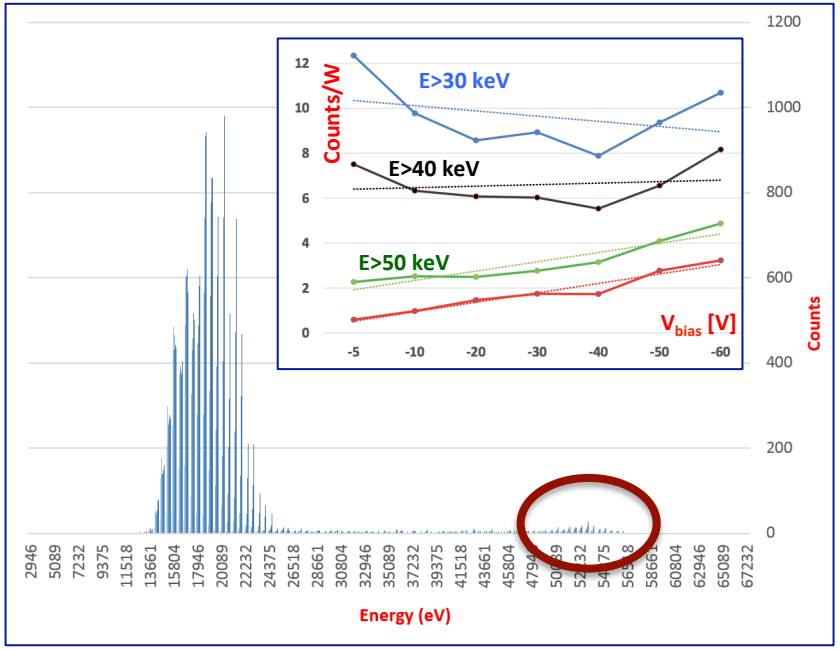
Fixed version delivered 29 Jan. 16

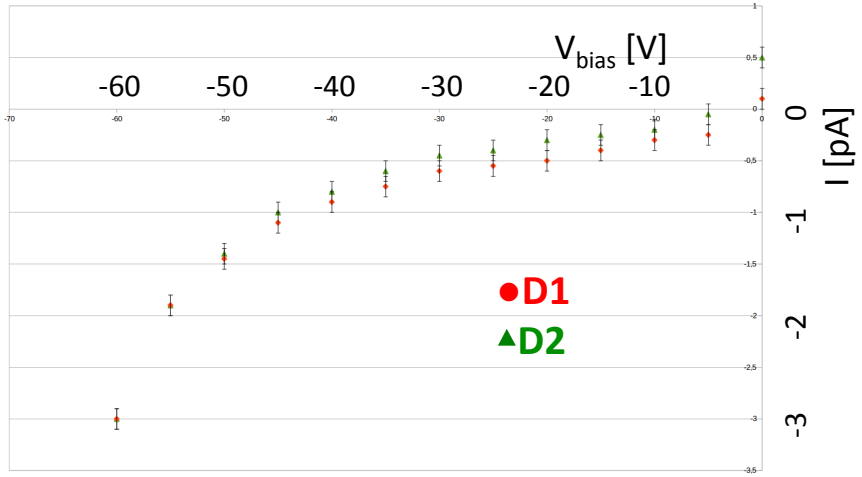
Design and layout by:

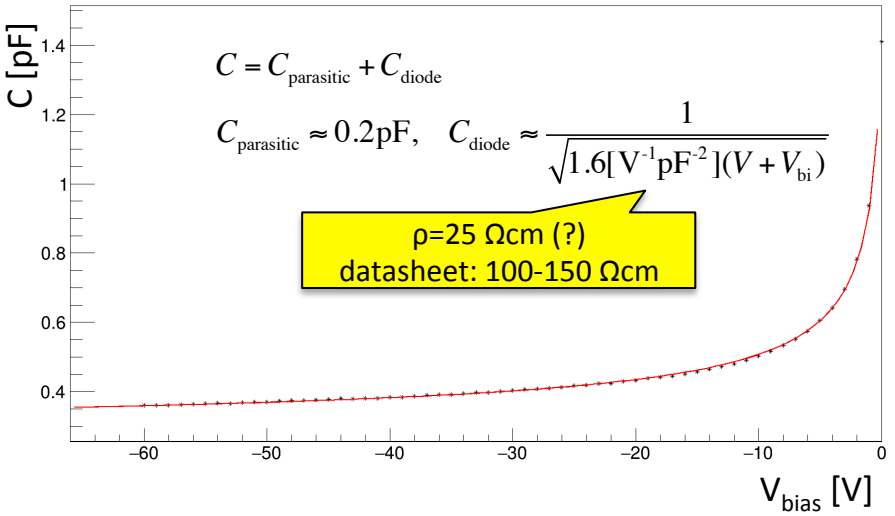
- *H. Shrimali and V. Liberali (MI)*

KC53A: diode characterization

- Only two passive diodes usable for tests:
  - I-V curve with backplane or front pad biasing
  - C-V characterization
  - Source measurement
    - low rate O(10^{-2} Hz) due to small active region
    - in qualitative agreement with $W = 0.3\mu\mathrm{m}\sqrt{\rho(V+V_{\mathrm{bi}})}$







Hybridization

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

Align & pressure

Deposition of SU8 photoresist by spinning

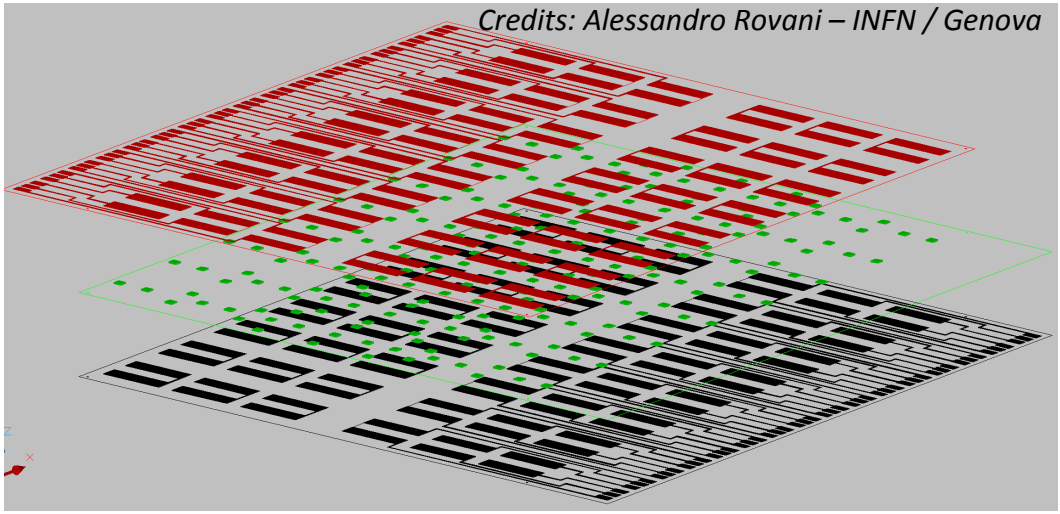
- In 2014 and mid 2015 test on "in-house" hybridization
  - Successful single chip assemblies and learnt on glue and SU8 deposition (spacers)
- Mid 2015 decided systematic tests on dummies
- Now systematic test on large chips (FE-I4 size) and wafer process for pillars
  - A batch of dummy wafer produces at FBK (Trento) with capacitive structures to test uniformity of glue thickness layer – **6-inch wafers, 24-32 capacitors (3-7 pF) per chip**.
  - Wafers: CW silicon + 1 µm Oxide + 1.2 Al 1%Si (no passivation)
  - The 6 wafers are at Selex together with pillar deposition mask – also 10 blank CW wafer provided to Selex to test SU8 spinning and photolithography – measurements of pillar uniformity will be done in Genova
  - PTA in Grenoble has been contacted for pillar deposition
  - Flip-chip at Genova and other labs – thermal/UV glue curing (preliminary studies done)
  - Electro-mechanical test, glue qualification planned on next months also in the framework of AIDA-2020 WP6.4
  - After successful testing plan to work on FE-I4 wafer (already available)

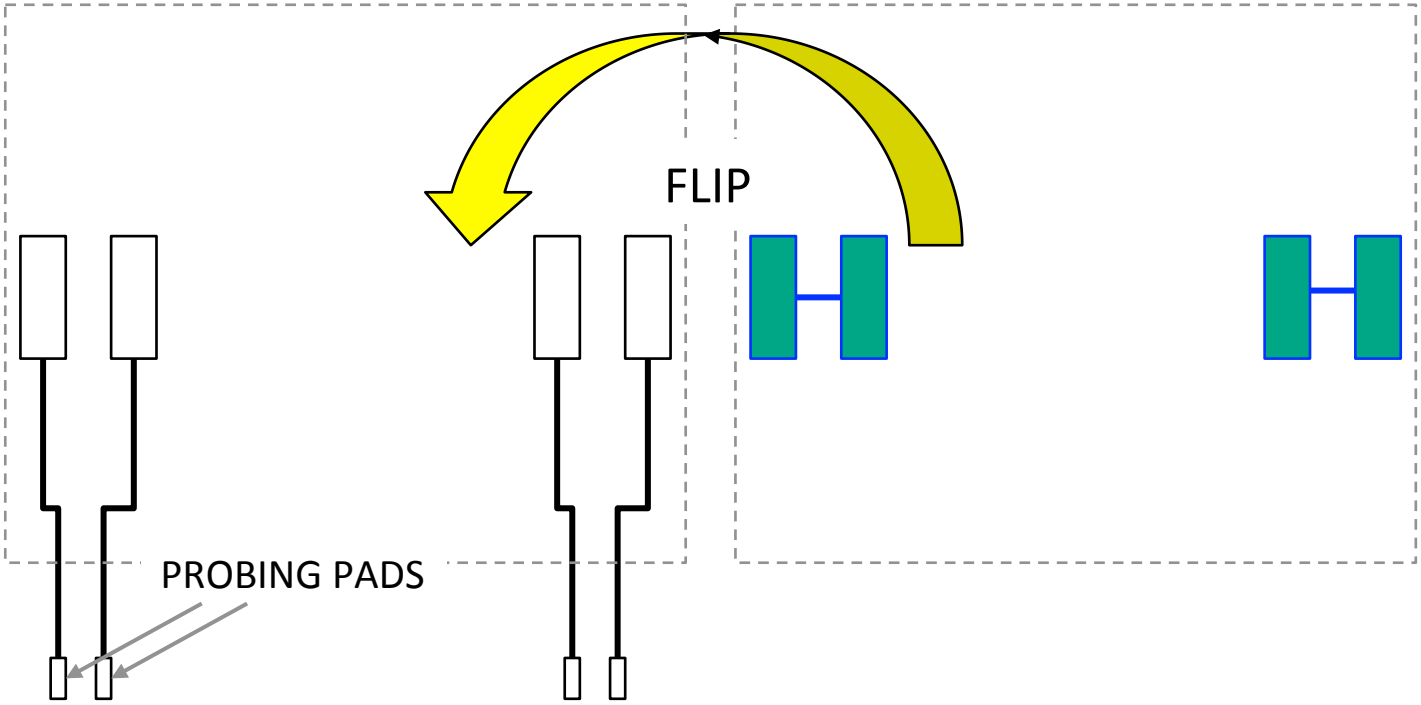
Hybridization: dummy wafers

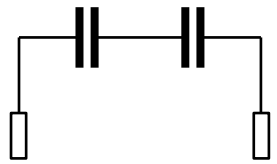
Istituto Nazionale di Fisica Nucleare

Test pillar and glue process on dummy wafers/chips

- 6-inch wafer with FE-I4 size dummies
- 32 (24) capacitors of 1 (2) mm^2
- test glue thickness uniformity







Equivalent circuit after flip C_{tot} = ½ C

TPM1 layout

- Inspired from demonstrator layout (picture below)
- Lateral space to be tuned to match alignment with FE-I4
- Leftover space ad bottom of pixel region is only 20 µm, may be increased in multiple of the 50 µm pixel size.

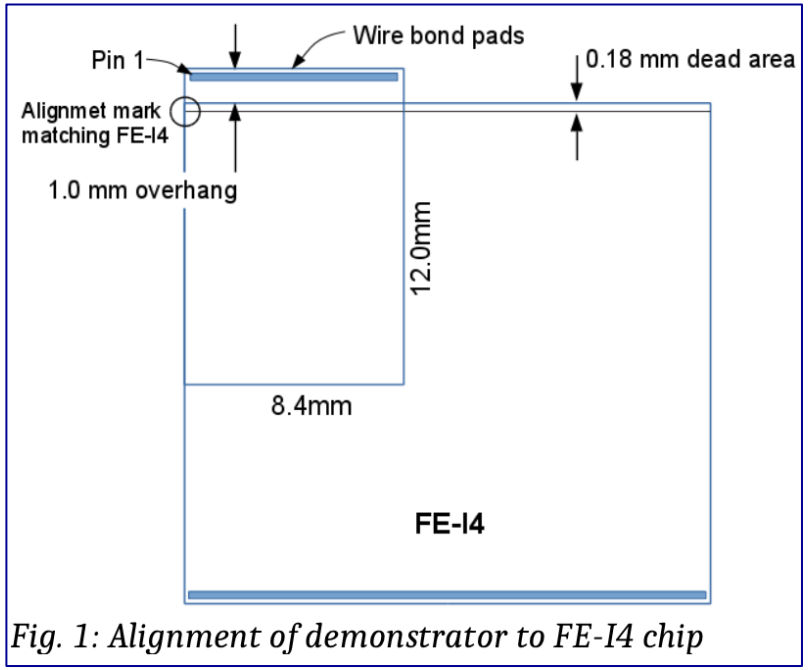
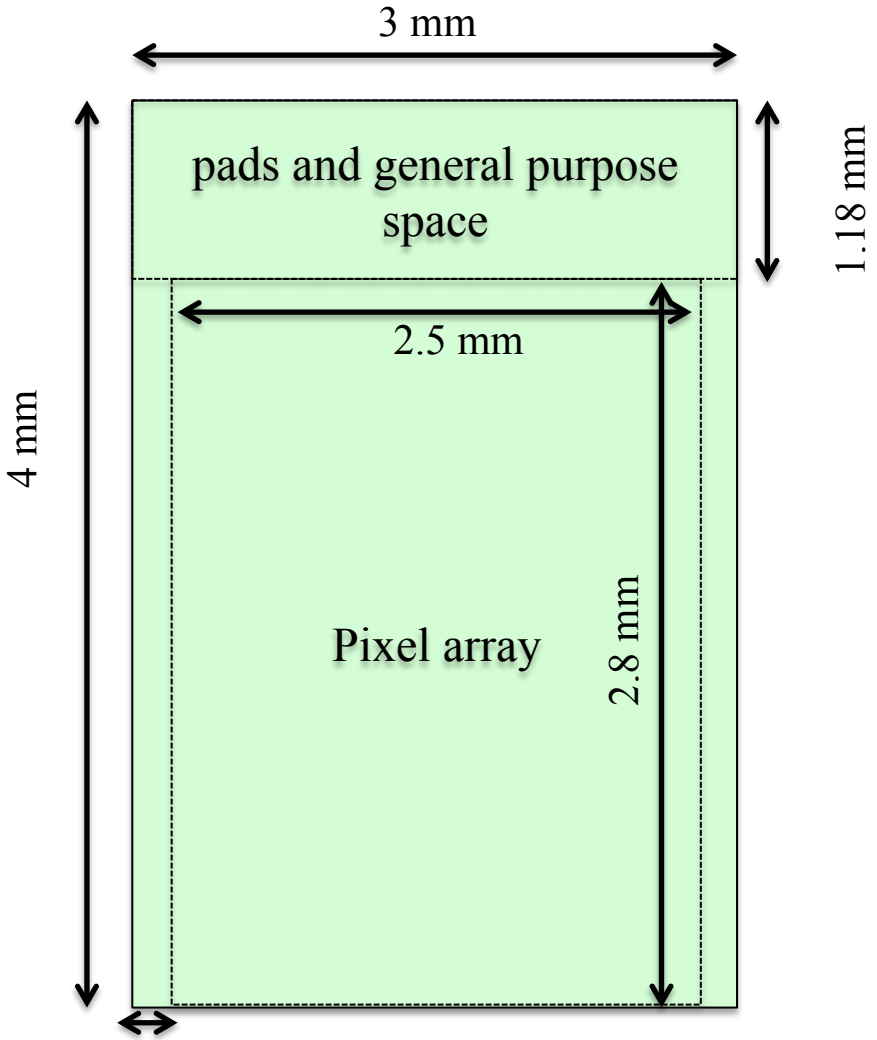
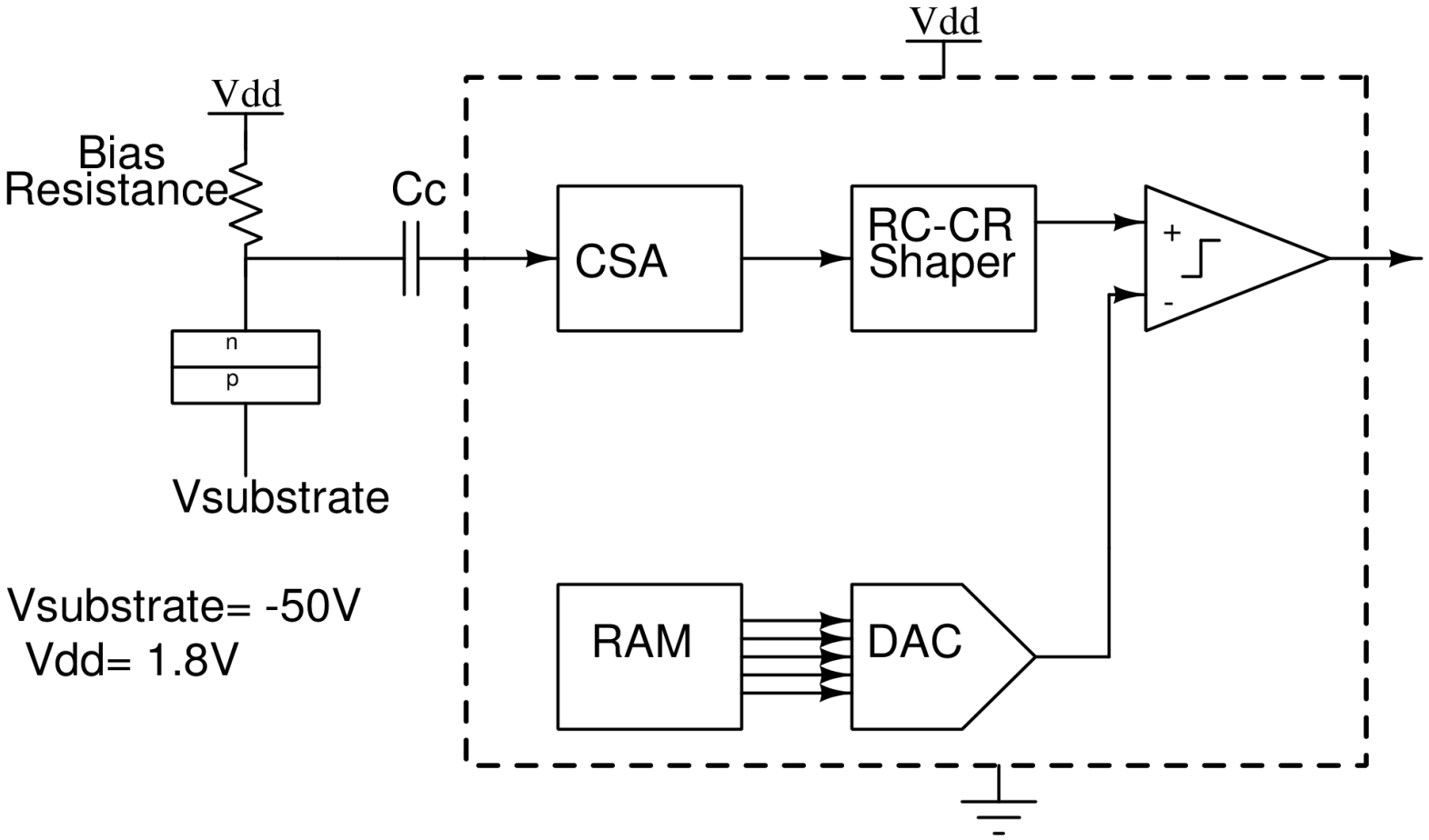


Fig. 1: Alignment of demonstrator to FE-I4 chip



Pixel cell



Genova + Mandi + Milano

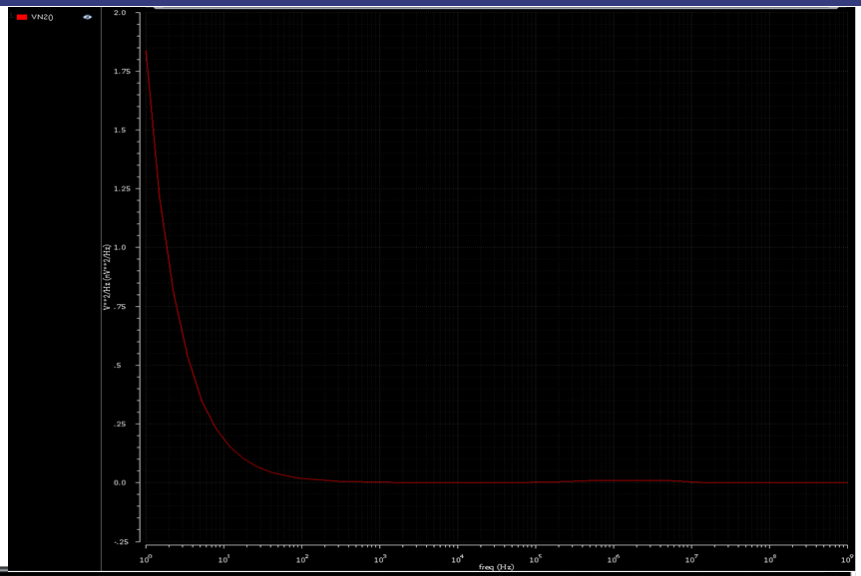
Noise performance

Device	Param	Noise Contribution	% Of Total
M30.m1	fn	0.00689093	26.71
M30.m1	id	0.00646208	23.48
M5.m1	id	0.00420071	9.92
M5.m1	fn	0.0036419	7.46
M41.m1	id	0.00333666	6.26
M41.m1	fn	0.00273693	4.21
M2.m1	fn	0.00238552	3.20
M1.m1	id	0.00235236	3.11
M3.m1	fn	0.0021559	2.61
M21.m1	id	0.00191197	2.06

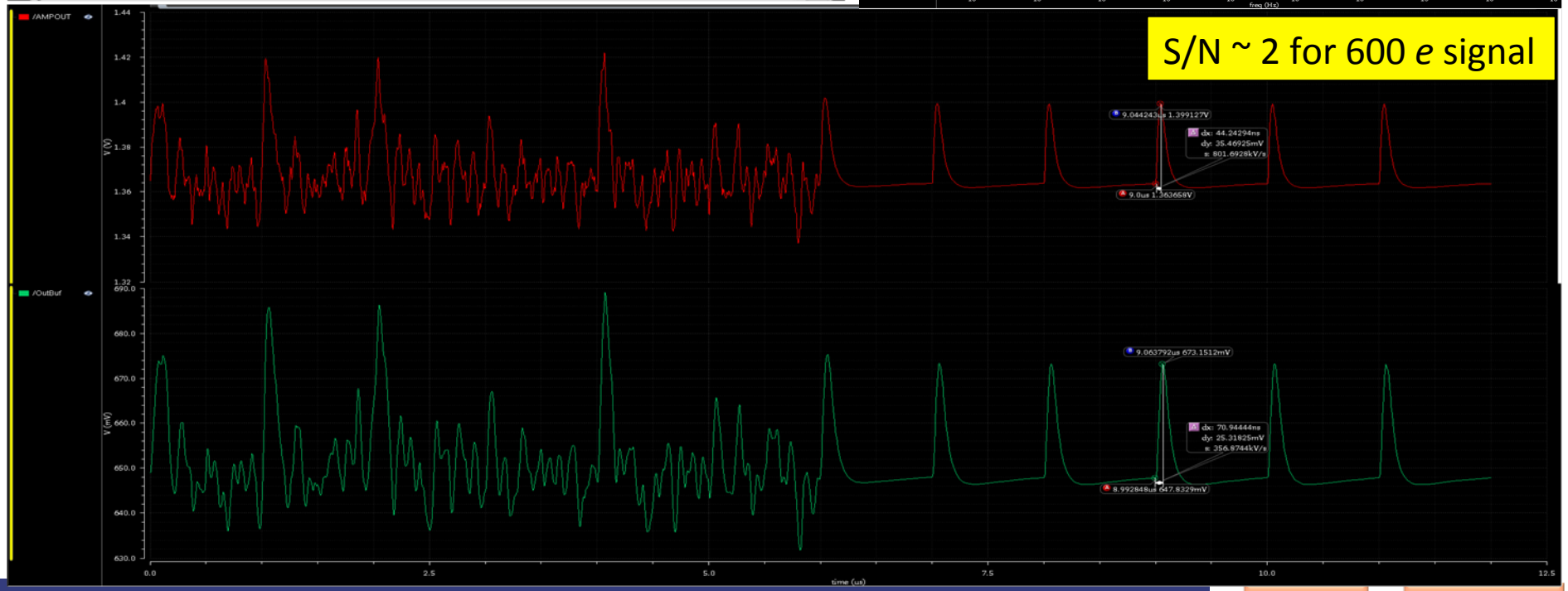
Integrated Noise Summary (in V) Sorted By Noise Contributors

Total Summarized Noise = 0.0133346

Total Input Referred Noise = 0.000239562 ⇐ =239uV ~ VIN

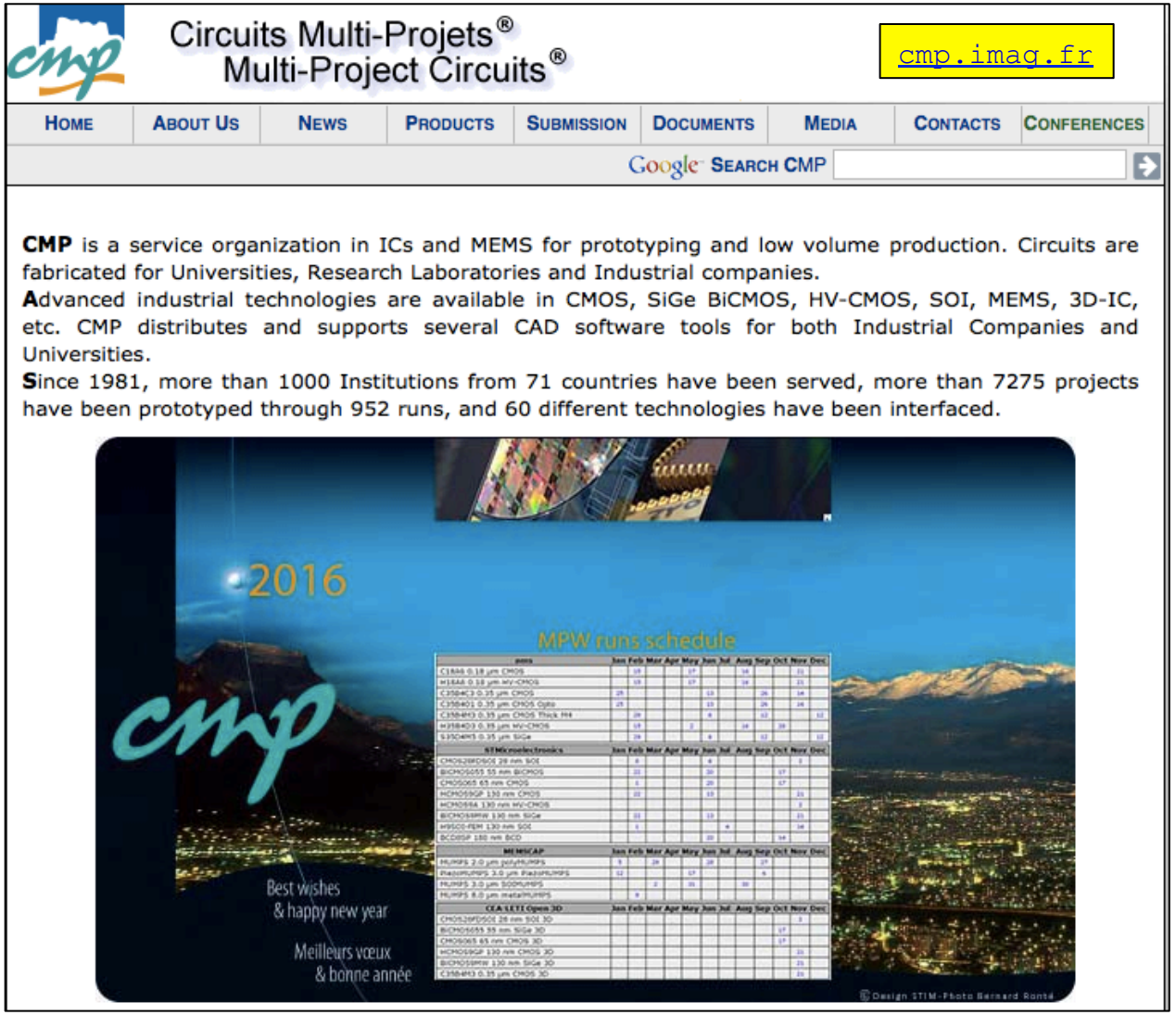


S/N ~ 2 for 600 *e* signal



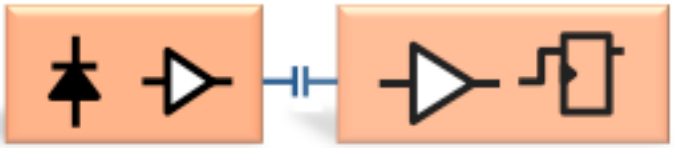
CMP

- BCD8 now available also through CMP
  - easier to get new people started
  - increase of costs with respect to initial informal contacts:
    - 2600 Euro/mm^2 if Area ≤ 5 mm^2
    - 13000 Euro + [(Area-5) * 2100 Euro] if 5 mm^2 < Area < 15 mm^2



Summary and short-term plans

- No problems observed in first irradiation tests
- Detected signal from passive diodes
  - still to fully understand depletion depth and rate
  - TCAD / Geant4 simulations (help welcome)
- In-house hybridization test satisfactory,
  - dummy wafers for FE-I4 size tests produced
- Fixed KC53AB received:
  - need to test if working properly
  - compare performance to Cadence simulation
  - plan complete set of irradiation tests
- Large pixel matrix to be submitted by mid-March
  - can be matched to FE-I4 chips



HVR - CCPD

BACKUP

High **V**oltage and High **R**esistivity CMOS **C**apacively **C**oupled **P**ixel **D**etector

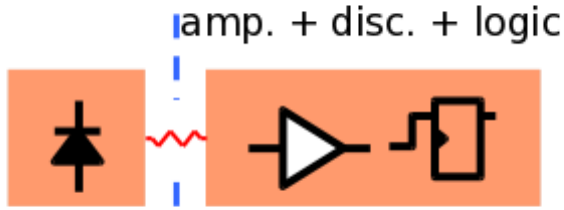
INFN CSN5 project, 2015-2017
INFN branches: Bologna, Genova, Milano

Purpose:

- To prototype an active CCPD (Capacitive Coupled Pixel Detector) by developing, testing and characterizing an **HV/HR-CMOS design** and its **integration** with a pixel detector chip for R/O. Initially the R/O chip will be the ATLAS FE-I4 and will be then moved to the RD53 (CHIPIX65) design, when this will become available.
- Aiming to large area, high rate, **high radiation environment** applications (High-Luminosity LHC as a reference benchmark)

HV-CMOS Hybrid pixels

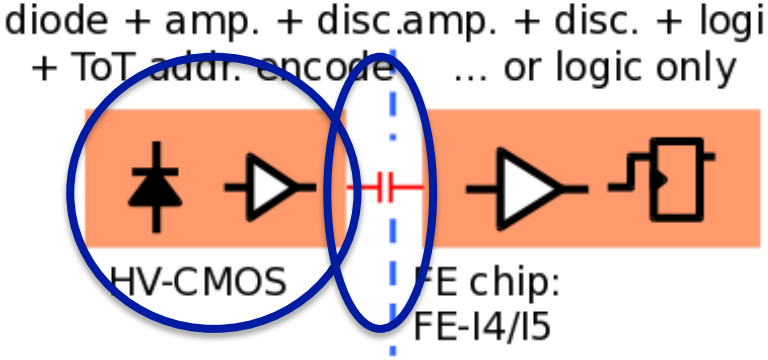
Standard hybrid pixels



Chip-to-chip bump-bonding → expensive

Pro's	Con's
Mature technology Radiation hard Multi-chip modules	Sensor/bump cost 4"÷6" sensor wafer Spatial resolution Cost/yield of BB

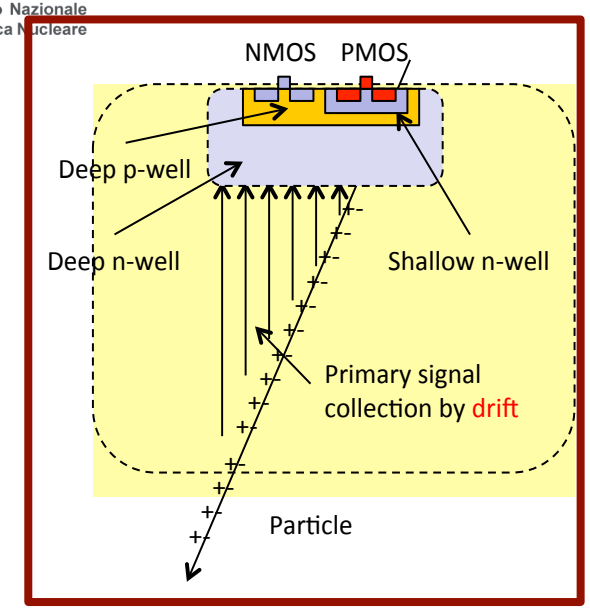
HV-CMOS hybrid pixels



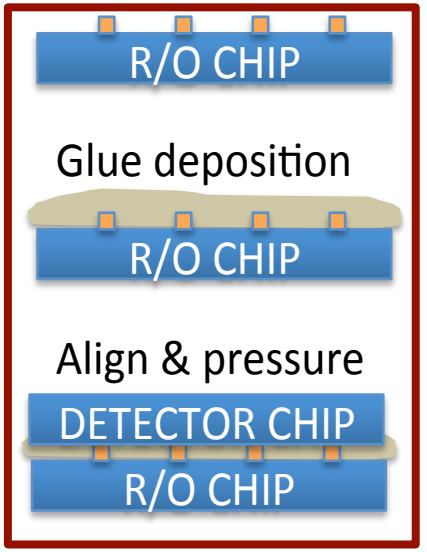
Wafer-to-wafer gluing
... or chip-to-chip
→ simpler/cheaper ?

Pro's	Con's
8" (or 12") HV-CMOS wafers "Standard" IC process Cheap BB (to demonstrate) Small pixel → resolution	Novel technology Small charge (800÷1500 e) Extreme radiation ? Single chip (multi-chip difficult)

HVR_CCPD pillars



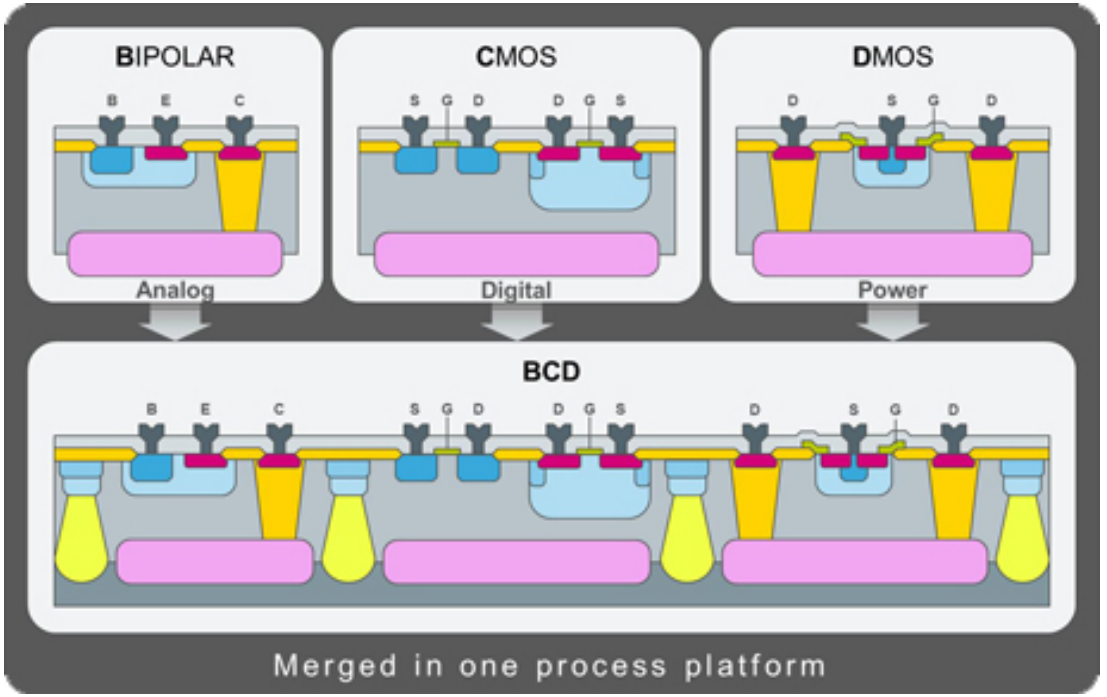
- In standard CMOS detectors charge generated by energy deposition is collected by **diffusion**.
- Combining commercial technologies sustaining HV (50-70 V) with high resistivity substrates results in a depleted (15-30 µm) region, where charge is collected by **drift**.
- Same advantages of CMOS detectors (*cheap*, *thin*)
- In addition: **larger and faster signals** and **better radiation tolerance**.

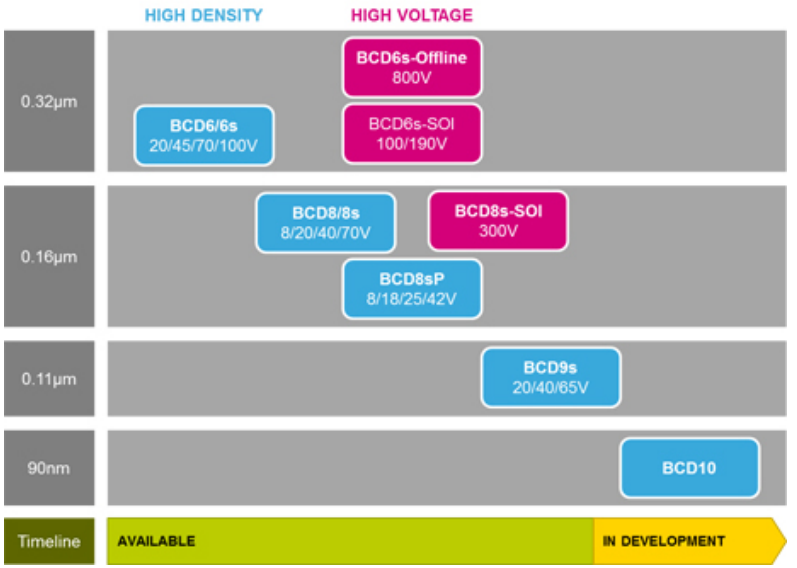


- Signal amplification on CMOS detectors allows **AC coupling** between the sensor and the readout chip:
  - **simpler** and **cheaper** than bump-bonding
  - **independent from density of pixels**
- Controlled flip-chip process:
  - growing of spacers in epoxy material (SU8) to control glue (dielectric) thickness
  - characterization of coupling, uniformity, radiation tolerance in single dies
  - **wafer level processing in external firms.**

BCD8 Technology STMicroelectronics

BCD = Bipolar + CMOS + DMOS





http://www.st.com/web/en/about_st/bcd.html

- Among the competing technologies BCD8 has several appealing features:
  - availability of different devices integrated in the same process
  - **epitaxial process**: can easily grow on different substrates.
  - possible to reach thick depletion layers: 30 µm looks an optimal compromise between signal and material thickness of the detector
  - **long-term availability**: it is one of the major production line for ST automotive products.