INFN activities on Pixel-Phase2 FE-ASIC: CHIPIX65 project

INFN CALL project - 2013 CSN5

Web-site: http://chipix65.to.infn.it

L.Demaria - INFN Torino
on behalf of the CHIPIX65 project

Pixel Ph2 Electr. Meeting - TKUpg-WEEK 11/11/2015

CHIPIX65 Project

Institutes:

Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa, Torino

People:

N.Demaria, G.Dellacasa, G.Mazza, A.Rivetti, M.D.Da Rocha Rolo, E.Monteil, L.Pacher, F.Ciciriello, F.Corsi, C.Marzocca, G.De Robertis, F.Loddo, C.Tamma, M.Bagatin, D.Bisello, S.Gerardin, S.Mattiazzo, L.Ding, P.Giubilato, A.Paccagnella, F.De Canio, L.Gaioni, M.Manghisoni, V.Re, G.Traversi, E.Riceputi, L.Ratti, C.Vacchi, R.Beccherle, G.Magazzu, M.Minuti, F.Morsani, F.Palla, V.Liberali , S.Shojaii , A.Stabile , G.M.Bilei , M.Menichelli , E.Conti , S.Marconi, D.Passeri , P.Placidi, S.D'Amico, C.Veri, A.Donno.

CHIPIX65 activities

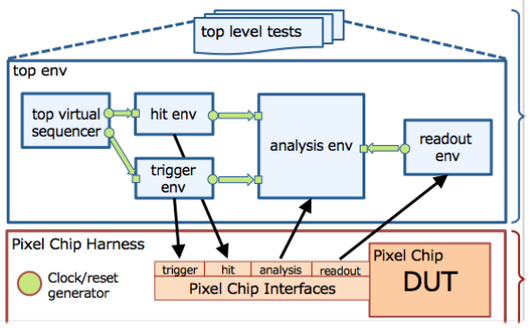
…at a glance

Radiation characterisation

- x-ray machine at LNL / Pd-INFN
  - Total Ionising Dose (TID)
  - 1 GRad in ~ 2 weeks
- Low-p at CN accelerator LNL
  - TID and Total Displacement damage
- TANDEM / SIRAD
  - Single Event Effects - with Heavy Ion
- Studies on n-MOS, p-MOS
- Irradiation of IP-block, Noise-measurements vs Irradiation

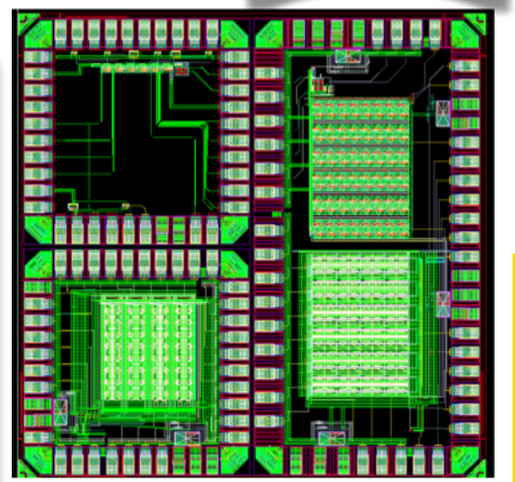
Digital Electronics:

- Simulation Framework
  - System-Verilog-UVM (VEPIX53)
- Digital Architecture Studies
- Input protocols definition
  - fast/efficient/continuos (while readout)
  - SEE robust



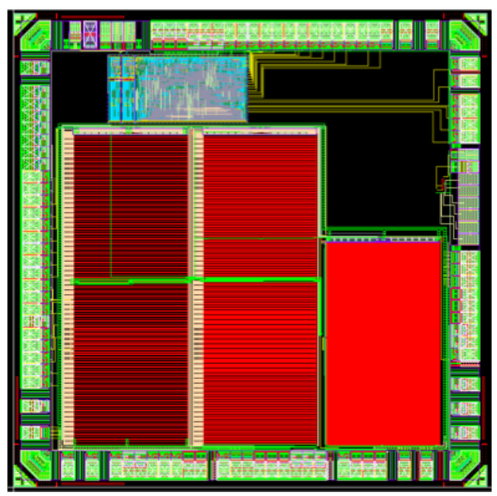
Design in 65nm

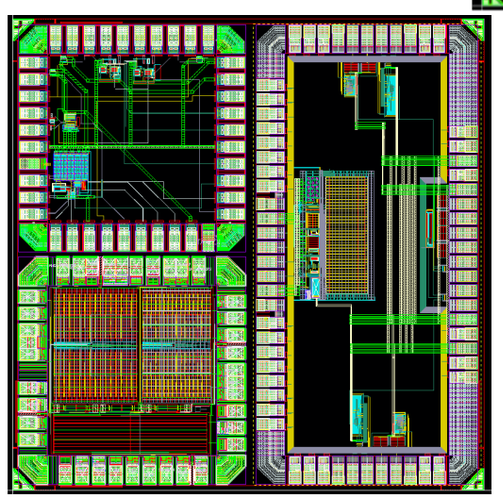
- 6 silicon dies 2x2mm2 submitted
- CHIPIX65 IP-blocks
  - DAC-curr, ADC, SRAM,
  - SER/DES, sLVDS(TX/RX)
  - BandGap, D2RA digital cells
  - JTAG
- CHIPIX65 Analog Very Front End
  - Synchronous chain
  - Asynchronous chain
- Integration of other RD53 IPs
  - DAC-volt (Prague)
  - SER (Bonn), BandGap (CPPM, CERN)

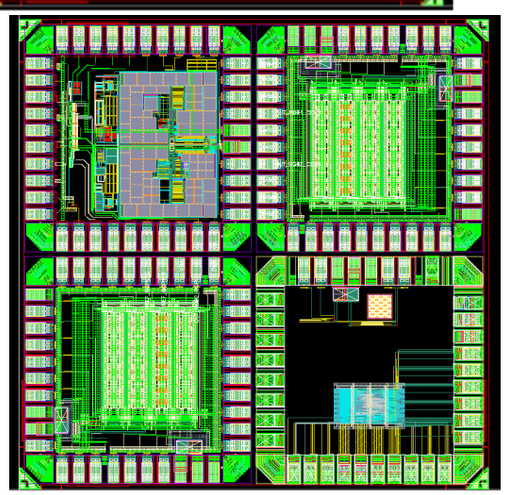


CHIPIX_VFE_1

CHIPIX_BIAS







CHIPIX_SRAM, CHIPIX_IP_3, CHIPIX_VFE_2

IP-Block

Developments of IP-block in CHIPIX65

	DESIGN	CHIPIX65 team	RD53 - other
Bias & Monitoring	BandGap	Pavia	CERN, CPPM
	BandGap	Milano	CERN, CPPM
	DAC-curr	Bari	Prague (Volt)
	ADC	Bari	
	DC-DC	LECCE	
High Speed IO core	DualRail Digital cells	Milano	
	DICE RAM	Milano	CPPM
	SLVS Tx / Rx	Pavia	
	SLVS Tx / Rx	PISA	
	SER	PISA	Bonn
	DES	PISA	n.c
	PLL	Torino	Bonn
	Padova		Bonn

BLOCK	DIMENSIONS	POWER	Performance / Main-Characteristics
Band-Gap	$100\times270\ \mu m^2$	65 μW	based on MOS only
10-bit DAC	$140\times240\ \mu m^2$	150 μW	DNL $<$ 0.4 LSB, INL $<$ 1LSB
12-bit ADC	$308\times535\ \mu m^2$		1V, 16-ch, 5kSample/s
SER	$100\times56\ \mu m^2$	2.3 mW	2 Gbps
DES	$180\times56\ \mu m^2$	17.8 mW	2 Gbps
sLVDS-TX	$160\times160\ \mu m^2$	2 mW	1.2 Gbps
sLVDS-RX	$70\times80\ \mu m^2$	0.2 mW	1.2 Gbps
Dice S-RAM	$1.8\times3.3\ \mu m^2$		SEE recover in 2.5ns

Prototype chip: CHIPIX65

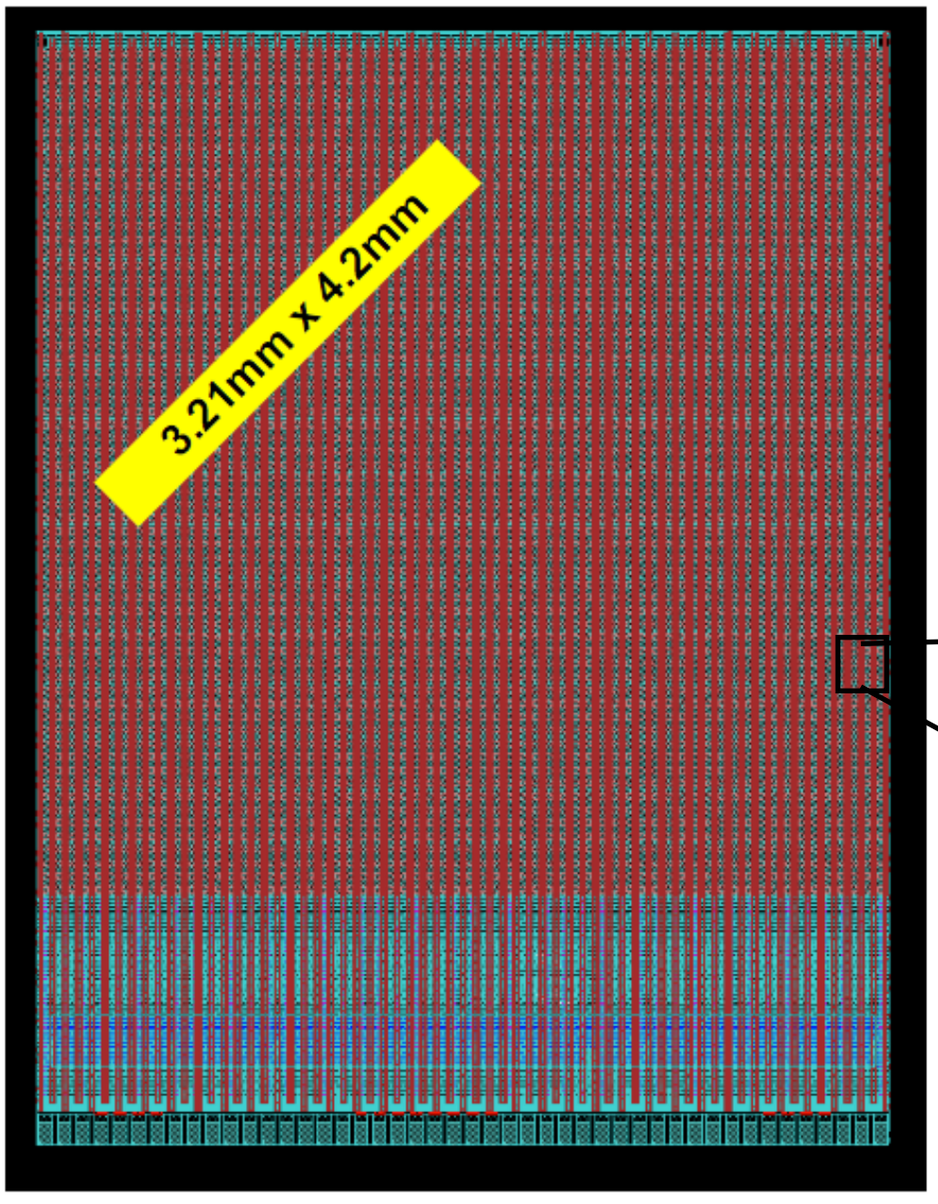
Motivation (1):

- design a small yet fairly complex pixel array demonstrator in 65nm CMOS technology (intermediate step before full-scale RD53 prototype)
  - **64×64** pixels with **50um×50um** pixel size
  - independent development from FE65_P2
- integration of **two different flavours of analogue front-end** into the same digital readout/configuration architecture
  - asynchronous front-end chain (Pavia)
  - synchronous design (Torino)
- design and implementation of a **realistic and new region-based digital architecture**
  - usage of the **RD53 SystemVerilog/UVM verification environment** from the beginning
  - digital architecture studies performed with hits and trigger patterns provided by the verification environment
  - baseline choice of a **4×4 pixel-region**

Prototype chip: CHIPIX65

Motivation (2):

- **no ambition** to extend the exercise to complex digital readout/slow control
  - SPI-based chip configuration
  - simple column arbitering with RAM-based FIFO derandomizer and serializer
- integration of available **silicon-proved RD53 IP blocks**
  - biasing DAC and monitoring ADC (Bari), bandgap (Bergamo/Pavia)
  - sLVDS TX/RX (Bergamo/Pavia), serializer (Pisa)
  - others if available and successfully tested
- usage of the **modified CERN I/O library**
- core design-team based on INFN/CHIPIX65 groups
  - gain expertise and promote among INFN units the **digital-on-top (DoT) design methodology**
  - **ClioSoft-based** distributed design environment
  - periodic and detailed design reviews among designers
- **Multi-Project Wafer (MPW) run** submission planned for **Q1/2016**



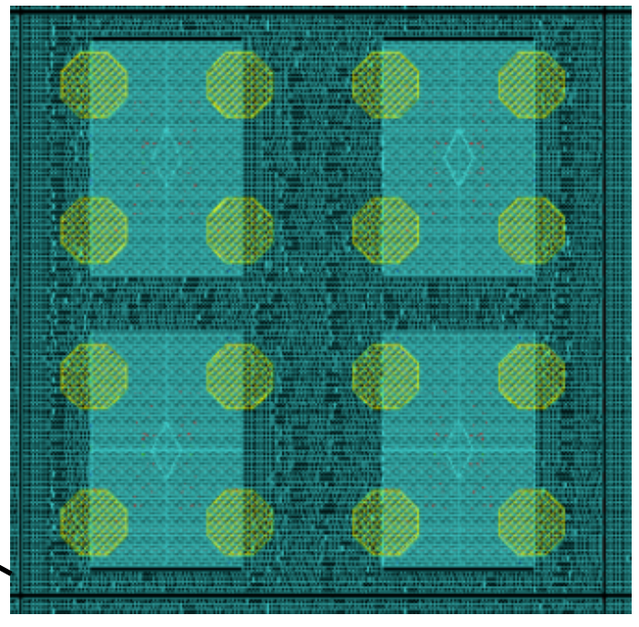
64x64 core pixel matrix

bias network

EoC digital bulk

sLVDS RX/TX and pads

4x4 pixel region



Main RD53 milestone: RD53A

- **2016 : RD53 Design of RD53A prototype**
  - 2-3 cm^2 prototype
  - Joined effort of the **whole RD53 collaboration**
  - Now definition / discussions o:
    - Technical Specs, Funding,
    - Milestone, Design team organization
  - submission end-2016
  - THIS WILL BE THE OUTPUT of RD53 Collaboration, closing the major part of R&D, communities will concentrate more into the chip for the experiments then.

- **CHIPIX65 contributions**
  - Provide Analog Front End(s)
  - Provide IP-blocks
  - Digital architectures (shared work)
  - CHIP integration (shared work)
  - IP-block whould be in a stable 'final' version by middle/end of 2016

Finance contribution:

about 1/5 of cost

cost ~ 500ke

CHIPIX65 providing ~5 FTE out of 10 (50%) - covering all aspects

BG: Gaioni, De Canio
TO: Monteil, Pacher, Paterno'
PG: Marconi
PI : Beccherie