Table Top Upgrade Board

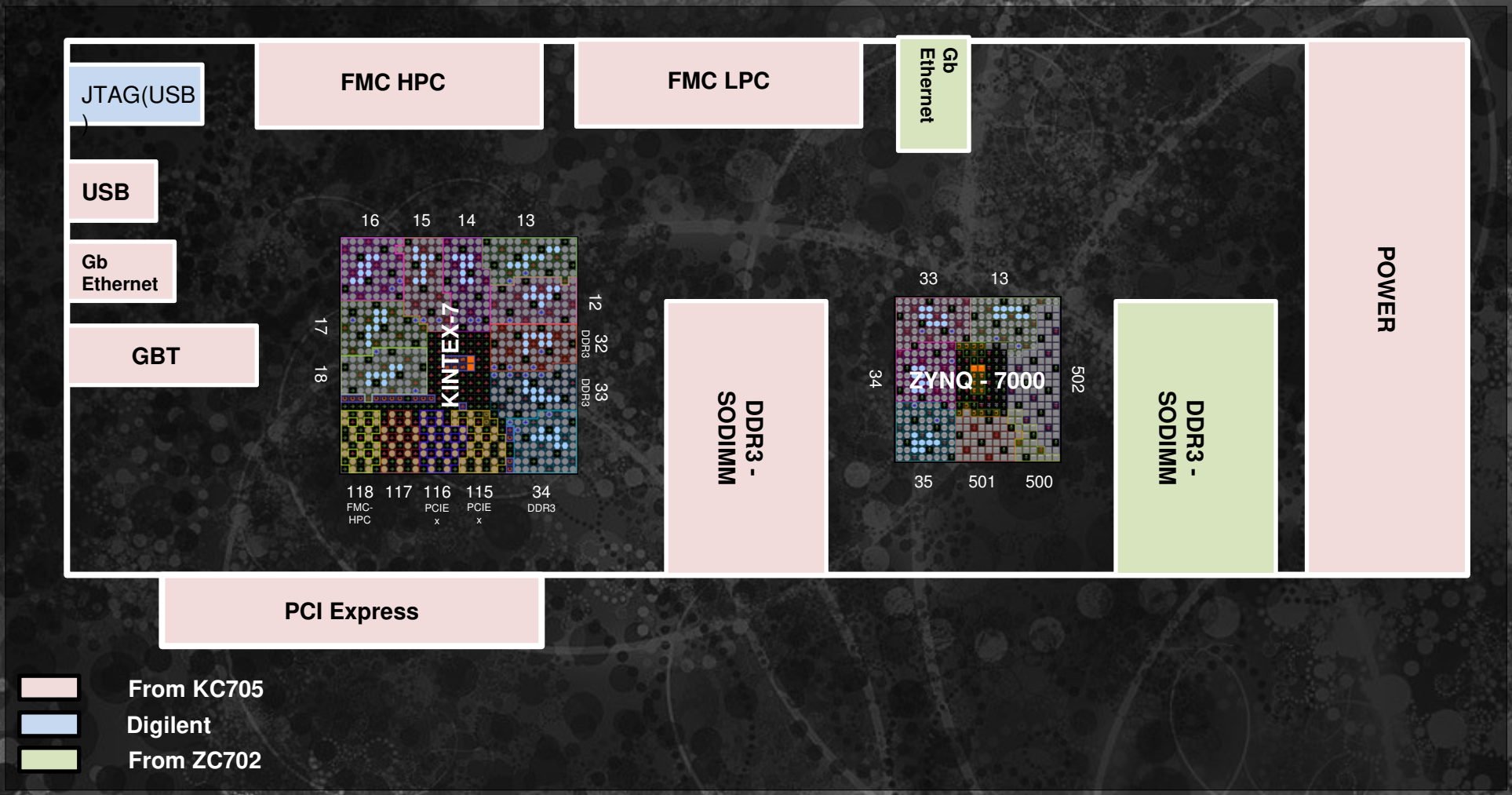
INFN Bologna

G. Balbi, D. Falchieri, A. Gabrielli, **L. Lama**, G. Pellegrini, C. Preti

Overview

- State of the project
  - Schematic nearly done
- Main Features
  - GBT
  - PCIE
  - Back Compatibility through FMC
- Production plans
  - One week to schematic closure
  - Probably a month to PCB Layout

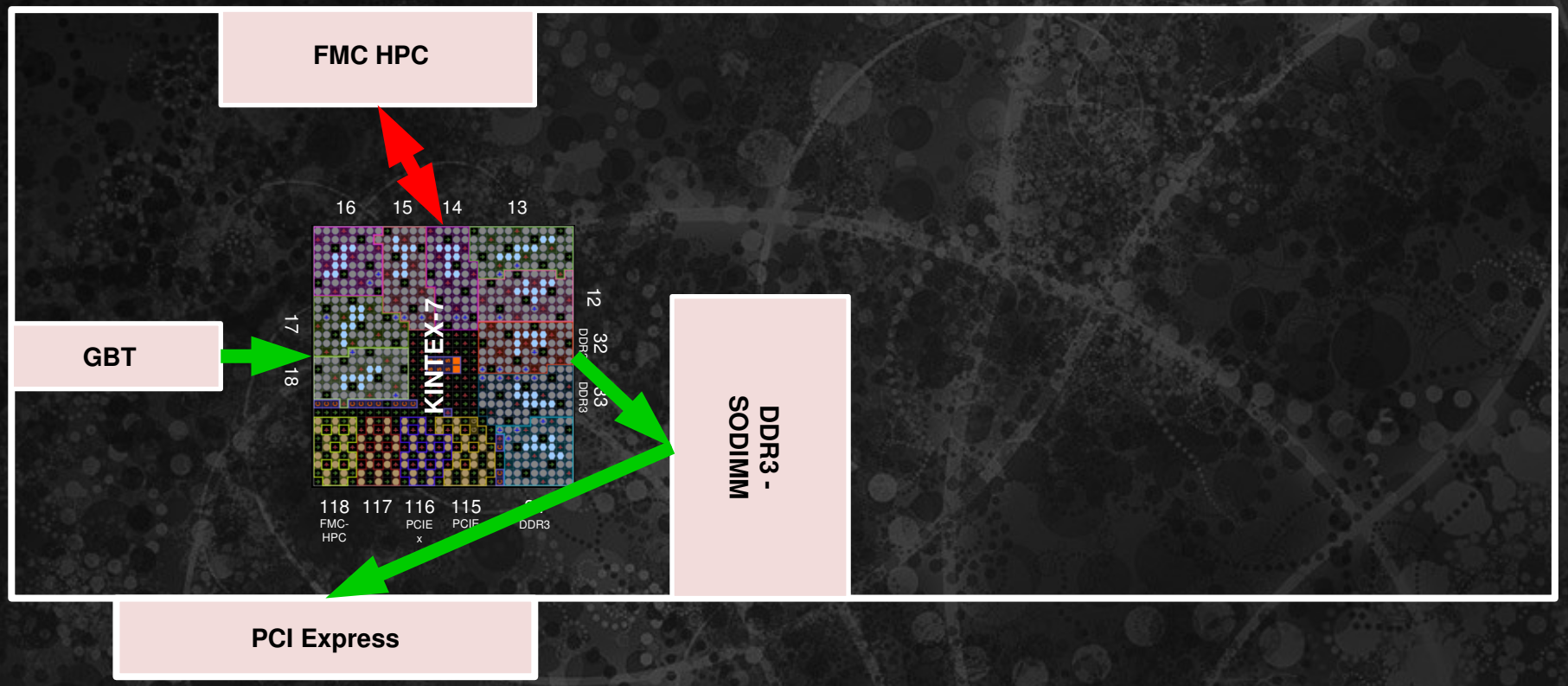
Block Diagram



Data Taking

- Two possible input paths
  - GBT
  - FMC (Snap 12)
- Two possible output paths
  - PCIE
  - FMC (QSFP)
- Depending on the firmware each combination is possible

Data Taking Paths

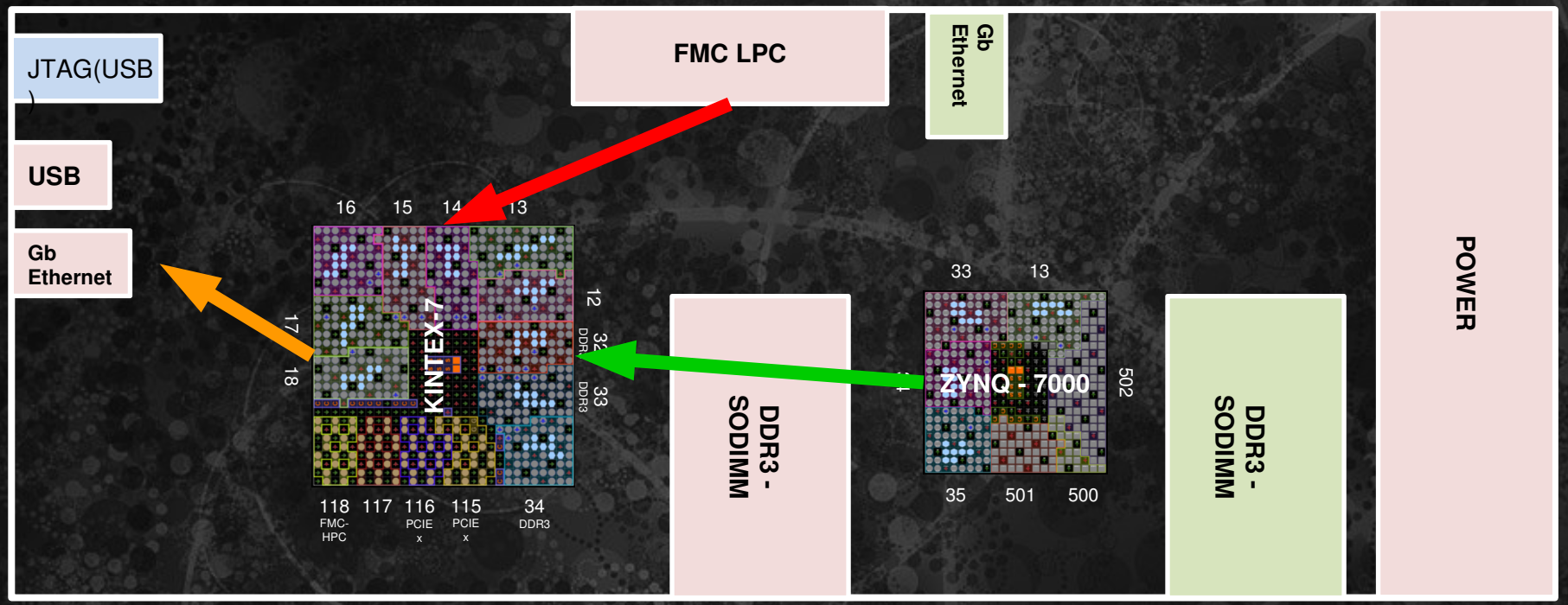


Every combination of the two is possible depending on the firmware

Control & Clock

- Architecture of these features changed dramatically from IBL ROD design:
  - Main Clock is fed directly to the Kintex
  - The Zyng is taking care of both programming and control tasks
  - JTAG chain can be split so the Kintex can be configured by the Zynq
  - FMC LPC connector is compliant with CERN TTCRQ FMC mezzanine
  - Calibration path is there to keep compatibility

Control Features



Clock (Can be back compatible with mezzanine)

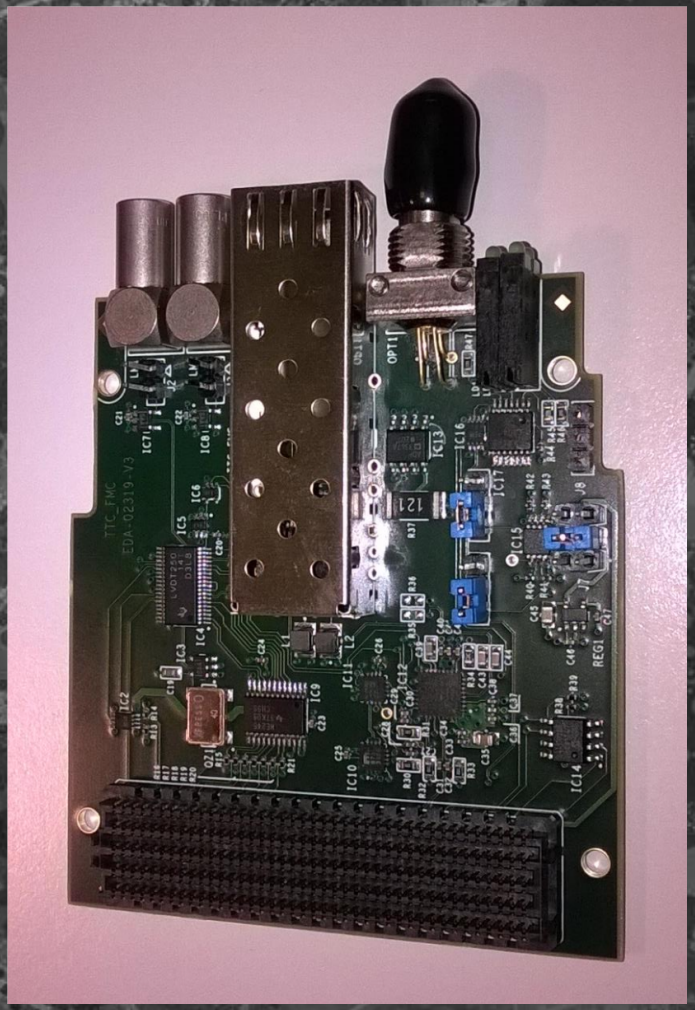
Maintaining Compatibility with calibration path

Changing from PPC to ARM

This Change will affect the C++ Code only a little and the main access through EPC will remain nearly the same

Expansions

- TTCRx LPC expansion board from CERN
  - The board is already prototyped and has only one clock line incompatible with the LPC connector specifics.



Expansions

- Snap12 and QSFP HPC expansion board
  - Since for these components we don’t need fast IOs we can keep them on the FMC

Production Plans

- The schematic development should end in one week.
- We should calculate one month for the layout because it needs some simulations.
- For the time being the requests will be taken into consideration only for another release.