Indium bonding @Selex

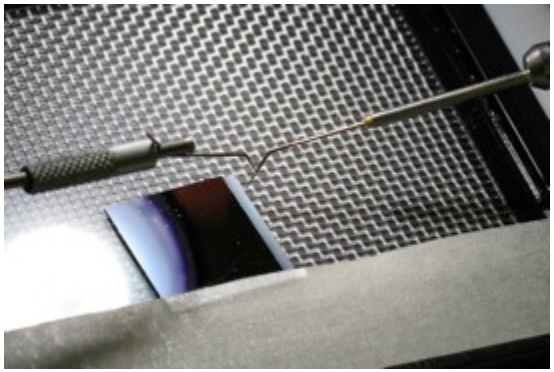
G.Alimonti, INFN Milano

Same technology used for about half the Atlas Pixel Detector modules but:

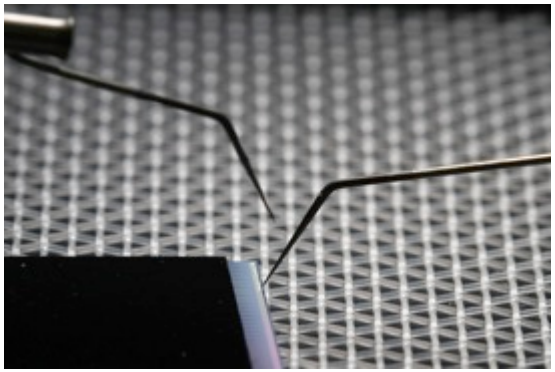
- larger (~20x20 mm^2 instead of 7x11 mm^2) and thinner chips with
- about 40 times more bumps (x5 compared to IBL modules)

Outline:

- Ongoing tests
- Next steps



Tests performed at Genova



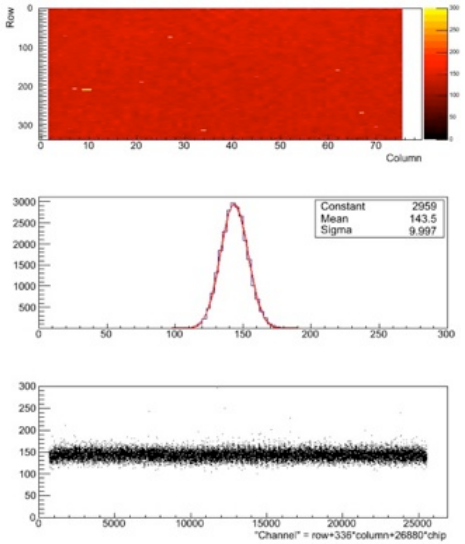
Risultati da R&S per IBL

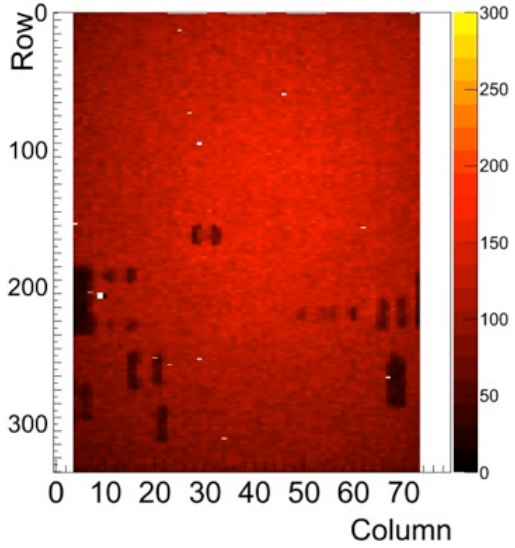
Il programma di R&S per IBL ha prodotto moduli (pochi):

-con un ordine di grandezza in piu' di bump rispetto ad ATLAS pixel

-di grande area 20x20 mm^2 confronto ai 7x11 mm^2 dei FE_I3

-assottigliati sino a 100 μm





Development of Indium bump bonding for the ATLAS Insertable B-Layer (IBL)

G Alimonti *et al* 2013 *JINST* **8** P01024 doi:10.1088/1748-0221/8/01/P01024

Programma di R&S con Selex

Lavorazione wafer da 6”:

-Sensori planari e 3D da FBK

-Produzione di moduli con FE-I4 sia per testare nuovi sensori, sia per completare la qualifica con chip sottili e di grande area

Lavorazione wafer da 12”:

-verificare l’uniformita’ di deposizione delle gocce di Indio

Bonding ad alta densita’ ed elevato numero di bump:

-Numero di bump x5 rispetto FE-I4 (≈120K bump/chip): ottimizzare il processo su catene resistive (dimensioni delle bump, apertura della passivazione, piazzola UB, geometria, forza e temperatura)

-Test elettrici e meccanici sulle catene resistive

Molto positiva la contemporanea collaborazione con FBK e Selex che rende piu’ “semplice” l’ottimizzaione del BB e lo sviluppo di nuovi sensori.

Next steps (1)

- Selex has upgraded its assembly line to process 6” wafers (4” and 8” up to now)
- FBK has upgraded its production line to 6” wafers (4” up to now)

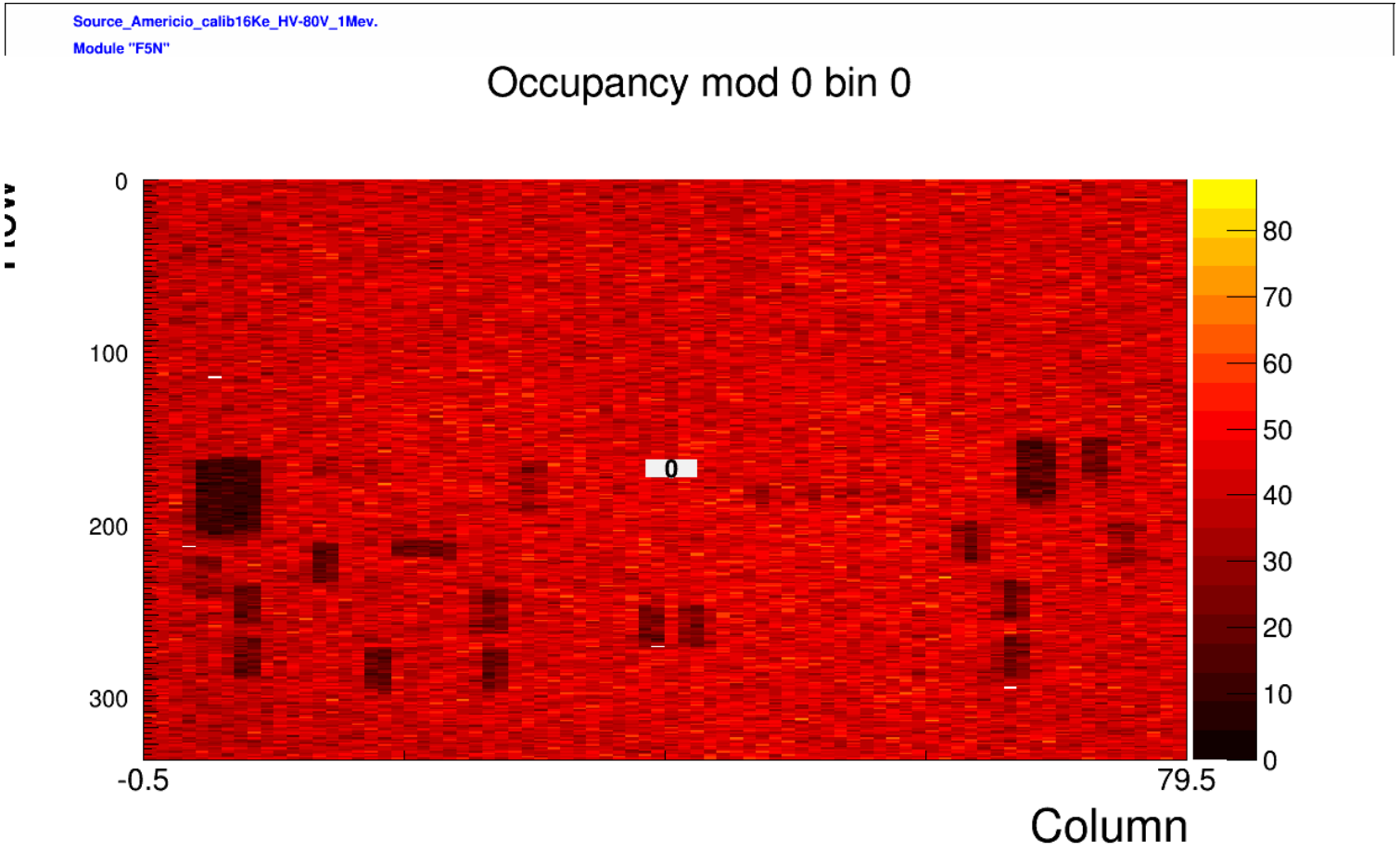
The first step is to produce “standard” modules (unthinned FE chips bonded to “known” FBK sensors) to test both Selex and FBK new lines

First results from planar module look OK (see next slide)

One binary module has just been assembled and sent to G.Calderini (LPNHE, Paris) for testing.

(Moreover 6” wafers with resistive chains are processed to test high density bumps)

16Ke Americium source



Next steps (2)

After testing the two upgraded lines, modules can be assembled for new developments:

- Test new 3D sensors from FBK, producing modules with unthinned FE chips First production by Feb 2016 will also test the “bump on column” solution

- Assemble several modules with known sensors and 100 μm FE chips to validate the thin module production (few modules produced up to now) Will be done after positive (hopefully) results from planar modules; low priority?....150 μm are OK.

Next steps (3)

- Assemble dummy modules with higher density (x5) bumps to investigate future module productions

Design, produce and measure resistivity bump chains dummies with high density bumps: 8 dummy wafers from FBK and deposition mask (see next slide) are at Selex.

Few modules have just been assembled and sent to GE for testing

Upgrade the production line for 12” wafers: photolithography adapted to larger size and 12” wafers arrived at Selex: first deposition test expected this month

FBK dummy wafers with resistive chains:

- 6-inch with 30 FE-I4 size dummy chips (or 4 x quarter chips)
- Metal pad: 18 and 20 μm
- Passivation open: 10 and 12 μm
- Indium bump size: 12 and 16 μm
- 120 k-bumps/chip, 40k bumps tested (248 chains with 160 bumps)

Credits: Alessandro Rovani – INFN / Genova

Dummy chip with resistive chains

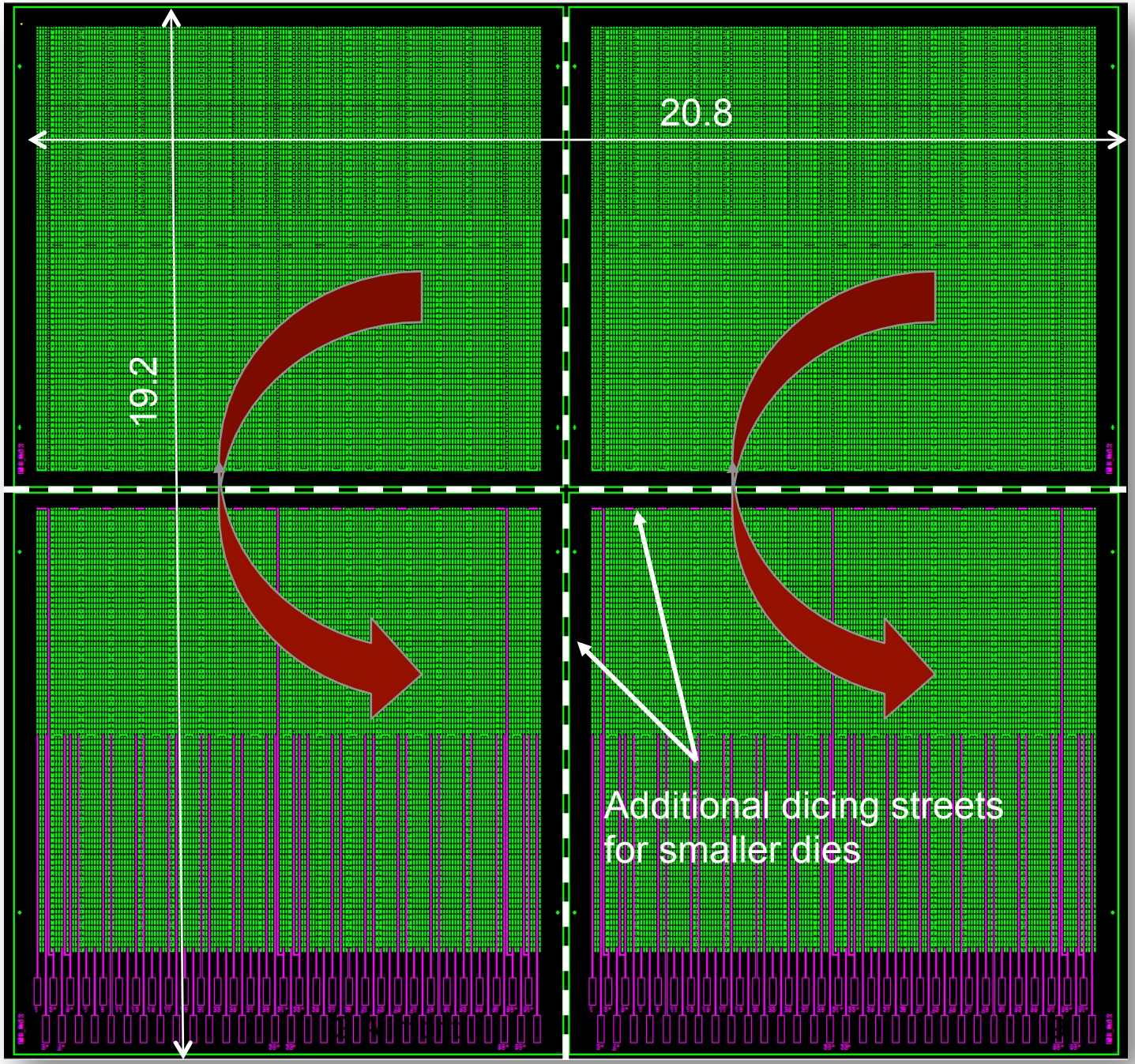
FE-I4 size

120k-bumps

40k-bumps tested

Sampled bump short test

¼ of bump and area by median dicing



2 Feb, 2016

Conclusioni

La linea di produzione a 6” sembra funzionare e continuera’ ad essere utilizzata e testata con nuovi moduli e con le catene resistive

Febbraio potrebbe essere un mese interessante per l’alta densita’:

-primo wafer da 12” per verificare l’uniformita’ di deposizione delle bump

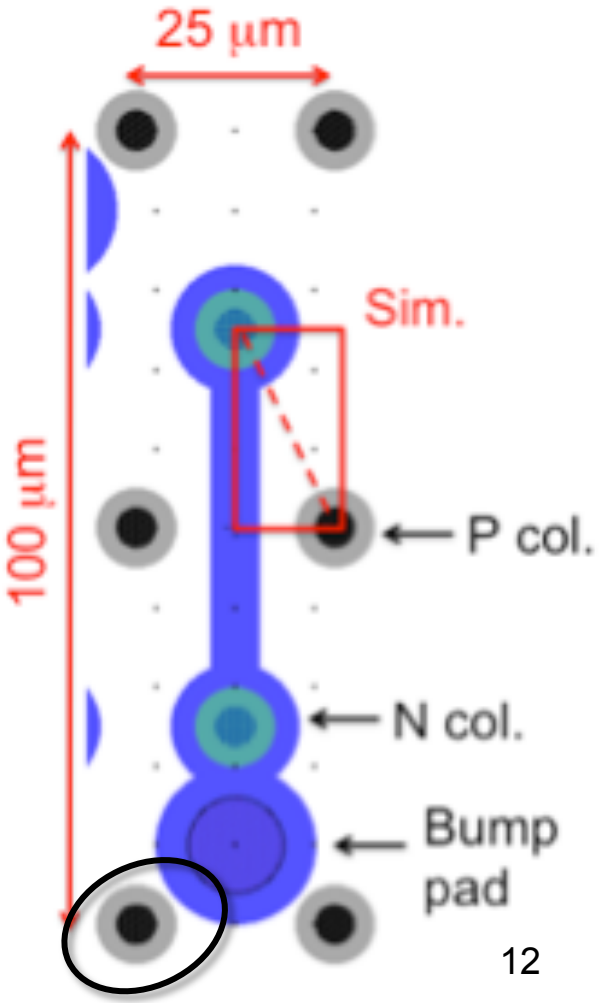
-primi risultati dai moduli con le catene resistive realizzati con nuovi parametri sulle bump e sul processo di bonding

Back up slides

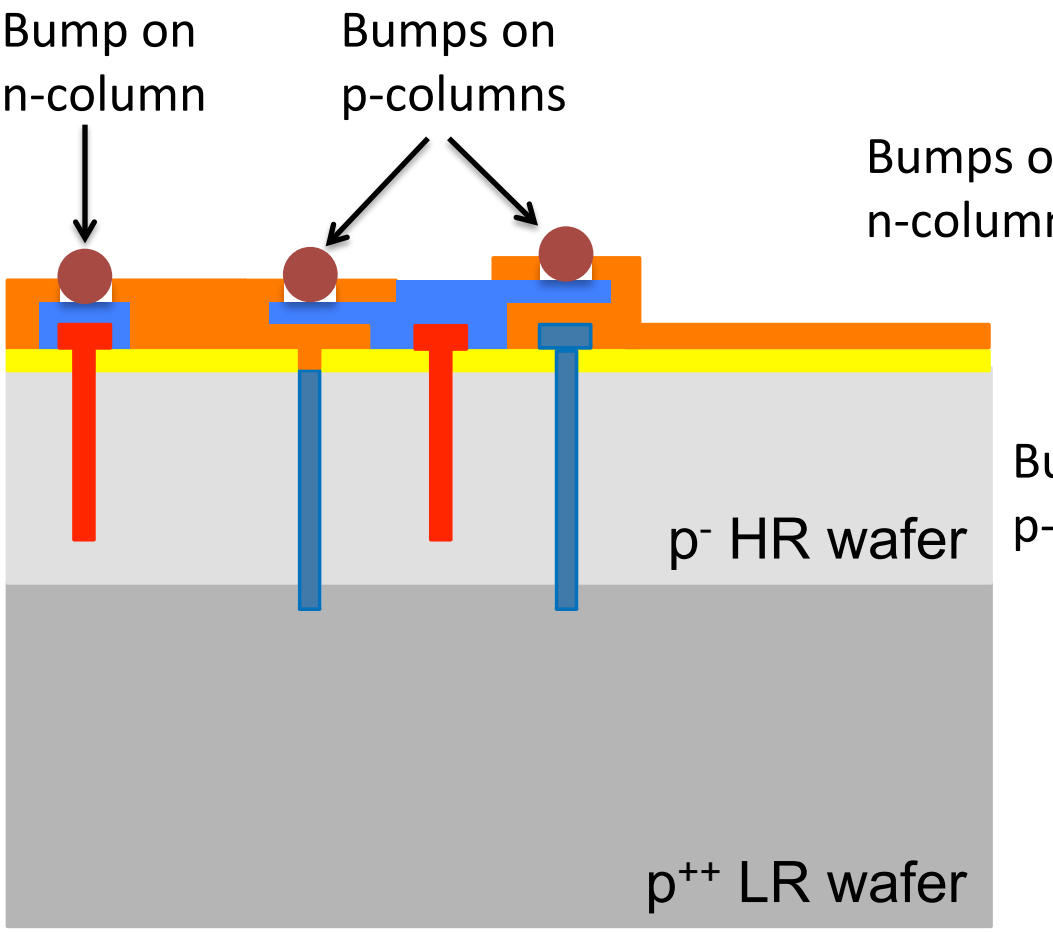
Specific Requirements for 3D

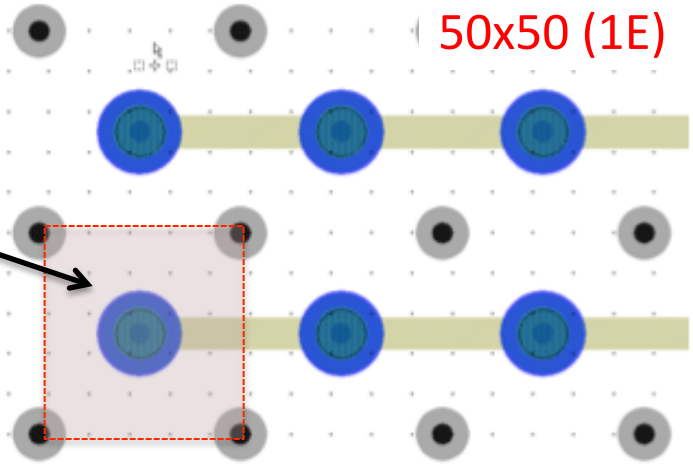
For 3D sensors layout is very critical with new geometries:

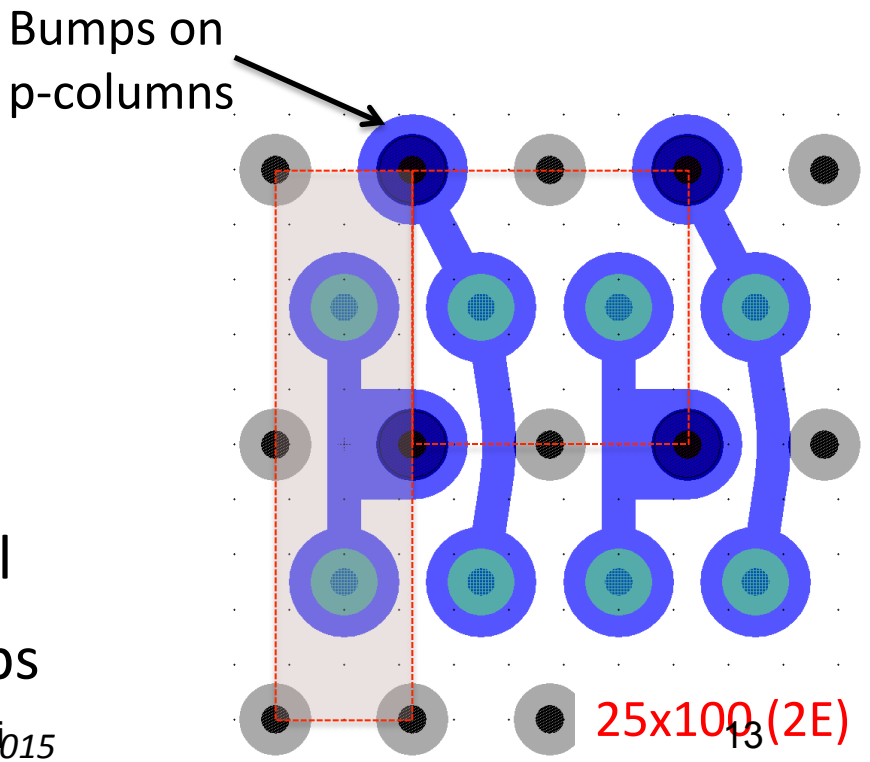
- Is it possible any optimization of the bump pads and bump dimensions?
- Default pad metal is 18 µm diameter and passivation opening 12 µm.
- Any micron gained in the metal would make safer the layout of the 3D sensors (increase distance between opposite sign electrodes: p-type and n-type columns
- Would it be possible to place the bump on top of the n-type (or p-type) columns? See next slide.



Bumps on columns

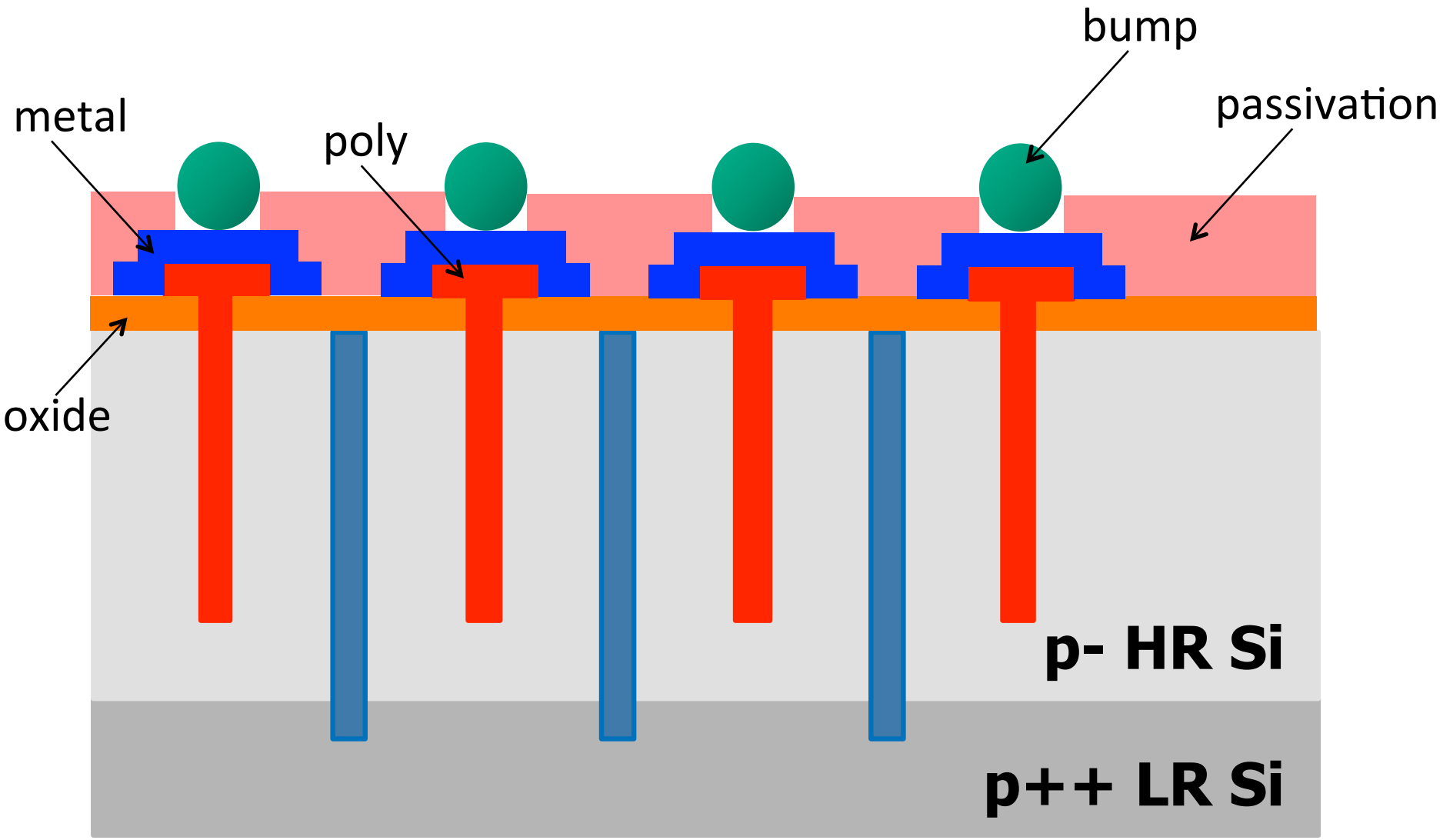






Ref.: G.-F. Dalla Betta, The INFN-FBK "Phase-2" R&D Program, PM2015

Bumps on n-columns

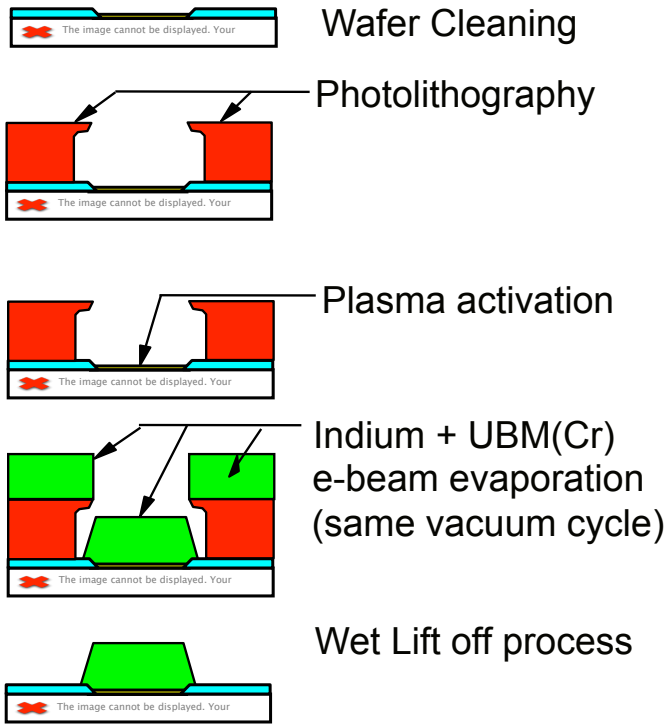


The indium bump-bonding technique is a two-step process:

- bump deposition on both the silicon sensor and the IC wafers
- the flip-chip assembly

In the first process the indium bumps evaporated through a polyimide mask are about 9 μm tall with a defect rate, measured by optical inspection, on the order of 10^{-5}.

The UBM process is very simple: after plasma activation, about 10 nm of chromium are deposited just before indium is evaporated in the same vacuum cycle, with the temperature never exceeding 50°C.



In the second step a cycle with controlled temperature and pressure allows the bumps to establish the electrical and mechanical connections. The resulting connection has an height of about 12 μm and a diameter of about 20 μm.

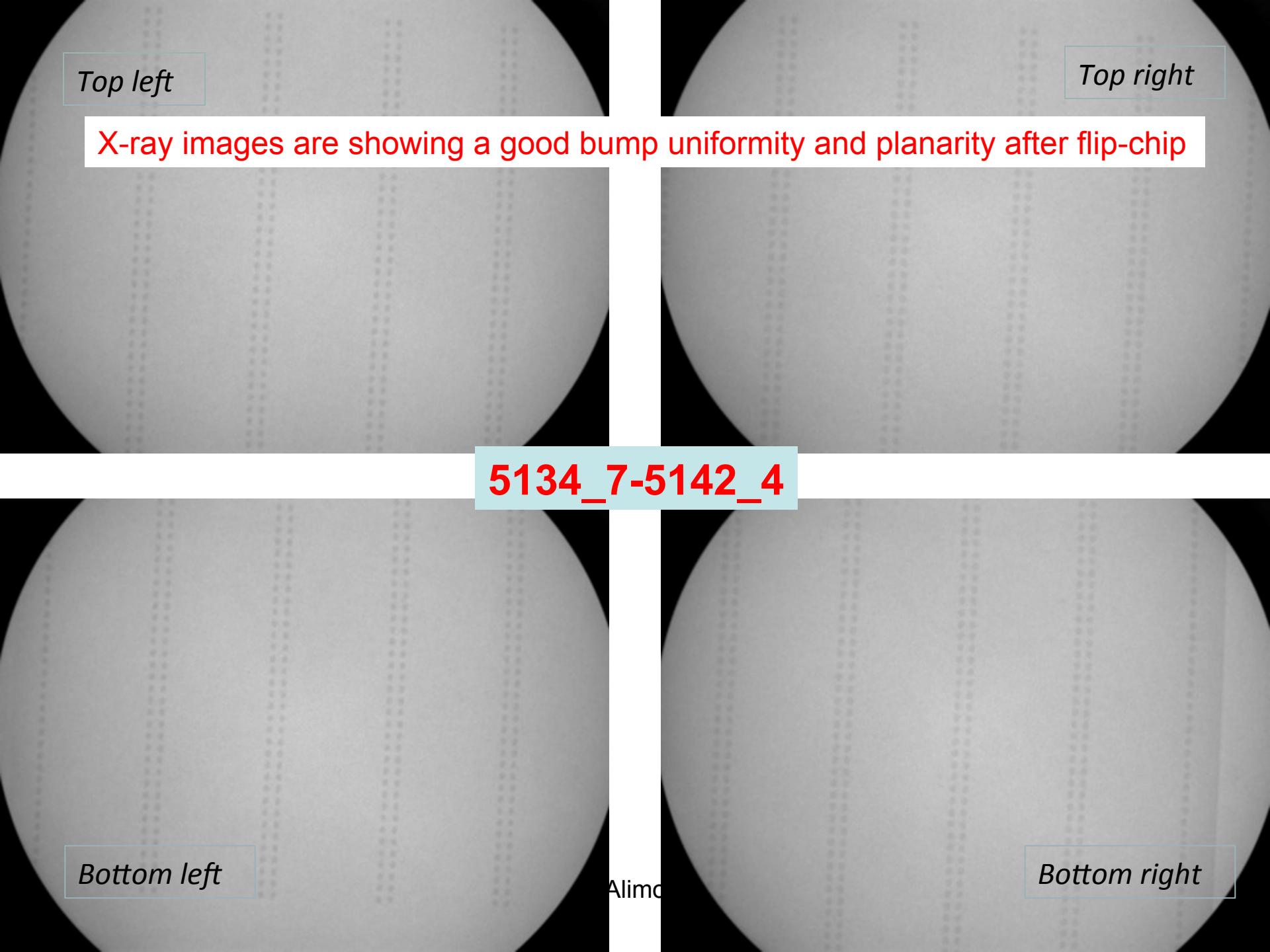
The critical parameters for the bonding process are the larger size of the read out chip, together with the requirement of a thin chip.

Possible origin of problems for the hybridization step are:

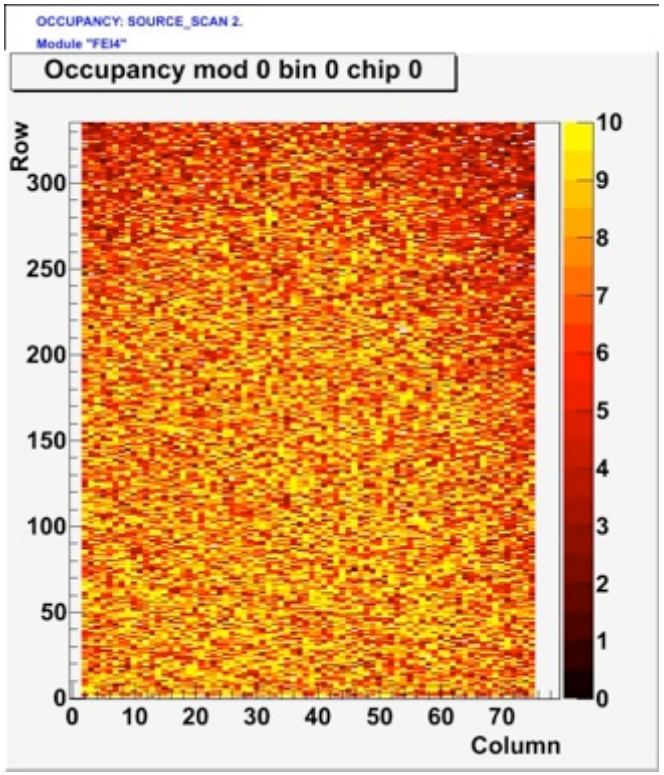
- handling of such a thin and large chip
- planarity with respect to the sensor during flip-chip
- deformations coming from internal stress of the chip and/or working temperature during the bonding step

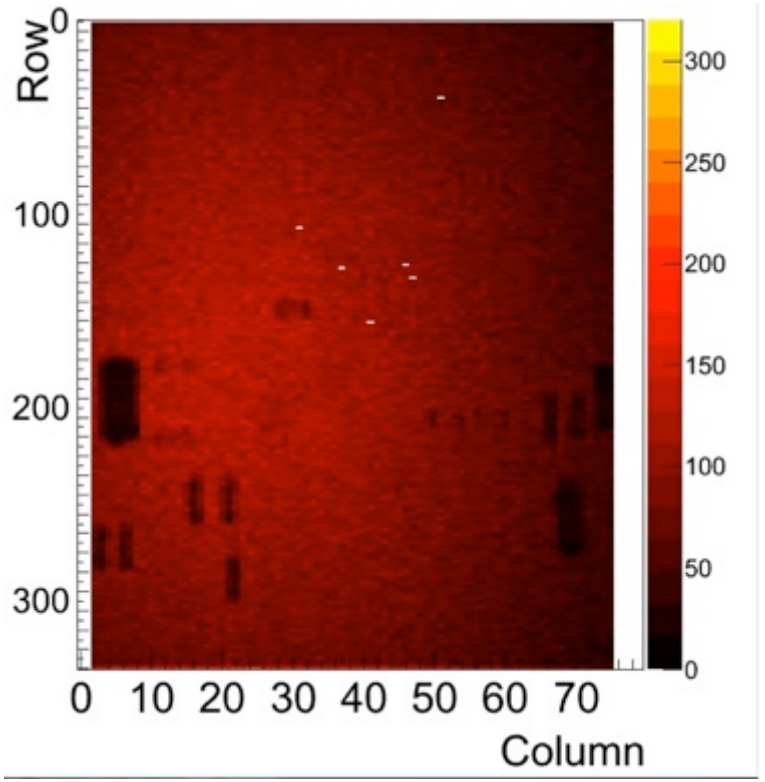
Potential advantages of the Indium bonding process are:

- a low (90°C) maximum working temperature
- a very simple one-step Under-Bump Metallization
- the pick-up tool with the applied bonding pressure is a natural support to prevent chip deformation when working with very thin dies


Top left
Top right
X-ray images are showing a good bump uniformity and planarity after flip-chip
5134_7-5142_4
Bottom left
Bottom right

ENC measurements and Am^{241} source hit-map of modules assembled using a planar (left) or a 3D sensor with a non thinned (725 µm) FE-I4a

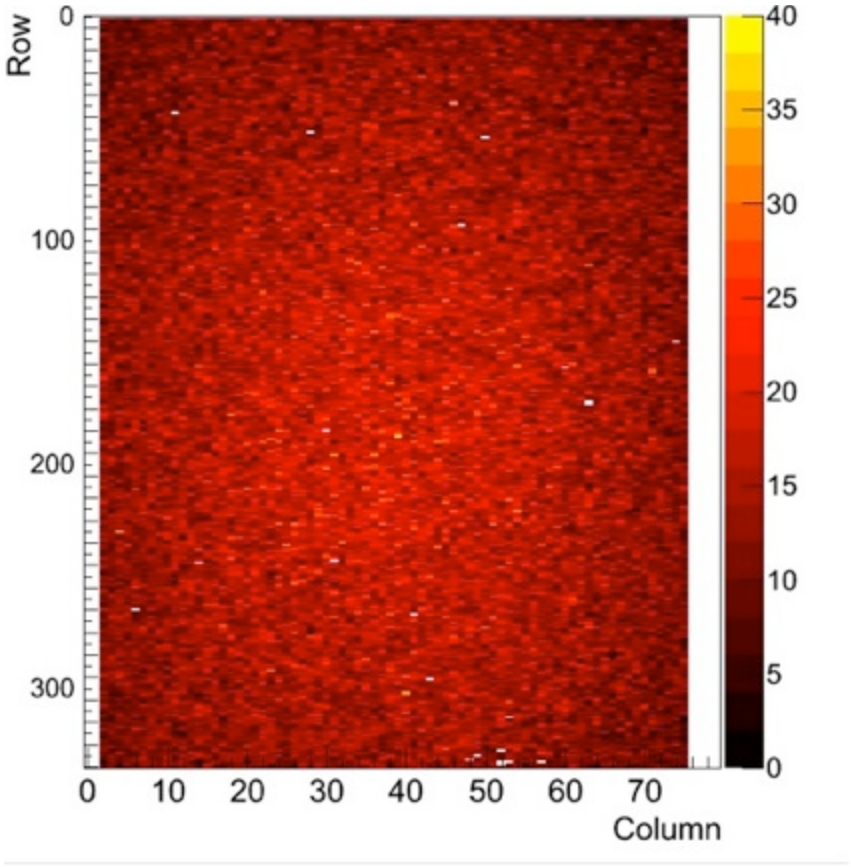




The detection of an Am^{241} source shows no problem in the modules. The shadows seen in the 3D module are coming from SMD components, which are loaded on the flex circuit glued above the module and attenuating the Am^{241} gamma rays.

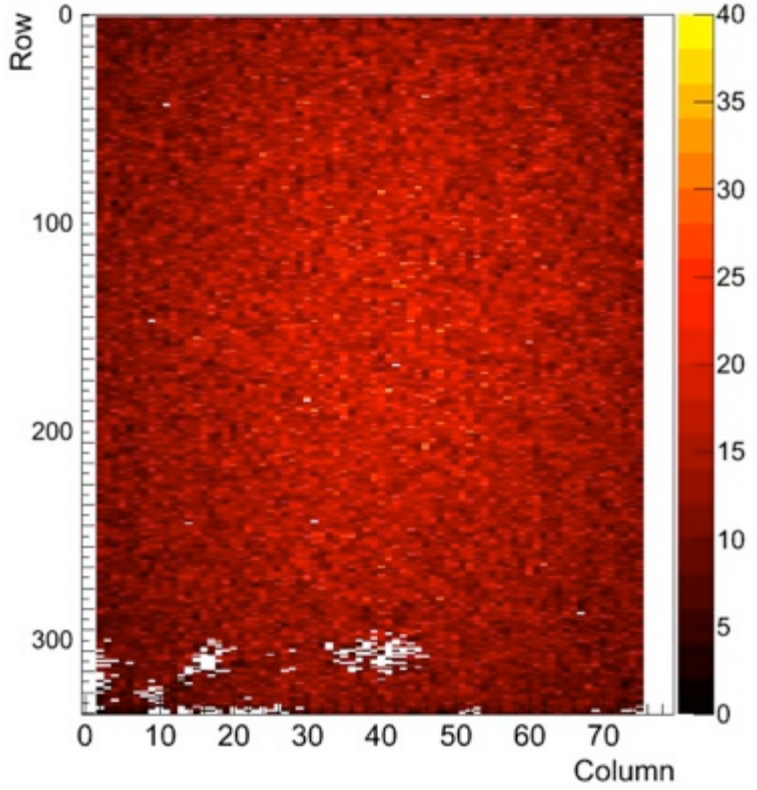
Good results are coming also from modules assembled with a planar sensor and a FE-I4a thinned to 200 μm. This is already an important step from the level reached for the ATLAS pixel production: the read out chips have about the same thickness but now have a much larger area that is a critical parameter for the indium bonding process.

- No pixel masked
- < 20 pixels not responding



Problems are first seen going to 100 μm thinned FE-I4a.

Areas of missing connections are clearly visible in the module: the fact that missing contacts are not on the border of the chip (could be originated by handling) and are present on different modules, points to a bonding problem.



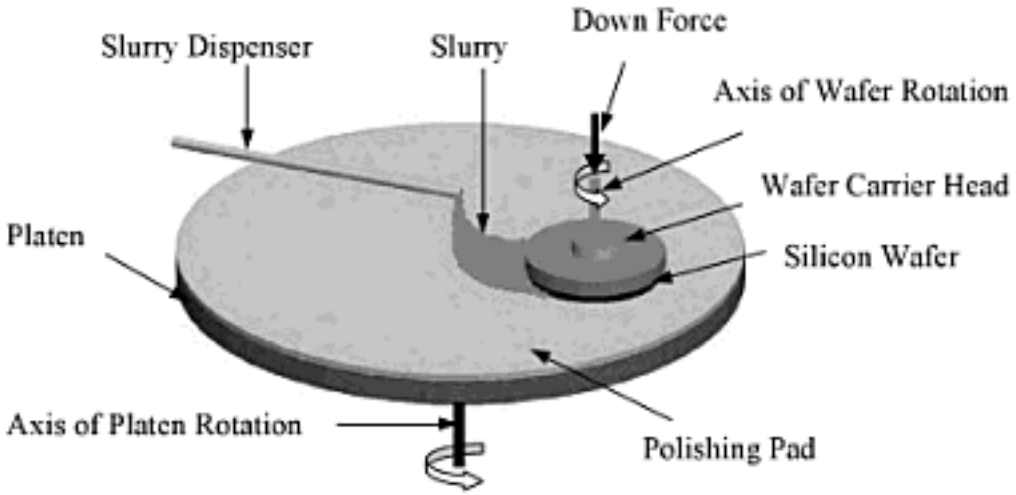
A deformation of the chips thinned to 100 μm had been already observed before bonding and this is thought to be the origin of the problem. Such a behavior is considered to be normal by people involved in thinning and dicing processes and originated by the different metal layers (8 for the FE-I4a) used to build the chip itself.

A stress relief step after thinning has been suggested to reduce the deformation.

This step, applied on the wafer back side, proved to be more difficult than expected due to the presence of a polyimide layer on the wafer front side to protect the indium bumps. Three stress relief processes have been tested: two gave good results.

Chemical Mechanical Process (CMP) with a maximum temperature of 35°C

The wafer is mounted on a rotating carrier head and pushed against a rotating pad with a colloidal silica dispensed between the two. The colloidal silica (slurry) etches the silicon surface and polishes the wafer. The pressure between the wafer and the pad, and the rounds per minute (RPM) in which the carrier head and rotating platen spin, determine the removal rate and temperature control.

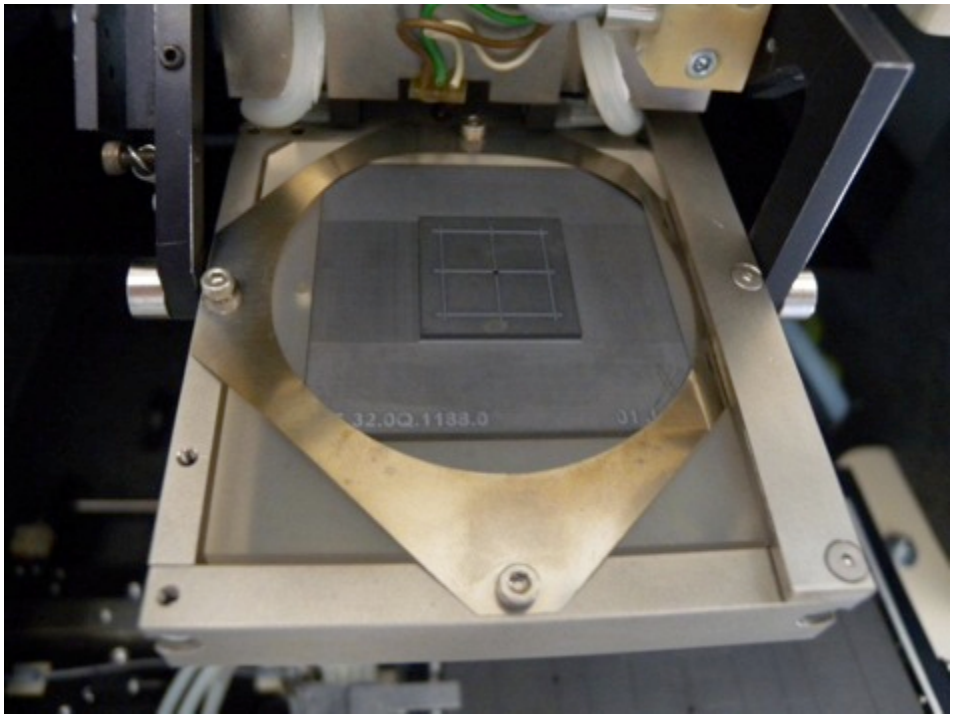


Dry polishing step, with the maximum working temperature not exceeding 90°C

A proprietary process, a specially developed polishing wheel containing non-diamond grit, is rotating in direct contact with the wafer and uses no chemical, slurry or water.

Furthermore, a modification has also been done in the bonding process to exploit the support provided by the the pickup tool that holding the thinned chip to a flat surface and applying a uniform pressure, is a natural support to flatten the deformed chip. Indium bonds at 90°C are still very weak (indium melting temperature is 156°C): after the flip-chip step (42 s at 90°C), the 160N force is not immediately released but is now kept until the assembly temperature cools down to 50°C.

Indium connections are then stronger and keep better in shape (flat) the bonded chip.



After these improvements results are very good for 100 µm thinned FE-I4a too, and similar to the non thinned or 200 µm thinned FE-I4a that do not require any stress relief process. Even if chips worked with the CMP process are better looking (showing a mirror like back side) than the chips worked with the polishing step, results on the modules do not show any significant difference.