RD_FASE2: INFN-FBK Sensors

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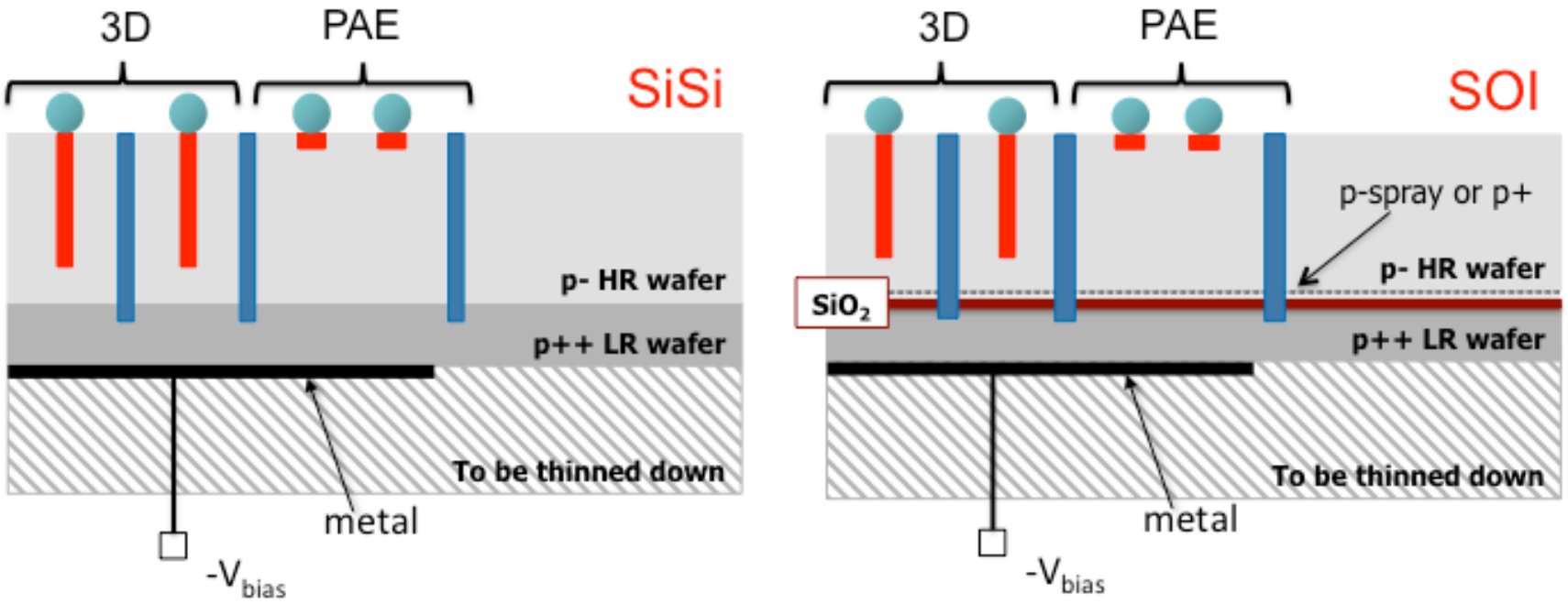
GOAL: development of new thin 3D and Planar Active Edge (PAE) pixel sensors on 6" p-type wafers at FBK:

- Technology and design to be optimized and qualified for extreme radiation hardness ($2x10^{16}$ n_{eq} cm^{-2})
- Pixel layouts compatible with present (for testing) and future (RD53 65nm) FE chips of ATLAS and CMS

Strong sinergy with WP7 of AIDA2020

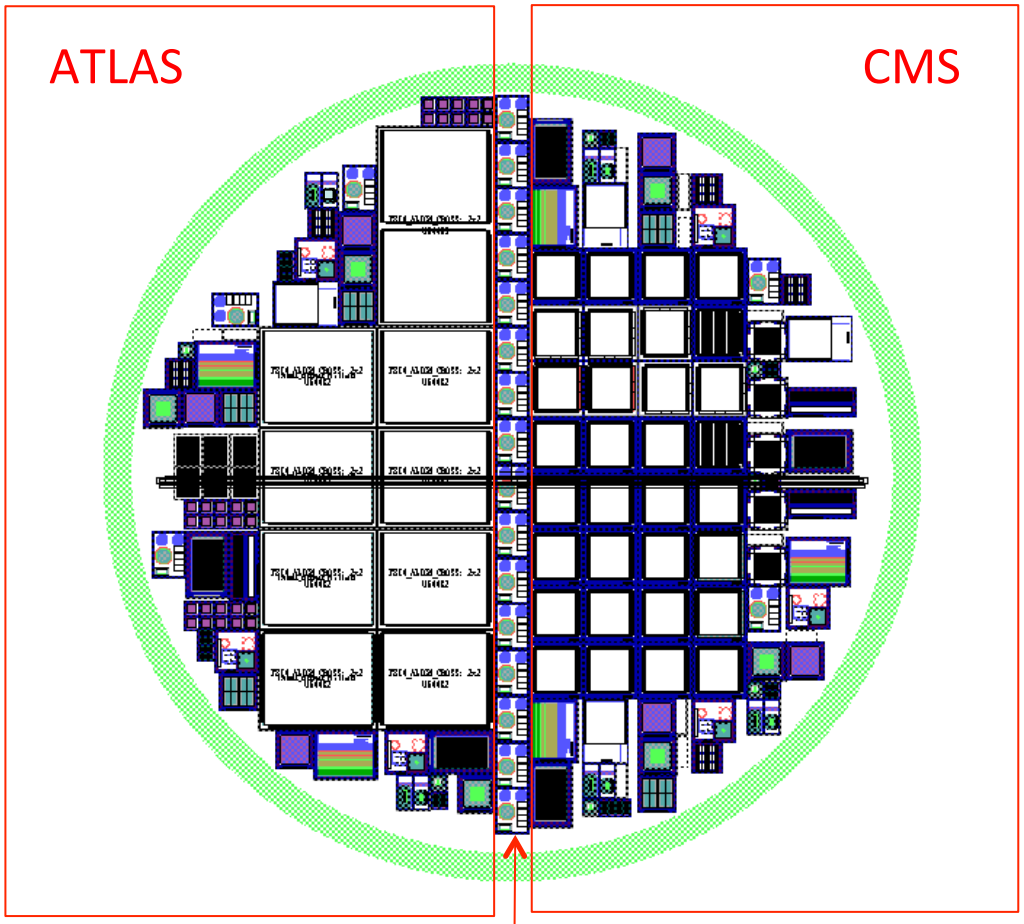
New single-side approach to 3D/PAE



- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~5 um
- Holes (at least partially) filled with poly-Si

Process Tests

Planar test batch



Test structures for SiSi DWB substrate qualification

Wafers

6” Si-Si silicon wafers (ICEMOS), 100±2μm and 130±2μm sensor layer thickness with ρ>3000 Ωcm (+500±10μm support wafer)

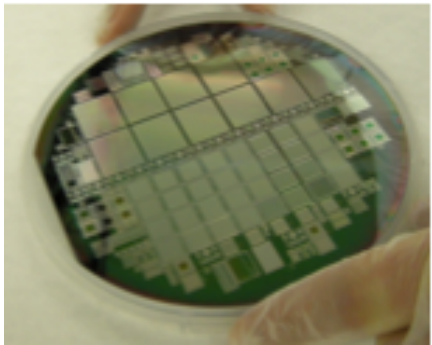
Process

- n-on-p planar process
- three different p-spray doses

Layout

- 10 ATLAS pixels (FEI4)
- 32 CMS pixels (PSI46)
- Many test structures

Batch completed at FBK in Dec. 2014

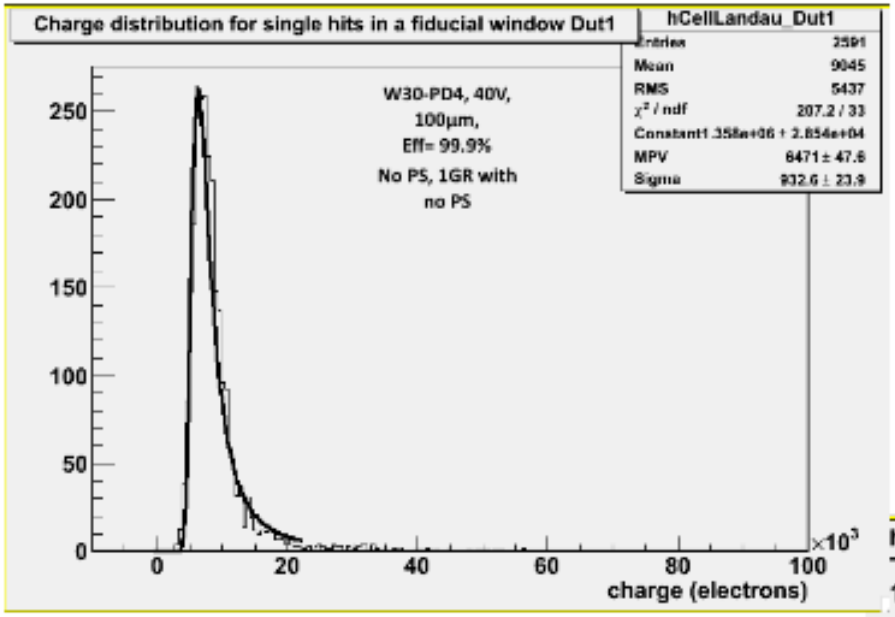


Summary of 2015 activity

- Tests on planar batch:
  - Good quality in terms of electrical characteristics (low defect density, low leakage current, low depletion voltage, high breakdown voltage)
  - Good efficiency and charge collection performance from test beam at FNAL Dec. 15 (before irradiation)
  - Deep diffusion of boron from LR substrate (~10 um)
- Successful technological tests for main steps of 3D:
  - Etching narrow (5 um) columns by DRIE
  - Two etchings from the same wafer side
  - Poly-Si filling of columns
  - Etching through oxide layer for SOI option
- Design and TCAD simulations

M. Meschini, INFN Firenze

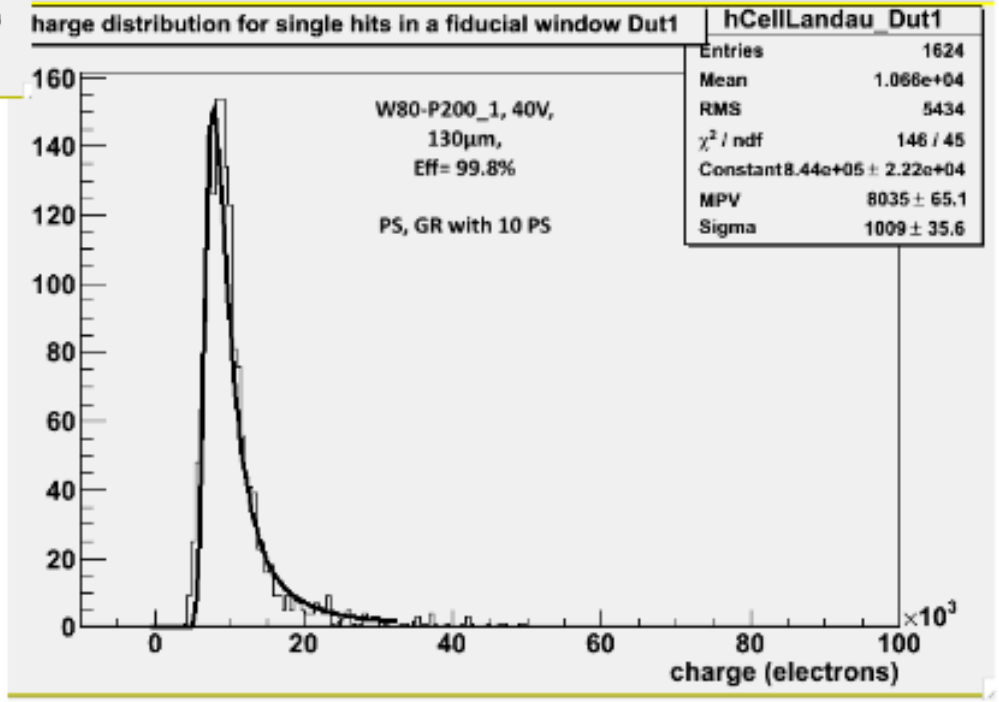
Spettri di Carica



MPV 100µ → 6400e⁻
MPV 130µ → 8000e⁻

Carica media 100µ → 9000e⁻
Carica media 130µ → 10600e⁻

Efficienze >99.8% sul volume fiduciale, ottenuto escludendo tutti i pixel non funzionanti e richiedendo 8 pixel attivi intorno al pixel attraversato dalla traccia



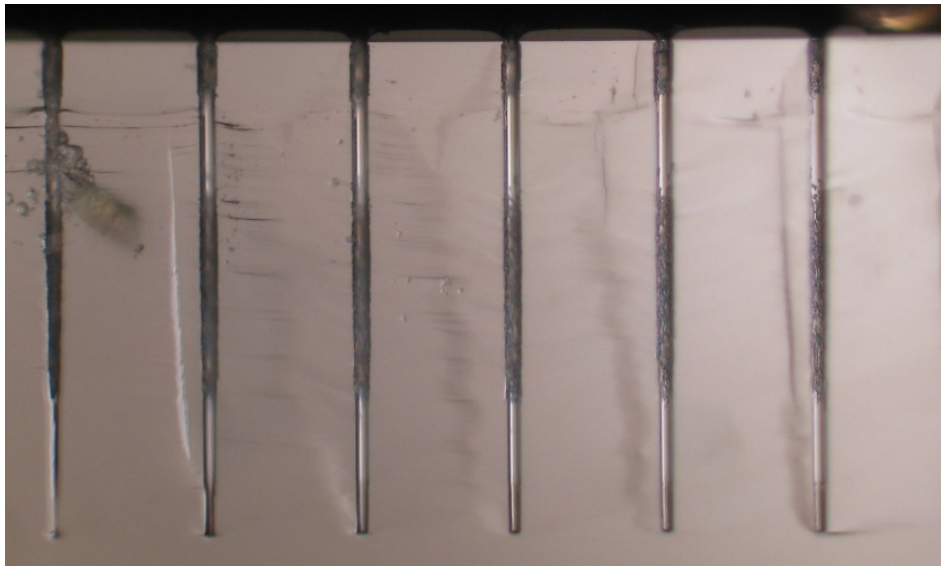
Etching test p-columns

S. Ronchin, FBK

p-holes > 130 µm

70' SDE+10' HER

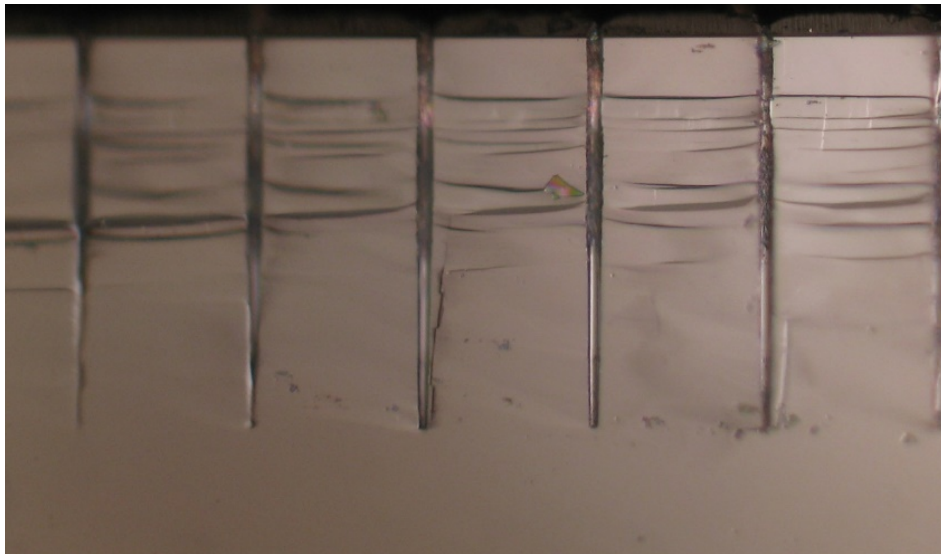
Position	depth (um)	Width at top	Width at bottom
c	**160**	5.3	4.0
t	159	5,5	2.25
f	156	5,8	3.2
dx	157	5, 5?	2.9
sx	**155**	4.85	2.6



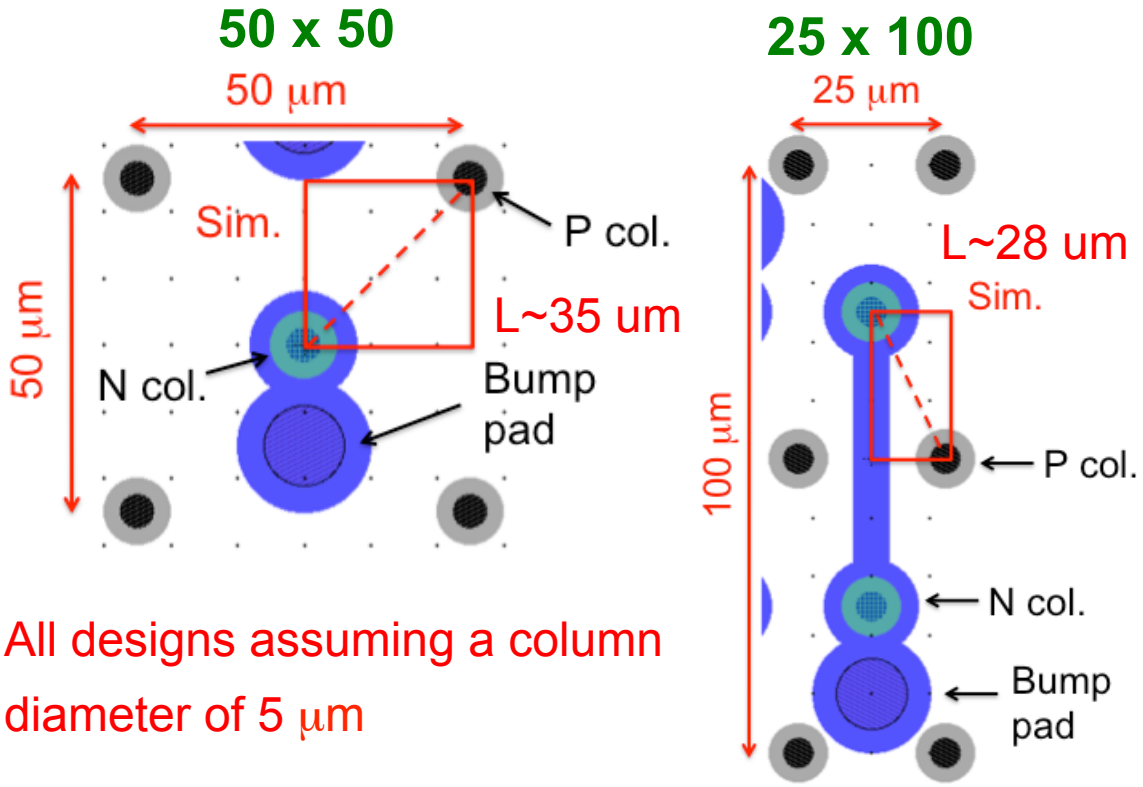
p-holes > 100 µm

43' SDE + 10'HER

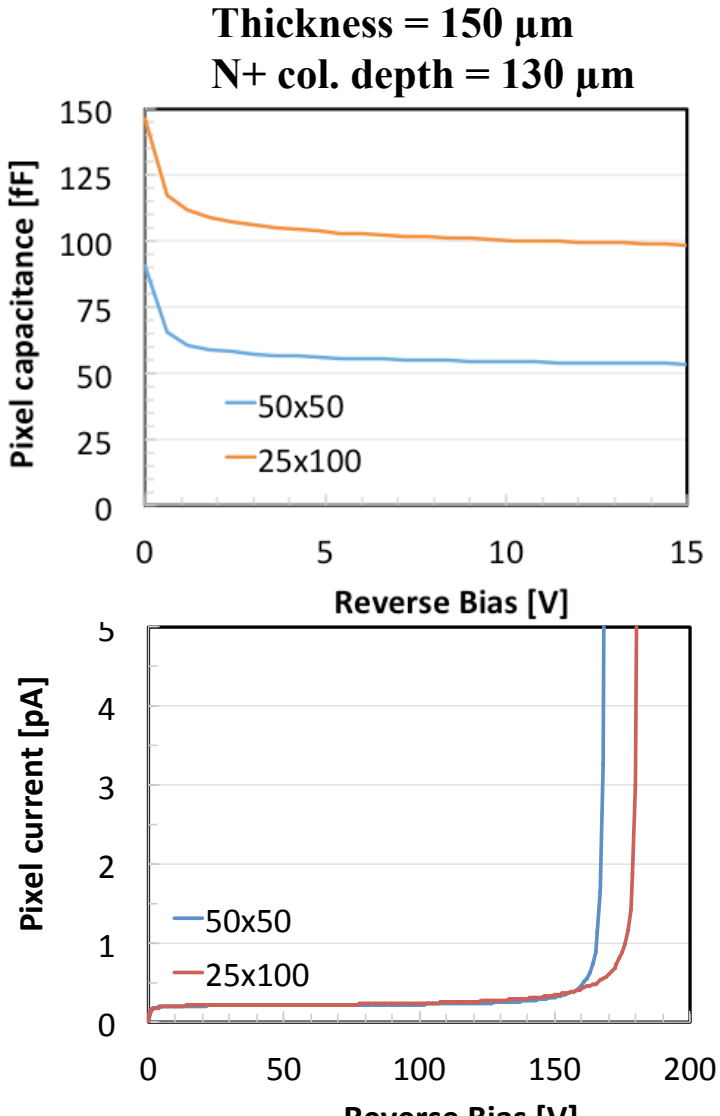
Position	depth (um)	Width at top	Width at bottom
c	**117**	4,7	3,2
t	117	4,4	3,2
f	114	4,7	3,2
Dx	115	5,2	3,2
Sx	**114**	4,8	2.4



New 3D pixels: design and simulations



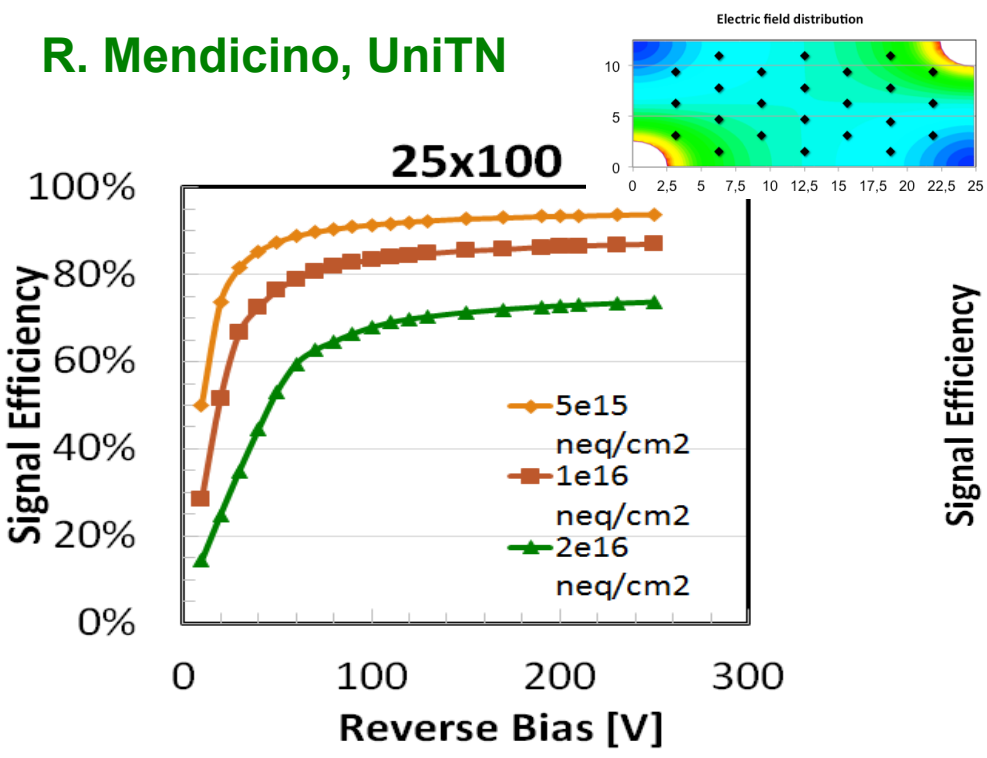
All designs assuming a column diameter of 5 µm

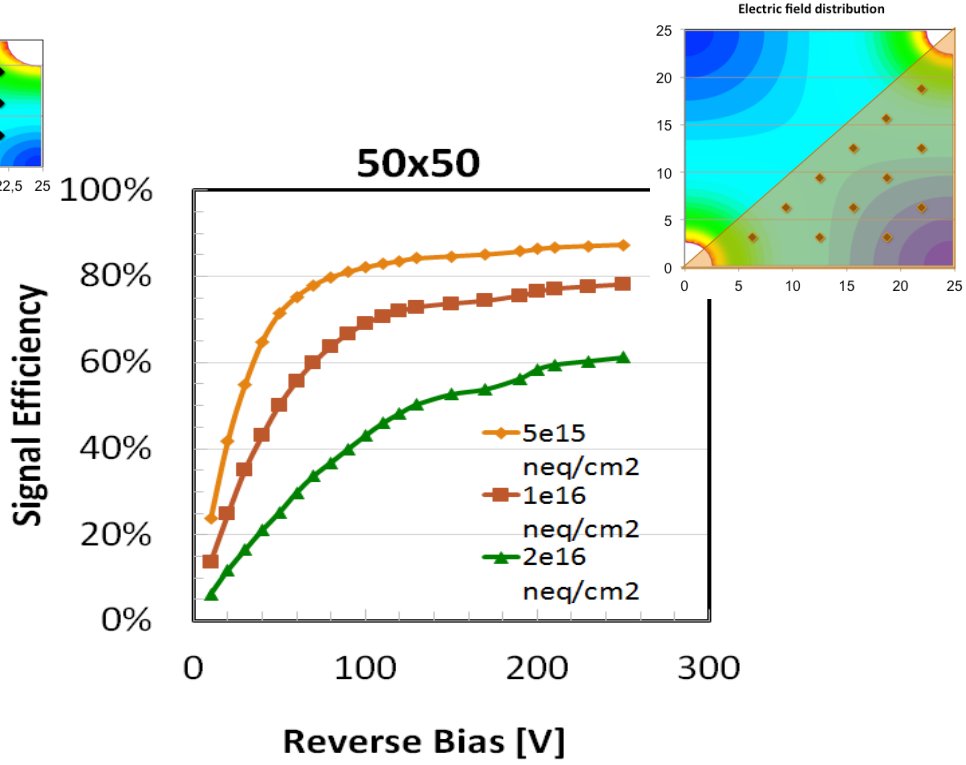


- 50x50 design safe, 25x100 is difficult … too little clearances (new ideas for bump pad to be tested)
- Capacitance compatible with RD53 specs
- Initial breakdown voltage high enough

Simulated signal efficiency (preliminary)

R. Mendicino, UniTN

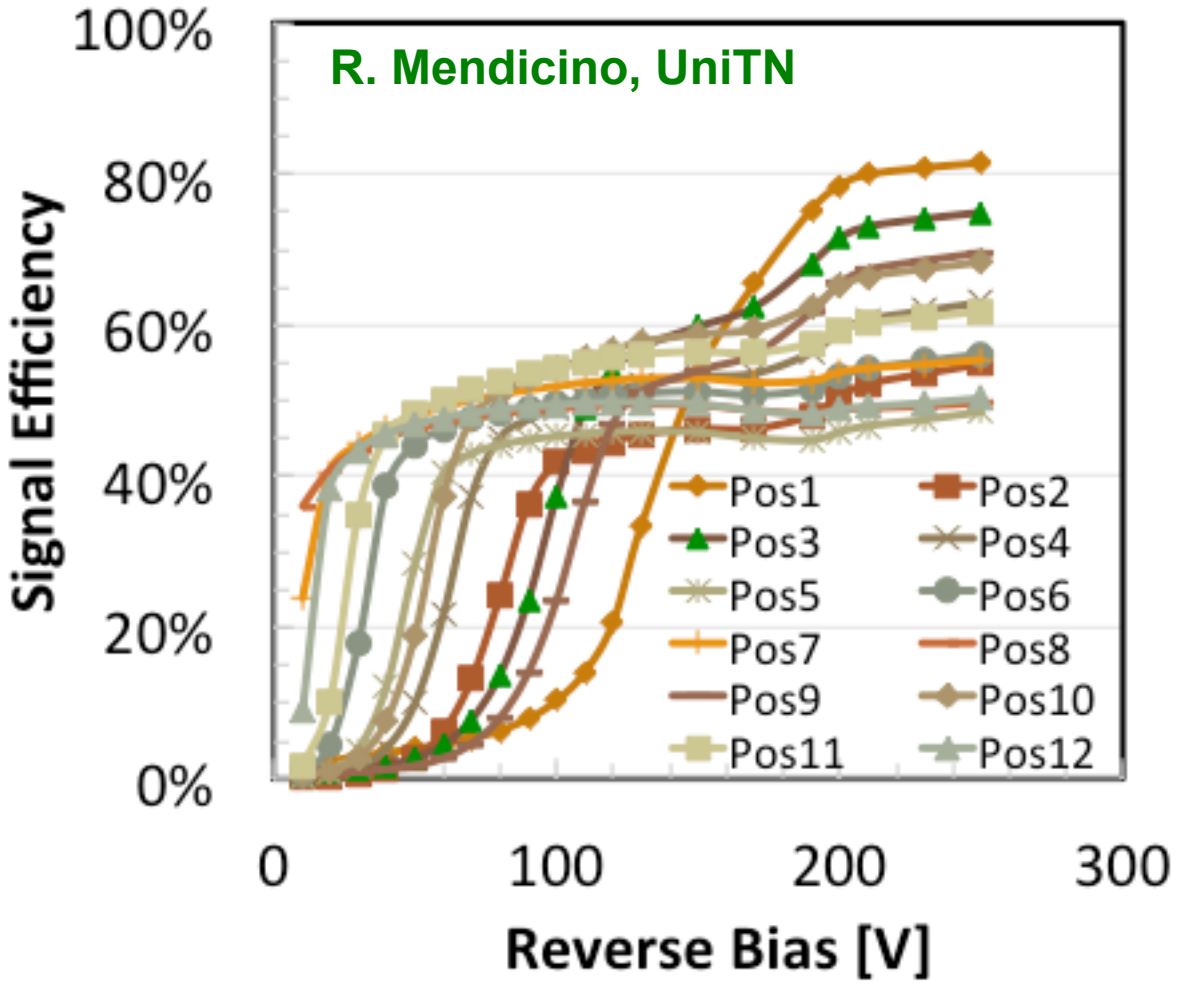


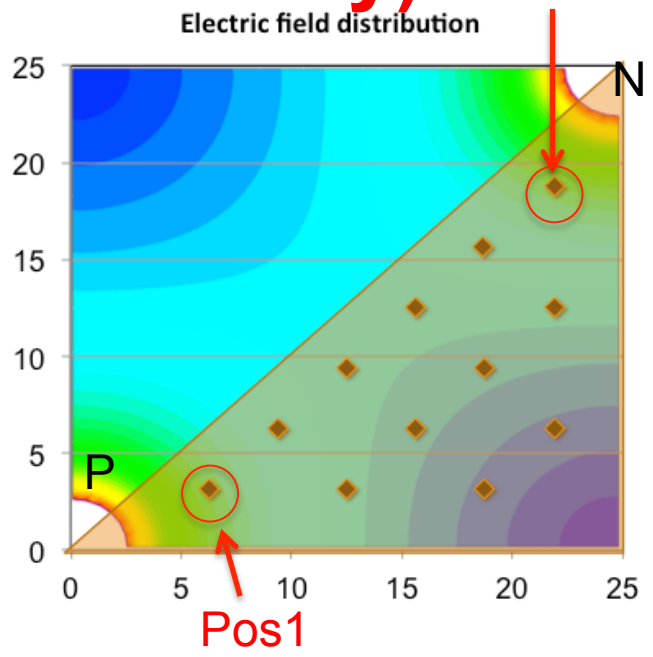


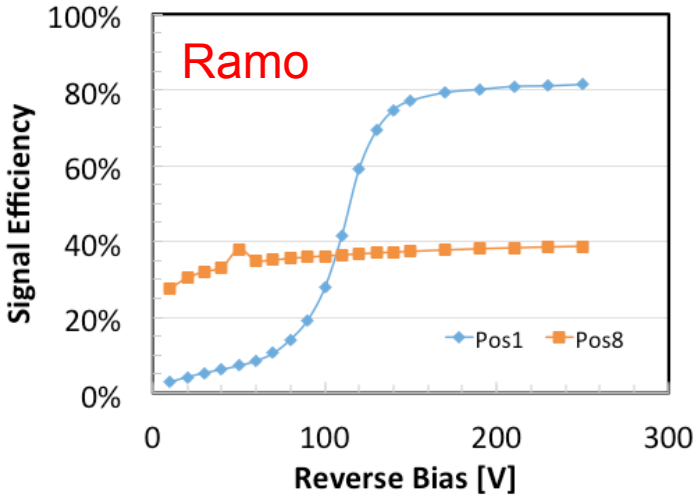
- New 3-trap level "Perugia" model, D. Passeri et al. (doi:10.1016/j.nima.2015.08.039)
- 1 μm thick (~2d) slice, with MIP vertical hits at several different points
- 20-ns integration of current signals, average, and normalization to injected charge
- Much better results than with previous trap model !
- Higher Signal Efficiency at lower V_{bias} in 25x100 (2E), as expected due to smaller L

Spatial non uniformity (preliminary)

Evidence of non obvious signal vs voltage features due to small pixel size

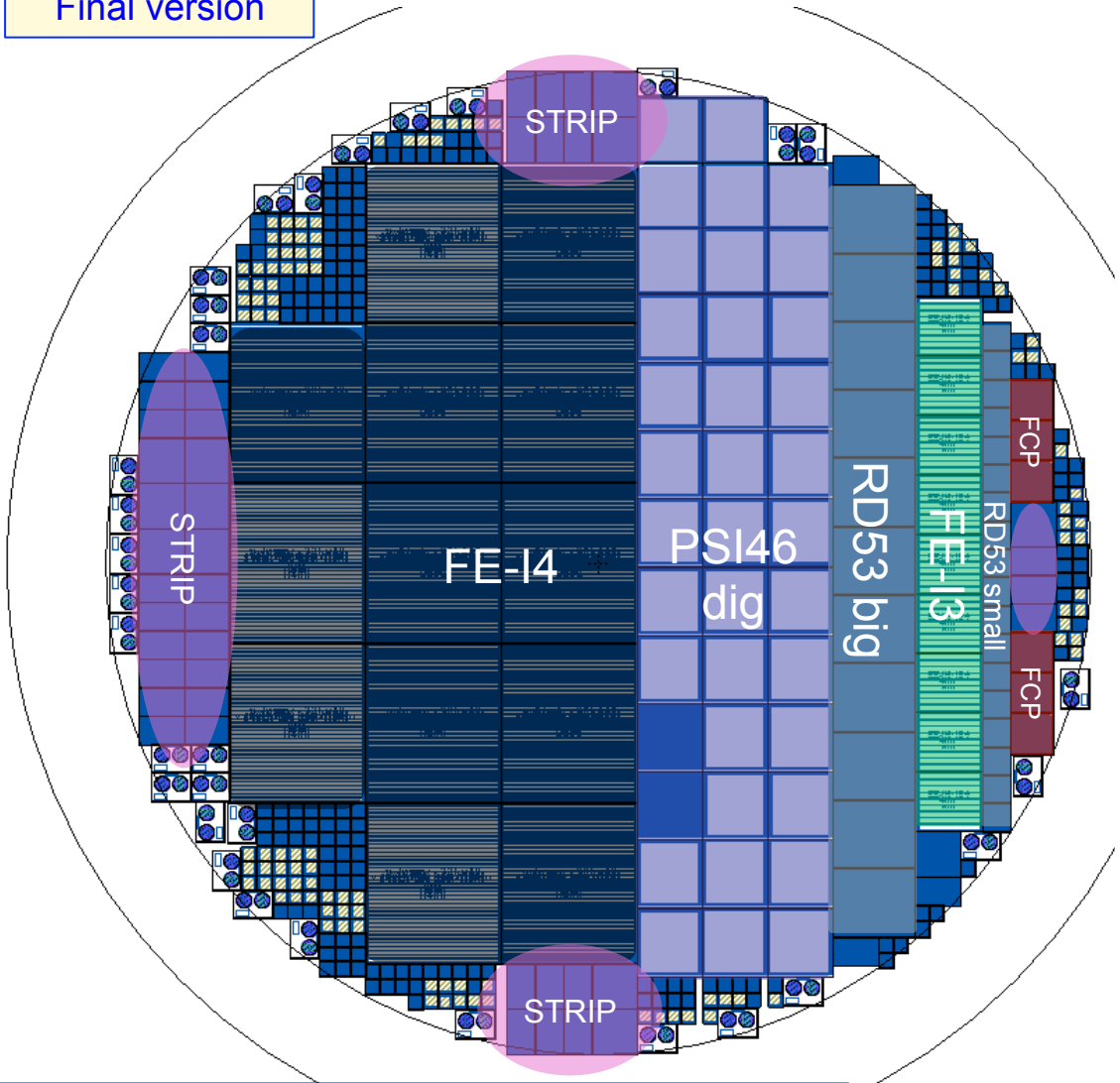






3D Pixel Wafer Layout

Final version



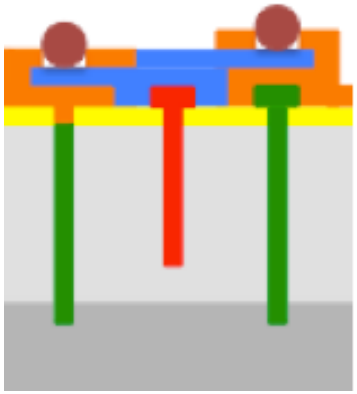
+ Test structures (strip, diodes, etc)

Many different pixel geometries and pitch variations:

- FE-I4
  - 50 x 250 (2E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
  - 25 x 500 (1E)
- FE-I3
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- PSI46dig
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E and 2E)
  - 50 x 100, 100 x 100 (2E + 4E)
  - 50 x 100, 100 X 150 (2E + 6E)
  - 25 x 100 (1E and 2E)
- FCP
  - 30 x 100 (1E)
- RD53
  - 50 x 50 (1E)
  - 25 x 100 (1E)
  - 25 x 100 (2E)

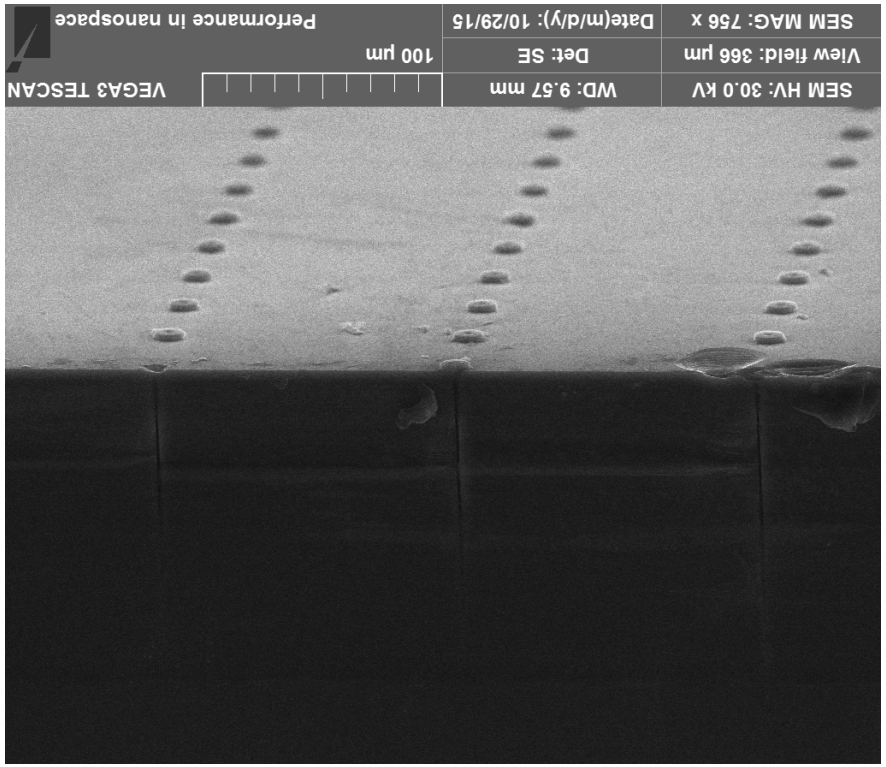
Fabrication status at FBK

- First 3D batch (15 SiSi DWB wafers) aborted at the end of October 2015 due to problem with Boron doping of ohmic columns …
- Four wafers (3D_rec) completed anyway to check all relevant process steps (under test)
- A new 3D batch (10 SiSi DWB wafers) re-launched in November 2015, now being completed:
  - 3 wafers 100μm thick, p-columns with poly “cap”
  - 2 wafers 100μm thick, p-columns without poly “cap”
  - 3 wafers 130μm thick, p-columns with poly “cap”
  - 2 wafers 130μm thick, p-columns without poly “cap”
- First two wafers ready this week …

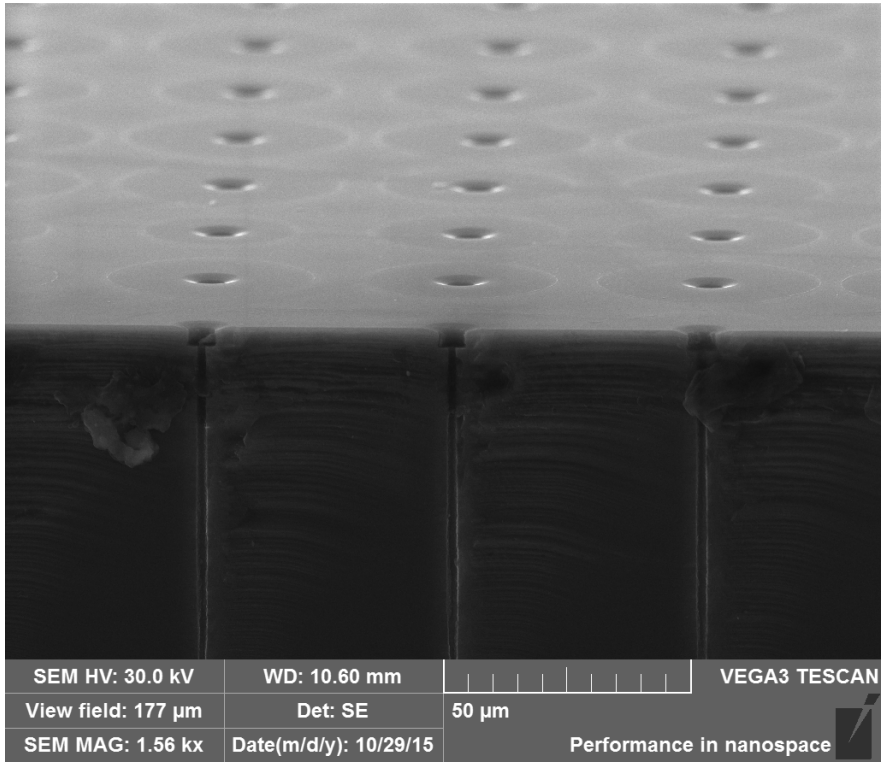


Fabrication at FBK (1)

P column etching/poly filling details



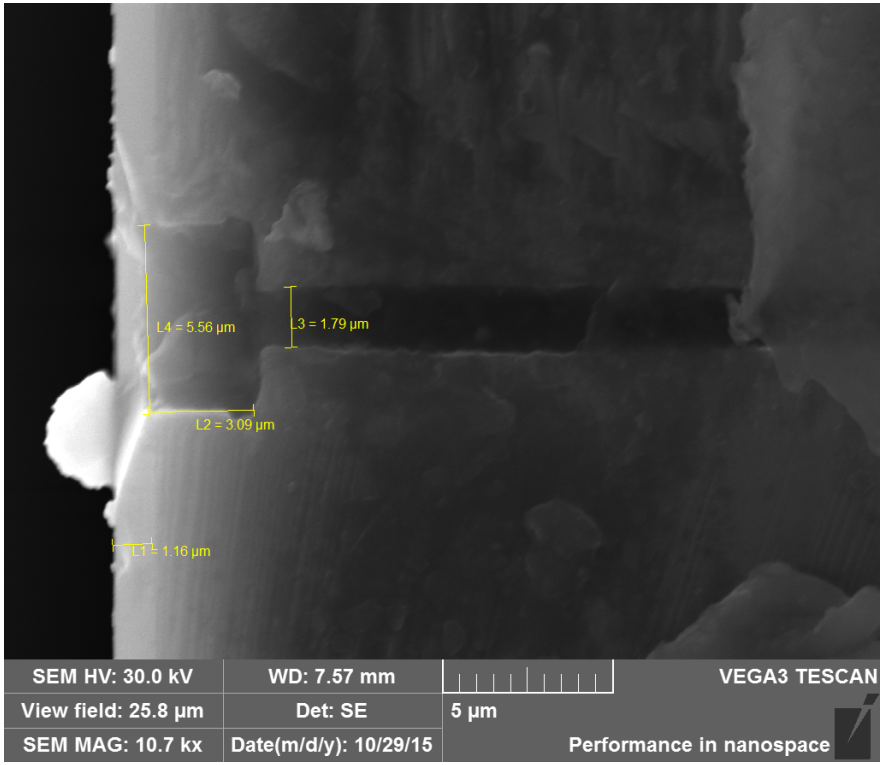
With poly cap



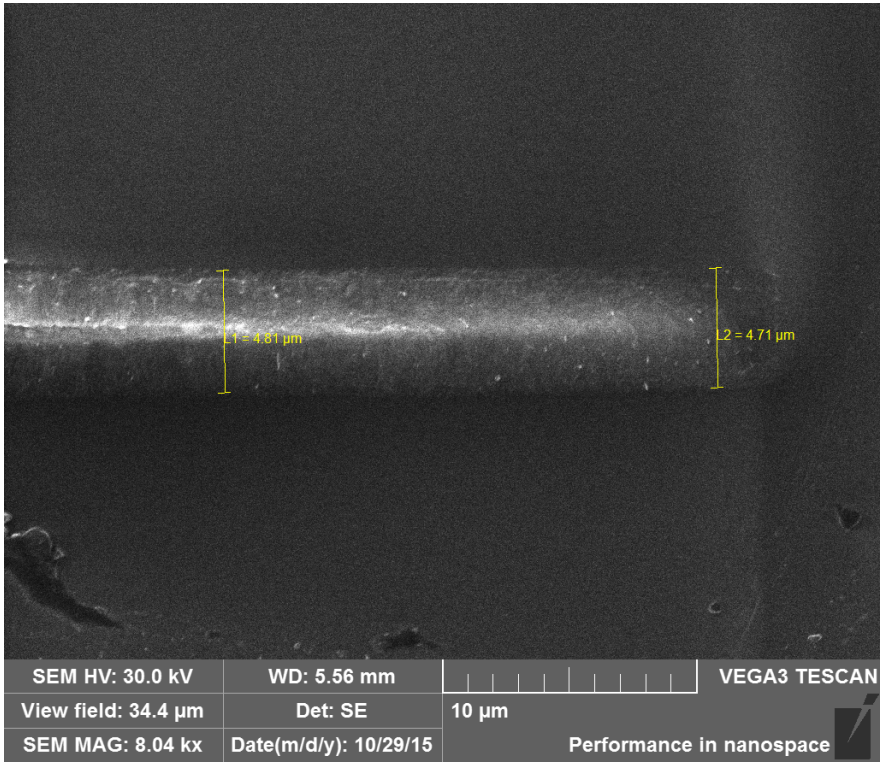
Without poly cap

Fabrication at FBK (2)

P column etching/poly filling details (w/o poly cap)



Column opening

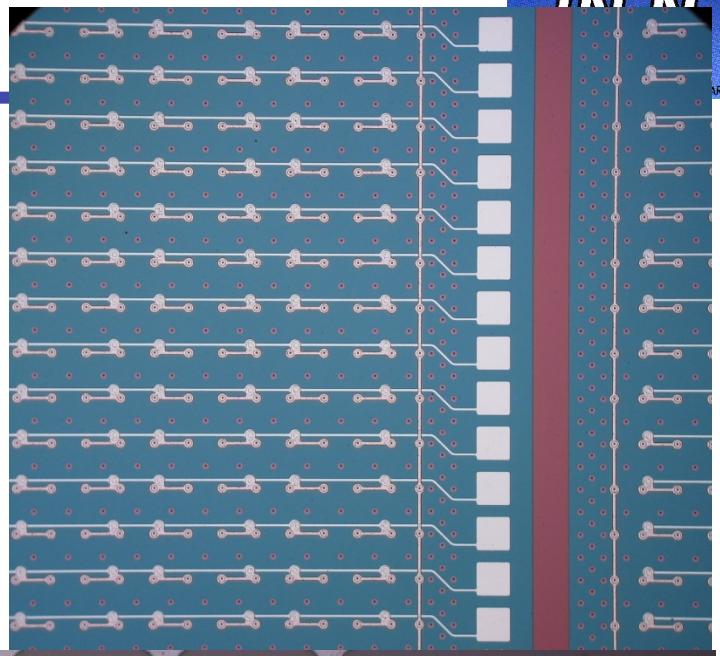


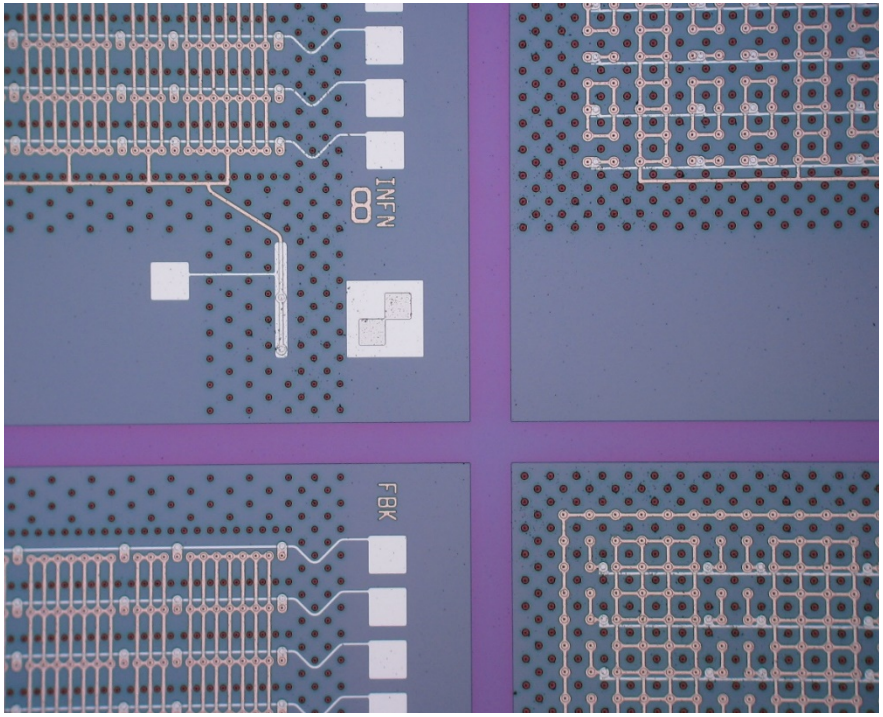
Column end

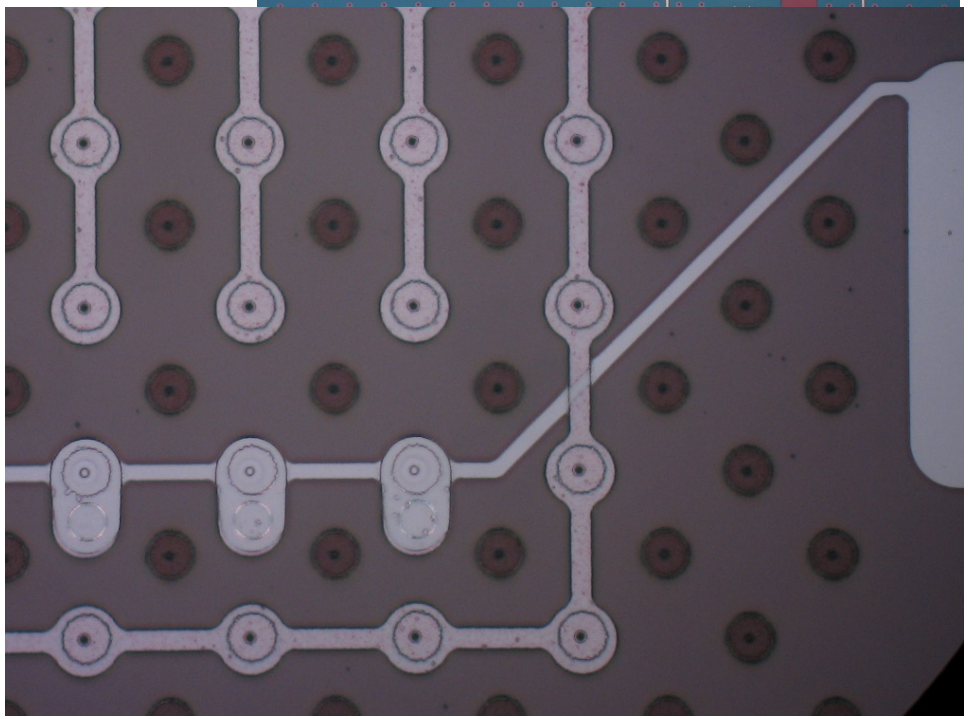
S. Ronchin, FBK

A few pictures from 3D_rec

- 4 wafers completed smoothly
- Good lithographical quality
- Tests confirm lack of ohmic doping

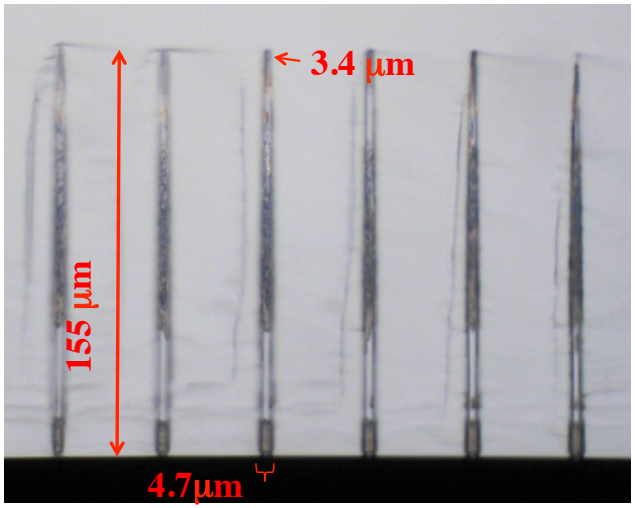




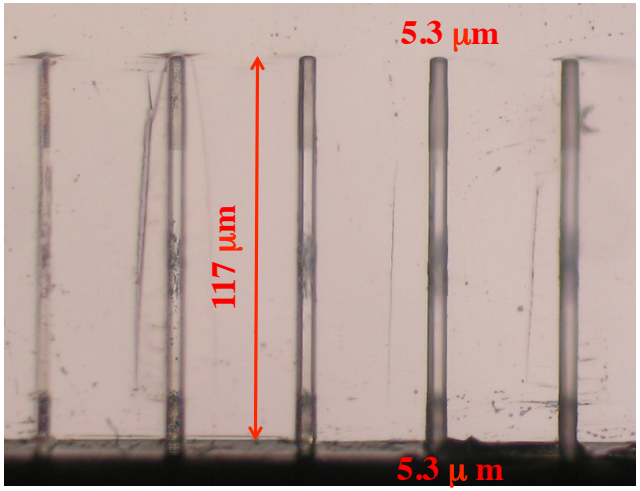


Back-Up slides

Etching narrow columns by DRIE

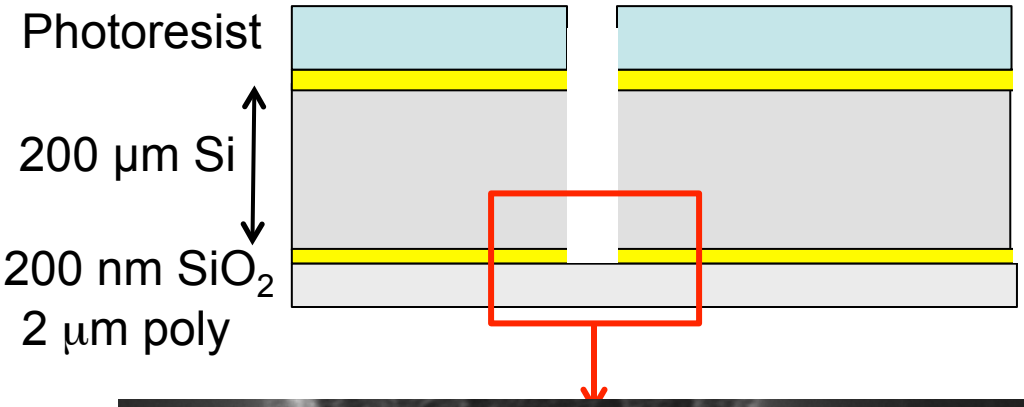


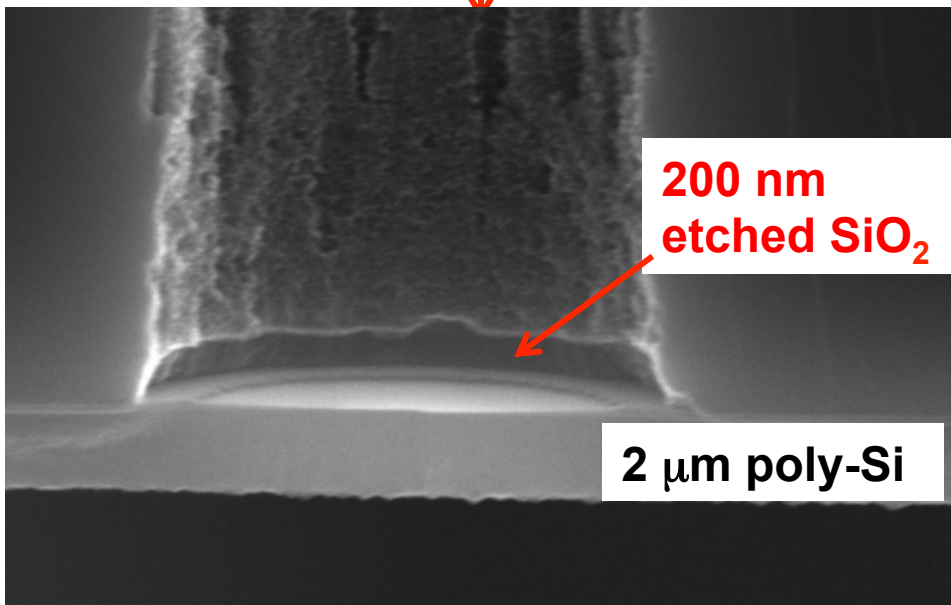
Ohmic columns optimized for depth



Junction columns optimized for uniformity

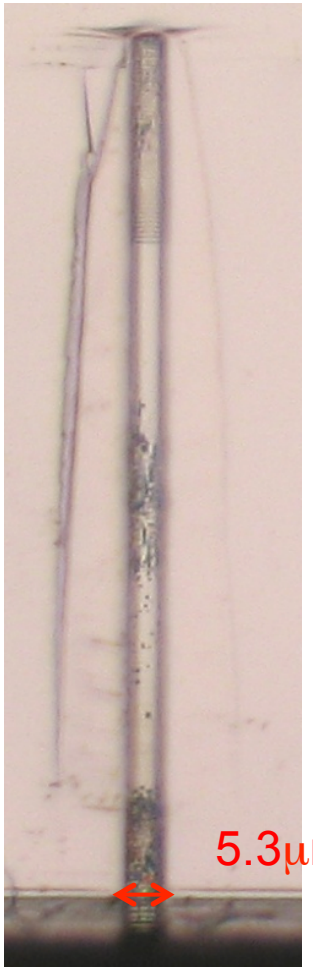
Testing different etching depth and etching through oxide layer for SOI approach



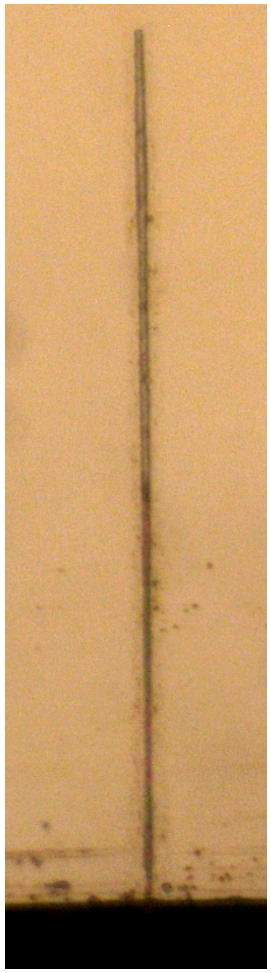


Poly-Si filling and 2nd DRIE

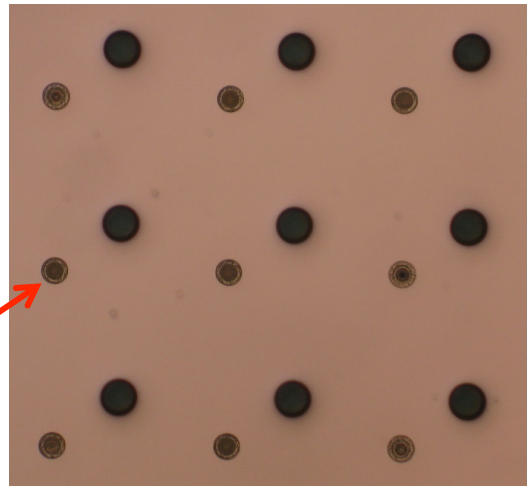
Reducing the hole diameter with poly-Si deposition to ease the 2nd DRIE on the same wafer side

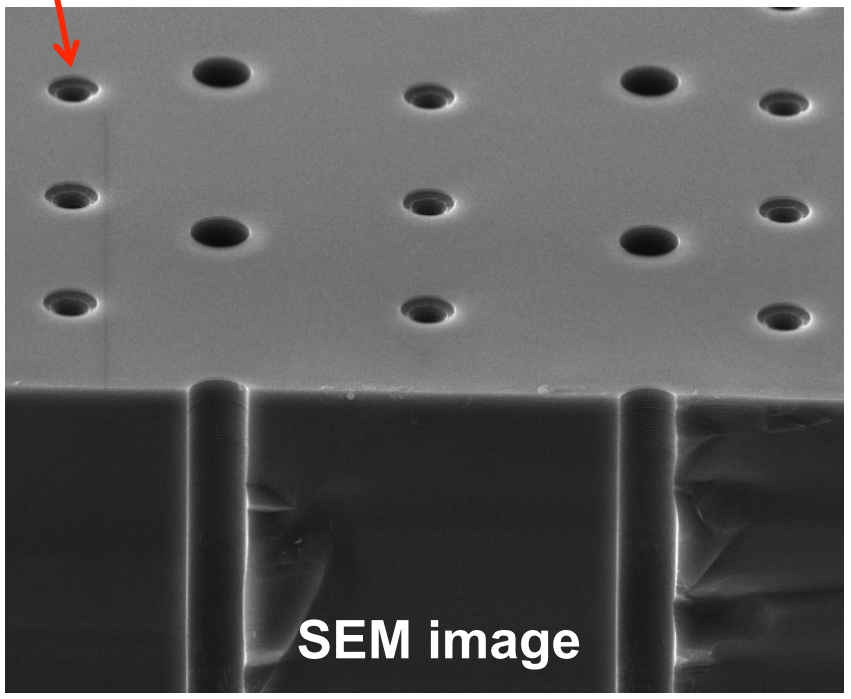


4μm poly-Si



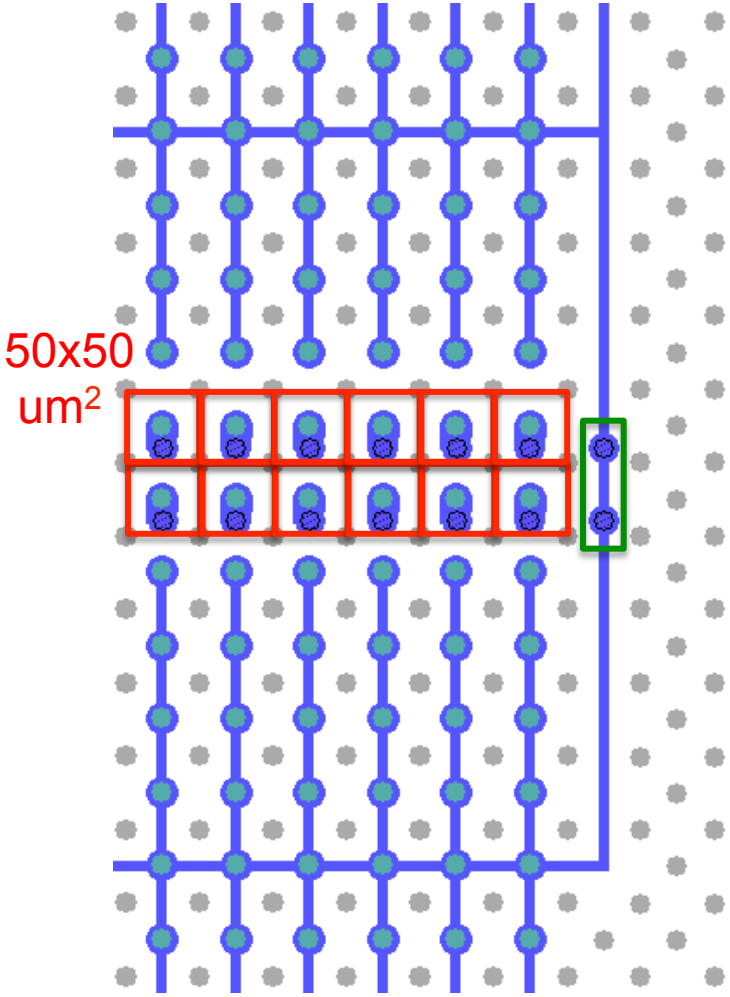
First holes partially filled with poly-Si



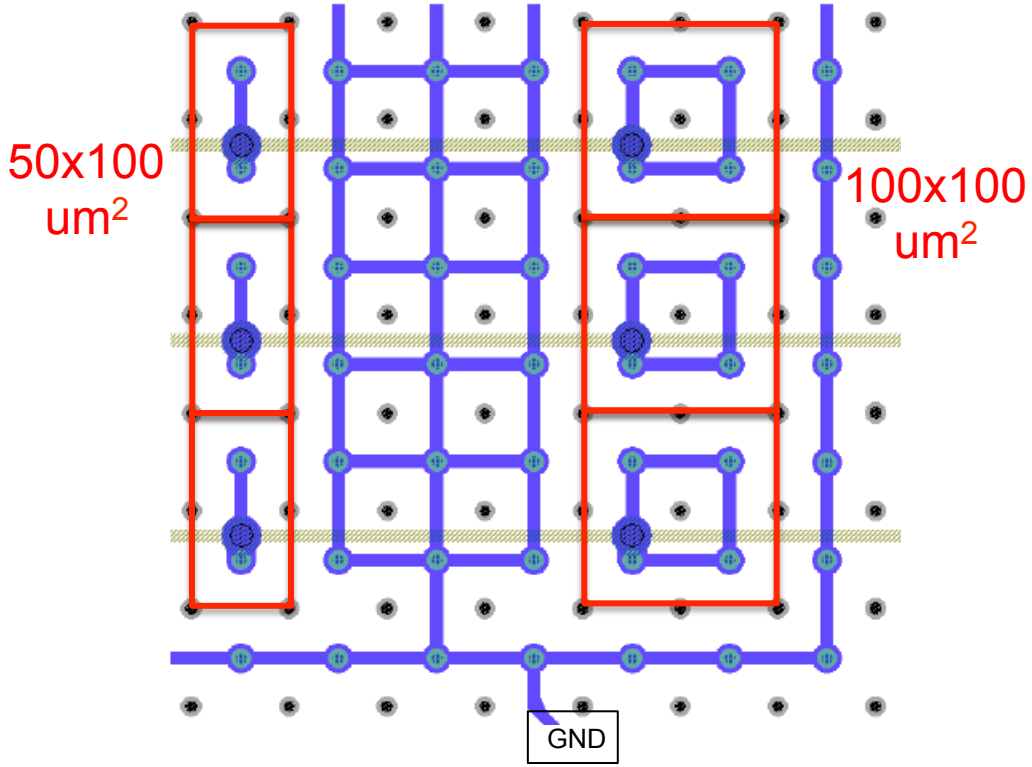


New pixels with existing ROCs ?

ATLAS FE-I4 50x50 (1E) + grid

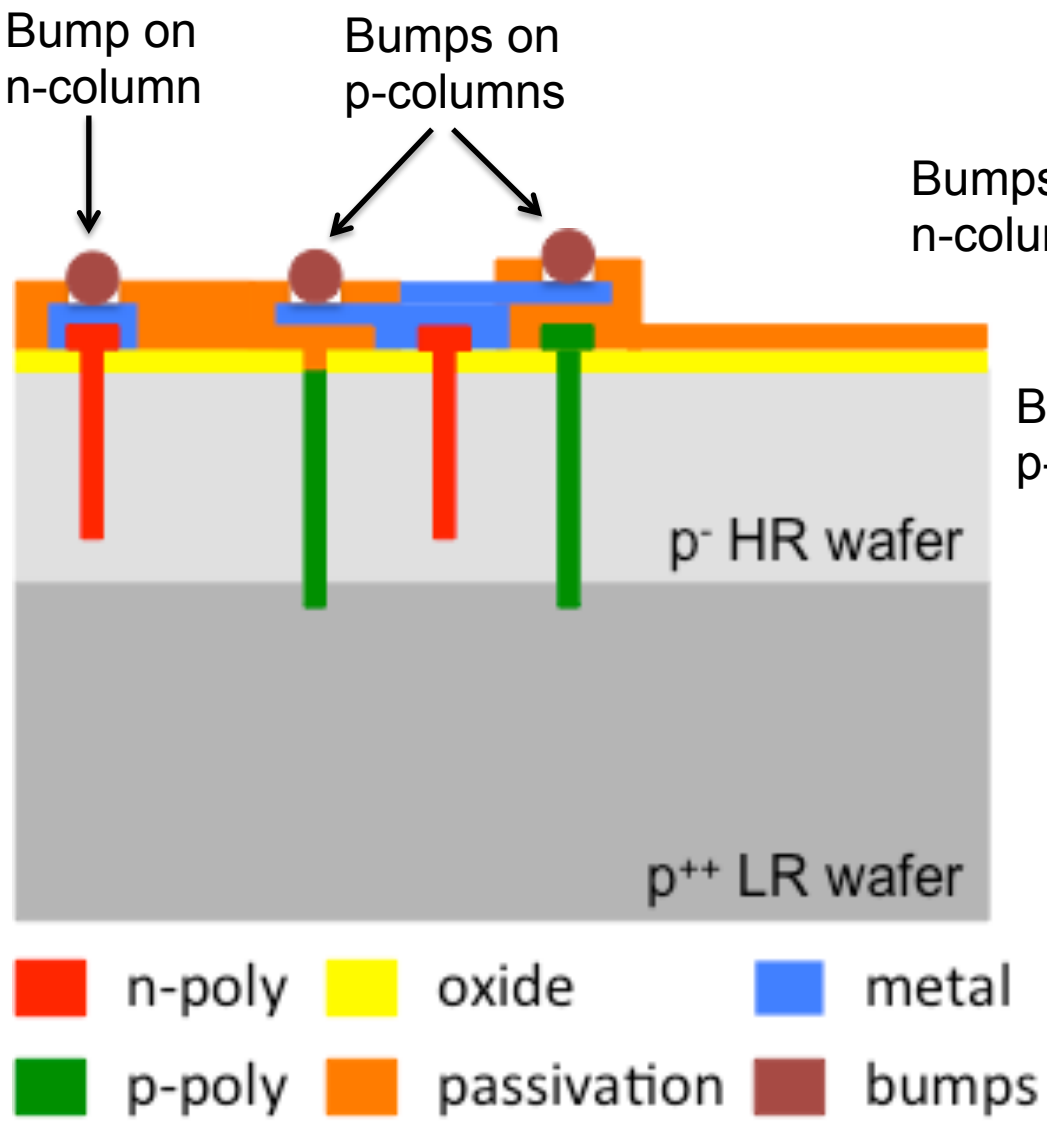


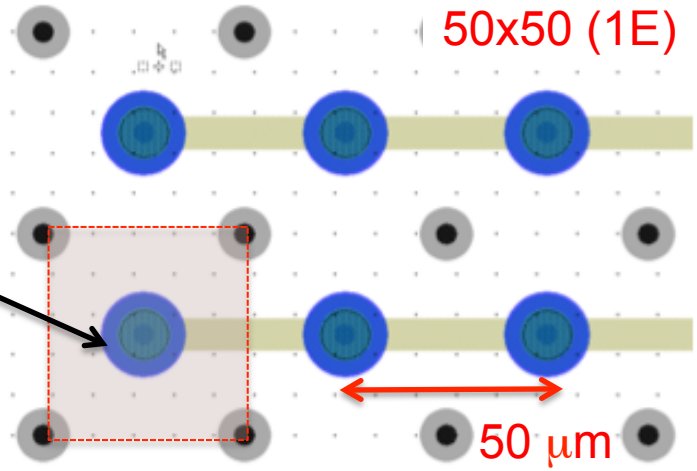
CMS PSI46: 50x50 (2E+4E) + grid

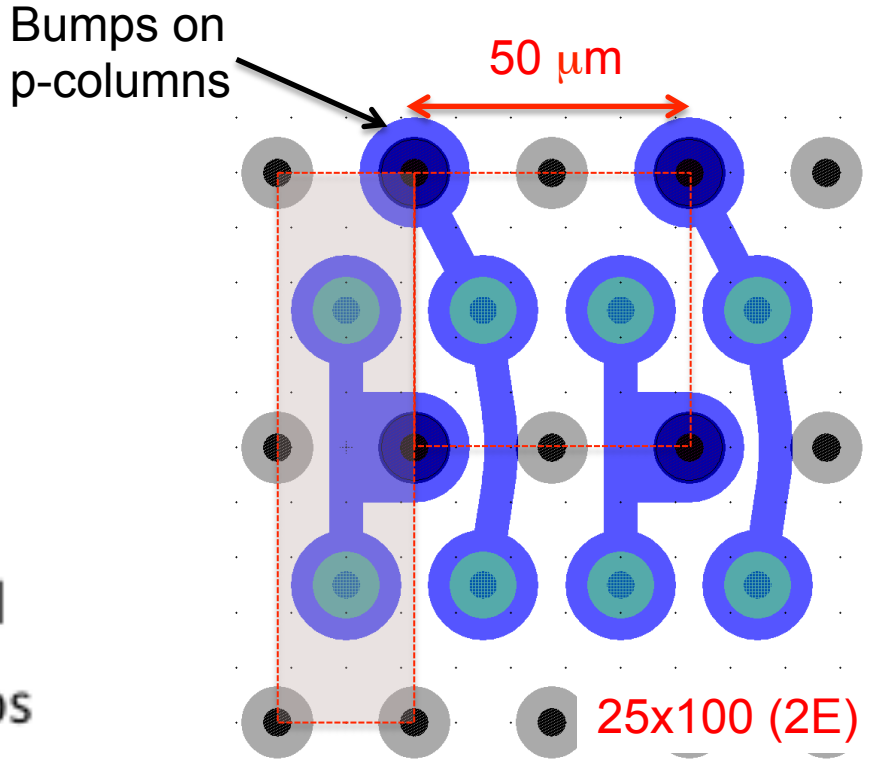


Small pixels take all bonding pads
+ rest of pixels at GND using a metal grid and extra-pads at the periphery

Bumps on columns

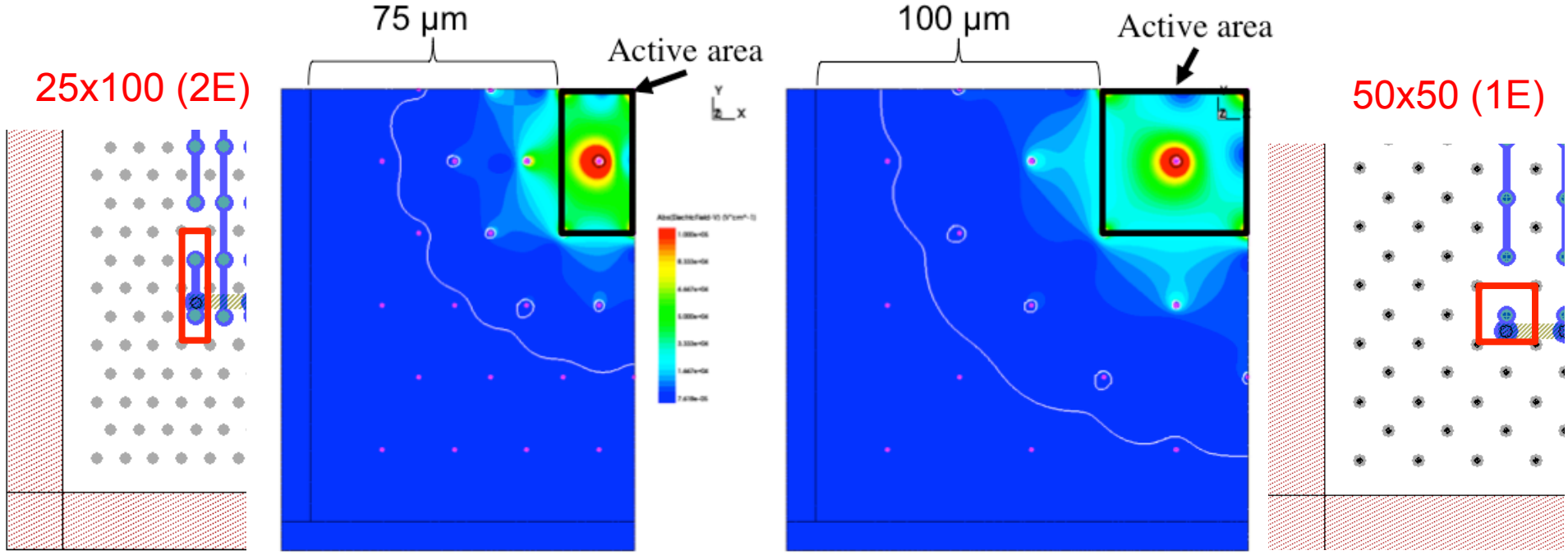






Slim edges

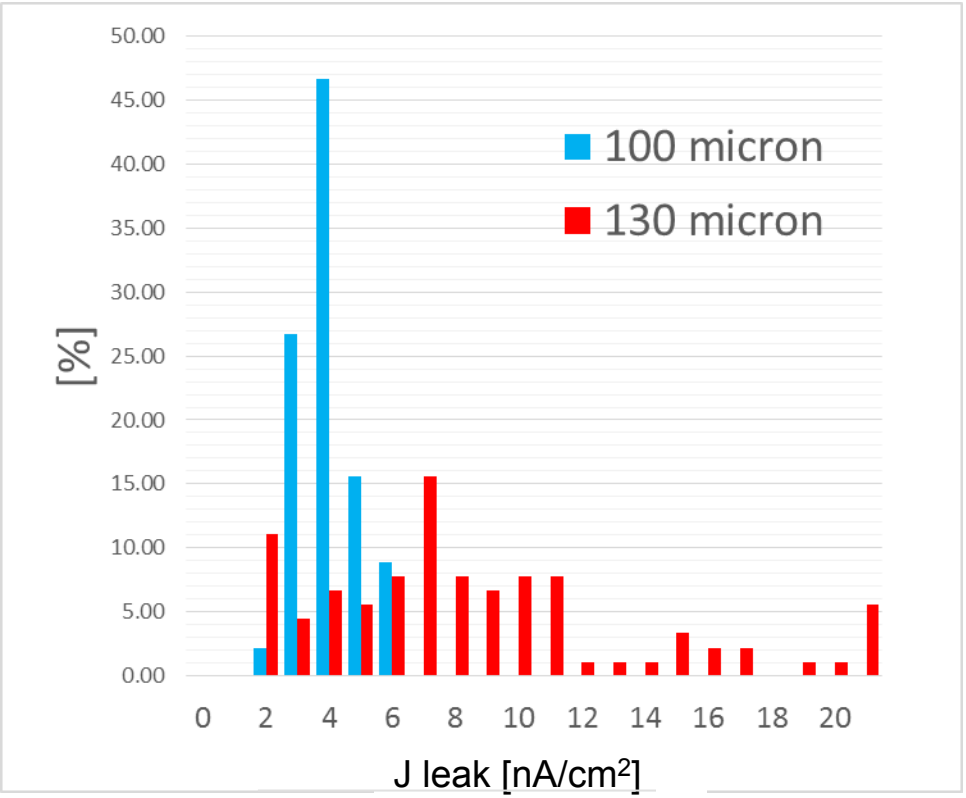
- Slim edge concept based on multiple ohmic columns termination developed for IBL (~200 μm) M. Povoli et al., JINST 7 (2012) C01015
- It can be made slimmer by reduced inter-electrode spacing (safely 75 - 100 μm, more aggressively down to ~50 μm)
- 3D guard rings also possible with similar dead area

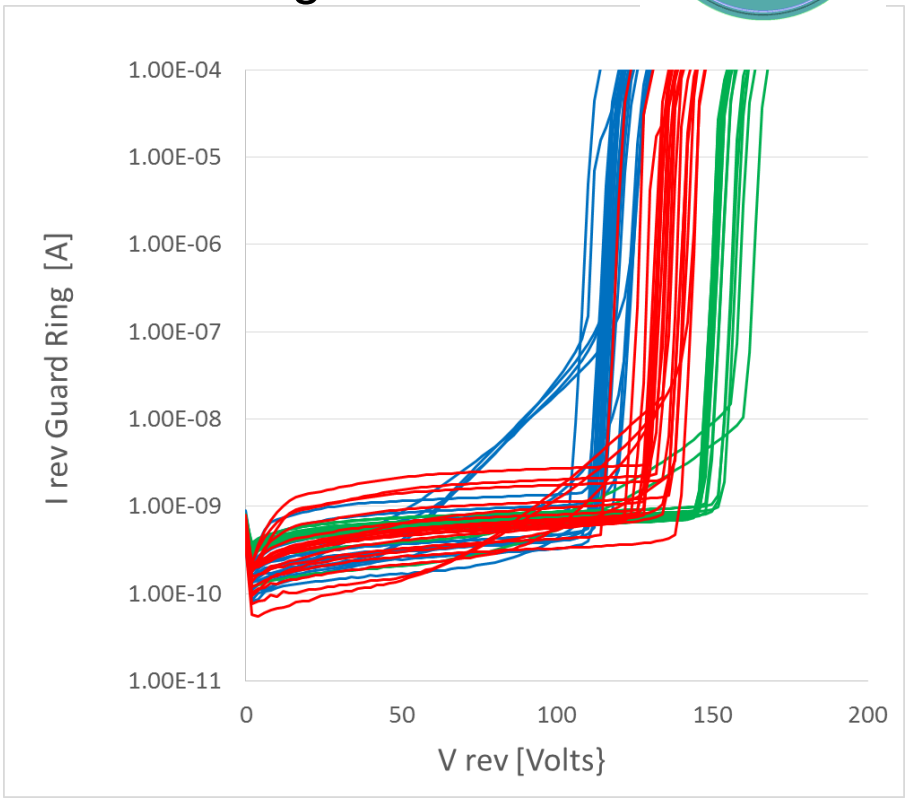


Test diode: I-V measurements

Measured at FBK up to 200 V

Circular diode, 4 mm^2, two Guard Rings





J_{leak} distribution on 135 diodes

→Different material quality ?

Guard Ring reverse currents on 3 wafers with 3 p-spray doses: Low Medium High (correct V_{bd} trend)

Test diode: C-V measurements

Measured at FBK

Depletion voltages:

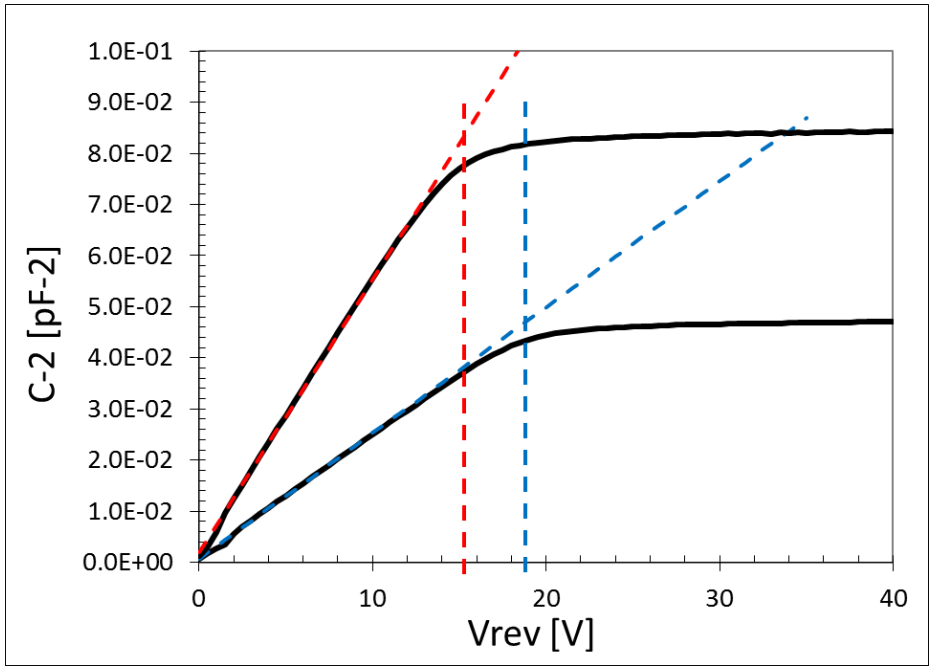
- V_{depl} ~ 16V for 130 μm thick.
- V_{depl} ~ 20V for 100 μm thick.

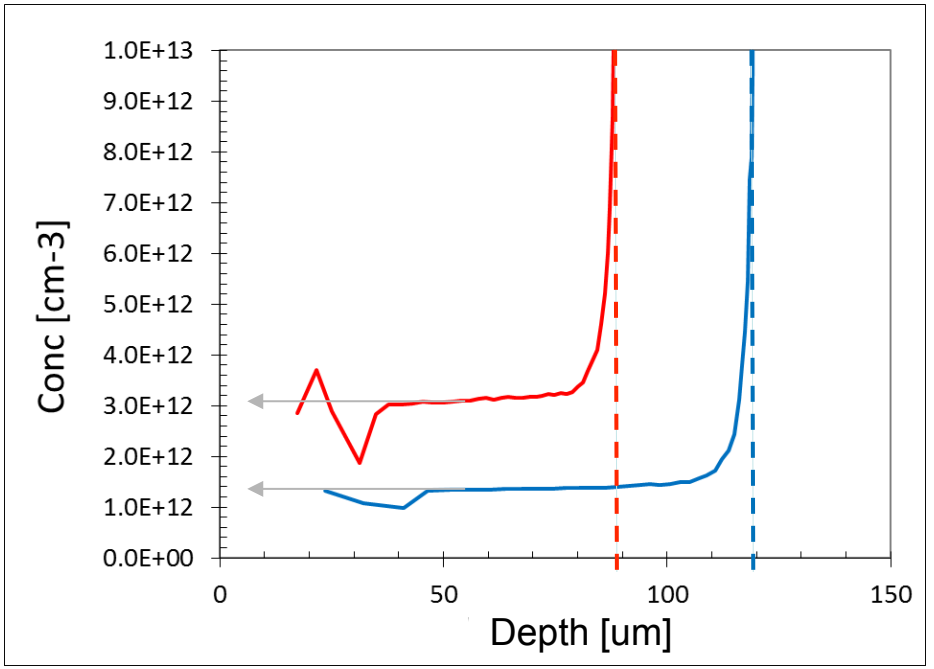
do not scale with square of thickness

→ Different resistivities …

Concentration profiles

- Doping 1 – 3 x 10^{12} cm^{-3}
- Thicknesses about 10 μm lower than the nominal values, compatible with Boron diffusion from support wafer and measurement limit (L_{debye})





Pixel sensors I-V measurements

Measured at INFN Firenze up to high voltage