

Simulation activities

Federica Fabbri on behalf of the group

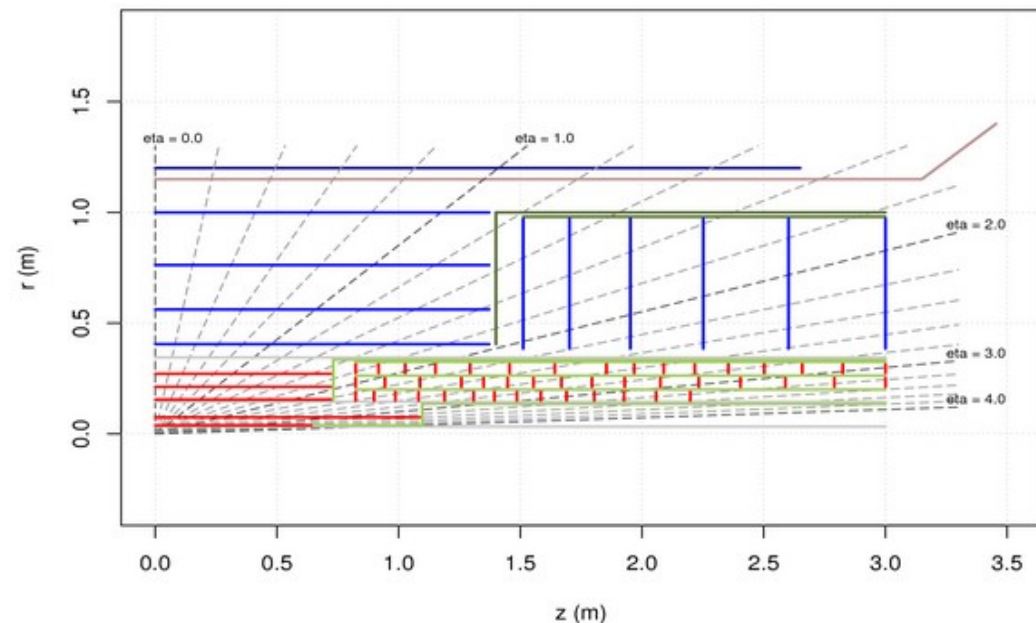
Outline

- Layout task force status
 - Layout task force timeline.
 - Status of step 1.
 - *People involved: Claudia Gemme (Ge), Silvia Miglioranzi (Ge).*
- Study of ITk layout optimization:
 - Study of ITk performance in terms of resolution, efficiency and fake rate.
 - Pile up stability.
 - Fake definition.
 - *People involved: Federico Massa (Pi), Claudia Gemme (Ge), Giorgio Chiarelli (Pi) e Chiara Roda (Pi).*
- Study of performance and maintenance of fast pixel digitization algorithm:
 - Fast digitization algorithm validation wrt the full digitization.
 - Use of the algorithm for upgrade studies (change sensor pitch and thickness).
 - Performance algorithm improvement (flexibility, time...).
 - *People involved: Antonio Sidoti (Bo), Matteo Negrini (Bo), Federica Fabbri (Bo), Carla Sbarra (Bo)*

Layout task force: step 1 layout summary.

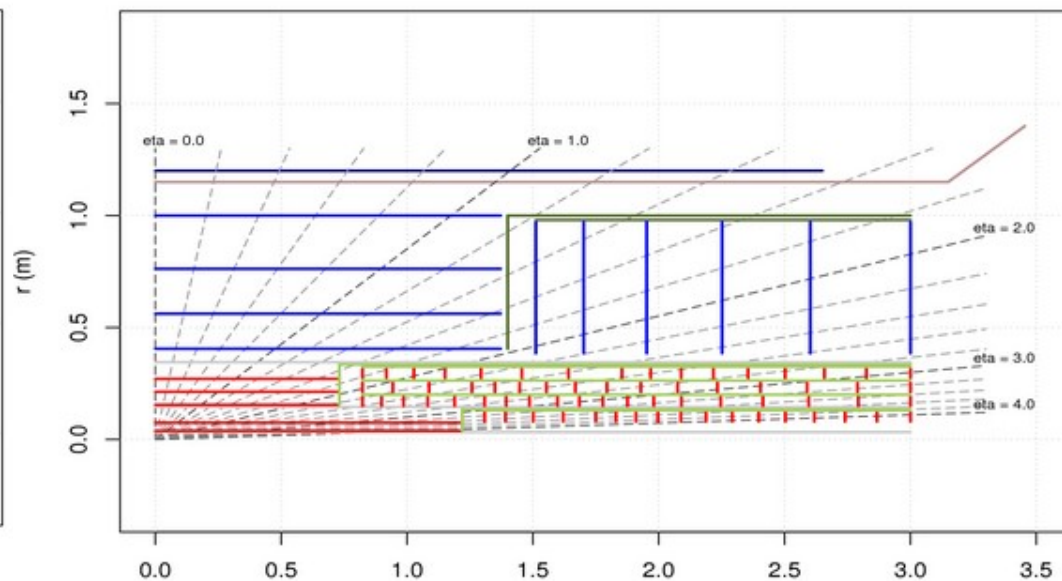
Extended_3.2

This layout is optimized for 9 space points up to $|\eta| = 3.2$.



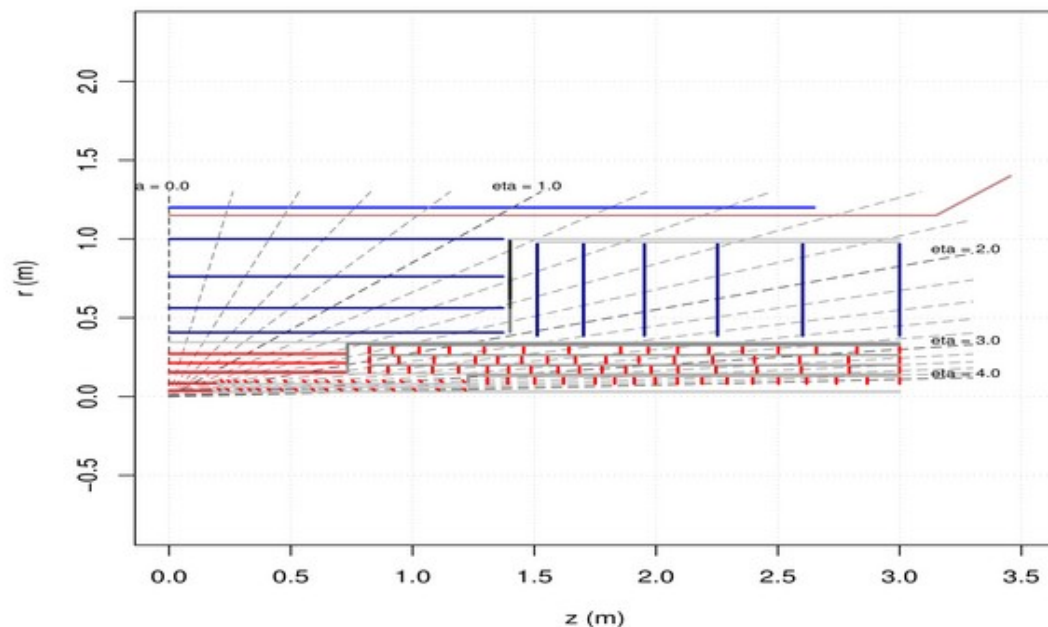
Extended_4.0

This layout is optimized for 9 space points up to $|\eta| = 4.0$.



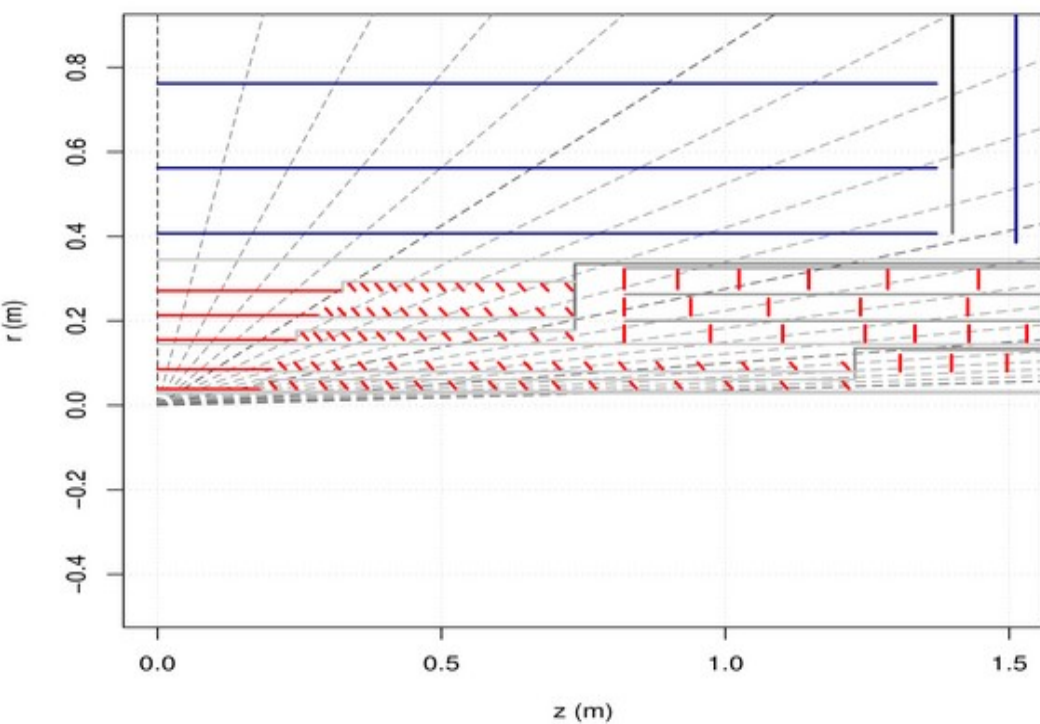
Inclined_4.0

This layout is optimized for 9 space points up to $|\eta| = 4.0$.

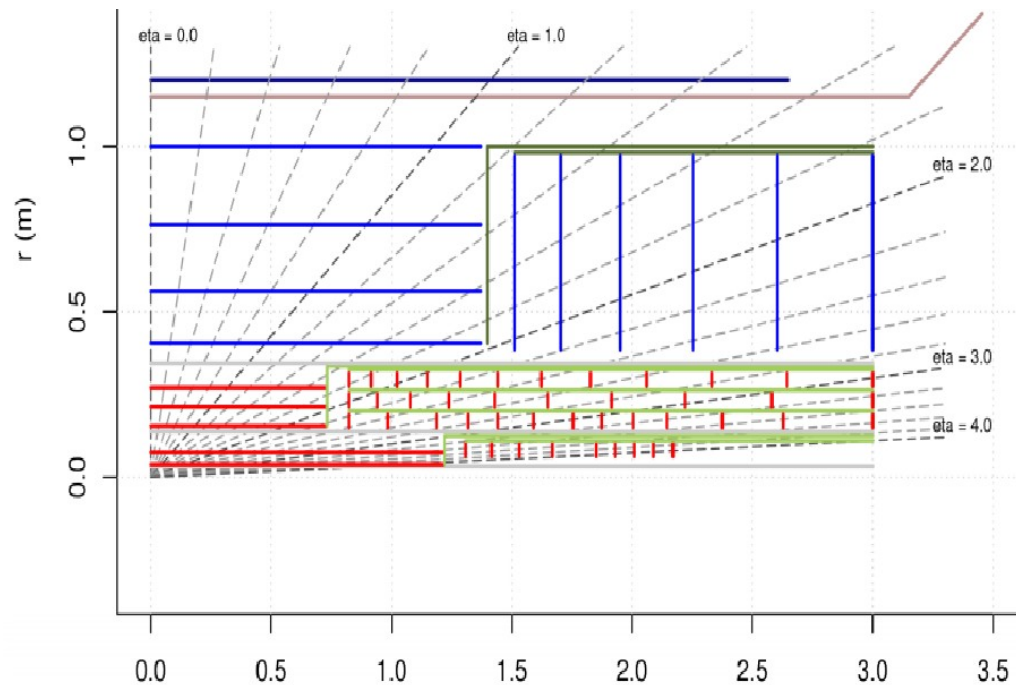


Layout task force: step 2 layout summary.

Fully included 4.0



Extended_4.0



Layout task force: step 1 scope.

Claudia Gemme, Andreas Salzburger

- ✓ Given the timescale the scope of STEP 1 has to be clear and focused.
- ✓ A small experts group has starting ~daily meetings to converge on a working release
 - Rob/Helen, Simon and Noemi, ...

Extended:

- ✓ More realistic tracking studies for the forward region, including comparing 3.2 and 4.0
- ✓ Pattern recognition studies and performance with long clusters, including simplify the forward region for STEP2 layout

Strips:

- ✓ Verify 8mm module gap fix in the barrel works
- ✓ Test strip performance vs Pixel layout input to strip TDR strategy

Late for STEP1 -> then we may have 1.5 for schedule opt.

Include strip petal description and module gap in EC

Inclined:

- ✓ Resolution and pattern recognition studies; quantify the advantage of multiple hits/layers
- ✓ Optimization of the full barrel and forward region for STEP2 layout

Layout task force: last year Timeline proposal.

Claudia Gemme, Andreas Salzburger

✓ STEP 1 layouts

- Tracking and vertex studies
- Input to optimize STEP 2 Layouts

✓ STEP 2 preparation

- **Petals description**
- Optimization of pixel

✓ Other inputs

- Mechanical supports
- Costing
- Trigger
- ...

✓ Workshop mid- end April

- Wrap up and launch of STEP 2 layouts
- These are final layouts, intended for the strip TDR and all the other big studies in 2016!!!

✓ STEP2 layouts

- All CP groups studies
- Physics benchmark channels
- Feedback to LAr

✓ Other inputs -

- Mechanical supports
- Costing
- Trigger
- ...

✓ Workshop Aug/Sep for final wrap-up and Decision

- Wrap up in the TF report → September
- Samples available for ECFA 2016 (~ 3 October)
- Samples available for strip studies (Sep in ITK, Nov in ATLAS)



Layout task force: new Timeline.

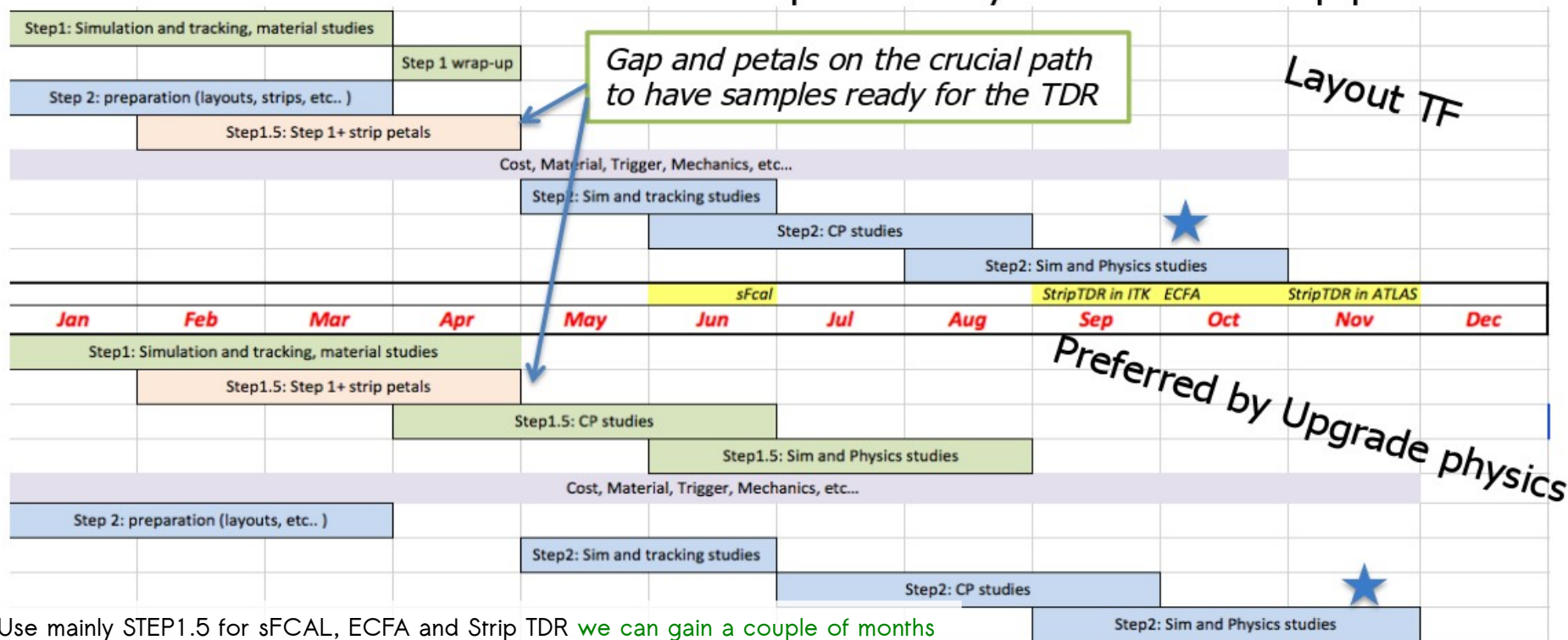
Claudia Gemme, Andreas Salzburger

Timeline

STEP1 three layouts – difference only in innermost Pixel

STEP1.5 two STEP1 layouts at 4.0 + strip petals

STEP2 two optimized layouts at 4.0 + strip petals



✓ Use mainly STEP1.5 for sFCAL, ECFA and Strip TDR we can gain a couple of months

- Strips geometry should not be very involved in STEP1/2 pixel optimization
- Petals description needs to be in!
- Include preliminary results from STEP2 if available

✓ Cons:

- Do twice the work!
- Delay Layout TF conclusion

✓ To be discussed: now, in any case, focus on finalizing STEP1 release

Layout task force: step 1 layout summary.

Claudia Gemme, Andreas Salzburger

Layout	Modules&Layer	Services	Reconstruction
Extended@3.2	positions defined & implemented	implemented, to be cross-checked	private version for long clusters, needs to be integrated
Extended@4	positions defined & implemented	implemented, to be cross-checked	private version for long clusters, needs to be integrated
Inclined@4	positions defined & implemented	use Extended@4 & scale by difference in modules	no studies done yet

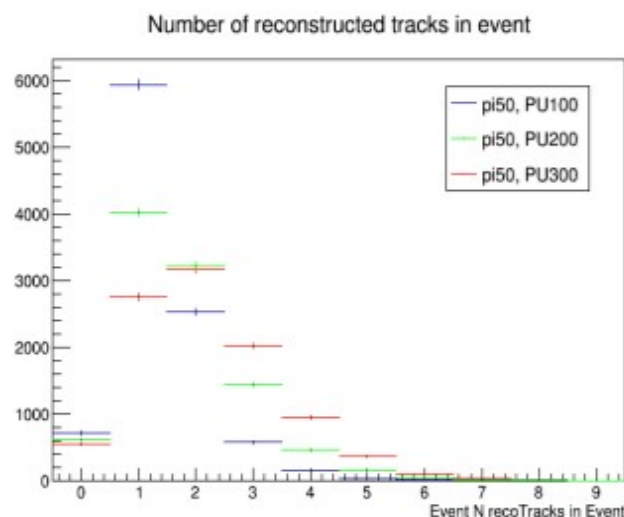
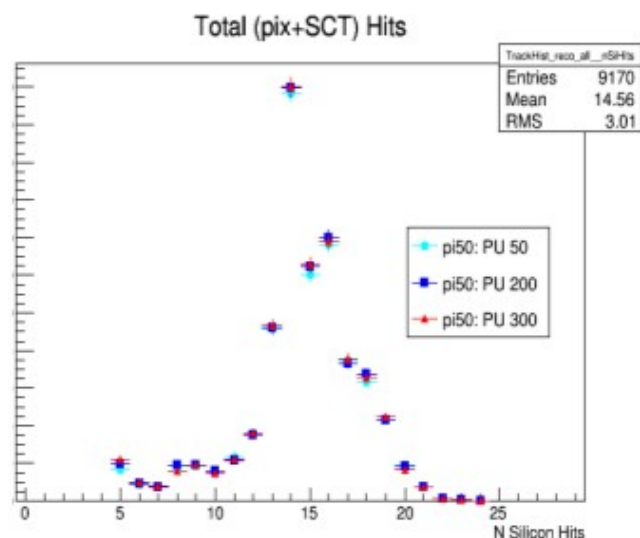
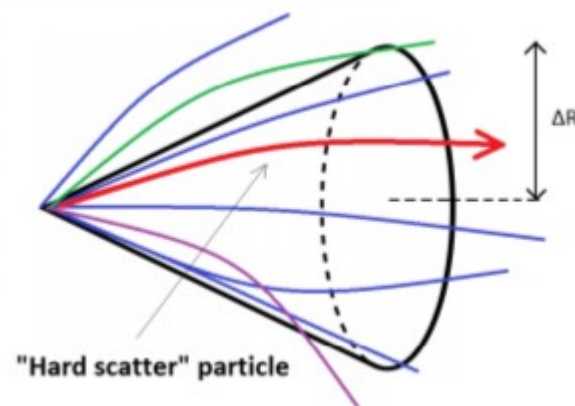
Study of ITk layout optimization:

Federico Massa, Claudia Gemme, Giorgio Chiarelli

- Currently working within Lol layout —► samples with new layouts not yet available!
- Study the dependence of the performance on the parameters used for simulation /reconstruction changing the $\langle\mu\rangle$.

Method of pileup reconstruction

- Generate hard scatter track
- Produce $\langle\mu\rangle$ (in-time) pileup tracks
- Simulated only tracks within a fixed $\Delta R = 0.1$ cone around the hard scatter track



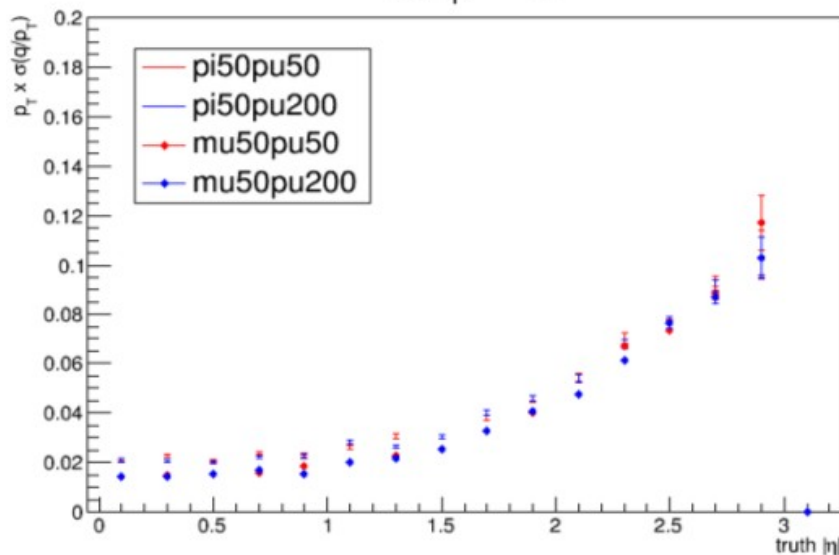
Used Sample

- 10000 main tracks: μ^- / π^+
- $\langle\mu\rangle = 50, 100, 140, 200, 300$
- Flat in $-3 \leq \eta \leq 3$,
- Flat in ϕ
- fixed in $p_T = 15, 50, 100 \text{ GeV}/c$

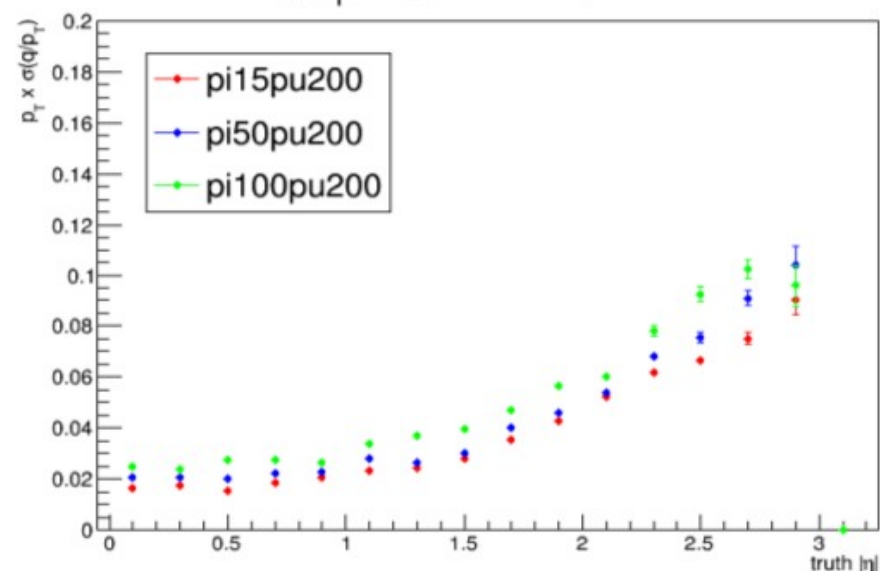
Study of ITk layout optimization: Resolution and Efficiency(Truth Matched)

Federico Massa, Claudia Gemme, Giorgio Chiarelli

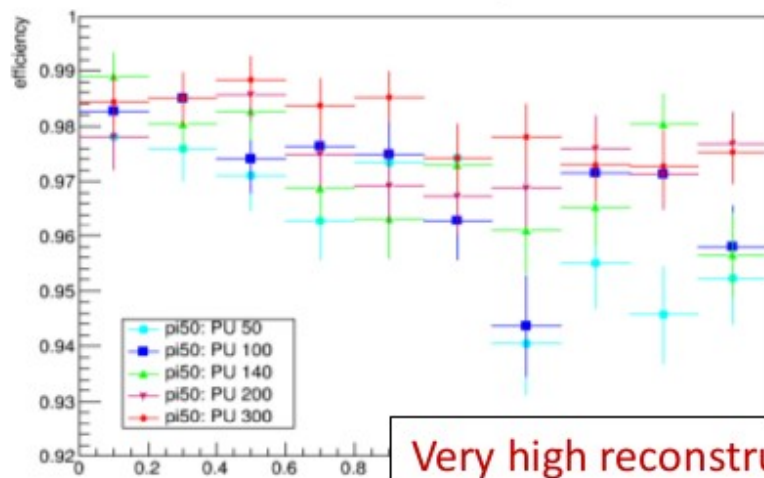
$\sigma(q/p_T)$ vs $|\eta|$



$\sigma(q/p_T)$ vs $|\eta|$ at fixed $\langle \mu \rangle = 200$



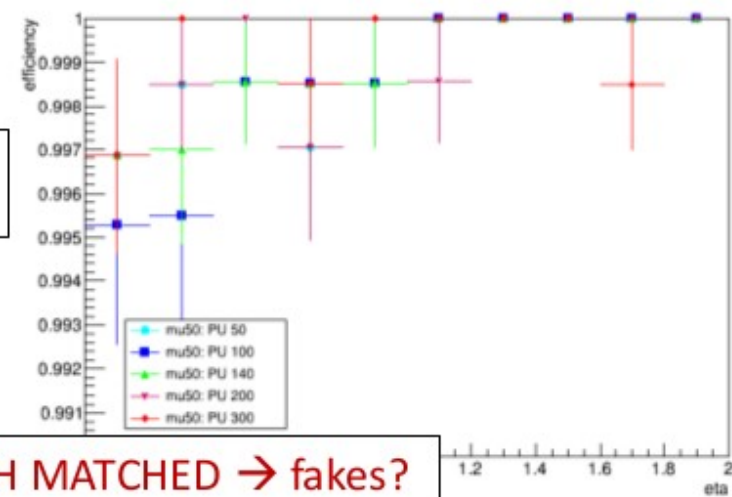
Track reco efficiency vs eta



$$\epsilon(\eta) = \frac{\text{Track BinContent}(\eta)}{\text{Truth BinContent}(\eta)}$$

Very high reconstruction efficiency – but TRUTH MATCHED → fakes?

Track reco efficiency vs eta



Study of ITk layout optimization: Number of hits and fakes (π samples)

Federico Massa, Claudia Gemme, Giorgio Chiarelli

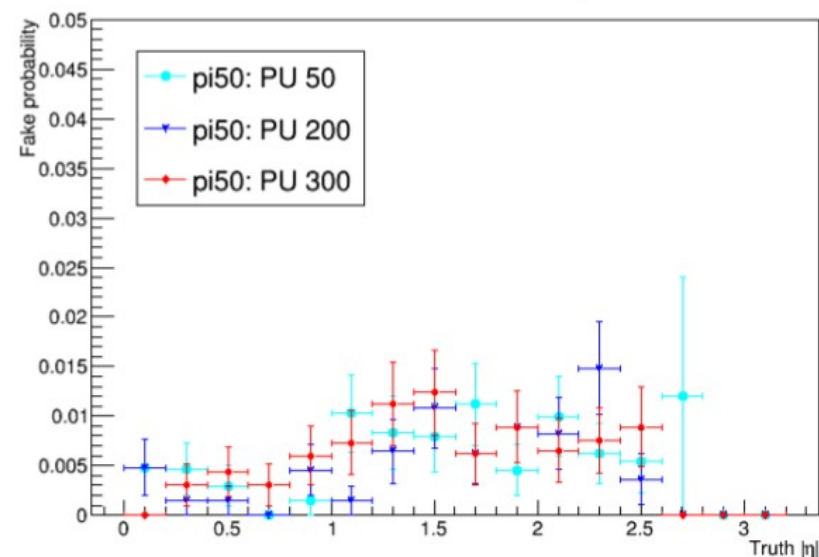
Fake definition:

track.TruthMatchProbability < 0.7

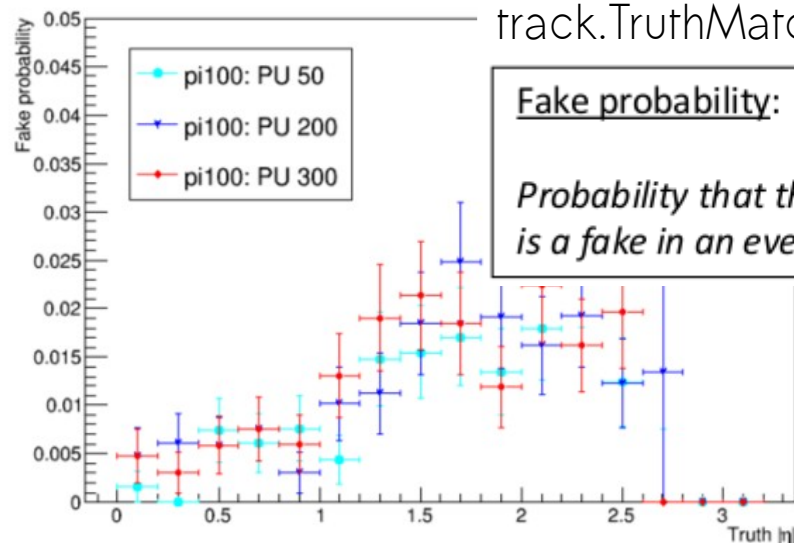
Fake probability:

Probability that the «hard scatter» particle is a fake in an event

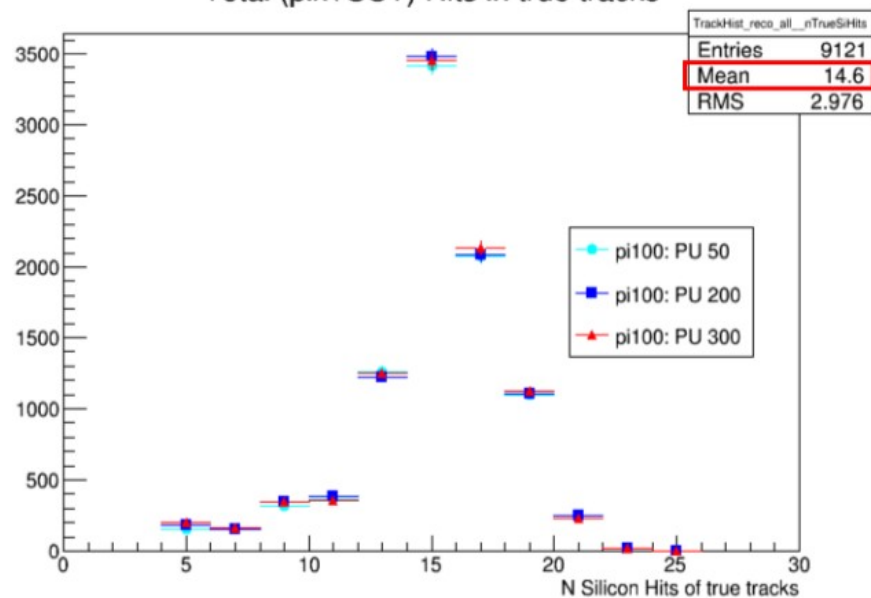
Fake Gun Probability



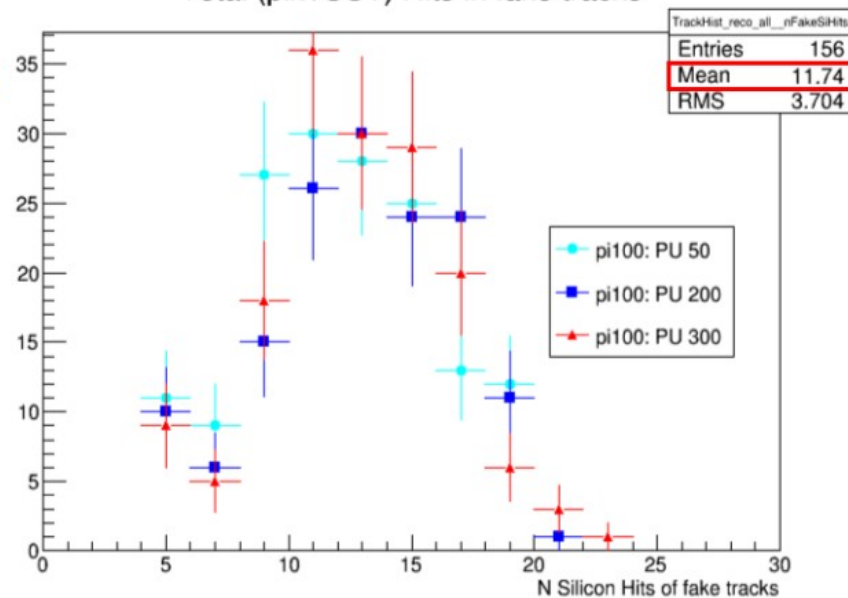
Fake Gun Pr



Total (pix+SCT) Hits in true tracks



Total (pix+SCT) Hits in fake tracks

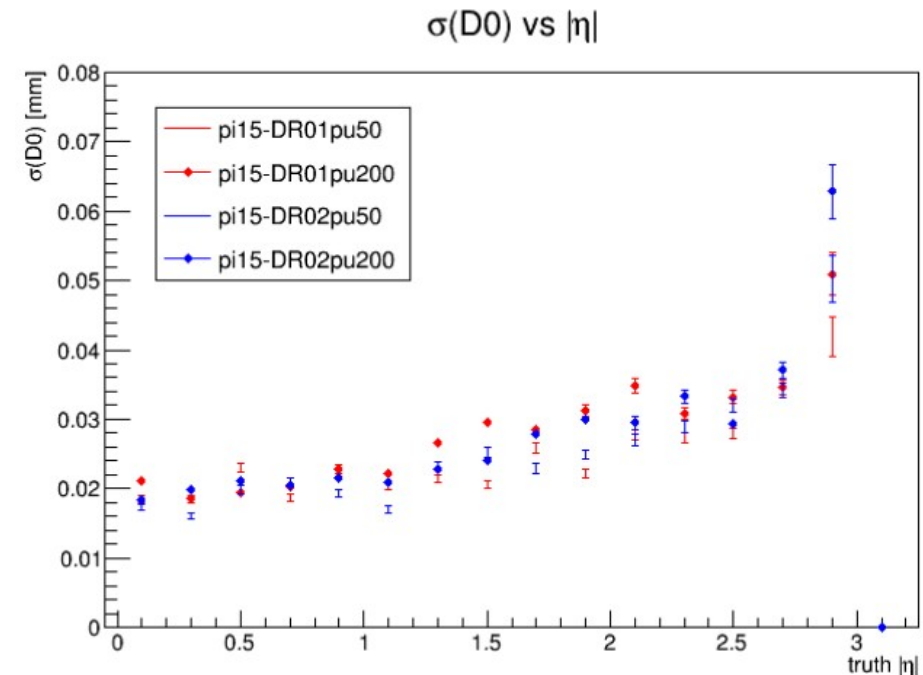
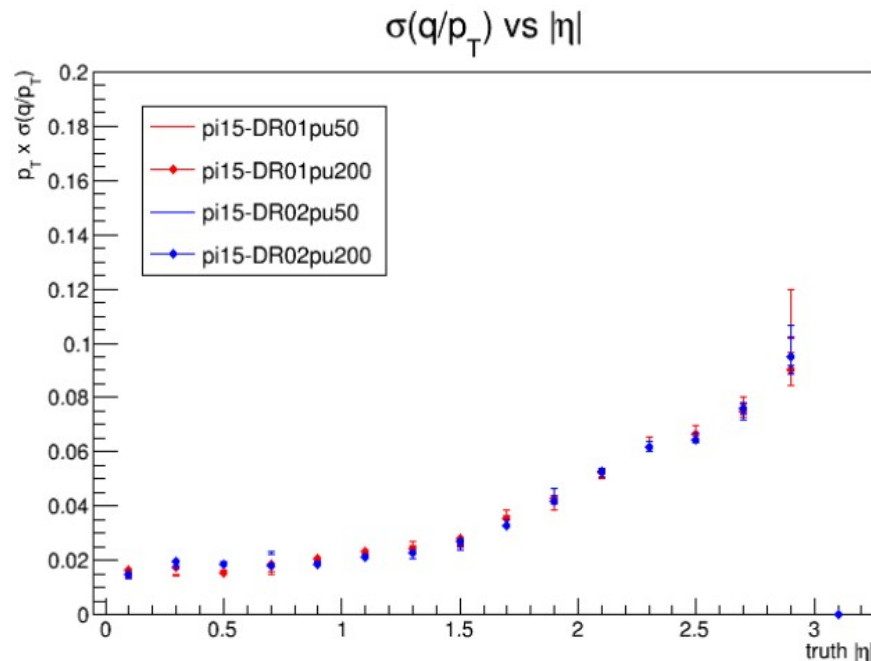


Study of ITk layout optimization: update on study of cone ΔR (Resolution)

Federico Massa, Claudia Gemme, Giorgio Chiarelli

- Generated new π^+ , μ^- samples with larger $\Delta R = 0.1 \rightarrow 0.2$, fixed $p_T = 15$ GeV/c
- Updated fake definition
 - Before: track with TruthMatchingProbability < 0.7 (not optimized for Itk)
 - Now :track-truth $\Delta R < 0.02$

Resolution: comparison between $\Delta R = 0.1$ and $\Delta R = 0.2$



Resolution and efficiency essentially unchanged (slight difference in D0)

Study of ITk layout optimization: update on study of cone ΔR (fakes)

Federico Massa, Claudia Gemme, Giorgio Chiarelli

Integrated fake Probability (%) ($ \eta > 1.2$)		
	$\langle \mu \rangle = 140$	$\langle \mu \rangle = 200$
DR 0.1	$0.56 \pm 0.05\%$	$0.59 \pm 0.05\%$
DR 0.2	$0.62 \pm 0.05\%$	$0.63 \pm 0.05\%$

Generate with a sample of 50000 events to reduce the statistical fluctuations

The fake probability slightly increase changing ΔR

For more details link at presentation at ITK Sim. and Perf. Group :

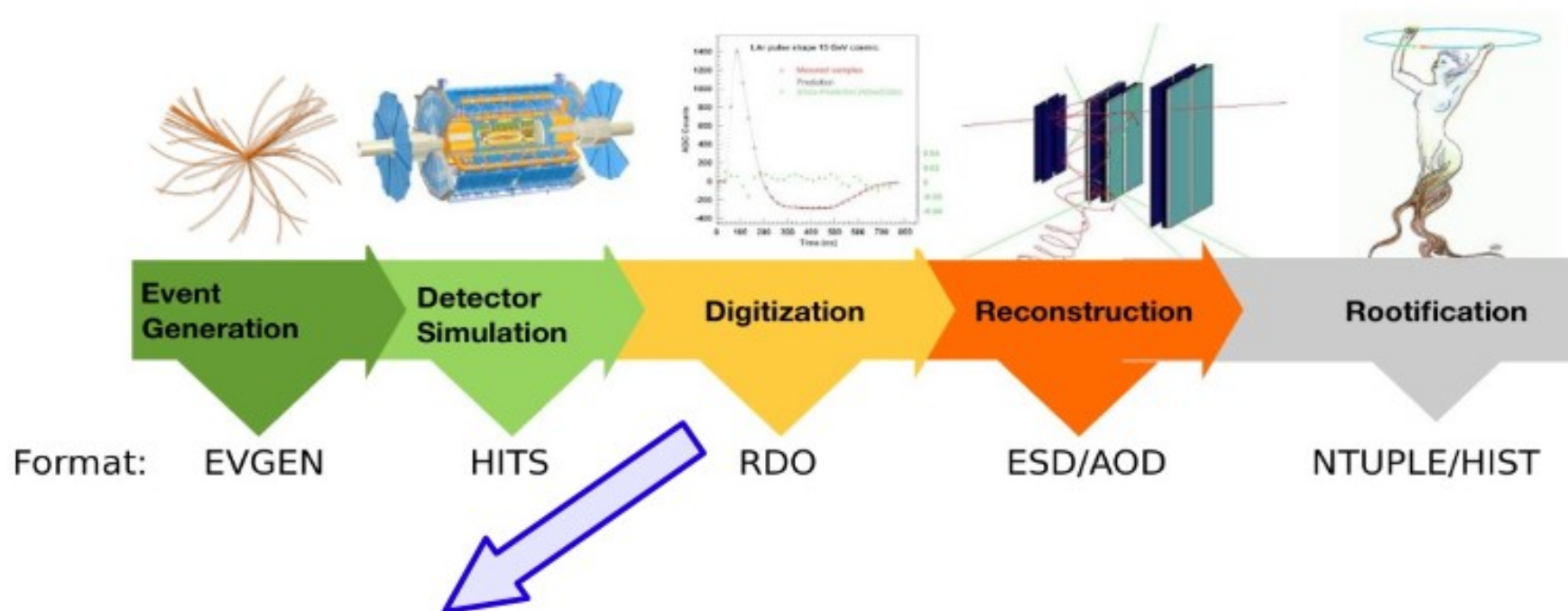
<https://indico.cern.ch/event/462611/>

<https://indico.cern.ch/event/464857/>

What's next:

- Generate other particles (b, e, τ) and use physics channel.
- While waiting for new geometry: study of performances vs pixel layers position in r.
- Switch on/off layers.

Fast pixel digitization algorithm



The fast pixel digitization is a geometrical digitization that takes as input information on hit position but not on amount of deposited charge.

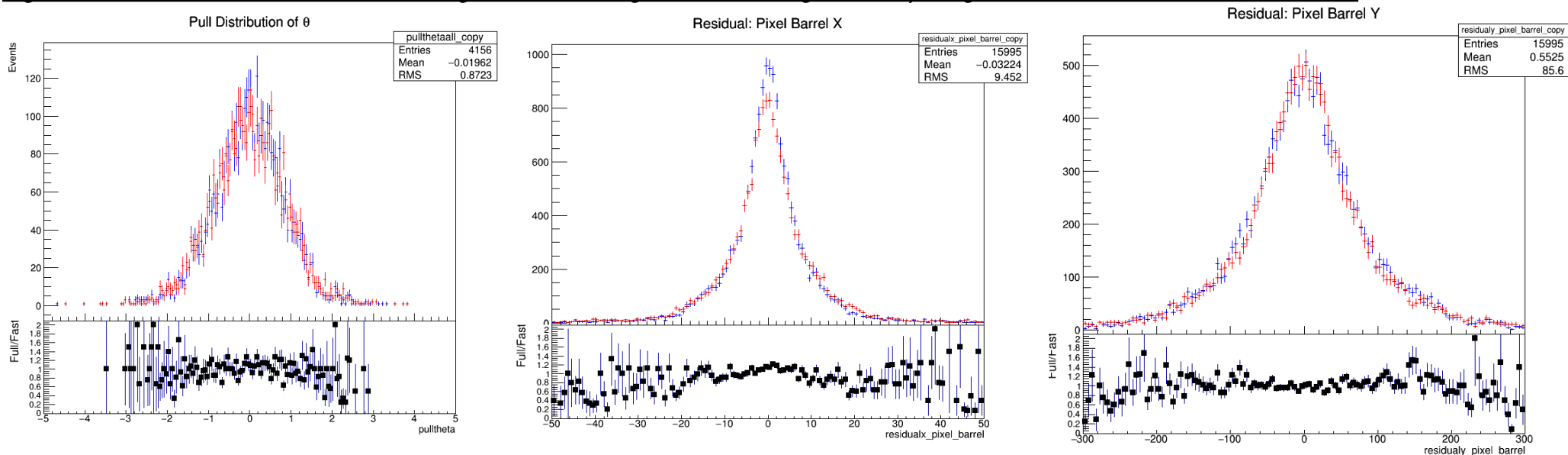
Allows to change pixel pitch directly during digitization without rerun GEANT4

Converts path length in each pixel in deposited charge (ToT) and directly creates clusters during digitization following the HIT direction.

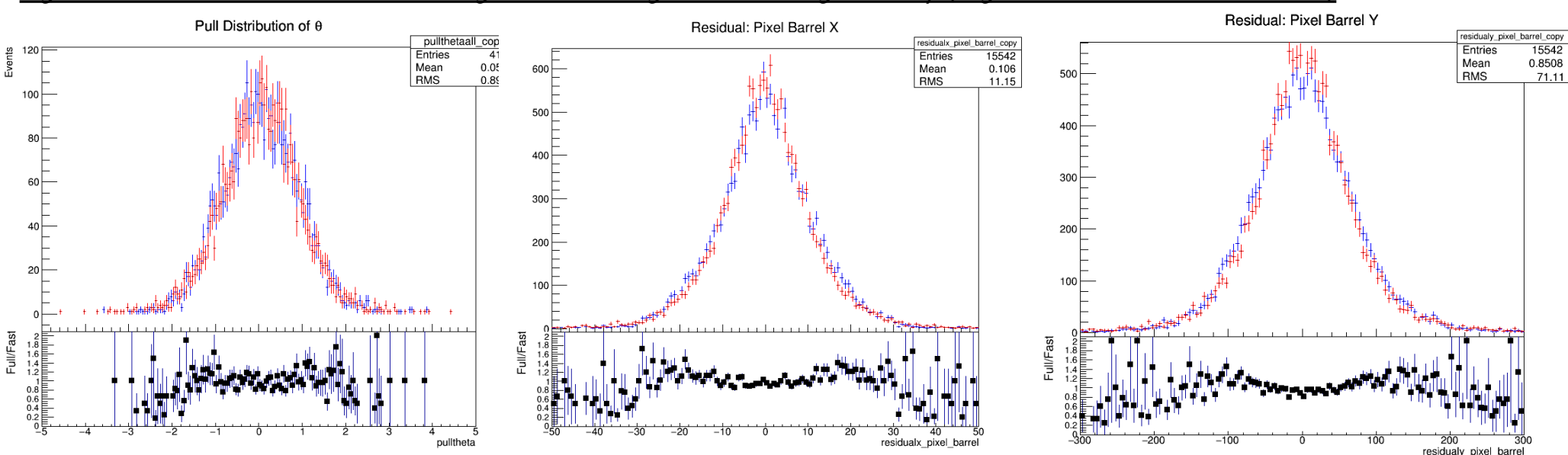
Fast pixel digitization algorithm: performance compared to standard digi.

— Full Digi
— Fast Digi

Agreement between fast and full digitization using the ATLAS geometry (tag: ATLAS-R2-2015-03-01-00)



Agreement between fast and full digitization using the ATLAS geometry (tag: ATLAS-P2-ITK-01-00-00)



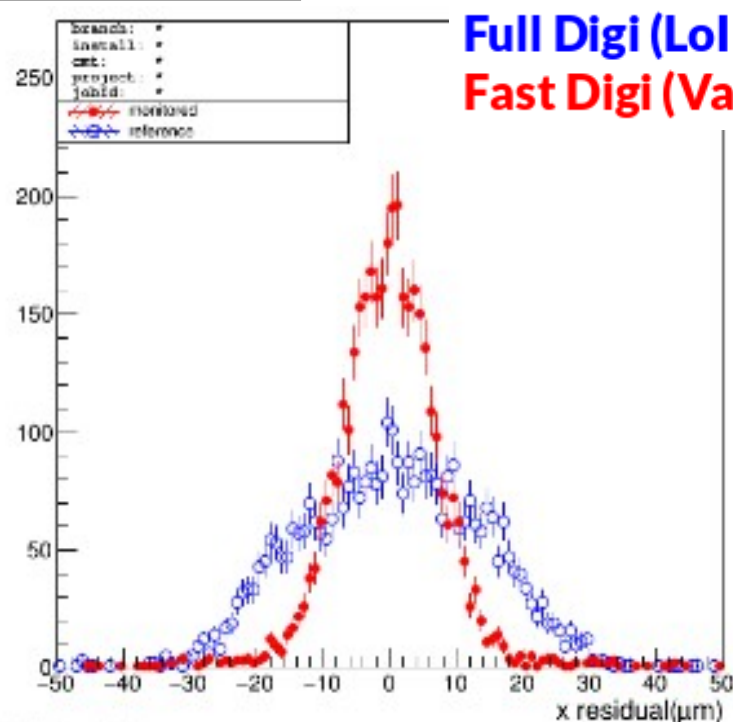
Input File: 5000 events of single muon with p_T of 100 GeV .

Fast pixel digitization algorithm: change pitch size.

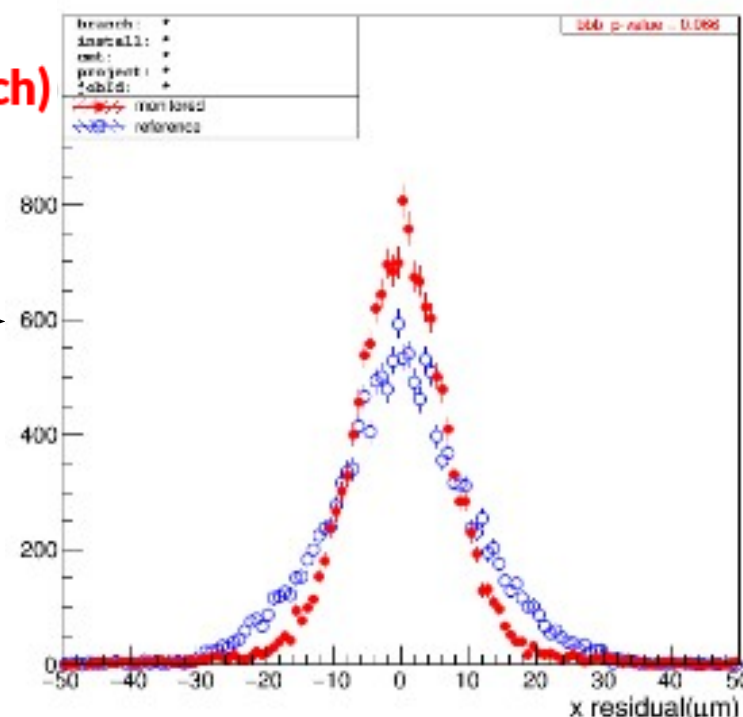
The pitch of the pixel can be changed quite easily:

Overwrite the information on pitch dimension for the selected layer read from the database, and change accordingly the information on the Id dictionary used to build the pixel Id. Keep constant the active area of the module (change accordingly the chip dimension, empty rows/column, number of chip!!)

Example: Using Lol geometry (HIT file generated using full sim) try to change pitchX of outermost layer from 0.05 mm to 0.025 mm



Effect on residual along x (phi in global coordiante) in layer 2



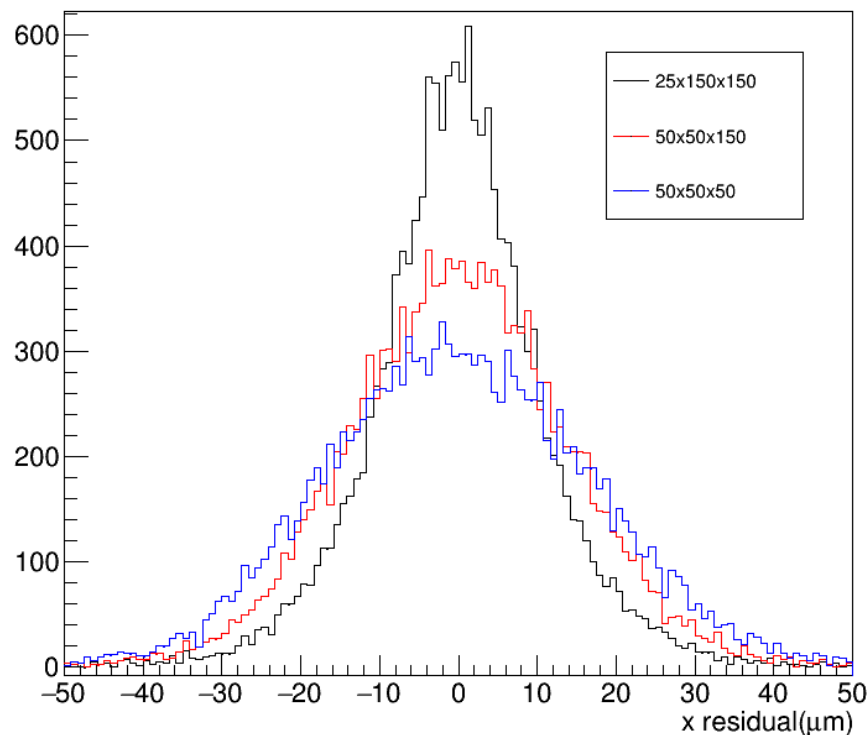
Effect on residual along x (phi in global coordiante)

Fast pixel digitization algorithm: started collaboration with HV_CMOS-I

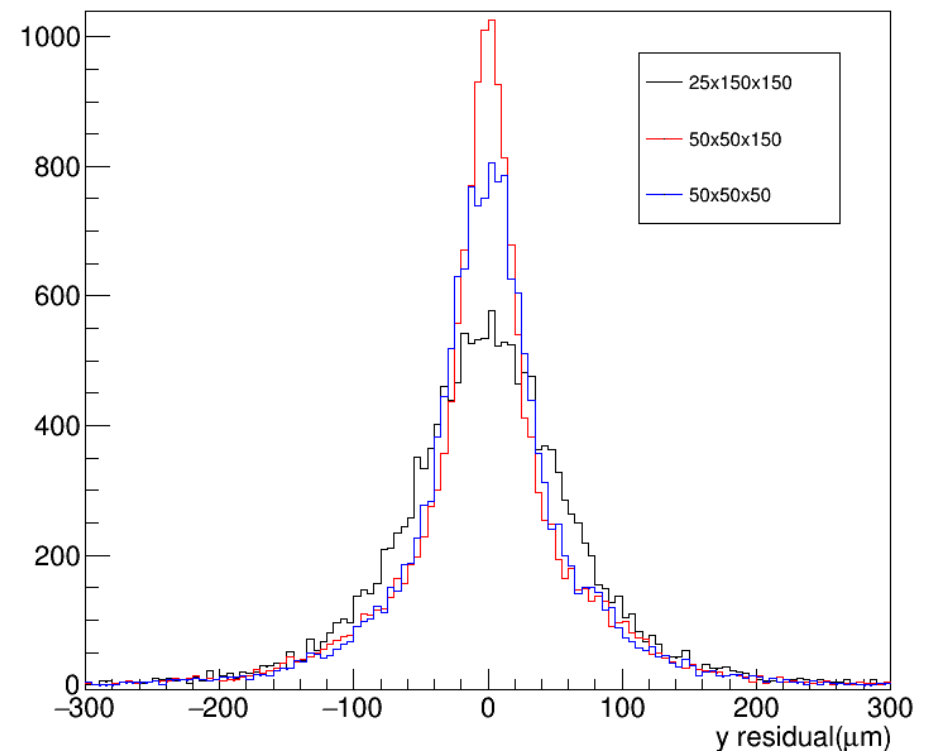
Federica Fabbri, Carla Sbarra

- Started in December activity in HV_CMOS group to simulate the performance of the pixel detector changing the dimensions accordingly to the new sensors.
- Separate the effect of the different technology and different dimension wrt the pixel in the Lol.
- At the moment changed pixel dimension in Lol geometry in the two innermost layer (pitchX x pitchY x thickness):

Residual: Pixel Barrel X



Residual: Pixel Barrel Y



Fast pixel digitization algorithm: status and next steps.

- The algorithm will be used in fast simulation chain and soon will start physics validation.
- The Fast pixel digitization tool can be used for upgrade and physics studies for pixel geometry optimization, using various sample with variable p_T and $t\bar{t}$ with or without pileup.
- Change the thickness of the pixel detector give some problem in passing geometry at the reconstruction step and in evaluating the effect of the magnetic field. (Working on this in the HV_CMOS collaboration)

What's next?

- Working with Noemi Calace and Andreas Salzburger to have a new version of the code that allow more flexibility and decouple the geometry part (evaluate path in each pixel) from cluster formation.
- Improve the capability of the tool for upgrade study.

More details:

- HV_CMOS: https://indico.cern.ch/event/490508/contribution/2/attachments/1219064/1781289/HVR_CCPD_simu_1.pdf
- HV_CMOS: <https://indico.cern.ch/event/490508/>
- ITK Sim & Perf: <https://indico.cern.ch/event/464856/contribution/1/attachments/1198389/1742681/2DecPres.pdf>

