CGEM ASIC Details

Chongyang Leng

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BESIII CGEM FEE/DAQ/Trigger Workshop

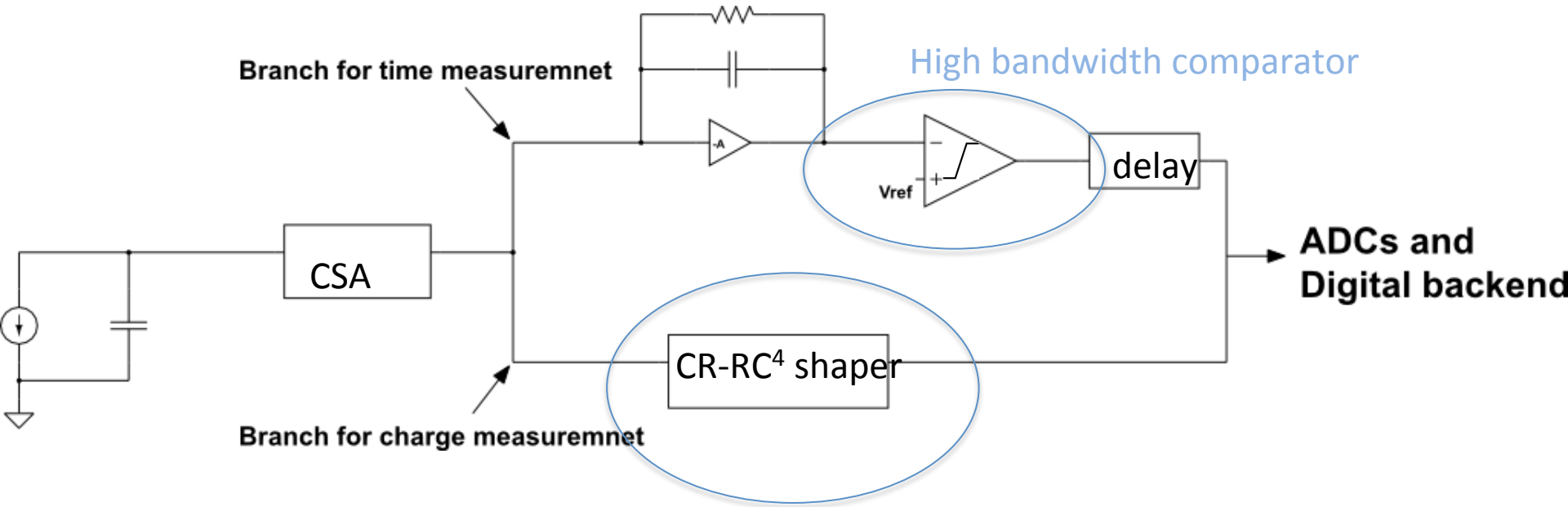
Outline

- Design pros of the Frontend ASIC
- Structure of the Frontend ASIC
- Charge measurement
- Time measurement
- Layout of the chip and post simulations

Front-end ASIC

- **Sensor parameters**
  - **Input charge : 1fC to 50 fC**
  - **Sensor capacitance : up to 100pF**
  - **Signal width : 50 ns to 100 ns**
- **ASIC Requirements**
  - **Data Rate : 60KHz (with safety factor of 4)**
  - **Power consumption per channel : < 10mW**
  - **Time jitter : < 5ns**
  - **ENC noise : < 1000e**

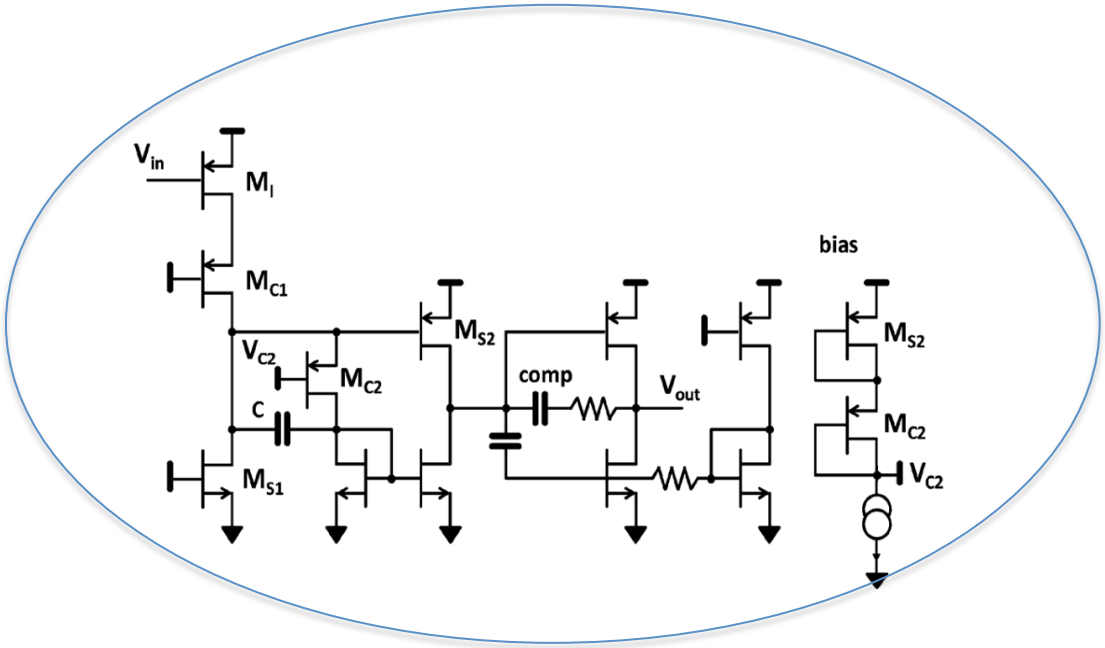
Channel Structure



CR-RC^4 shapers with conjugated poles

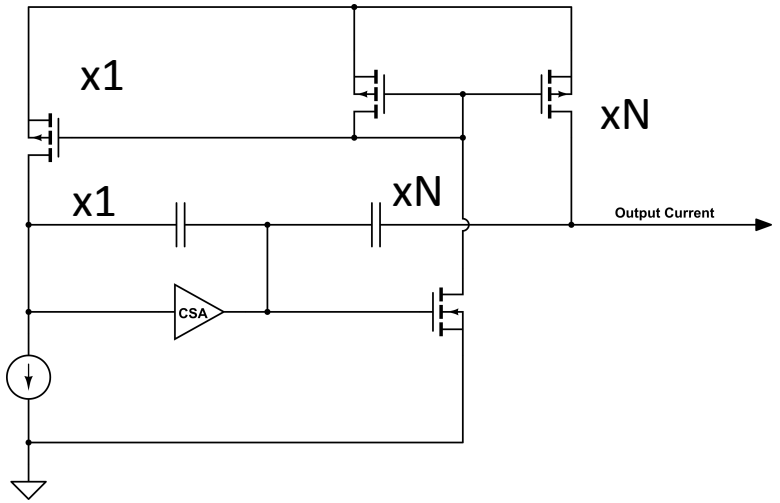
Preamplifier Implementation

A low noise charge sensitive amplifier strategy



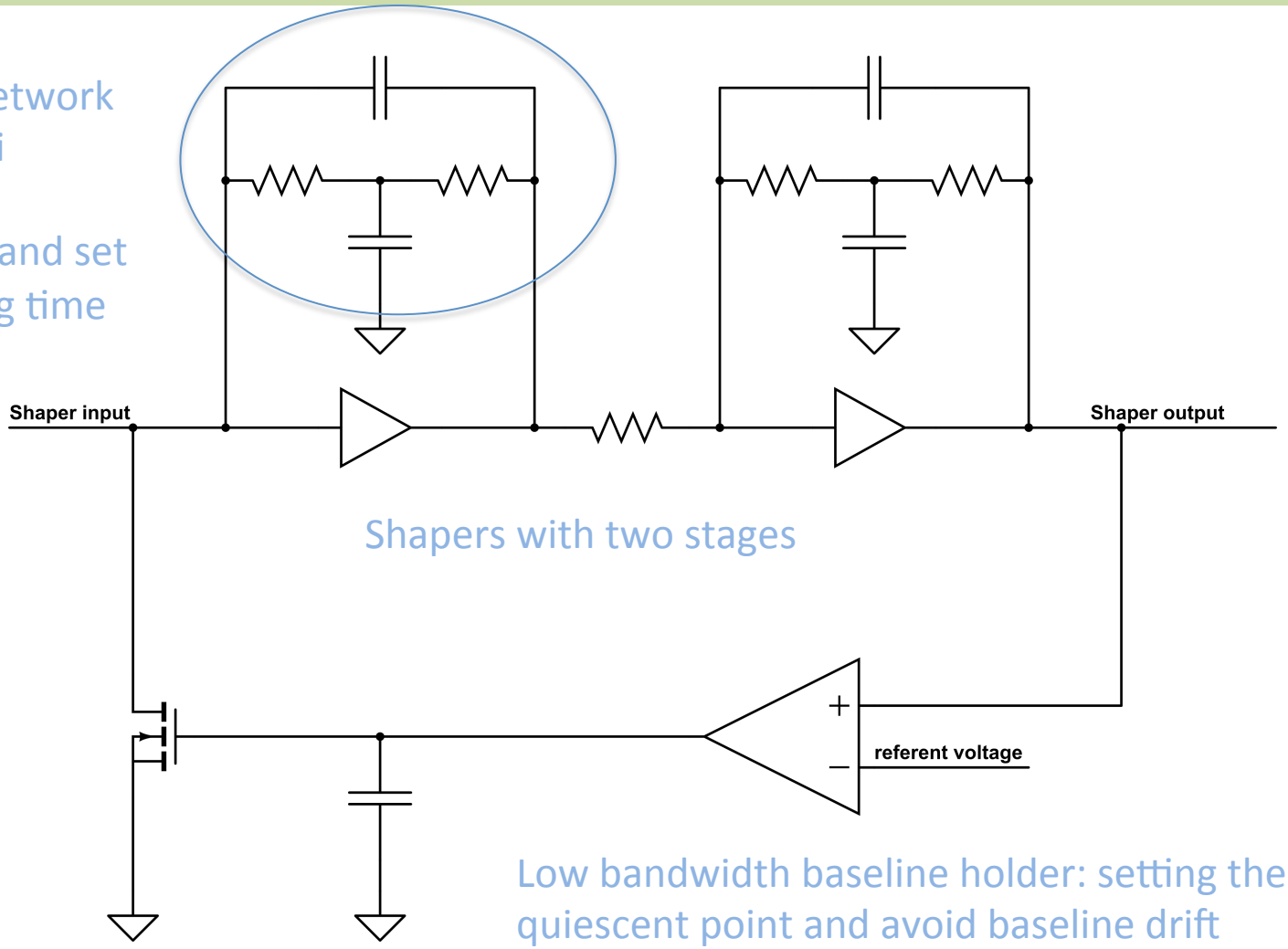
Charge Sensitive Amplifier

Current mode feedback structure, to get precise duplicated input signals for both branches



Charge measurement

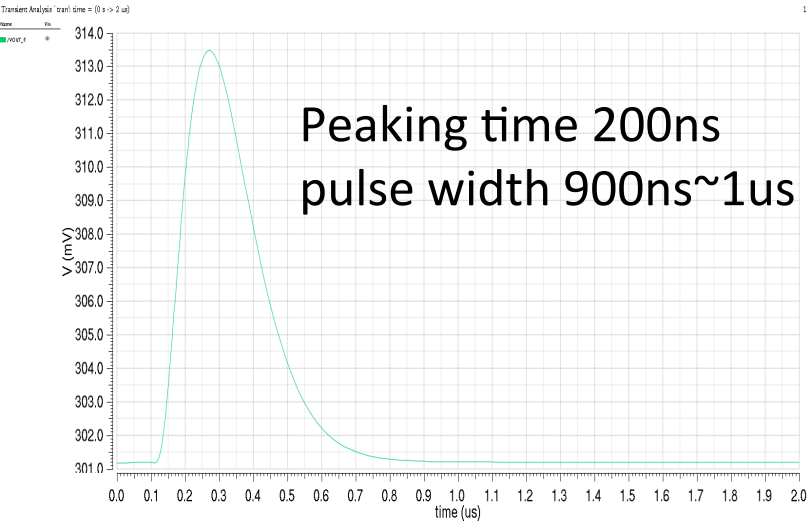
T-bridge network to get semi Gaussian waveform and set the peaking time to ~ 200ns

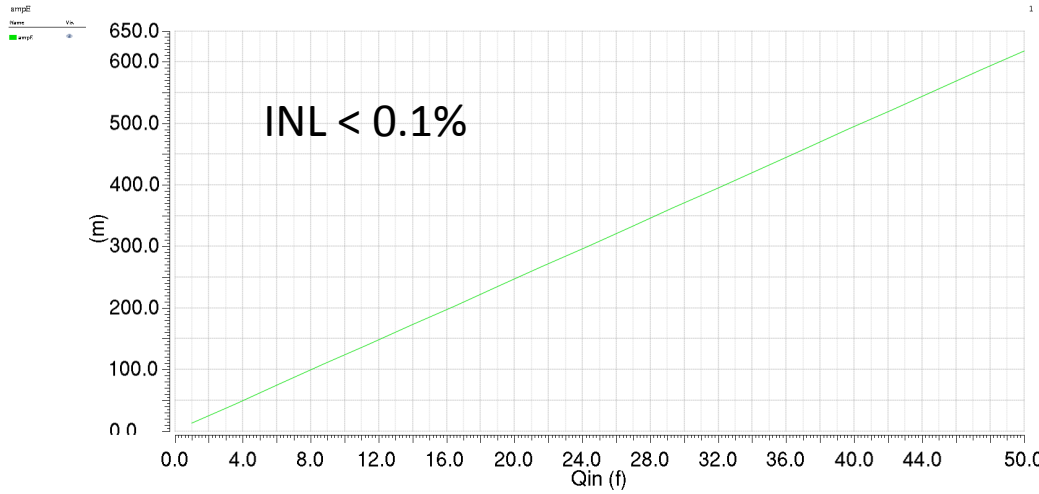


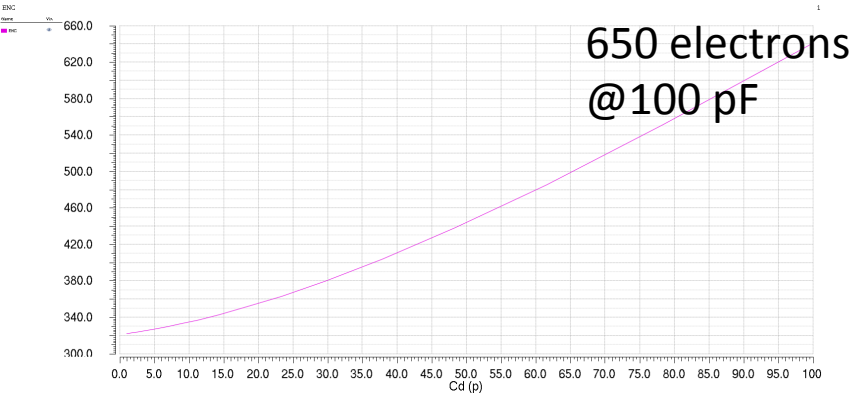
Shapers with two stages

Low bandwidth baseline holder: setting the quiescent point and avoid baseline drift

Performance and Results

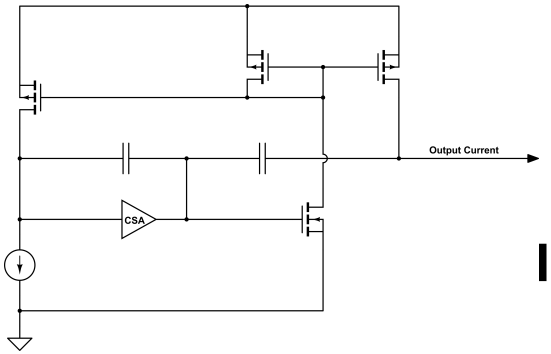


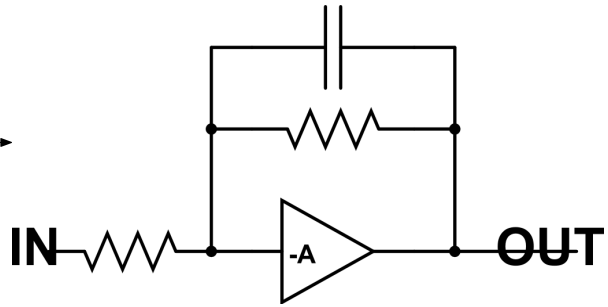


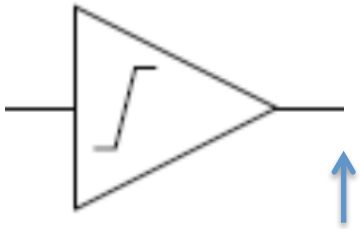


- Detector capacitance up to 100pF
- ENC: <700 e @peaking time =200ns,
- Power consumption per channel ≈ 5mW
- Full signal pulse width < 1us
- Non-linearity = 0.08% (1fC to 50fC)
- Noise ratio ≈ 3.6 e/pF
- Gain ≈ 12mV/fC

Timing Jitter Measurement



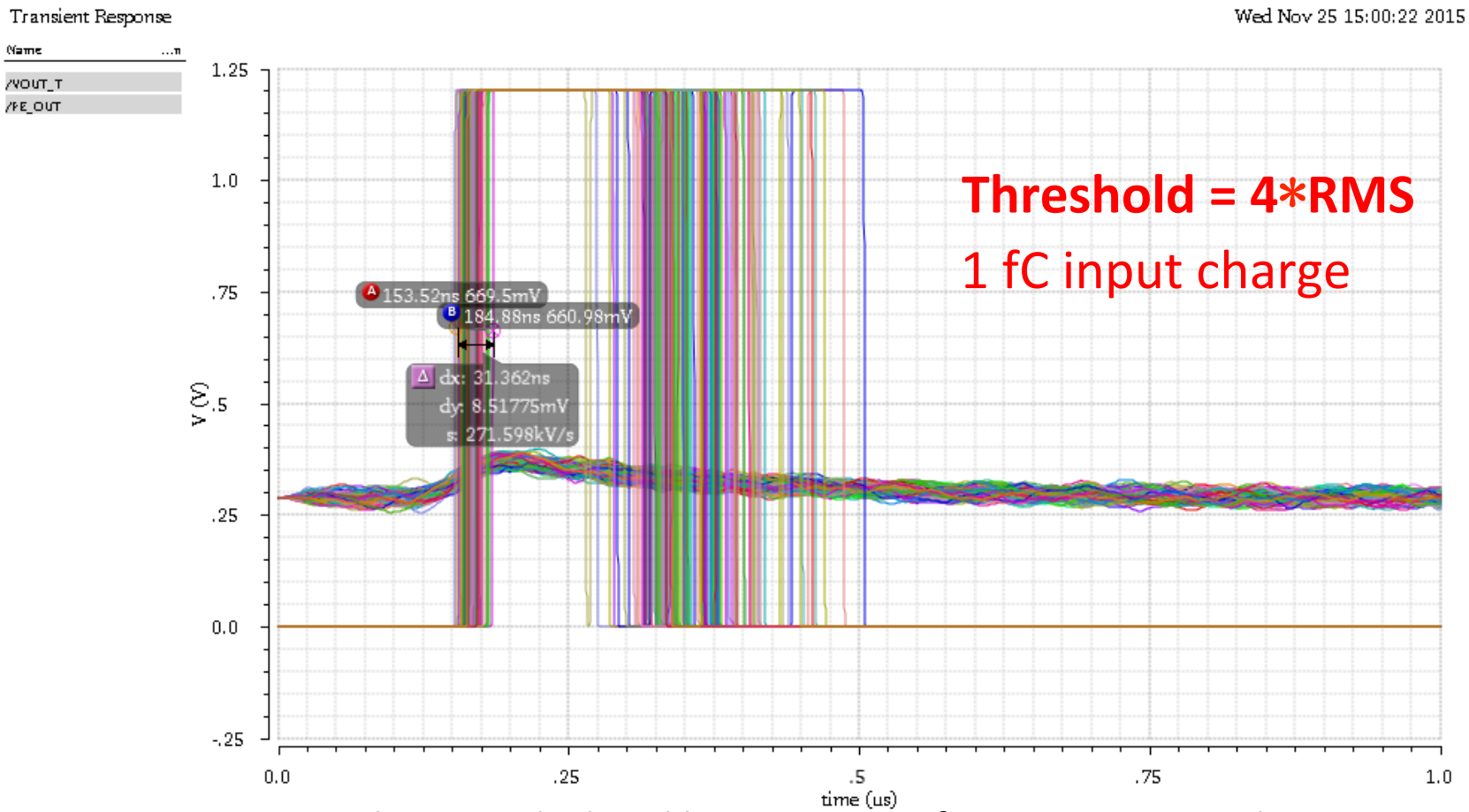




Discriminator Output

Observing the output of the discriminator in the transient noise simulation (100 runs), we can get the time jitter by the plot or by empirical formula.

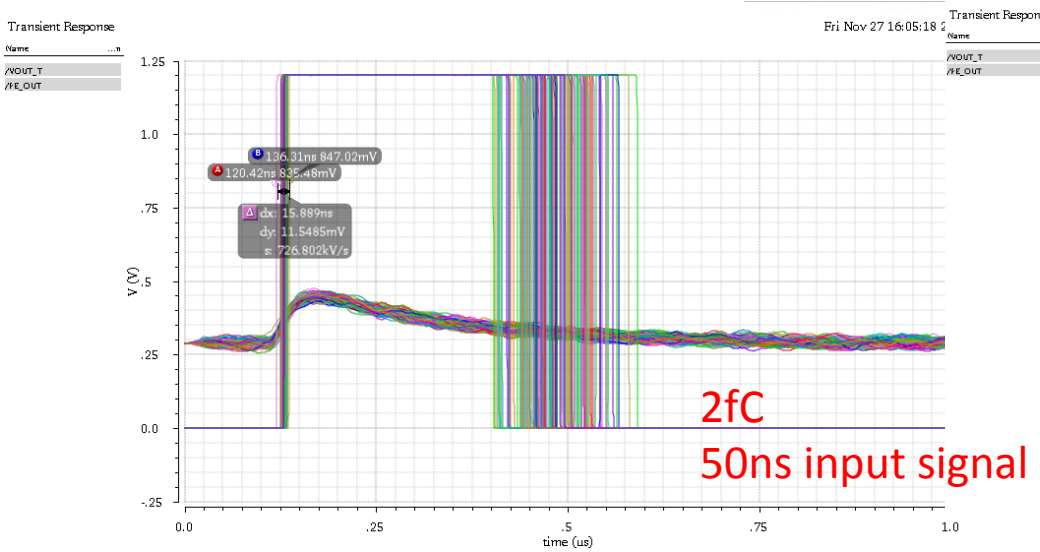
Timing Jitter Measurement

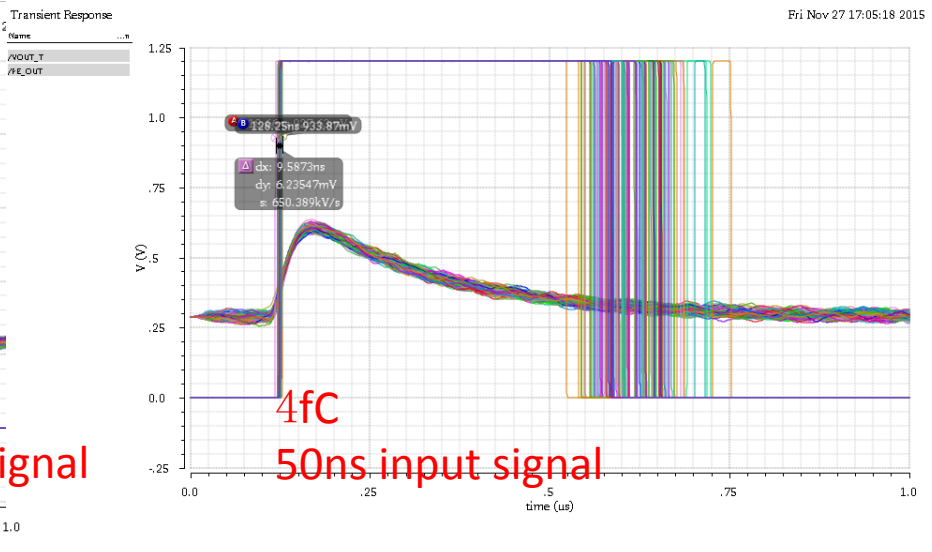


Jitter Simulation: Calculated by equation refers to Maximum slope

⇒ jitter =rmsNoise/slope≈ 5.5ns

⇒ From output of discriminator: jitter = dx/6 = 5.2ns

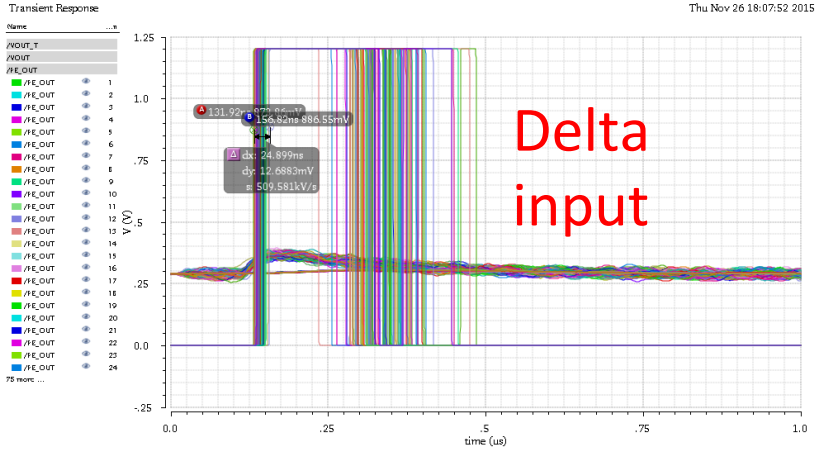




Input= 2fC jitter= 15.8ns/6 = 2.63 ns

Input= 4fC jitter=9.6ns/6= 1.6ns

Timing jitter will be exactly the reciprocal of input charge. If we will not always have input signal as small as 1fC, the jitter performance would be better.

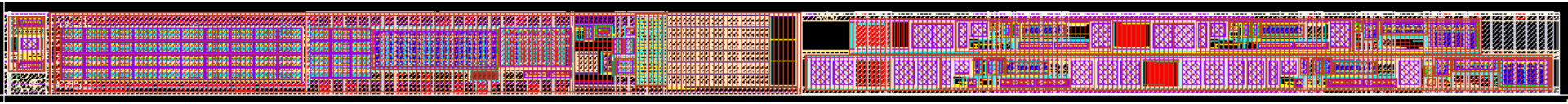


Concerning the FEE itself(delta input signal) Peaking time = 65 ns

jitter = 24.8ns/6 = 4.2ns

Faster output also leads to less time jitter.

Layout

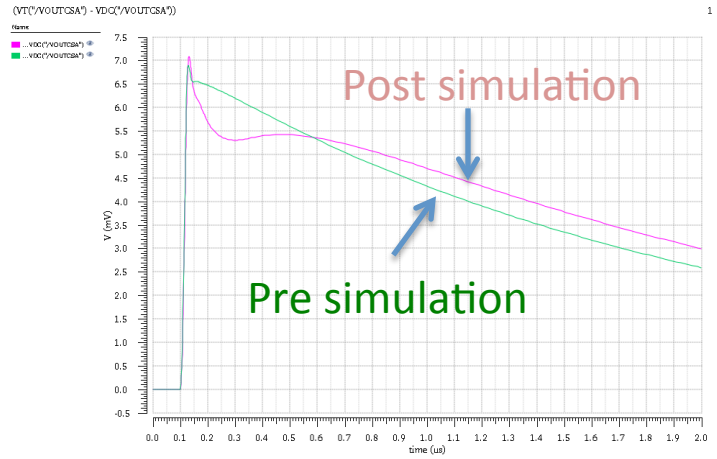


Layout of one single channel. Size 72um* 1350um.

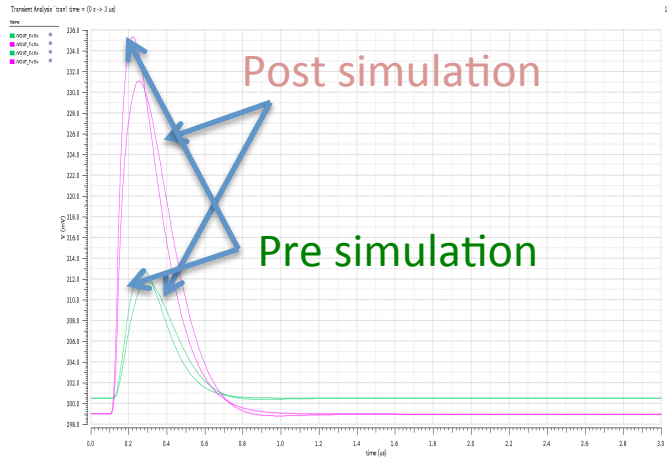
Parasitic problems in post-layout simulations:

- Parasitic resistance
  -> Noise increased from the input parasitic resistance
- Parasitic capacitance
  -> introducing small feedback capacitors in the loop and then oscillation in system
- Resistance and inductance introduced by the power grid
  -> Amplitude deterioration
- Crosstalk between neighboring channels

Post simulations



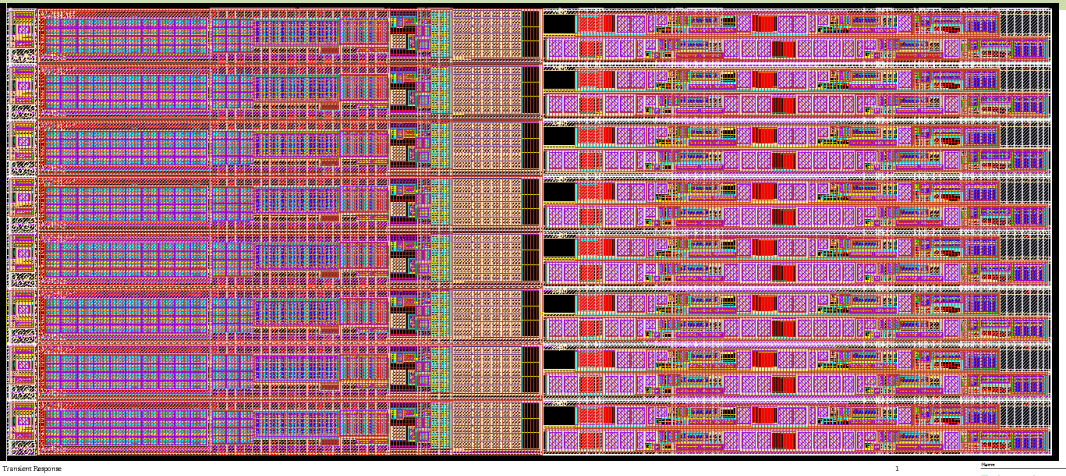
Output of the Charge sensitive amplifier



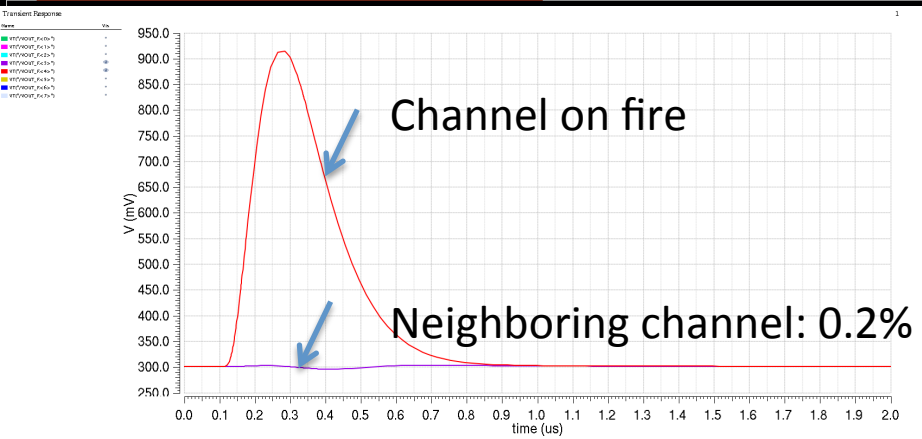
Output of the shaper(Charge and time branch)

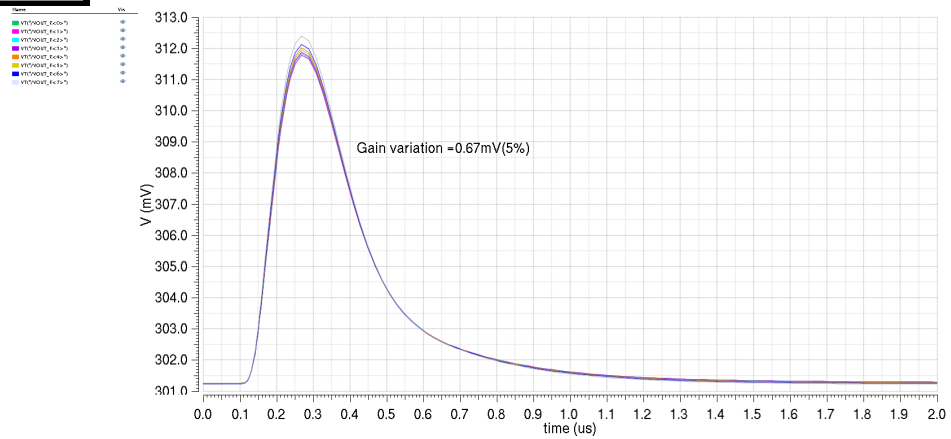
	Pre-Simulation	Post-Simulation
ENC noise/e	640	698
Timing jitter/ns	5.5	6.0
Output amplitude/ mV	12.3	11.0
Pulse width/ns	830	910
Linearity	< 0.1%	<0.1%

Post simulations



Simulations with 8 channels





Crosstalk results. Simulated with 50 fC input charge and 2nH inductor(Considering the power bonding)

Gain Variation: about 5% between channels. This will be better after power grid applied.

Summarys

- 64 channel layout ready
- Layout of bias cells undertaking
- Post simulation results : ENC noise, time jitter 10% larger than pre simulation. Output Gain 10% decreased. Power consumption , output width(data rate) and linearity not effected much.
- Small modification on going before integrated with back-end

THANK YOU!