TOFPET ASIC

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on behalf of the TOFPET design team

Workshop on CGEM FEE, DAQ and Trigger for BESIII experiment

Torino, 13.04.16

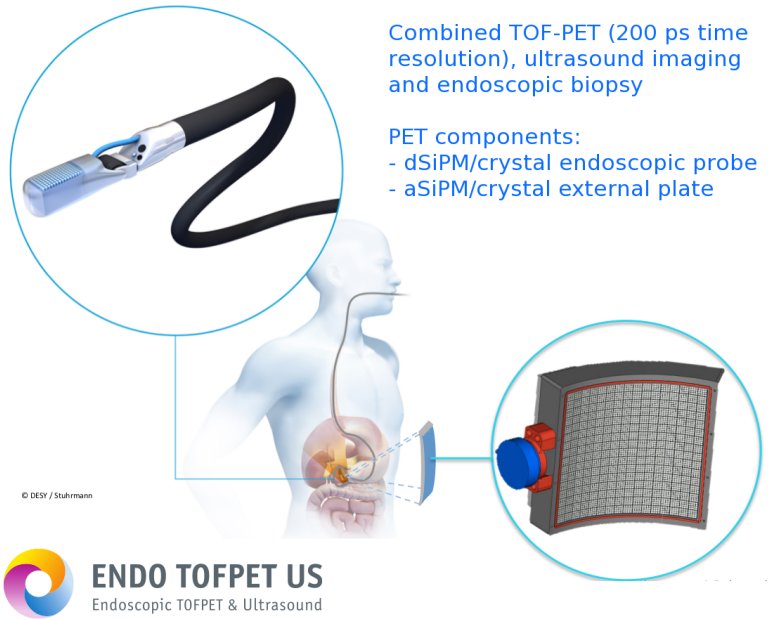
1. IC Design forTime-of-Flight PET
   - TOFPET in a nutshell
   - TOFPET summary of results
   - TOFPET specs and channel overview
2. TOFPET2
   - TOFPET2 specs and channel overview
3. TOFPET2_IP for BESIII
   - Improvements for BESIII CGEM readout ASIC

Outline

TOFPET: Design of a readout ASIC for Time of Flight applications

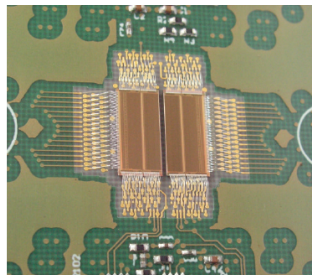
FP7 **EndoTOFPET-US**: combined (Time-of-Flight) PET, ultrasound imaging and endoscopic biopsy

- Need to extract of TOF information to enable endoscopic imaging (enhance SNR)
- FE electronics with very good timing, low-noise, low-power, high density
- External PET plate: crystals, SiPMs and custom ICs:

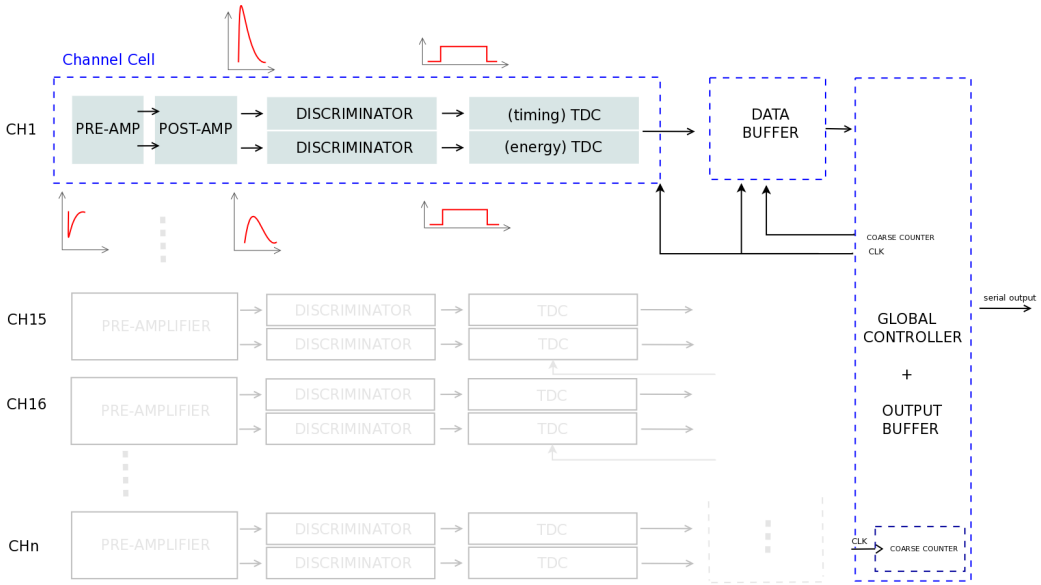


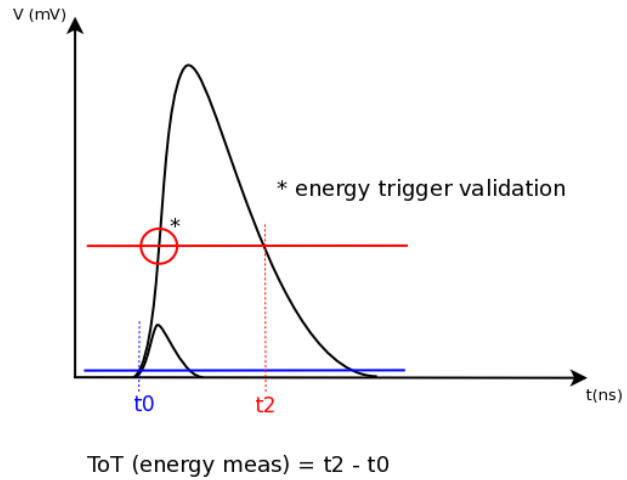
The TOFPET chip in a nutshell:

- 64-channel ASIC for high-capacitance photodetectors (350 pF)
- amplification, discrimination circuitry and time-to-digital conversion
- 25 ps r.m.s. intrinsic resolution
- fully digital output, data rate up to 640 Mb/s
- optimized for low-power (less than 10 mW p/channel) and high-rate (160 kHz/channel)



TOFPET: overview and architecture



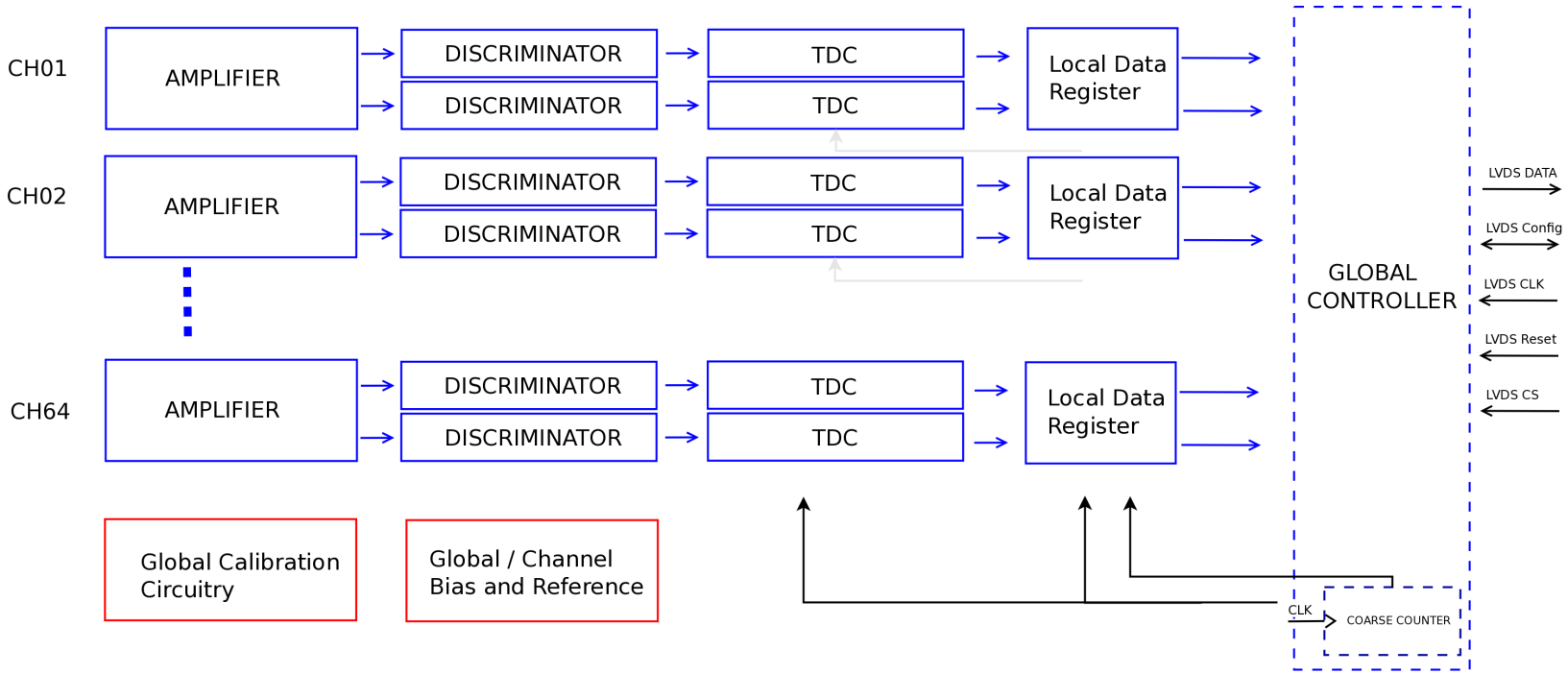


- gm-boosted common-gate input stage
- SiPM HV bias adjustment
- Charge measured with Time-over-threshold
- Time and charge measurements with independent TDCs
- **Low-power TDC** with analogue interpolation
- Trigger level **0.5 p.e.** with SNR = 25 dB
- LVDS 10 MHz SPI configuration link and dark count measure
- LVDS up to 640 Mbps data output interface; 8B/10B encoding

✓ Patent WO/2014/077717
"Reading device and method for measuring energy and flight time using silicon photomultipliers"

Overview of the chip architecture

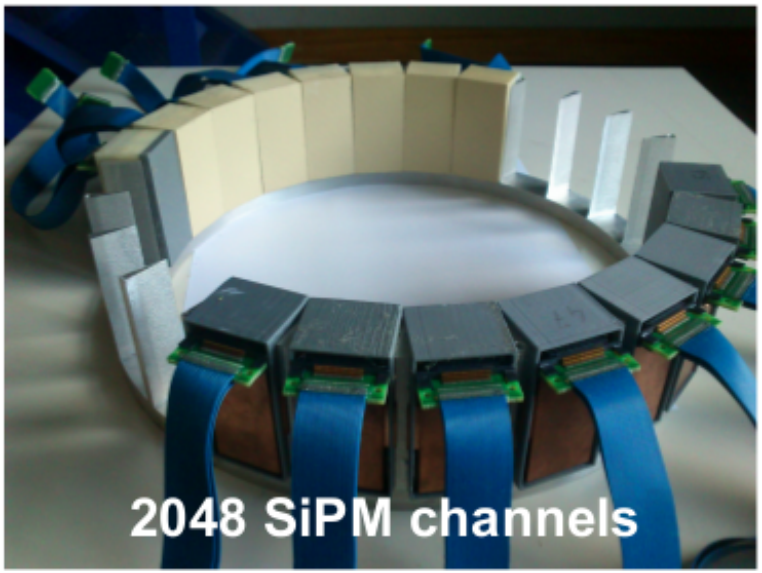
The TOFPET ASIC consists of a 64-channel analogue block, calibration circuitry, Golden-references and Bias generators and a global controller.

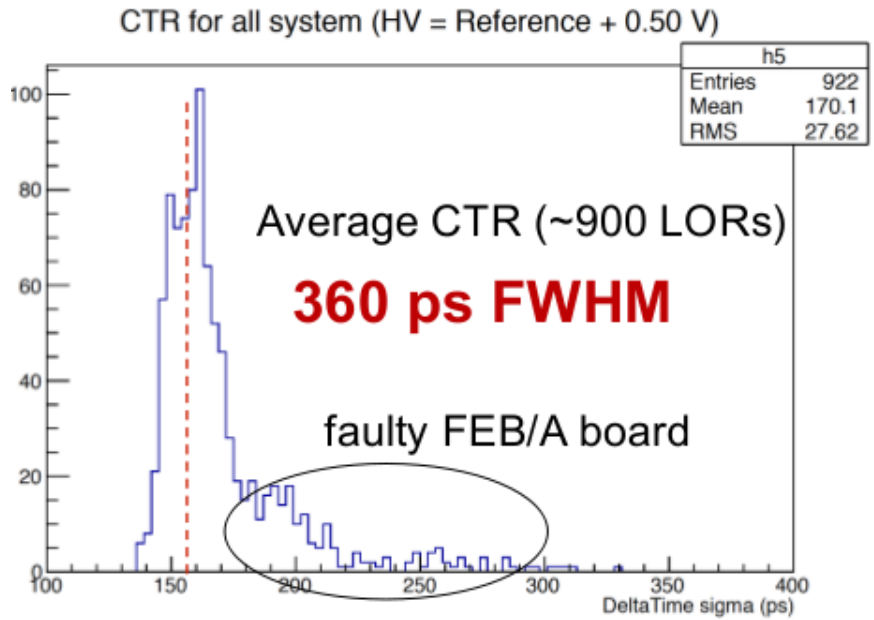


- LVDS 10 MHz SPI configuration link and dark count measure
- LVDS up to 640 Mbps data output interface; 8B/10B encoding
- On-chip DACs and reference generators

TOFPET: highlight of system-level results

- 21-35 ps r.m.s. channel resolution (internal TP, laser)
- 310 ps FWHM CTR with 15 mm long crystals
- 360 ps FWHM CTR System-Level: 16 detector modules, 2048 SiPM channels



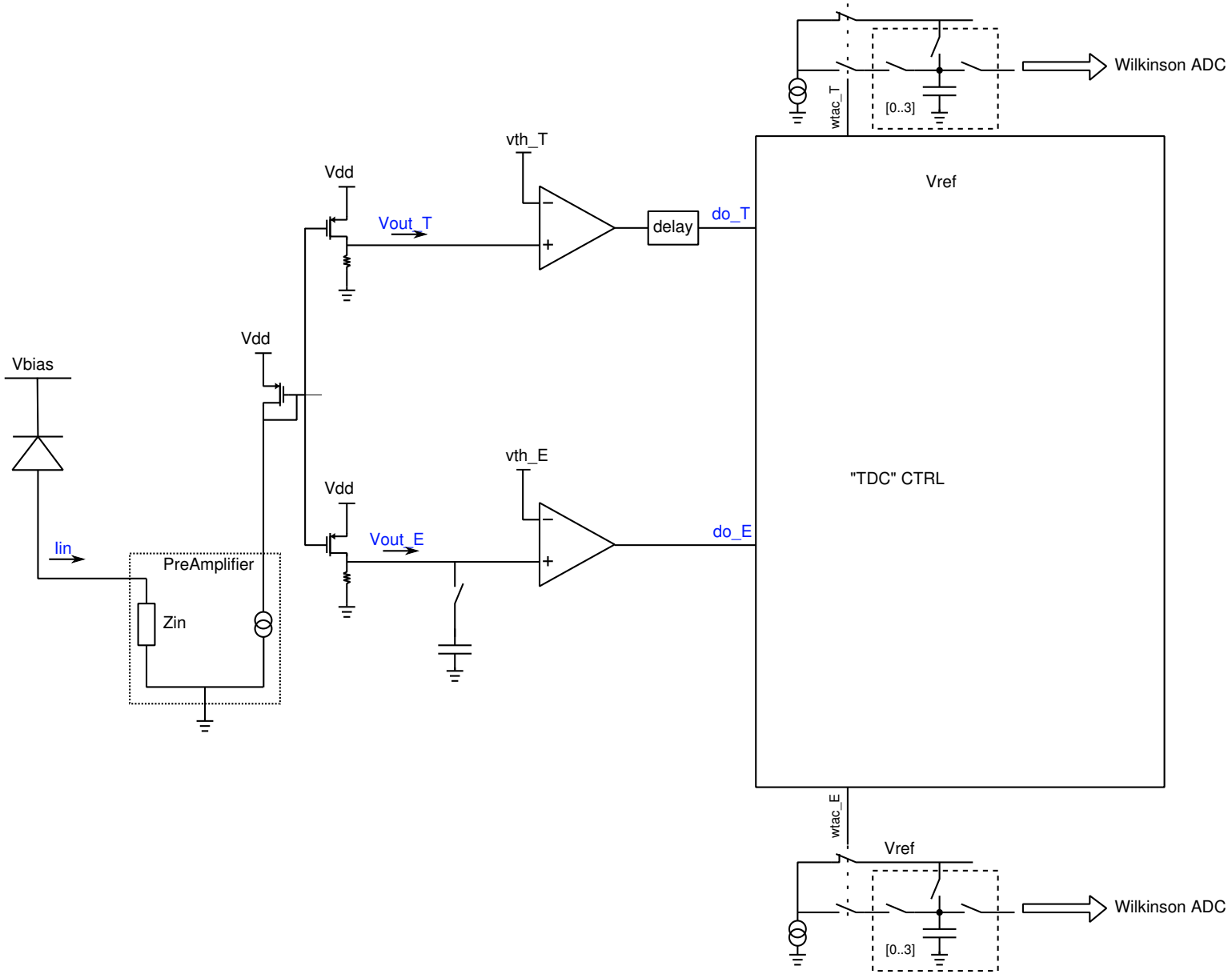


TOFPET requirements

Input signal	0 – 2500 p.e. from a LYSO scintillator
MPPC gain	0.75×10^6 – max 300 pC input charge
MPPC fine bias adjustment	0–500 mV
Time resolution	200 ps FWHM
Event rate per channel	160 kHz
Energy measurement	Time-over-threshold
Time discriminator	0 – 20 p.e., 0.5 p.e. resolution – time trigger
Energy discriminator	Same as time discriminator[1]
Dark count rejection	Multiple methods, up to 1 MHz.
Internal dark event counter	10 bit
Clock frequency	160 MHz
TDC binning	50 ps (25 ps option)
Output	Digitized events, grouped into 1024 clock frames
Output rate	160 – 640 Mbit/s, 8B/10B encoded
Configuration	Full digital configuration
Power consumption	5 mW/channel.

[1] Dark count rejection only

TOFPET channel overview



Outline

Improvements for TOFPET2

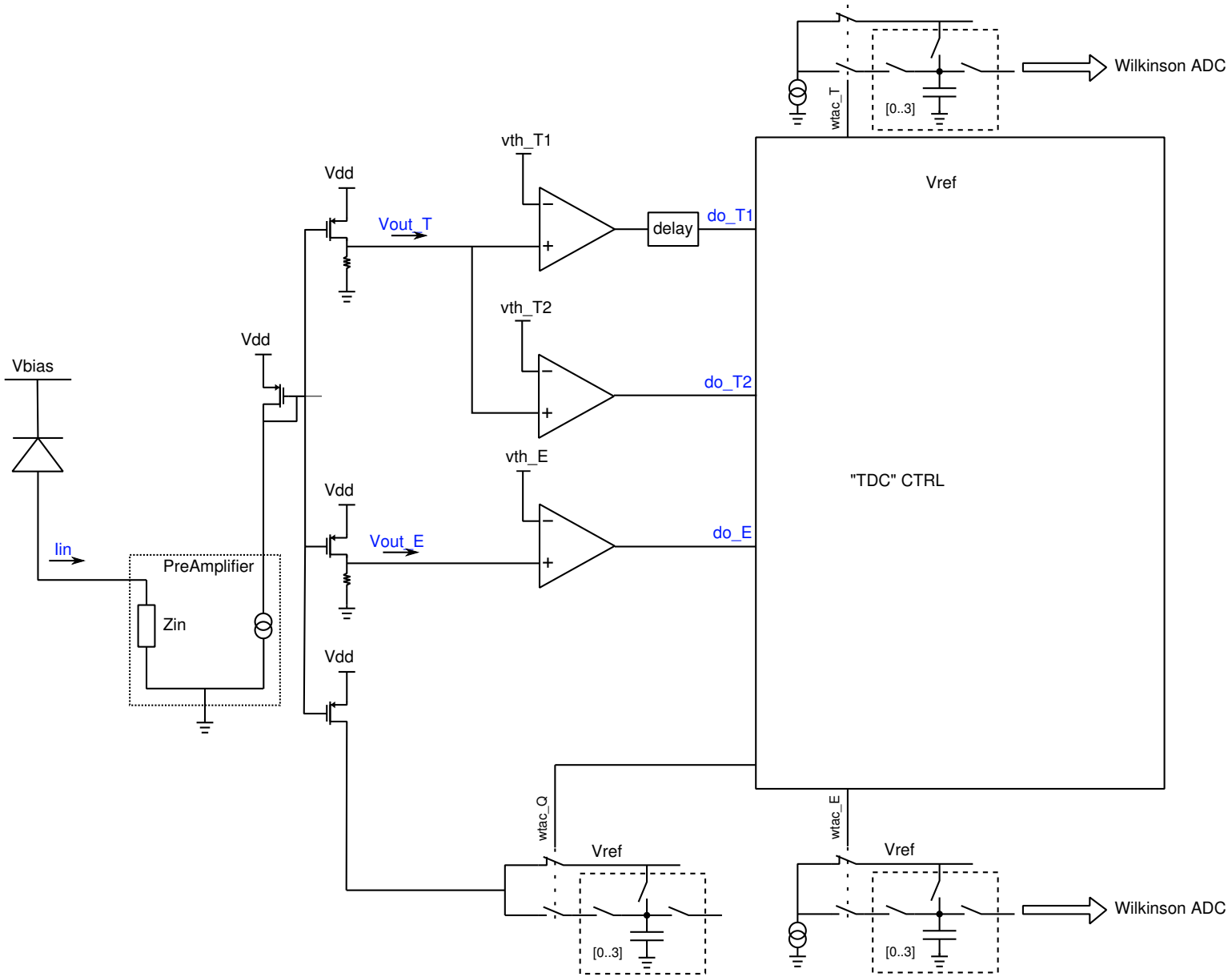
- Revised front-end: increased immunity to digital interference noise
- Light sharing applications require higher event rates.
- A better amplitude measurement is required (linear and not sensitive to photon statistics).
  - Integration of charge on the full dynamic range
  - keeps ToT measurement as option
  - uses Wilkinson ADC
- Event grouping best done in FPGA (changed for BESIII IP).
- TX modes with training sequences for FPGA deserialiser logic.

Requirements for TOFPET2

Input signal	0 – 2500 p.e. from a LYSO scintillator
MPPC gain	1.25×10^6 or 3.5×10^6– max 500 or 1400 pC input charge
MPPC fine bias adjustment	None
Time resolution	200 ps FWHM
Event rate per channel	600 kHz [2]
Energy measurement	Time-over-threshold OR linear charge measurement with configurable integration time
Time discriminator (1)	0 – 4 p.e, 0.25 p.e. resolution – time trigger
Time distriminator (2)	0 – 20 p.e. – delay based dark rejection
Energy discriminator	0 – 1000 keV
Dark count rejection	Delay based, up to 2 MHz.
Internal event counter	24 bit, multiple counting options.
Input clock frequency	200 or 400 MHz
TDC clock frequency	200 MHz
TDC binning	50 ps (100 ps and 25 ps option)
Output	Digitized events, no grouping
Output rate	200 – 3400 Mbit/s, 8B/10B encoded
Configuration	Full digital configuration
Power consumption	5 mW/channel.

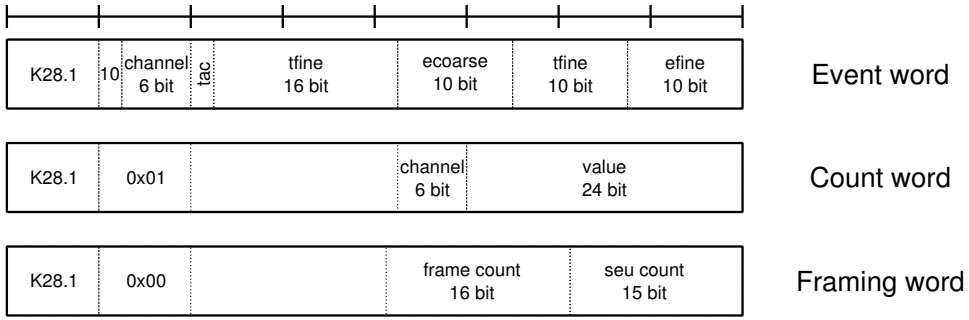
[2] 100 kHz of maximum amplitude events

TOFPET2 channel overview



Outline

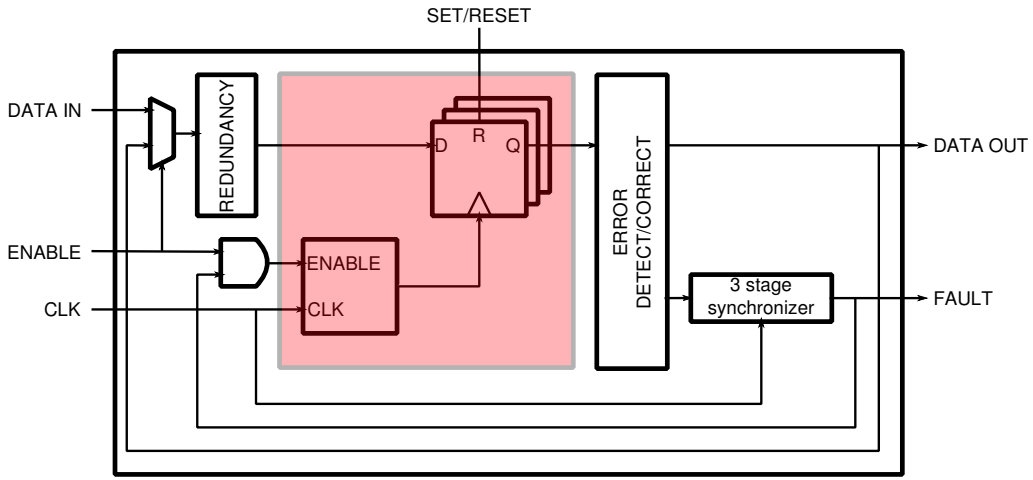
Data transmission



- K25.5 used for idle
- Event words – no change
- Count words – no change
- Framing words – new for BESIII

A framing word is generated every 2^{15} clock cycles and queued for transmission (top priority; delay is 0–79 clock cycles). Frame count is incremented and SEU count is reset.

SEU protection



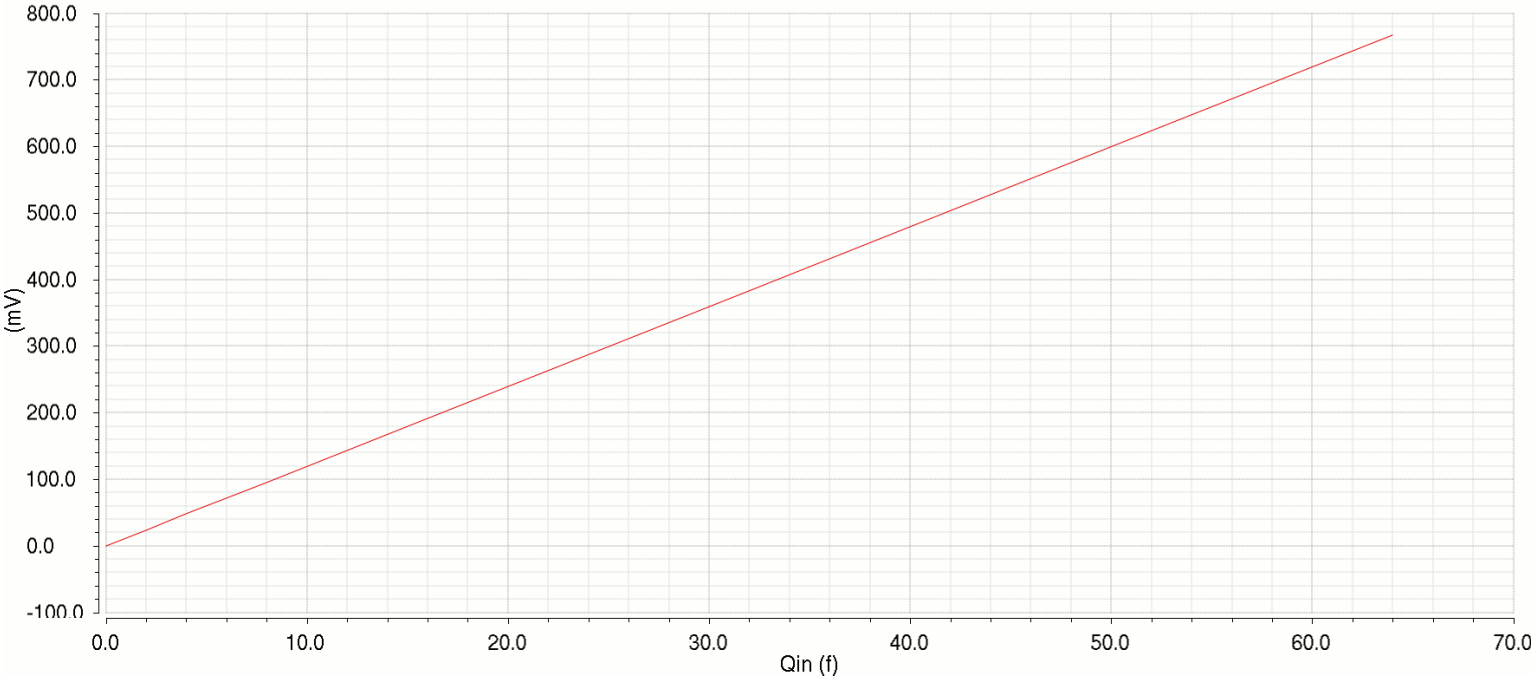
- Module: register bank with reset and clock enable.
- Fault output feeds to a global counter.
- Two level module, hierarchical optimization disabled for lower level to keep redundant .
- TMR for state machines and etc.
- Hamming(255,247) for configuration/payload registers.
- Automatic scrubbing, if clock is active.
- Fault output feeds to a global counter.

Layout of Digital back-end

- Global Controller width increased from 505 um to 525 um to accomodate SEU protection logic.
- Pin spacing between Global Controller and Channel Controller increased to 0.96 um, providing more space to solve antenna violations.
- Buffers added in channel configuration pins.
- New trigger mode added in channel controller (integrate on TP, measure time on discriminator).

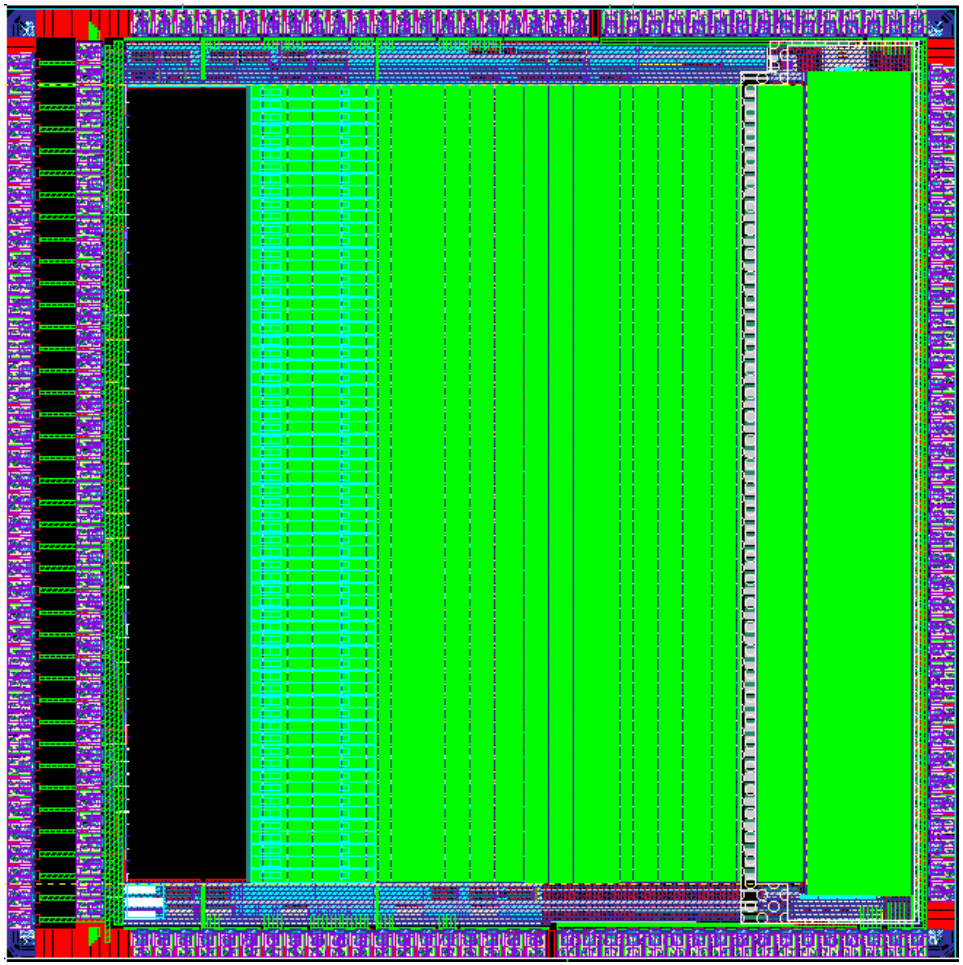
Integrator design for BESIII

- Redesign of the TOFPET2 integrator for better linearity on the charge measurement
- Sampling of the Slow shaper output



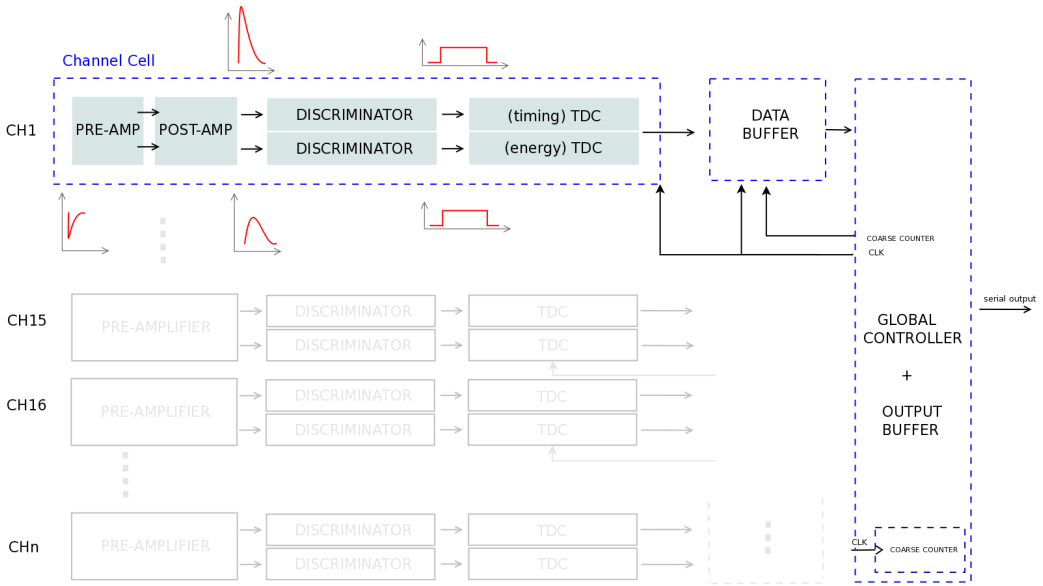
Status and Outlook

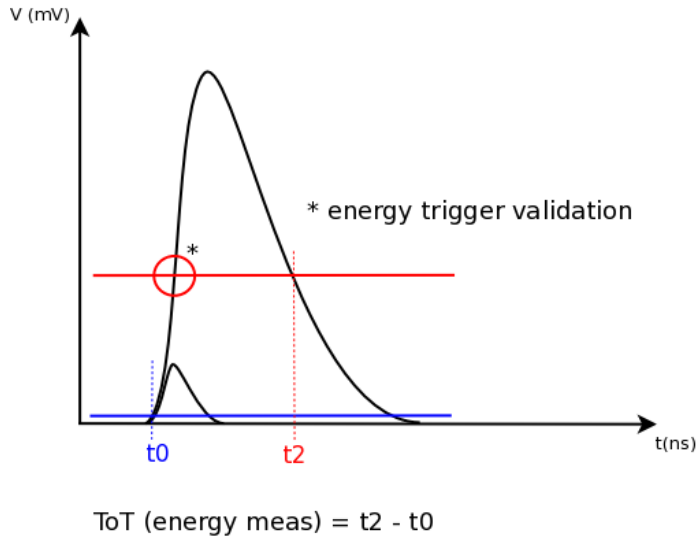
- TOFPET2_IP top layout and schematic ready for integration (DRC, LVS clean)
- work ongoing on channel-level design



Thank you!

Inputs for TDC



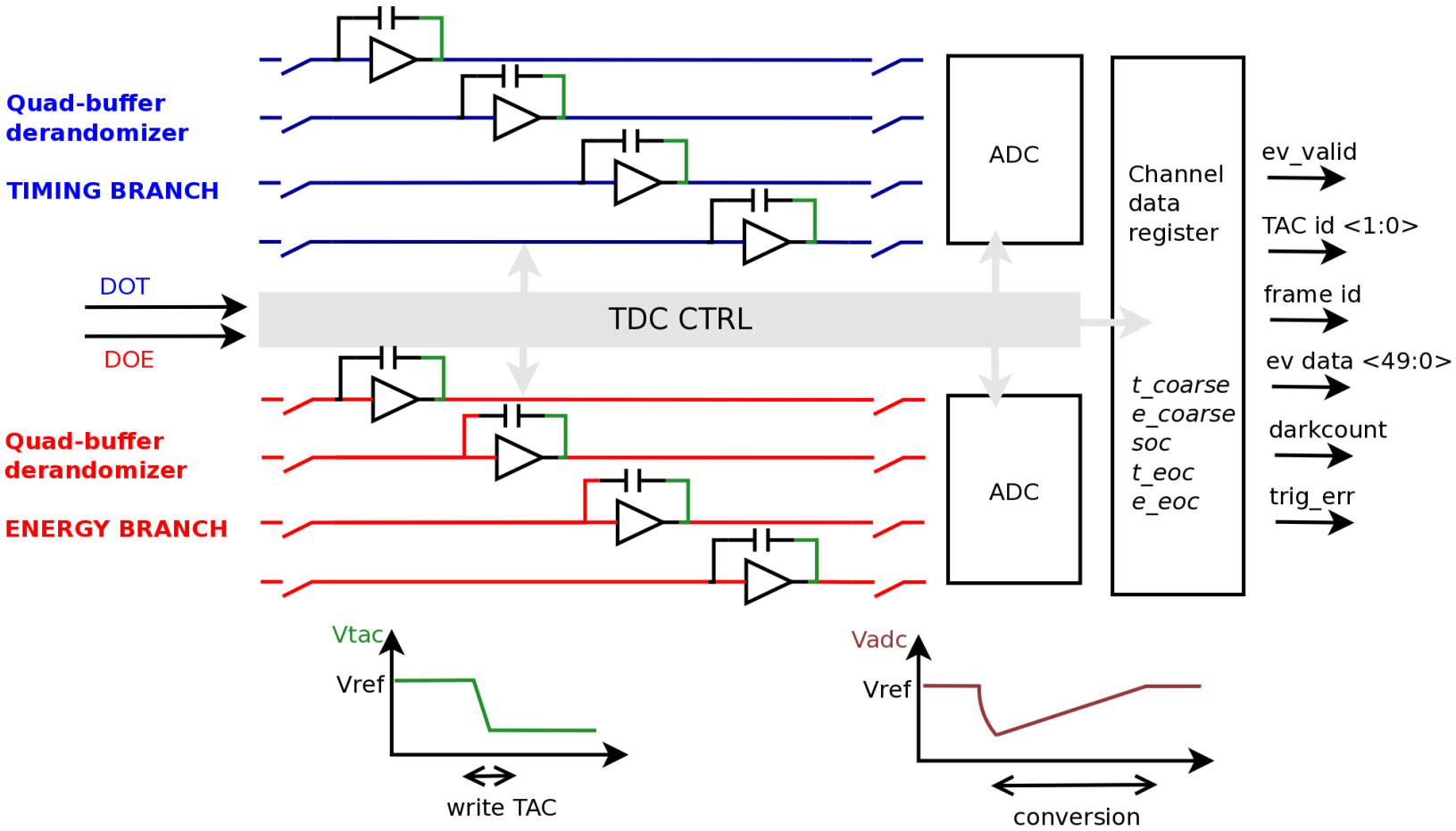


- t0: 50 ps time stamp from rising edge of DOT
- t2 : 50 ps time stamp from falling edge of DOE

Time-to-Digital Converter

Analogue TDC with 25ps/50ps time binning - based on Analogue Interpolators

- TDC Control: switching, hit validation, buffer allocation, data reg.
- Time stamp: 10-bit master clock count + Fine time measurement



TDC overview