CGEM ASIC GENERAL

Huaishen Li

14-April-2016, Turin

BESIII CGEM FEE/DAQ/Trigger Workshop

Design Team

- Designers (Analog Front-end):
  - H. S. Li (IHEP, INFN)
  - C. Y. Leng (INFN, IHEP)
  - J. Y. Chai (INFN, IHEP)
- Technical Advisors:
  - A. Rivetti (INFN)
  - M. Rolo (INFN)

CGEM FEE

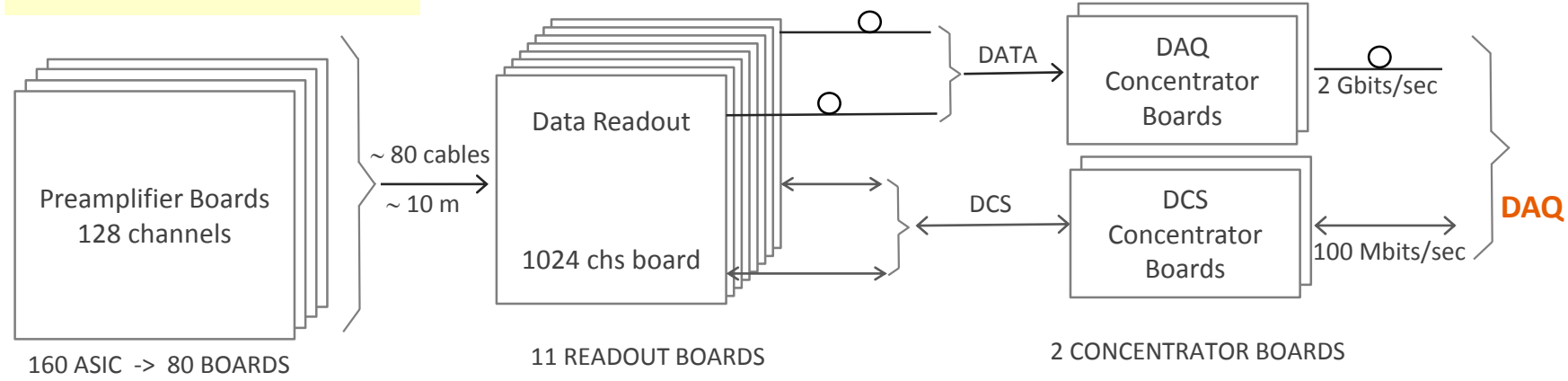
- Goals
  - Spatial Resolution ~ 120 μm
  - Time Resolution of the order of 4-5ns
  - Short Dead Time < 1μs (shaping time+analog-to-digital conversion time) to limit Pile-up probability at a few %
- Channels
  - ~ 10 000 Channels → 160 ASICs → 80 PCB
  - 64 Channels per ASIC → 2 ASICs per PCB
- ASIC Requirements
  - 1 – 50 fC Input Charge
  - Up to 100 pF Sensor Capacitance
  - 60 kHz Rate per Channel (safety factor of 4 included)
- Trigger Latency 6.4 μs

CGEM ELECTRONICS

FEE BLOCK DIAGRAM

ON-DETECTOR ELECTRONICS
~ 10 000 CHANNELS

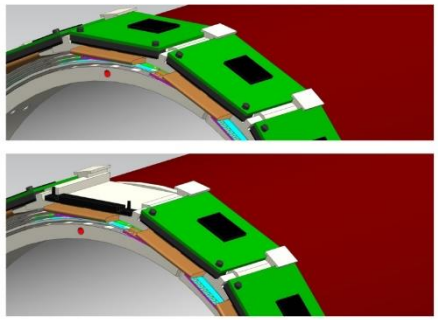
OFF-DETECTOR ELECTRONICS

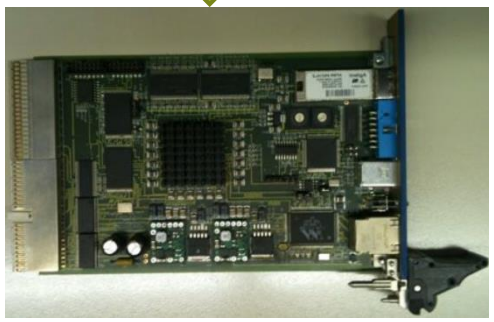


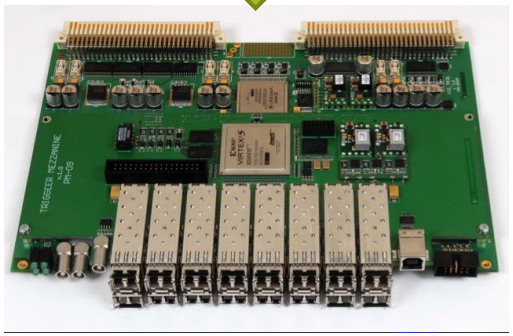
160 ASIC -> 80 BOARDS

11 READOUT BOARDS

2 CONCENTRATOR BOARDS







INFN-TORINO
IHEP-China

INFN-FERRARA **INFN-LNF**

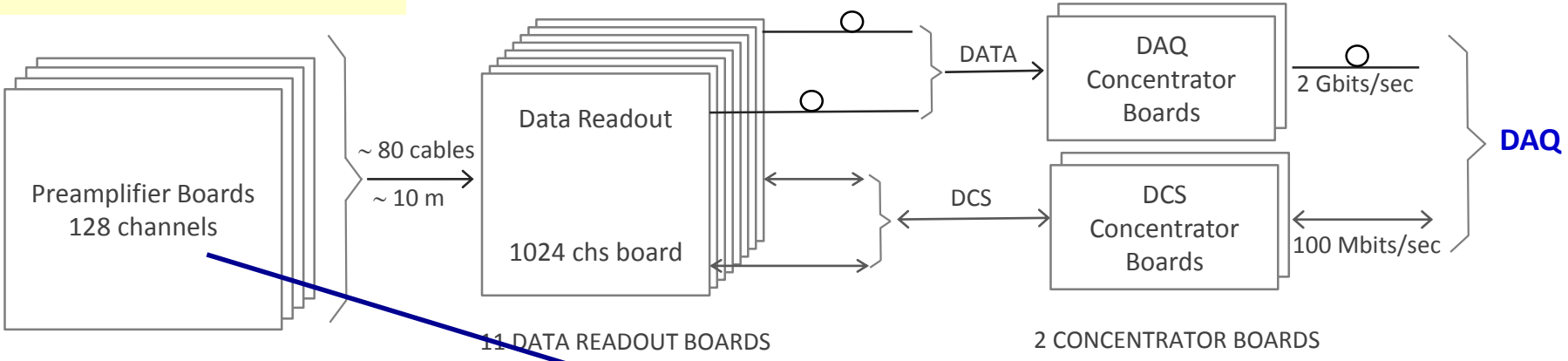
Uppsala U

Turin, 14-April-2016

FEE BLOCK DIAGRAM

ON-DETECTOR ELECTRONICS
~ 10 000 CHANNELS

OFF-DETECTOR ELECTRONICS

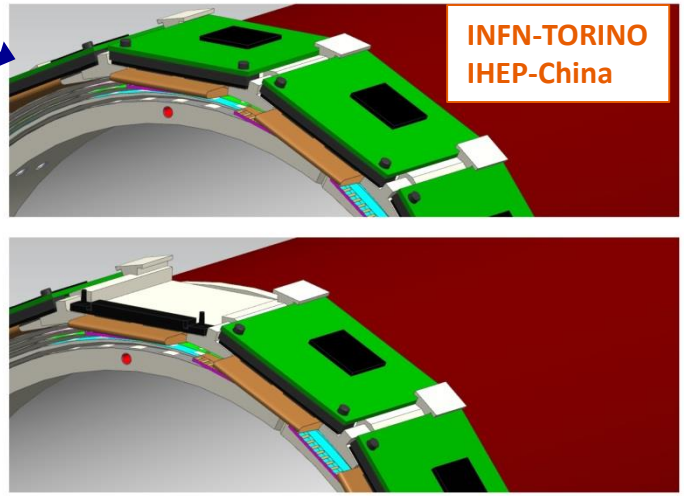


GEM LAYERS

I 32 ASICs 16 PCB
II 56 ASICs 28 PCB
III 72 ASICs 36 PCB

NUMBERS

64 Channels per ASIC
1 PCB → 2 ASICs
10 240 Ch → 80 PCB



CGEM ASIC

CGEM ASIC under development at INFN-Torino in Collaboration with IHEP, which provides two PhD students(2x3 years) and one Expert (2 years) for ASIC design and tests , with two technical advisors (A. Rivetti and M. Rolo)

Design started from TOFPET ASIC and TOFPET2 ASIC

- TOFPET used for Medical PET Applications ,
  IBM 130nm, (TOFPET2 UMC110nm)
  no SEU protection, FEE suitable for SiPM signals

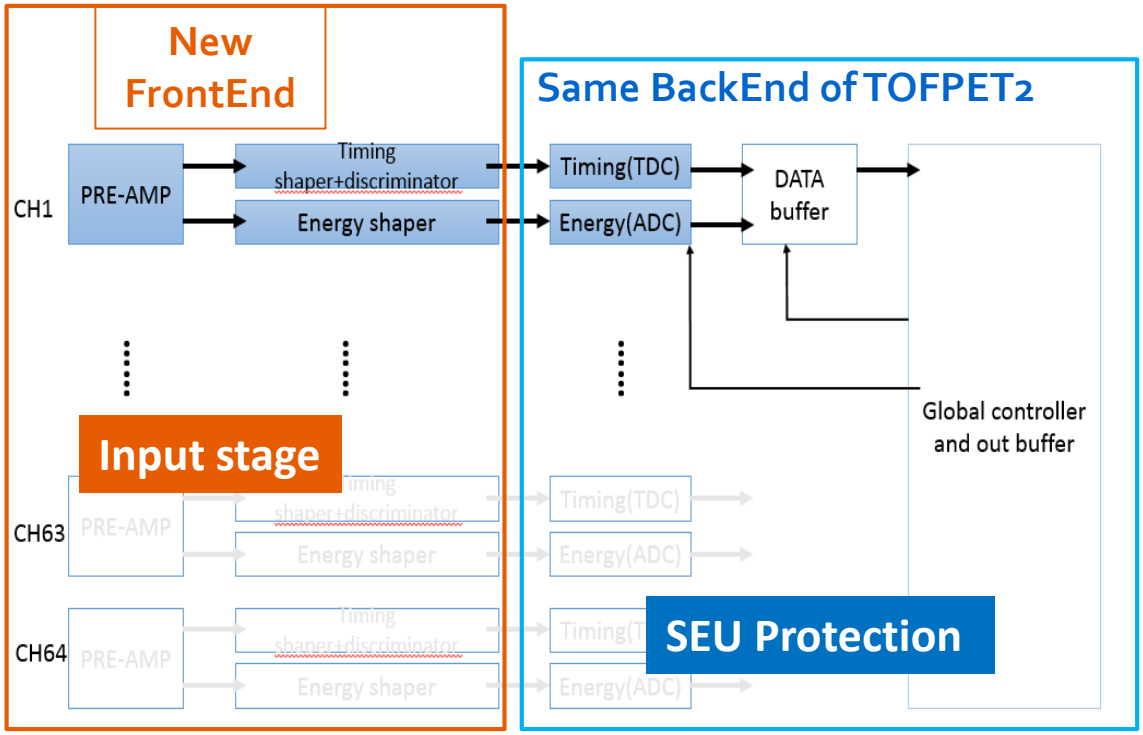
- CGEM-ASIC developed for BESIII experiment,
  UMC 110nm (exportable in China, limited power consumption,
  reduced cost wrt IBM, to be tested for Radiation Tolerance),
  SEU protection, FEE suitable for GEM signals

-Time and charge measurements by TDC and ADC
-Digital output

About TOFPET ASIC,
Please see M. Rolo 's slides

CGEM ASIC

Overview of the channel architecture after August 2015



64 Channels

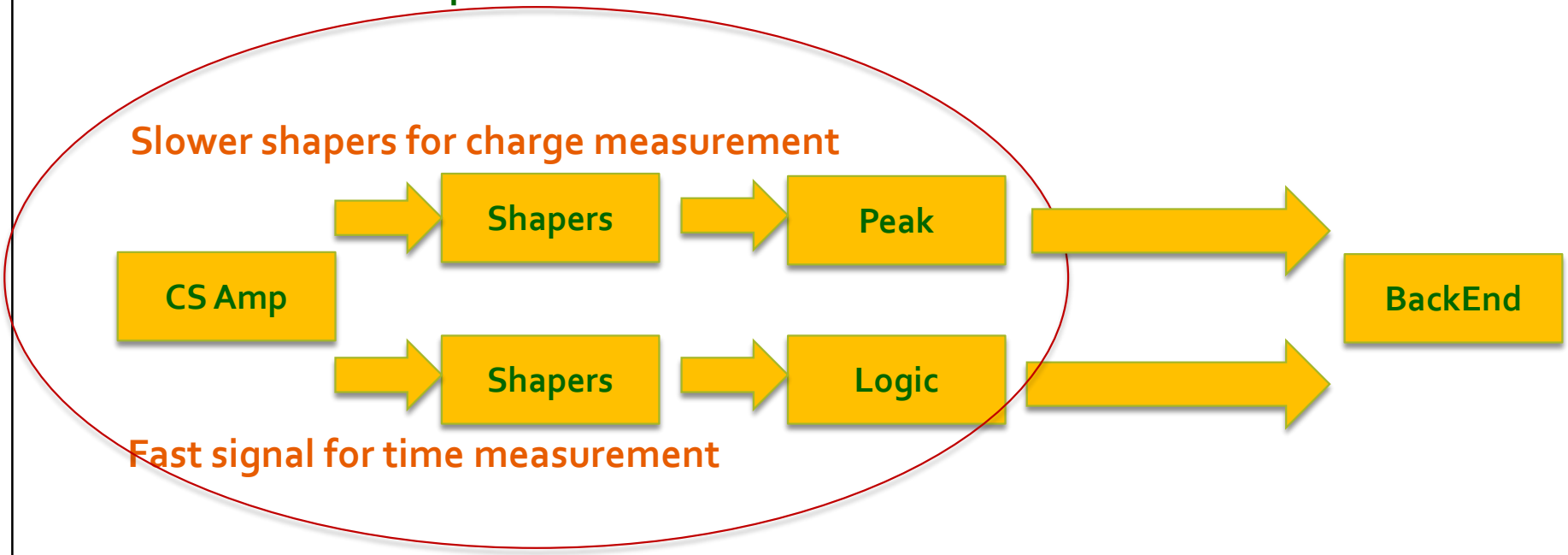
BackEnd compatible with the previous one
More functionalities included

LVDS output

- TOFPET2 BackEnd, developed for PET application, will be used instead
  - UMC 110 nm
  - Charge is measured by an ADC
  - SEU protection has been implemented

PREAMP AND SHAPER

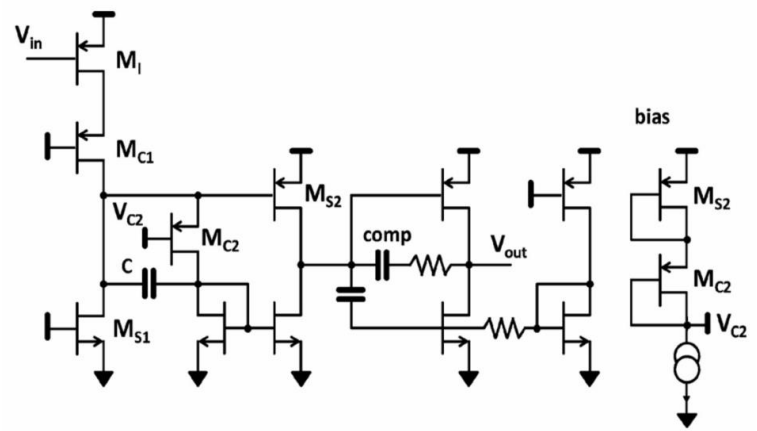
- Based on PMOS input transistors



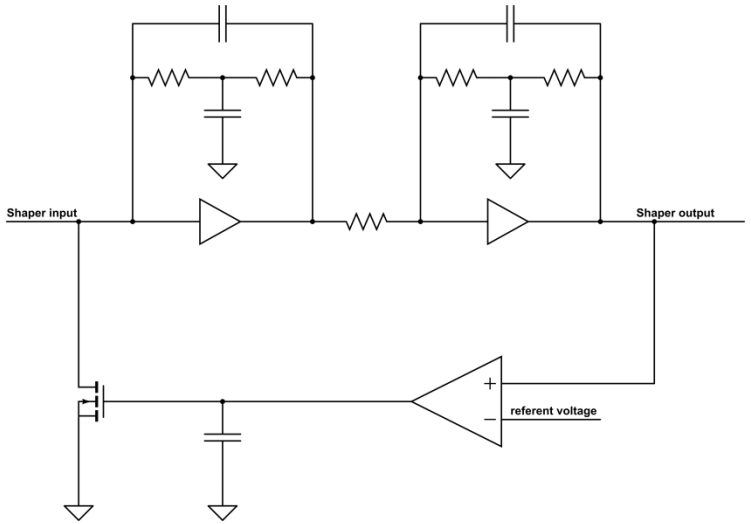
Detector capacitance: up to 100pF

- **Noise performance related to the adjustable peaking time:**
  <700e- @200ns
- **Timing performance 5.5 ns@1fC input, 100pF**
- **Power consumption ≈ 5mW (Preamp+shaper) + 4mW (digital part) total < 10mW**
- **Full signal pulse width (energy branch) ≈ 900ns**
- **Output gain (energy branch) ≈ 12mV/fC**

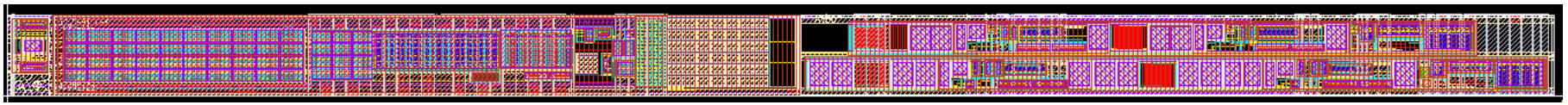
Preamplifier and shape



Core of the pre-amplifier



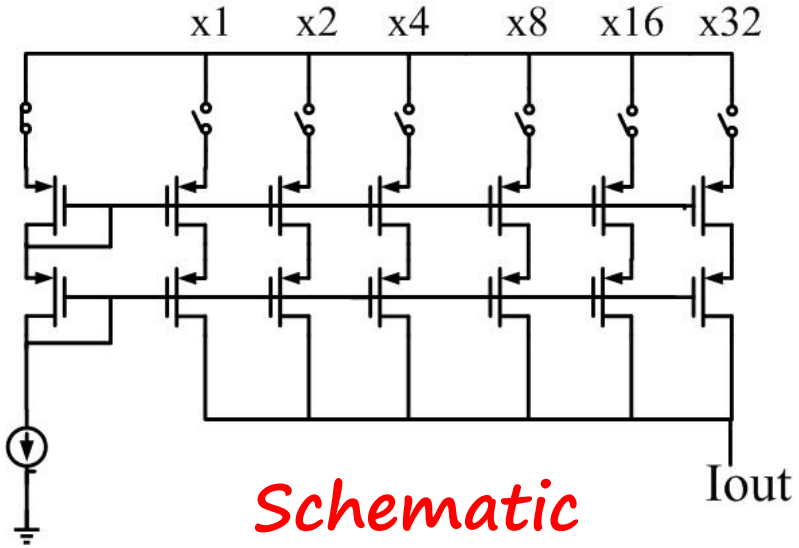
shaper



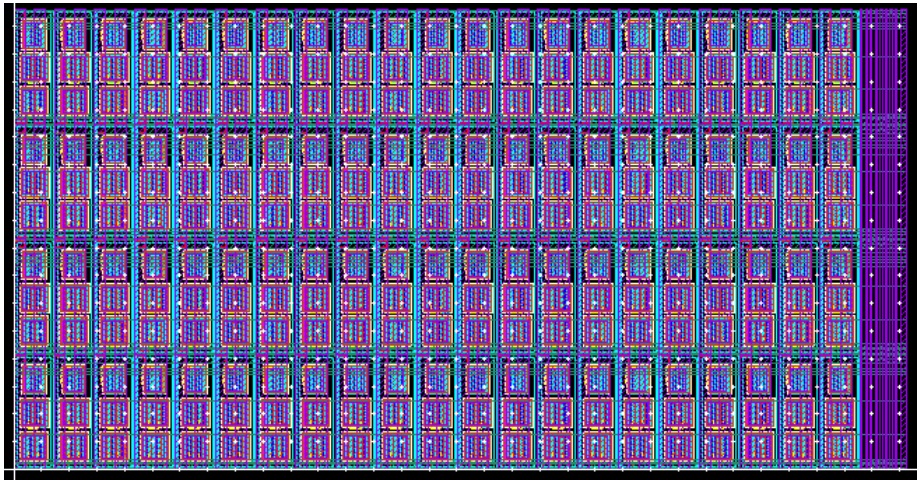
Layout of one channel of the preamplifier and shaper : 72 μm x 1350μm

Details of the front-end, please see Chongyang's slides

6bit DACs design



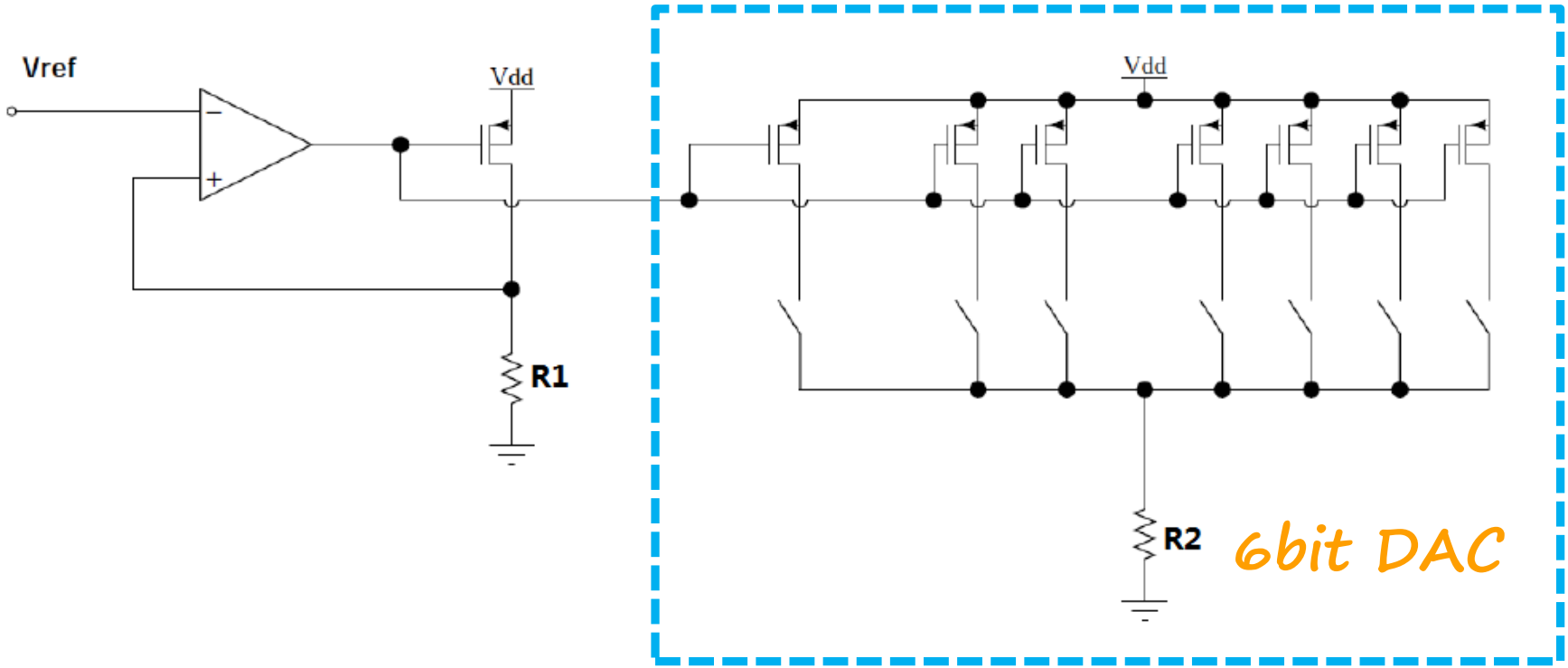
Schematic



Layout

- **Only for the bias, no demand of speed**
- **LSB=3.6uA**
- **Output: 0V→0.7V（64LSB@3kΩ）**
- **Area: 160um x 80um**

Bias circuit



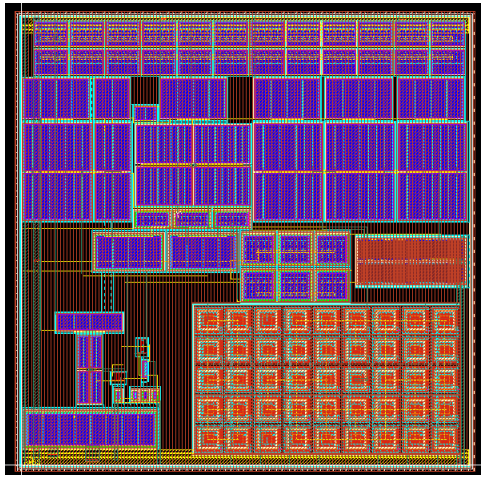
Some analog parameters of the preamplifier need to be fined tuned for the optimized performance

Bandgap Design

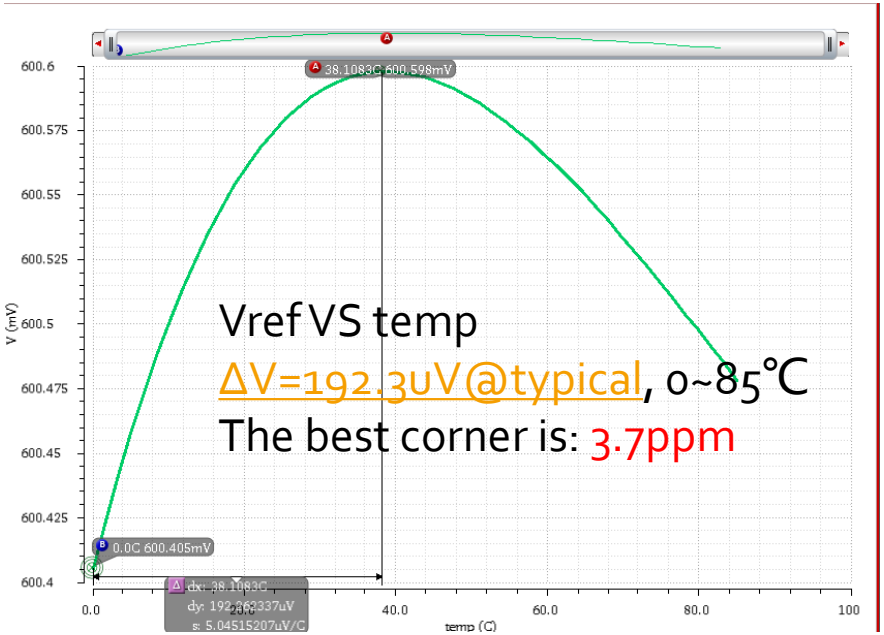
To get a temperature and power supply independent voltage reference.

To generate a precise references for the chip.

This Bandgap IP is ready to be used in a second version



Area: 300um * 300um, Power: 250uA

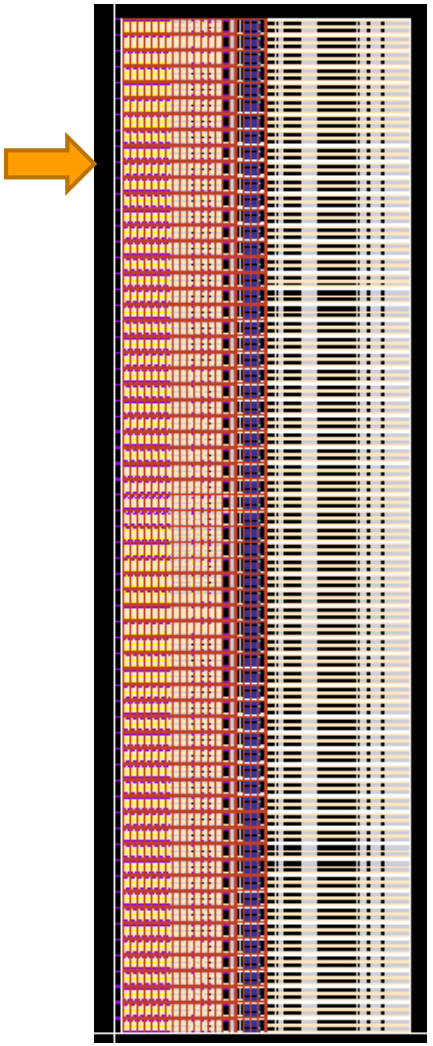


- V_{REF}=601.4mV@27℃ Typical
- V_{supply_min}=1.0V
- Temperature coefficient: 3.77ppm/ ℃
- $\Delta V_{out}/\Delta V_{supply}$=6.8mV/V
- $\Delta V_{out}/\Delta T$=0.03mV / ℃
- Power=0.3mW
- Area: 300X300 μm^2
- RMS Noise： $44\mu V$

Layout of the Front-end

- 64-channel pre-amplifier and shaper is OK
- Power Grid finished
- Post simulation shows it works well

- Bias layout design is ongoing



Summary

- Front-end
  - The 64-channel layout finished
  - Post simulation results are good
  - Some layout needs to be modified for fitting the back-end
- Back-end
  - SEU protection included
  - Some reset function included
  - Ready for integration
- Submit at the beginning of May, 2016

Thank you!