BES-III off-detector readout electronics for the GEM detector: an outline

Ricardo Bugalho, Stefano Chiozzi, Angelo Cotta Ramusino, Giulietto Felici, Roberto Malaguti, Marco Mignone, Pawel Marciniewski, Manuel Rolo

Summary:

- Introduction

- Current design specifications for the off-detector electronics:
  - ASIC specifications for the configuration and data ports
  - BES-III Trigger/Timing system specifications
  - Specifications of the interface between the GEM detector/DAQ and the BES-III Detector Control System (DCS)
  - Specifications of the interface between the GEM DAQ system and the BES-III Run Control System

- Current design baseline for the off-detector electronics:
  - Proposed system layout
  - Prototyping:
    - transmission of 8b/10b encoded data at 160MHz over candidate cable
    - testing the 2Gbps communication links between the off-detector readout cards and the data concentrators
  - Review of estimated data rate of raw and trigger matched data

- Open questions

- **Introduction**

This presentation starts with a summary of the current knowledge about the specifications to which the off-detector readout system for the GEM detector of BES-III should be built.The acquisition of the specifications is still in progress.
This workshop will offer the opportunity to clarify and finalize most of them.

The presentation continues with the description of the baseline design; it implements an architecture which should satisfy the currently known specifications and be flexible enough to accommodate possible future requirements. The setups prepared to test the key parts of the system are presented next, along with some preliminary results.

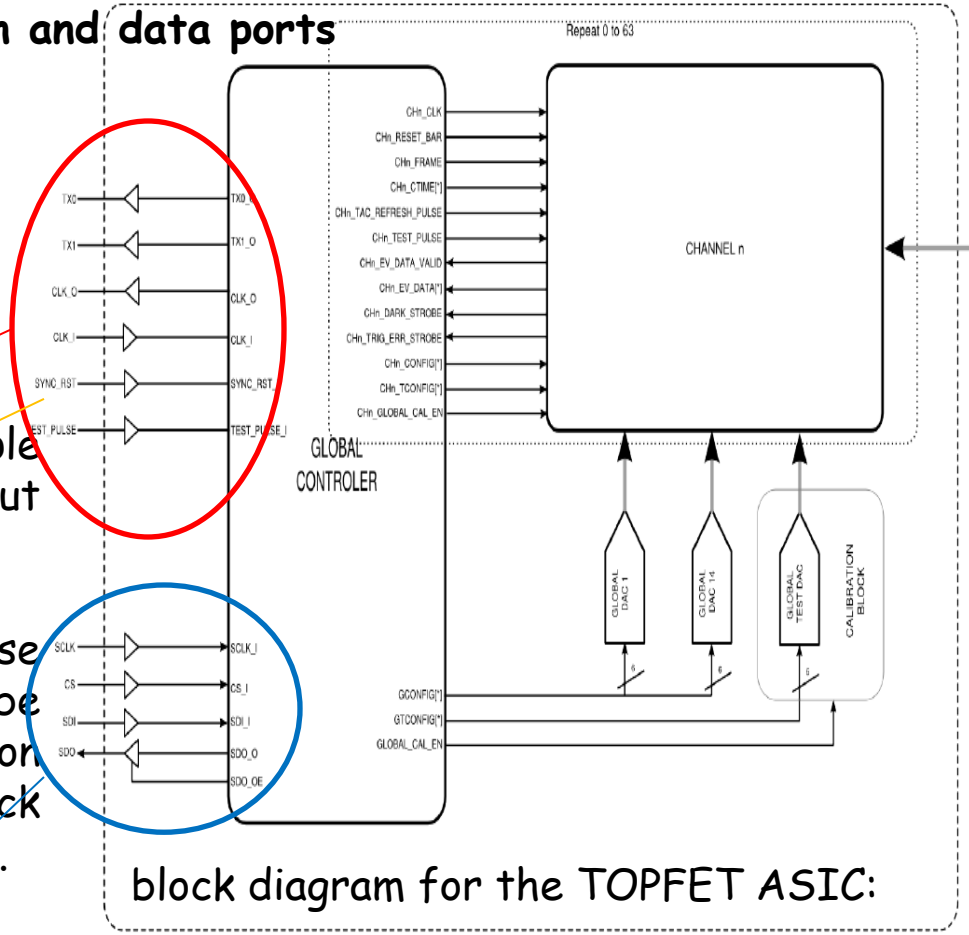
A summary of the data rate estimates at the input and at the output of the GEM off-detector readout system is then presented, along with a proposal for data formats

Finally a summary is presented of open issues about design specifications and constraints.

- **ASIC specifications for the configuration and data ports**

The readout ASIC for the on-detector part of the GEM detector (GEM-ASIC in short) is being developed.
Some of the characteristics of its output interface are summarized below:

- 200 MHz, 8B/10B encoding and multiple operation modes, allowing for an output bandwidth of 200 to 800Mbit/s;
- 1, 2 or 4 active output links
- The "SYNC_RST" signal is a dual purpose reset: a single clock active high strobe causes everything BUT the configuration registers to be reset. A two or more clock strobe causes the entire ASIC to be reset.



block diagram for the TOPFET ASIC:

- CONFIGURATION interface:
  - 10 MHz, SPI-like
  - serves several purposes: write and read <u>channels' settings</u> (buffer current, channel enable, gain, thresholds, etc) and <u>global settings</u> (coarse buffer current, TAC refresh rate, TX training mode,etc).

- **ASIC specifications for the configuration and data ports: configuration interface (work in progress):**

ASIC (TOPFET) control link

The ASIC's control link is SPI-like and consists of 4 lines:

- CS (chip select)
- SCLK (serial clock, 10 MHz)
- SDI (serial data in)
- SDO (serial data out)

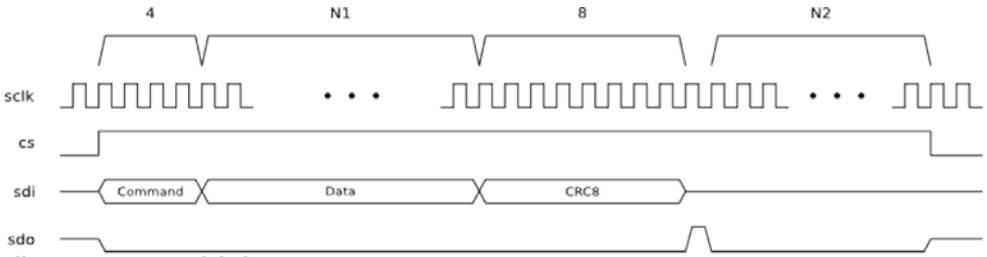


Illustration 6: SPI Global Write

- The commands to the ASIC follow a general structure:
  - 4 bit command
  - 7 bit channel address (if applicable)
  - N1 bit long command data (if applicable)
  - 8 bit CRC

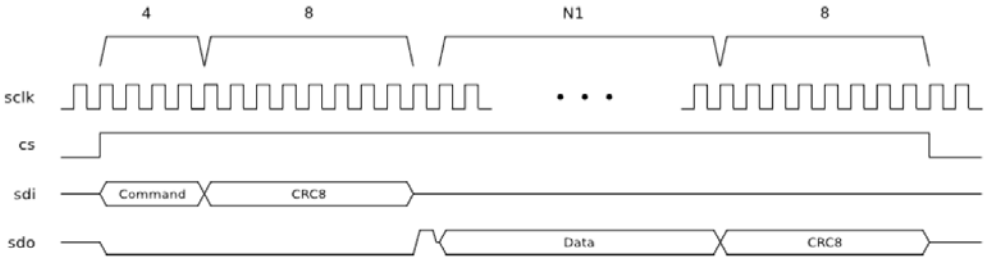


Illustration 7: SPI Global Read

- After the command has been sent, the ASIC will set SDO to "1" if the command was successfully acknowledged, "0" else. If the command is not validated, the ASIC will not take any internal action. Write commands require that CS and SCLK to be kept active for an extra N2 clock cycles, while the ASIC's internal machinery works.
- In case of read commands, data will be written after the acknowledgment cycle.
- Read data will also be followed by a CRC8.

All fields are transmitted MSB first.

The 8 bit CRC's polynomial is x8 + x2 + x + 1 (CCITT CRC) with an initial value of 0x8A.

NOTE I/O Timing (TOPFET ASIC)

The ASIC has 2 clock inputs (*clk_i*, *sclk_i*) and one clock output (*clk_o*).
clk_i is the main 160 MHz clock. *sclk_i* is the 10 MHz configuration clock.
The rising edge of *sclk_i* MUST be aligned with the falling edge of *clk_i* ± ns.

CONSTRAINT REMOVED FOR THE GEM-ASIC!!! (R.Bugalho, M. Rolo 2016-04-13)

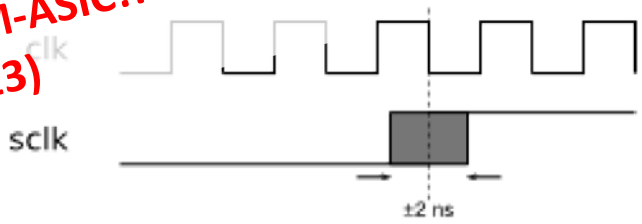


Illustration 10: Clocks relationship

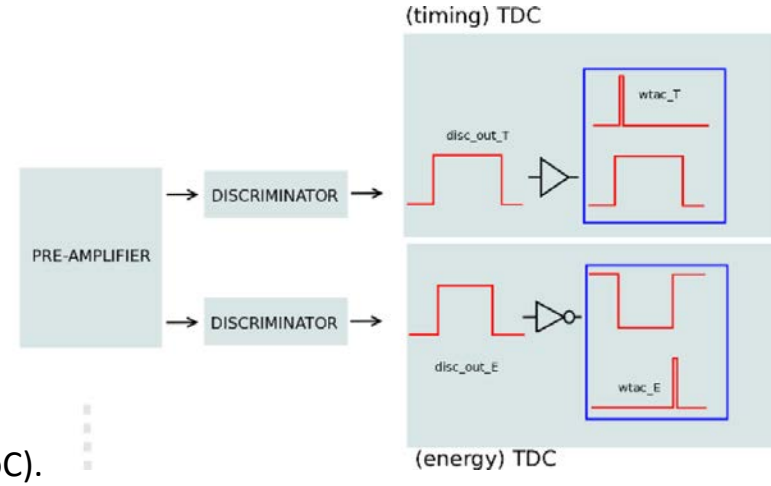
- **ASIC specifications for the configuration and data ports: timing measurements (work in progress):**

TDC overview (TOPFET ASIC/ GEM-ASIC)

Each channel amplifies the input signal and provides two digital timing measurements:

- Time when the amplified signal rose above the time threshold (T trigger)
- Time when the amplified signal dropped below the energy threshold (E trigger).

Signals that do not pass above the energy threshold are discarded.



Each timing measurement consists of 3 values:

- The value of the coarse counter when the trigger occurred.
- The value of the coarse counter when the TDC started the conversion (SoC).
- The value of the coarse counter when the TDC ended the conversion (EoC).

The coarse counter is a 16 bit counter that counts clock cycles.

The difference between SoC and EoC provides the fine counter value: FC = EoC – SoC – Kf

Kf is a configurable, ASIC wide, 8 bit value whose purpose is to make the most out of FC's dynamic range, since the TACs have a dynamic range of 1 – 3 clocks.

The actual time calculation method needs to take into account a number of cases, which depend on the coarse and fine counter values. The correction will be implemented in the receiving FPGA.

Thus, the ASIC will output 4 values.

1. T coarse counter (16 bit)
2. T fine counter (10 bit)
3. (E coarse counter – T coarse counter) (10 bit)
4. E fine counter (10 bit)

- **ASIC specifications for the configuration and data ports: output data format for GEM-ASIC:**

source synchronous mode not used GEM-ASIC!!! (R.Bugalho, 2016-04-12)

GEM-ASIC Data Output Link

The ASIC will support ~~both source synchronous and~~ "calibrated" reception schemes. Data is distributed across active links in octets.

Each link is individually 8B/10B encoded; a special control code K28.1 is used to mark the beginning of 64bit words. Control code K28.5 is used as filler.

The K28.1 and K28.5 characters also provide the receptor means to align the deserializer: their "0011111xxx" or 1100000xxx" sequences will not show anywhere else in the bitstream.

GEM-ASIC data stream description (Ricardo Bugalho):

"*The current strategy, we have now in TOFPET 2 is simply to transmit the events as soon as the TDC finishes conversion…*

The events contain a 16 bit coarse time tag (64K clock cycles) which given the 0~2K clock cycle conversion+transmission delay is more than enough for the FPGA to disambiguate what is the global time of an event.

So, what I have implemented for BESIII is:

t = 0 -- Send frame word 0

send events (belonging to frame 0)

t = 32K -- Send frame word 1

send events(some still belonging to frame 0, most to frame 1)

t = 64K -- Send frame word 2

send events(some still belonging to frame 1, most to frame 2)

t = 96K -- Send frame word 3"

- **ASIC specifications for the configuration and data ports: output data format for GEM-ASIC:**

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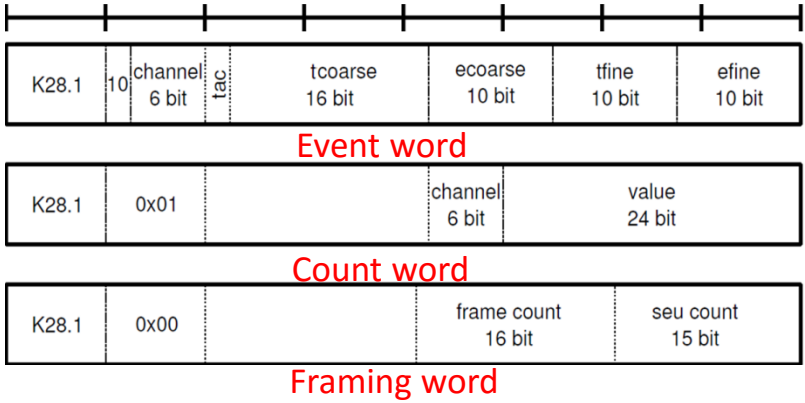
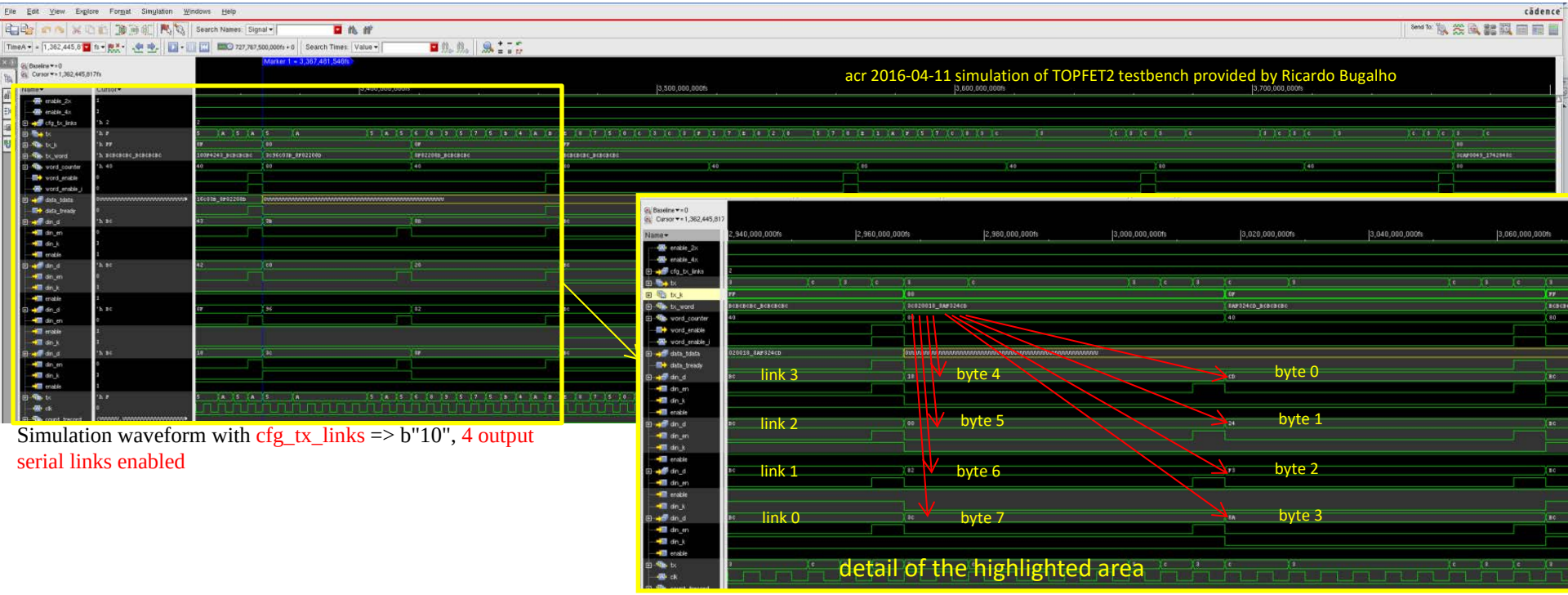
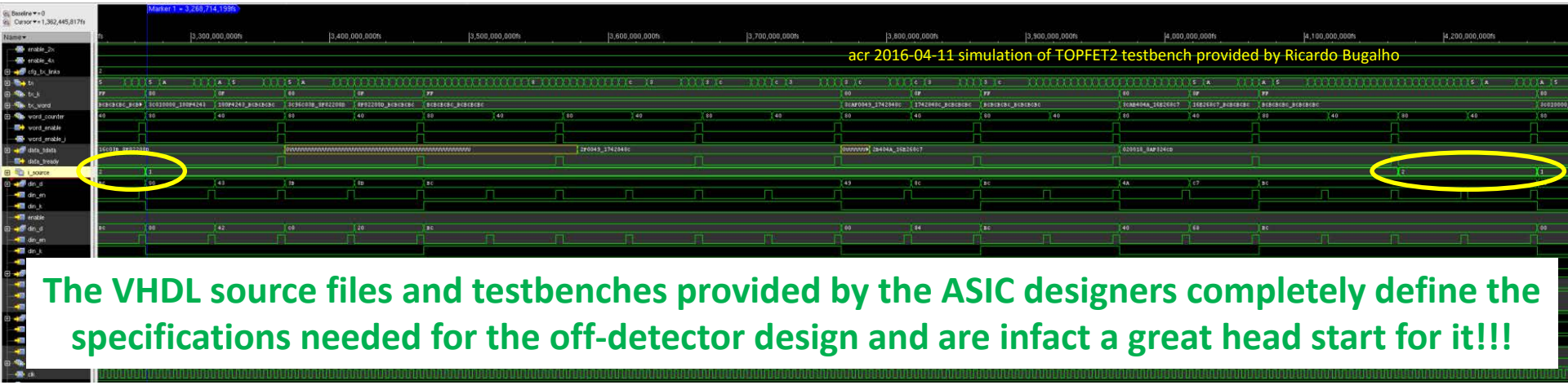


A framing word {new for BESIII} is generated every 2^{15} clock cycles and queued for transmission with top priority (but It could be delayed 0 ÷79 clock cycles). Frame count is incremented and SEU count is reset.

- **ASIC specifications for the configuration and data ports: output data format for GEM-ASIC:**



Simulation waveform with cfg_tx_links => b"10", 4 output serial links enabled



The VHDL source files and testbenches provided by the ASIC designers completely define the specifications needed for the off-detector design and are infact a great head start for it!!!

Simulation waveforms with alternating data (i_source = b"01"), and framing (i_source = b"10") word

- **BES-III Trigger/Timing system specifications:**

Illustration of trigger related signals (provided by A. Calcaterra):

Three signals from the trigger system will be provided to the ZDD electronics, one signal needs to be provided to the trigger system by the ZDD electronics. Table 1 shows the signals and their definitions.

Name	Direction	Level	Definition	Comment
L1	To ZDD	+3.3V LVPECL	Level 1 trigger	Width of 8 clock cycles, high effective
CHK	To ZDD	+3.3V LVPECL	Check of trigger number	Width of 8 clock cycles, high effective
CLK	To ZDD	+3.3V LVPECL	System clock	41.65MHz
FULL	From ZDD	+3.3V LVPECL	Readout memory almost full	High effective
Connector : LEMO EPG.00.302.HLN Plug : LEMO FGG.00.302.??? (One sample) Connector and Plug used together.				

For the signals L1 and CHK, a width of 4 clock cycles check is proposed to avoid the fault signals.
For the signal CHK, please refer to the following words. One CHK signal is generated and transmitted to the electronic systems and trigger system every 256 L1. At present, there is an 8-bit counter in each electronic module to count the number of L1 received. Before data acquisition (before the first L1 generated and transmitted), the counter is reset to zero. The counter increases by 1 when a L1 comes (L1 is generated and transmitted after DAQ begins). When the 256 L1 comes, the counter should be zero. And when the 256 L1 generated and transmitted out, the global trigger module should generate one CHK signal. In each electronic module that has the trigger number counter, a comparison between the current trigger number and zero needs to be done, when it receives the CHK signal. When the CHK signal comes, if the current trigger number is zero, then, it's Ok, else, there is some problem. The problem may be due to the interferences, the algorithm of the readout module, or others. When this kind of problem occurs, the DAQ needs to stop. The CHK signal will be generated and transmitted out with a delay of 20 clock cycles to the 256 L1.

Yesterday's presentation by JI, Xiaolu and ZHAO, Jingzhou and the following discussion have offered the opportunity to learn more details about the Trigger/Timing system!

- **Specifications of the interface between the GEM detector/DAQ and the BES-III Detector Control System (DCS)**

A set of specification which are missing at the moment (and which this workshop could contribute to define) is related to the need of providing the BES-III Detector Control System (DCS) with:

- the resources to control the configuration of the GEM detector readout electronics (i.e. ASIC's settings for comparator threshold, masks, operating modes,…)
- the resources to monitor relevant detector status informations (i.e. ASICs status informations, temperatures, current consumptions,..) in order to determine whether the detector is ready for data taking
- diagnostic resources for commissioning and calibration purposes (test pulse generation and acquisition, for instance)

Such resources must be planned in the design of the off-detector DAQ system at this stage.

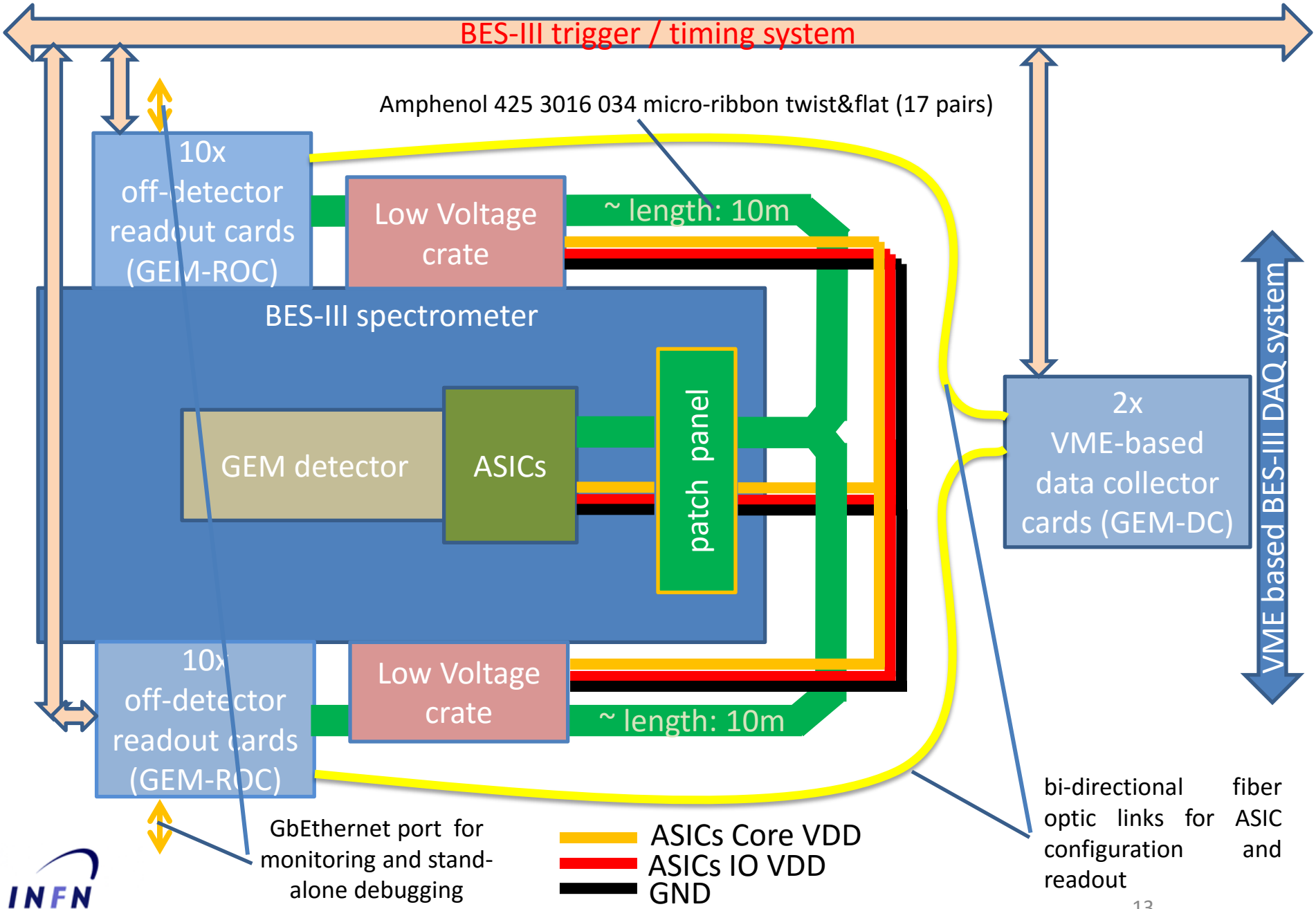
- **Specifications of the interface between the GEM DAQ system and the BES-III Run Control System:**

A set of specification which are missing at the moment (and which this workshop could contribute to define) is related to the need of providing the BES-III Run Control System with:

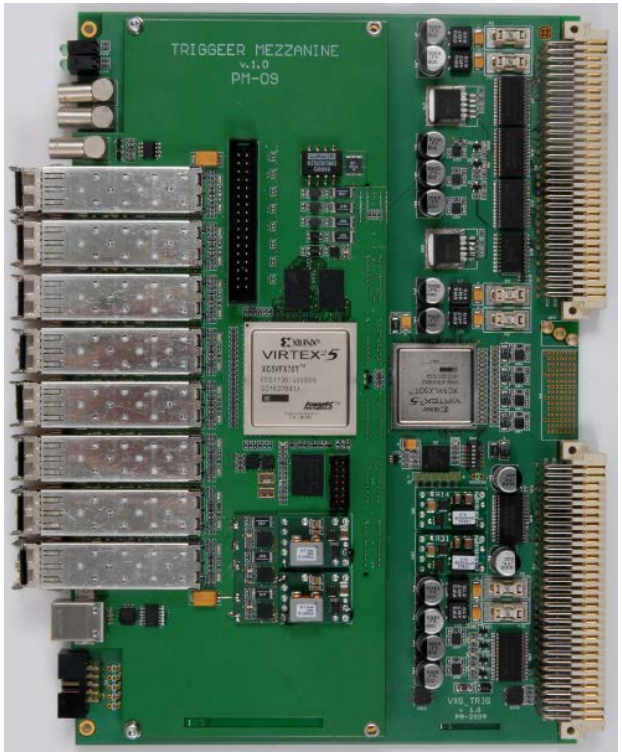
- information on whether or not the GEM detector and its associated electronics are ready for data taking
- information about critical conditions of the GEM detector and its readout electronics which would require pausing the trigger from the experiment or stopping of the run

The resources needed for the implementation of such exchange of informations must be planned in the design of the off-detector DAQ system at this stage.

- **Current design baseline for the off-detector electronics: proposed system layout**



- **Current design baseline for the off-detector electronics: VME-based data collector (GEM-DC)**



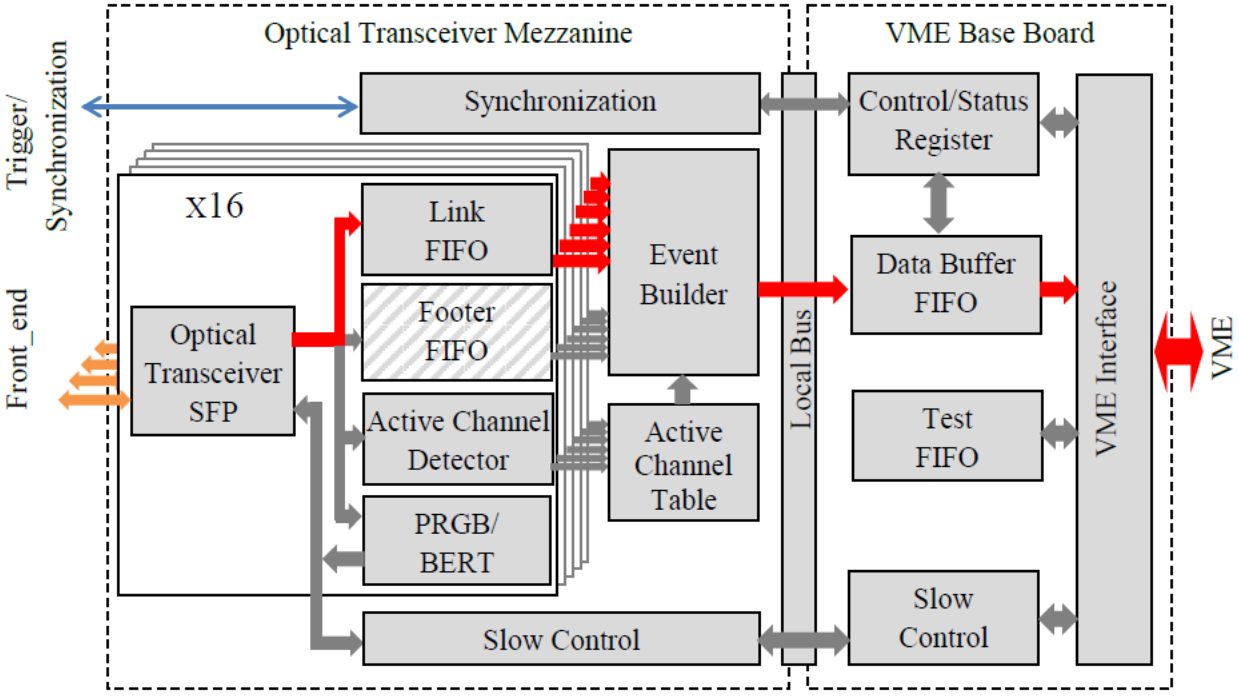


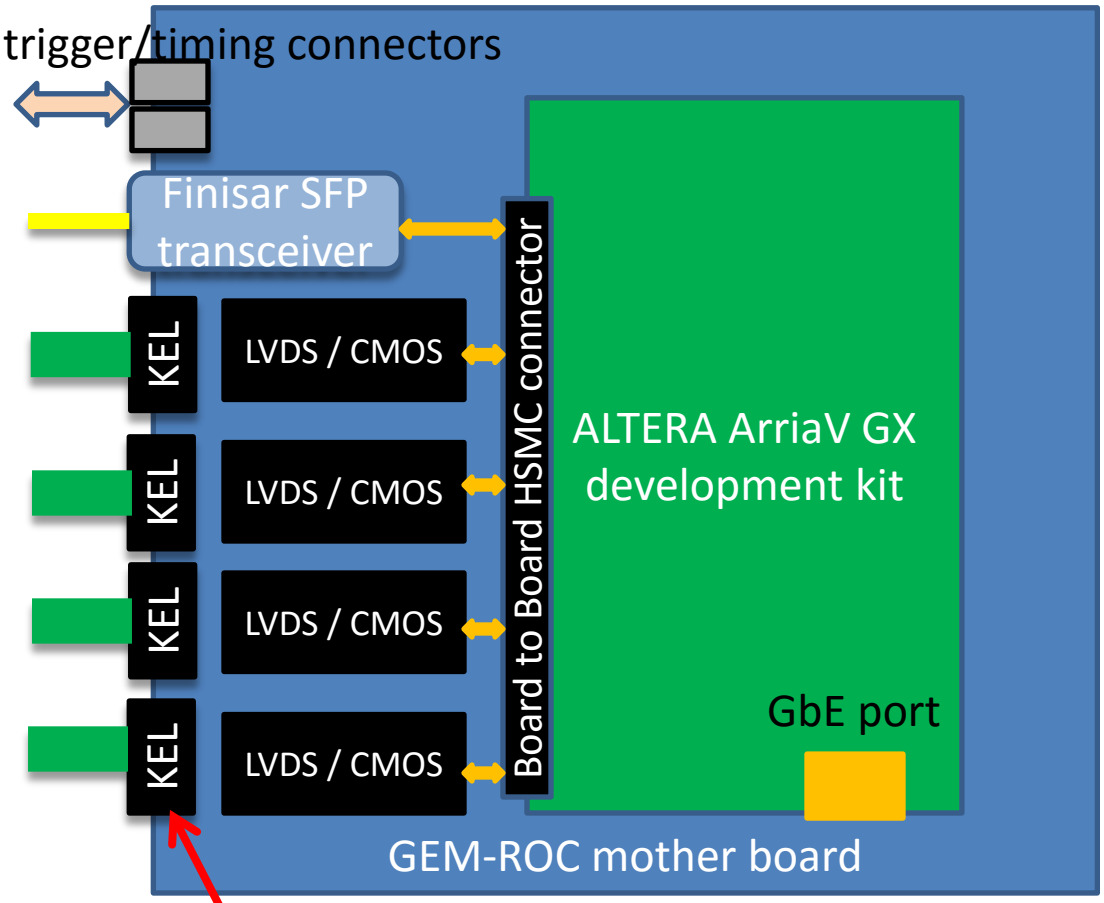
Figure 4. ATLB/Data Collector. Functional Diagram

(picture and description from ATLB/Data Collector documentation by Pawel Marciniewski)

The Optical Transceiver mezzanine receives data from up to 16 front-end devices over optical links running at 2 Gbit/s and stores the data in individual 16kB Link FIFOs. The optical data links as well as the most of the system are 32-bit word oriented. In the Event Builder module the received data are time sorted, framed and send over the Local Bus to the Data FIFO on the VME Base board. During the process of data receiving and sorting a number of data consistency checks is performed to detect errors in the DAQ at the earliest possible stage. Depending on the experiment, different data sorting algorithms are used.

The Data Collector (GEM-DC) is described in detail in Pawel Marciniewski's talk

- **Current design baseline for the off-detector electronics: off-detector readout card (GEM-ROC) prototype**

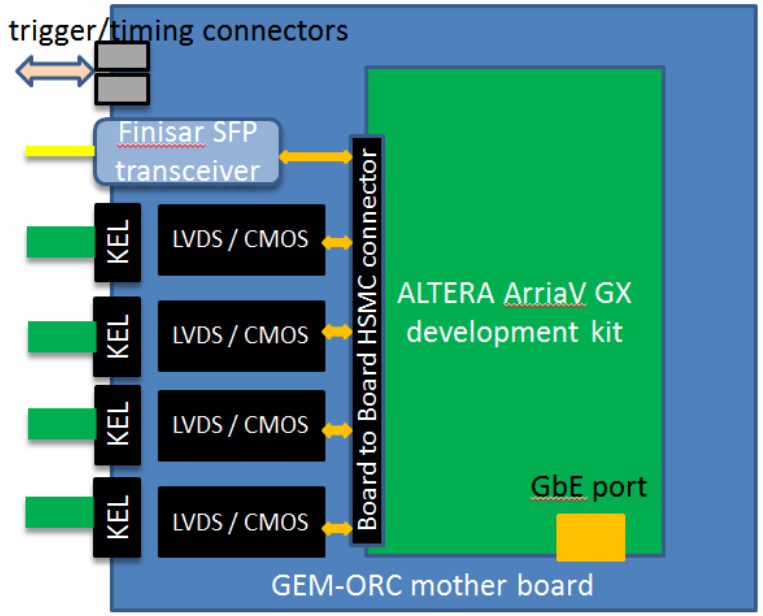


Each board handles 4 ASIC PCBs <-> 8 ASICs
A first prototype will be based on an ALTERA development board for an ArriaVGX FPGA coupled to the motherboard through an HSMC high performance connector.
The motherboard provides the electrical and physical interfaces to the ASIC carrier PCBs and to the data collector.
The format of the GEM-ROC will probably be a double width 6U VME. 10 board will be hosted in a crate

from the KEL web page: http://www.kel.jp the KEL connectors are available

No.	Contact	Catalog	Part Number	Description	Status	RoHS
1			8831E-034-170LD-F	1.27mm Pitch, 2 piece, IDC for 0.635mm FC Connector, Plug (PCB side Connector), With hooks, 0.25µm min. Gold plating, Right angle, 34 pin	Active	RoHS Compliant
2			8831E-034-170LD	1.27mm Pitch, 2 piece, IDC for 0.635mm FC Connector, Plug (PCB side Connector), With hooks, 0.25µm min. Gold plating, Right angle, 34 pin, Replacement: 8831E-034-170LD-F	Obsolete	Non RoHS

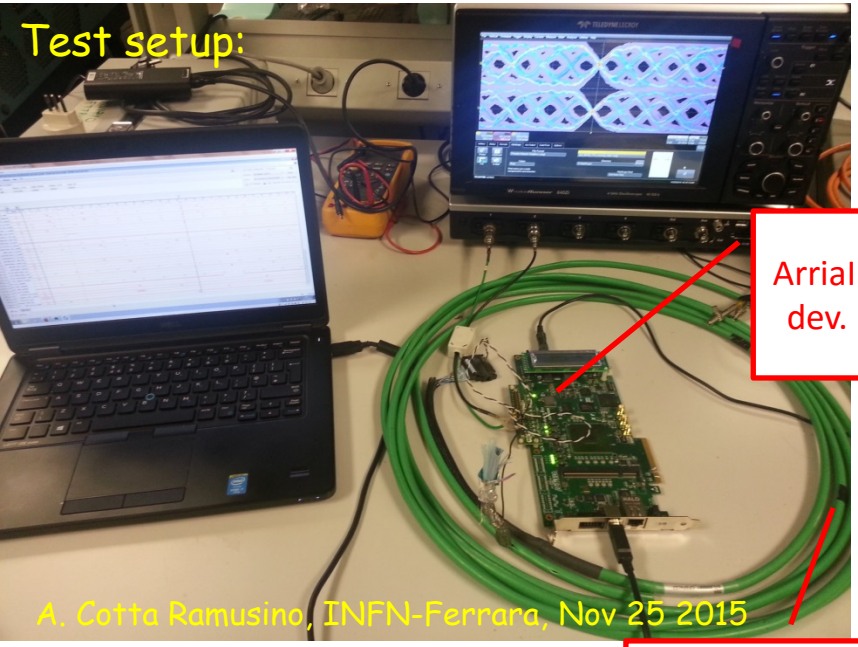
- **Current design baseline for the off-detector electronics: off-detector readout card (GEM-ROC) prototype**



A preliminary signal assignment to the cable seems to confirm that a 17 pair signal cable is sufficient:

- pair 3..0: 4 LVDS outputs (most likely only 2 will be used) from ASIC 0 of the front end PCB
- pair 7..4: 4 LVDS outputs (most likely only 2 will be used) from ASIC 1 of the front end PCB
- pair 8: 1 LVDS output synchronous clock from ASIC 0
- pair 9: 1 LVDS output synchronous clock from ASIC 1
- pair 10: 1 LVDS reference clk to both ASICs (fanout on board?)
- pair 11: 1 LVDS reference reset to both ASICs (fanout on board?)
- pair 12: 1 LVDS serial configuration clock to both ASICs (fanout on board?)
- pair 14..13: 2 LVDS pairs Serial Data OUT, Serial data IN for ASIC 0
- pair 16..15: 2 LVDS pairs Serial Data OUT, Serial data IN for ASIC 1

- **Current design baseline for the off-detector electronics: prototyping**
  - transmission of 8b/10b encoded data at 160MHz over candidate cable



Test conditions:

- Signal cable: 17 pairs Amphenol 425 3016 034 micro-ribbon twist&flat
- Test signal: stream of 8b/10b encoded bytes comprising idle (K-code) and data (D-code) characters generated by an FPGA
- Signaling level: LVDS
- **Error detections: the FPGA receives and checks all 8-bit characters looped back through the cable**

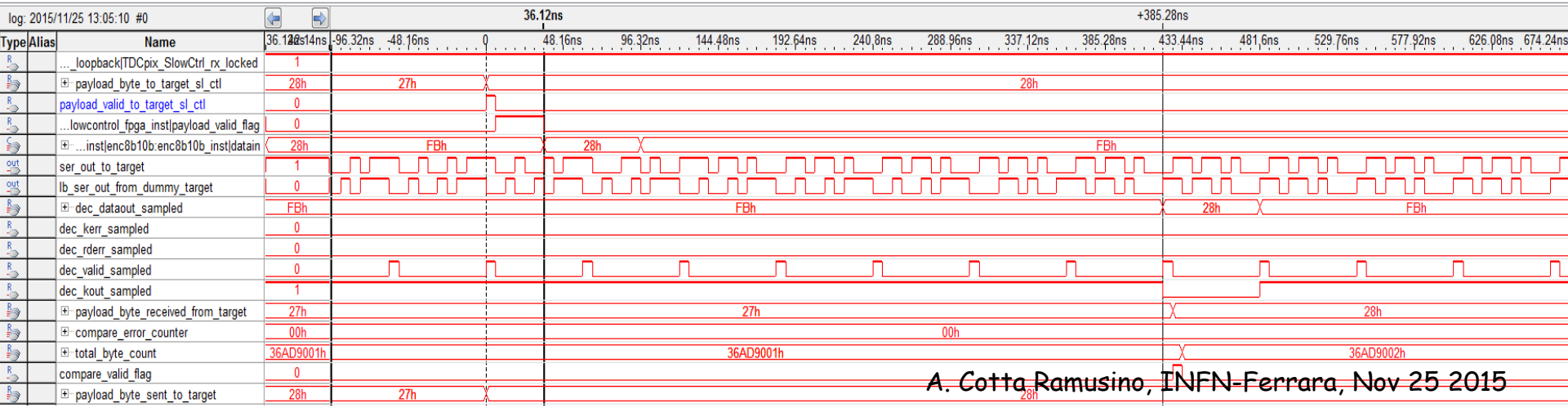
Test goal:

- Determining the effect of cable losses on the link reliability

TEST RESULTS:

- A real 8b/10b encoded LVDS signal has been transmitted over a candidate signal cable up to 17m in length @166Mbps
- No errors were detected after transferring at least 4.3 billion "payload" byte
- Taking also the idle characters into account one can estimate a bit error rate lower than 1 in 0.5 10^{12} at the length of 17m

- **Current design baseline for the off-detector electronics: prototyping**
  - transmission of 8b/10b encoded data at 160MHz over candidate cable

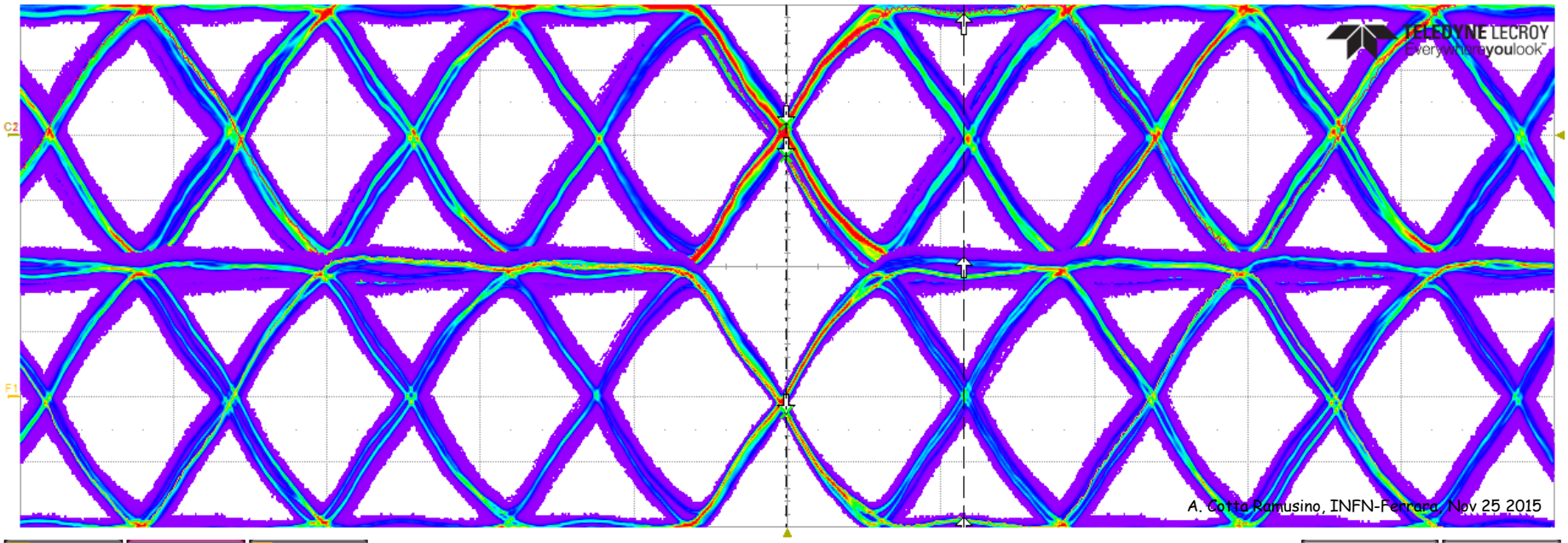


The screenshot shows the activity of a few signals inside the FPGA:

- The FPGA checks for errors in the received 8b/10b encoded symbols an sets the **dec_kerr_sampled** and the **dec_rderr_sampled** in case any K-code or running disparity error is found
- The **total_byte_count** is the total number of data byte transmitted (not counting idle characters)
- The **compare_error_counter** is incremented every time the received echoed data byte is different from the sent one

During the test a total of at least $2^{32} \approx 4.3\ 10^9$ byte are sent.
The test takes about 1 hour to complete.

- **Current design baseline for the off-detector electronics: prototyping**
  - transmission of 8b/10b encoded data at 160MHz over candidate cable

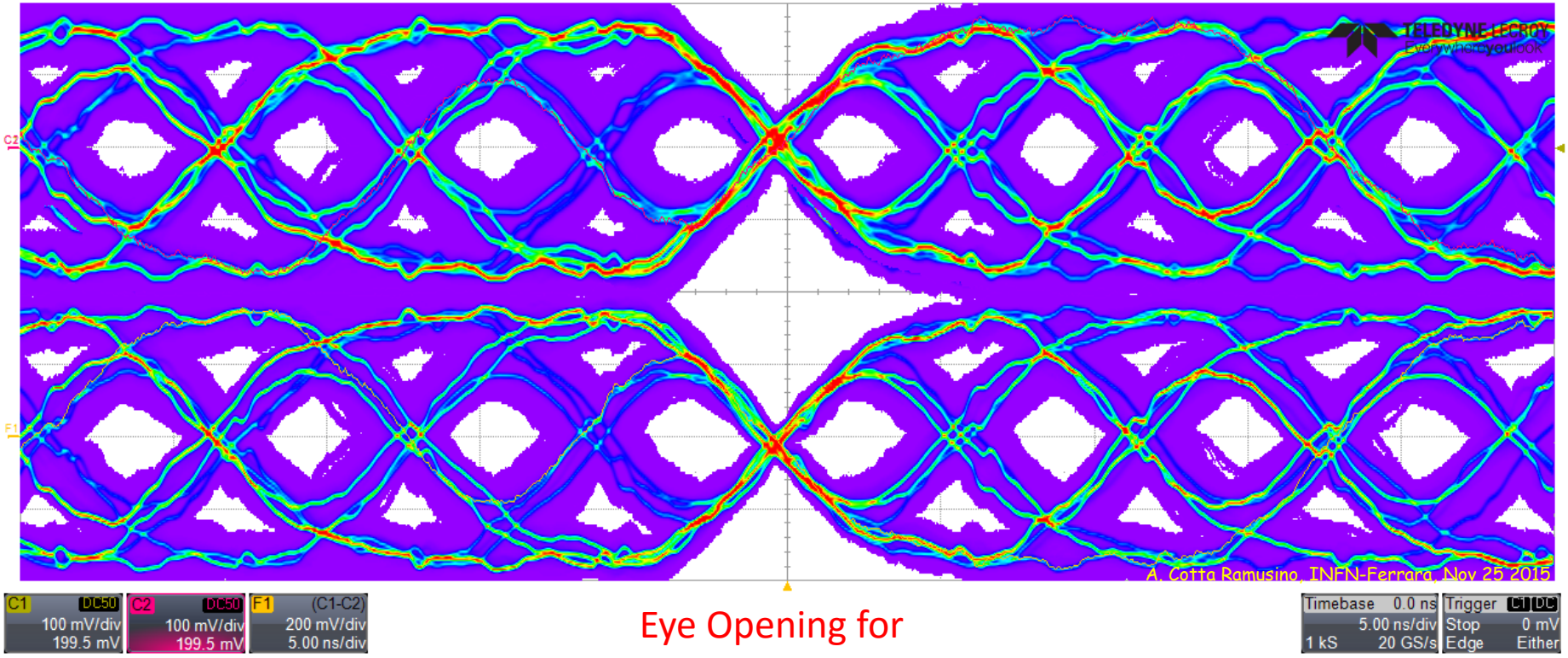


Eye Opening for
Cable length: 8.5m

Test conditions:
The signals above are picked up at the input of the link controller with 100nF coupling capacitors and sent to ch1 and ch2. The 50 input terminations of the scope channels act as differential termination of the cable under test

No errors were observed after a total of at least $2^{32} \approx 4.3\ 10^9$ data byte were sent (not including the idle characters which are also checked by the 10b/8b decoder)

- **Current design baseline for the off-detector electronics: prototyping**
  - transmission of 8b/10b encoded data at 160MHz over candidate cable



Eye Opening for
Cable length: 17m

Test conditions:

The signals above are picked up at the input of the link controller with 100nF coupling capacitors and sent to ch1 and ch2. The 50 input terminations of the scope channels act as differential termination of the cable under test

No errors were observed after a total of at least $2^{32} \approx 4.3\ 10^9$ data byte were sent (not including the idle characters which are also checked by the 10b/8b decoder)

- **Current design baseline for the off-detector electronics: prototyping**
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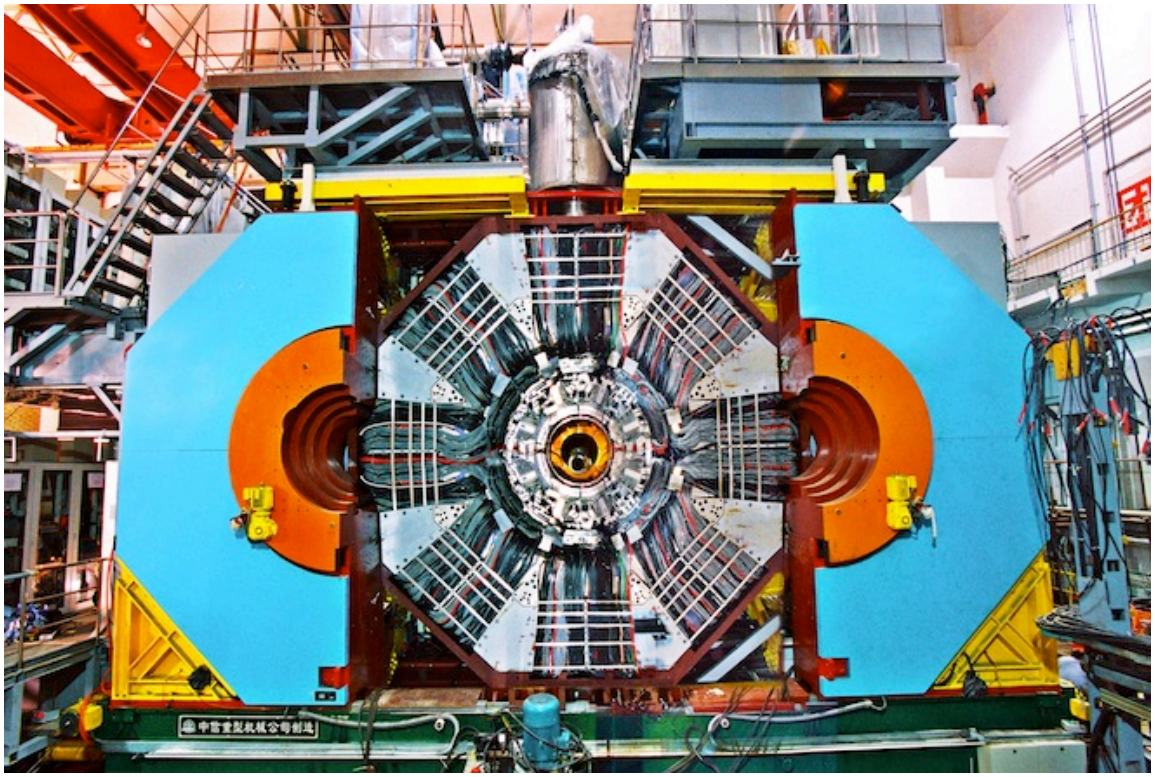
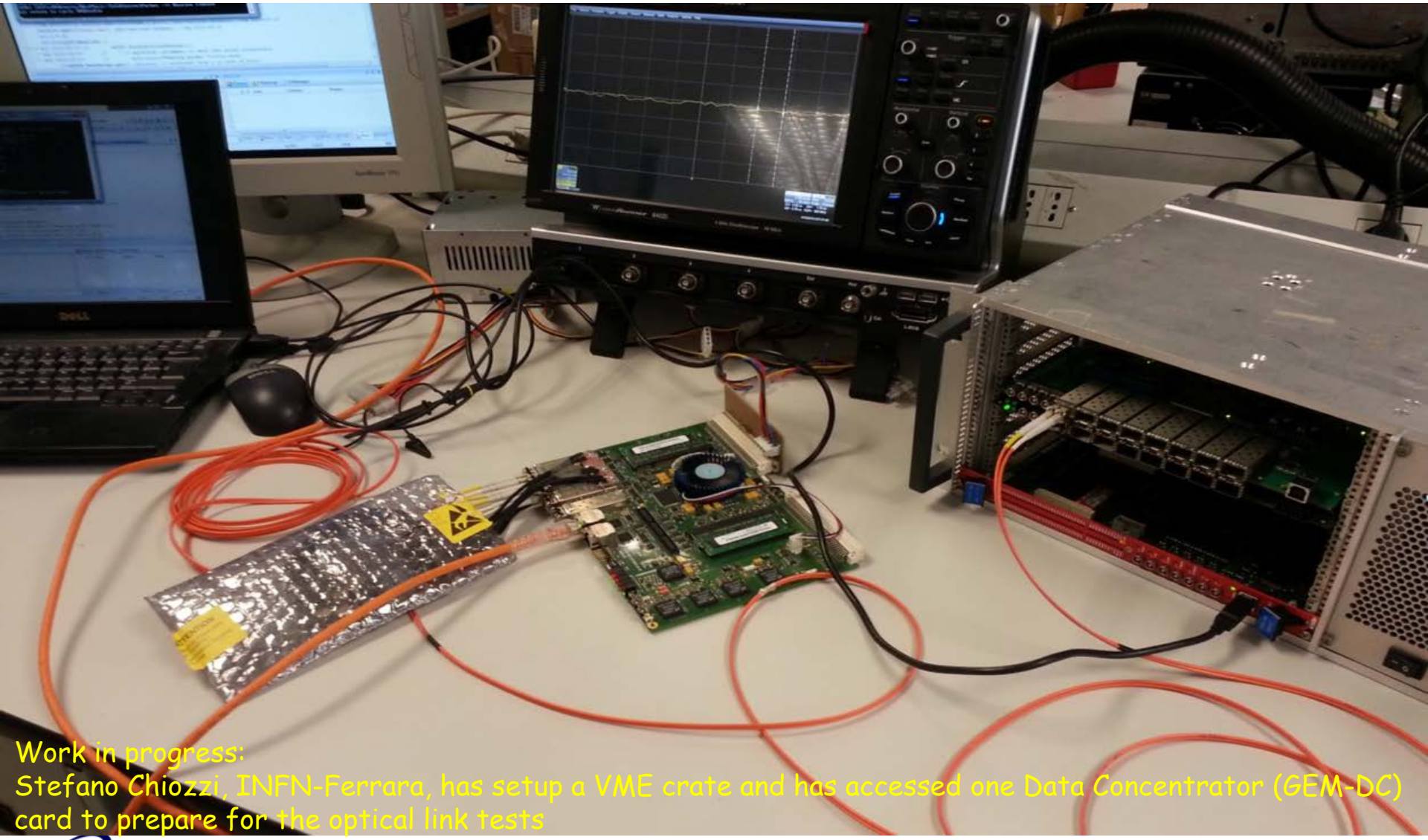


While no errors were observed even with the 17m long cable @166MHz, it would probably be better to reduce the length of the signal cables between the ASICs and the GEM-ROC cards.

Could the BES-III organization consider the proposal of installing the 2 GEM-ROC crates (and possibly also the LV ones) on new small platforms located as close as possible to the detector?

- **Current design baseline for the off-detector electronics: prototyping**
  - transmission of 8b/10b encoded data at 2Gbps



Work in progress:
Stefano Chiozzi, INFN-Ferrara, has setup a VME crate and has accessed one Data Concentrator (GEM-DC) card to prepare for the optical link tests

- **Current design baseline for the off-detector electronics: prototyping**
  - Review of estimated data rate of raw and trigger matched data

A first attempt at the data rate estimates presented was the outcome of the:

"Technical meeting on off-detector readout electronics"

held at LNF on Nov. 17 2015 and attended by Giulietto Felici (convener), Michela Greco, Pawel Marciniewski and the writer.

The results have now been updated after further interactions with the ASIC designers and the analysis of the ASICs simulation results.

An estimation of the GEM detector rate per channel was presented in the CDR document.

Applying the safety factor suggested by Gigi Cibinetto, **the peak rate per channel in layer 1 is expected to be ~60kHz / channel.**

An average rate of 25kHz is considered in the following while evaluating the GEM detector event size and readout data bandwidth.

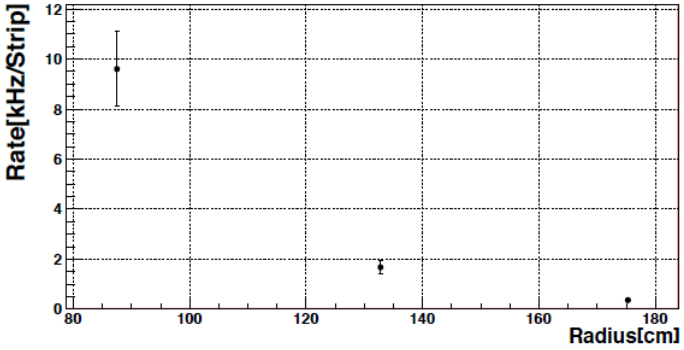


Figure 1.7: Expected average rate per X-strip on the CGEM-IT as function the radius.

- **Current design baseline for the off-detector electronics: estimated raw data rate**

Assumptions (UPDATED for TOPFET2):
- "hits" encoded in 8Byte (80bit after 8b/10b encoding)
- serial link speed 200MHz → 20MB/s of 10b encoded data Byte (it was assumed 160MHz for TOPFET)
- 4 links per ASIC
- **Physics and Noise rate expected per channel (average): 25kHit/s**

Results (neglecting the overhead introduced by the framing words):
- Time to transmit 1 hit over the serial links: 100ns
- **REALISTIC hit rate** for the **ASIC @ 25kHit/s (physics+noise) per channel:**
  1.6MHit/s per ASIC
- **MAXIMUM hit rate** allowed by the serial output links of the **ASIC**: 4x(20MB/s 10b encoded) -> 4x(2.5MHit/s) ->
  10MHit/s per ASIC equivalent to ~156kHz MAX HIT RATE PER CHANNEL

NOTE: the expected hit rate per channel is much lower than the MAX HIT RATE PER CHANNEL figure ->

Note: there should be no pile up at the transmitting stage of the ASIC
- Hits are NOT time ordered! The off-detector FPGA has to sort them out before trigger matching

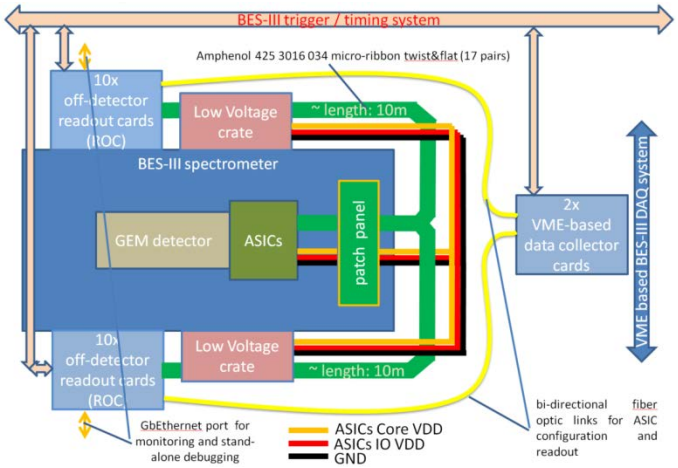
- **Current design baseline for the off-detector electronics: estimated TRIGGER MATCHED data rate**

Assumptions:
- **trigger rate: 4kHz**
- **trigger matching window: 1us**
- **Physics and Noise rate expected per channel (average): 25kHit/s per channel**
- the packets sent by the GEM-ROC card to the GEM-DC with trigger matched data are enclosed between an header and a trailer word, 8Byte each

Results (neglecting the overhead introduced by the Header/Trailer words of the trigger matched packets):
- **REALISTIC trigger matched data bandwidth for the entire GEM detector (ASSUMING 25kHz/channel)**: 1us * 1.6MHit/s * 160 ASICs * 4kHz =
  ~1MHits/s (Trigger Matched) → 8MB/s
  realistic estimate of event size for the GEM detector: ~2kB

- **MAXIMUM** trigger matched data bandwidth for the entire GEM detector **allowed by the ASICs' serial output bandwidth**: 1us * 10MHit/s * 160 ASICs * 4kHz =
  ~6.4MHits/s (Trigger Matched) → 51.2MB/s

preliminary proposals for data format and system layout: **estimation of size of circular data buffers for trigger matching on board of the off-detector readout card (GEM-ROC)**



Assumptions:
- system built according to the baseline design
- a GEM-ROC receives raw data from the ASICs through 4x LVDS links @200MHz
- a GEM-ROC communicates with the VME-based Data Collectors (GEM-DC) through optical links @2GHz; these are bi-directional communication channels, also used for ASIC configuration/monitoring
- 8 ASICs (= 4 CARRIER PCBs) connected to each GEM-ROC
- **L1 trigger latency = 6.5 ÷ 8us** (source: Giulietto)
- **interval between two consecutive L1 trigger requests ≥ 8us** (source: Alessandro Calcaterra)

Results:
- hit data from ASICs (up to 4MB/s) are stored on circular memory buffers in the GEM-ROC FPGA pending L1 trigger request
- assuming realistic data rate from ASIC = 1.6MHit/s -> 13Hit for an 8us L1 latency interval
- assuming max data rate from ASIC = 10MHit/s -> 80Hit for an 8us L1 latency interval
- as pointed out by Pawel we should consider the (stochastic) latency of transmission of a hit across the serial data links: one hit is transmitted in 100ns and the ASIC transmitter is shared by 64 channels -> assuming round robin processing of the channels, the latency of transmission of a channel's hit could be no less than 6.4us if the ASIC's channel occupancy is 100% -> the hit transmission latency could be of the order of the L1 trigger and this must be taken into account while designing the trigger matching logic!!

  -> all of the above taken into account, it appears that the circular buffers (size in the order of ~ 128 locations per ASIC) for data pending the trigger matching could be easily implemented with internal resources of the GEM-ROC FPGA

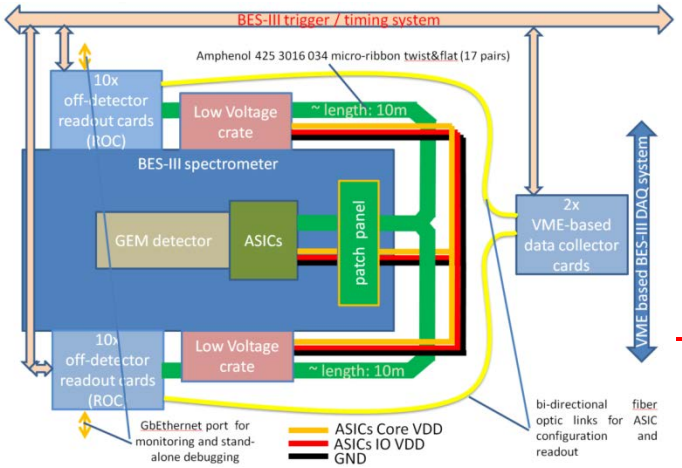
continues…

preliminary proposals for data format and system layout: **estimation of size of circular data buffers for trigger matching on board of the off-detector readout card (GEM-ROC)**

… continuing:

Assumptions:

- one GEM-ROC is connected to the GEM-DC via one optical link @2GHz
- the GEM-ROC is connected to BES-III trigger and timing network and it could generate a FULL signal to the BES-III DAQ (if it foresees such a mechanism) when it receives a back-pressure signals from the GEM-DC (through the slow control optical link)
- **Physics and Noise rate expected per channel (average):** 25kHit/s



- **the trigger matched packet is framed by**:
  - one 64 bit (2 * 32bit word) **HEADER WORD** containing:
    - ASIC_ID (relative to the board, 3 bit)
    - event number (8 bit)
    - event wordcount (6 bit)
    - L1 trigger timestamp with BES-III clock resolution (#bit to be determined)
    - status flags (#bit to be determined)
  - one 64 bit (2 * 32bit word) **TRAILER WORD** containing:
    - ASIC_ID (relative to the board, 3 bit)
    - event number (8 bit)
    - L1 trigger timestamp extension (#bit to be determined)
    - status flags (#bit to be determined)
    - CRC-32

the 64-bit HEADER, TRAILER and DATA word are formatted into 2 consecutive 32bit words whose bit 31 is (it helps the GEM-DC data processing): 1 for header and trailer / 0 for data words

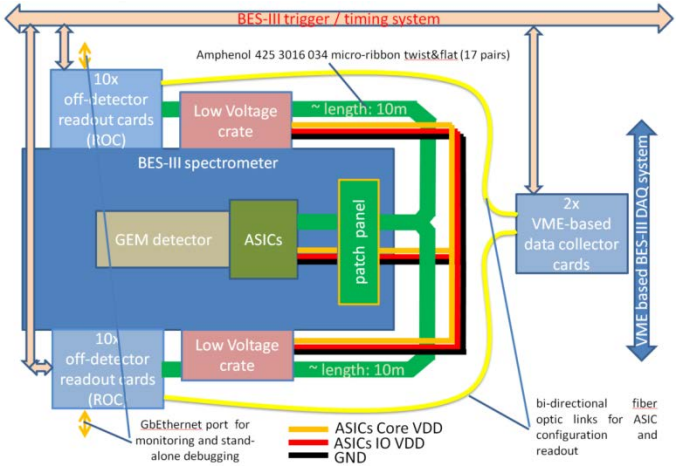
Results:

- each ASIC contributes in average: 1us * 1,6MHit/s = ~2Hit/trigger packet -> Header and Trailer overhead not negligible!
- data bandwidth on the optical link: (8B(header)+8B(trailer)+16B(2 hits))*8(ASICs)*4kHz =~1MB/s -> much lower than the optical link would allow! OK!!!

preliminary proposals for data format and system layout: **estimation of triggerless readout bandwidth over ethernet supported by the GEM-ROC in stand alone mode**

Assumptions:

- **the ROC is equipped with a GbE interface for standalone readout during system debugging**
- the maximum raw bandwidth of a GbE link is 125MB/s
- any protocol needed to transport user data from source and destination nodes in a network will introduce an overhead and reduce the net user bandwidth
- **the triggerless mode is a debug / standalone operating mode and some on the maximum allowed rate per ASIC or on the number of ASICs monitored concurrently is accepted**
- **Physics and Noise rate expected per channel (average): 25kHit/s**



Results:

- 8 ASICs produce a **realistic** aggregated data rate of 8 * 1,6MHit/s = **102,4MB/s**
  → barely compatible with the GbE bandwidth if UDP protocol is implemented.

  Stefano Chiozzi, INFN-Ferrara, has developed an Ethernet MAC (for the StratixIV FPGA used in the NA62 GTK readout and L0TP systems) which could, if the UDP payload is properly filled, provide enough banadwith to read the 8 ASICs. Otherwise either a subset of the ASICs could be selected to be monitored or the entire subset of ASICs could be multiplexed to the monitoring PC.

- **Open questions on specifications:**

- Values of L1 trigger latency and trigger matching window?

- Value of minimum time interval between 2 consecutive L1 triggers (i.e. does the trigger matching processing have to be pipelined or a new L1 trigger comes only after the previous trigger matched event is readout)?

- Is there a maximum allowed time for trigger matching processing (i.e. from the L1 pulse to the event buffer ready flag)?

- Are the GEM detector event size and data bandwidth compatible with the BES-III readout bandwidth?

- What are the physical standards (signaling levels, connector pinout) for the timing and L1 trigger signals?

(We need documentation on the components of the Fast Control and Clock system distribution delivered at the VME crates for the MDC described in yesterday's presentations by the IHEP collaborators)

- Are specifications available for the interface of the GEM readout and the GEM-LV systems to the BES-III Detector Control System (slide 11)?

- Are specifications available for the interface to the BES-III Run Control System (slide 12)?

- Will BES-III provides the VME CPUs to readout the GEM-DC?

- Will BES-III take care of the on-line software needed to operate the VME based Data Collectors?

- What would be the closest possible installation location for the GEM-ROC crates?

- What information is available on the radiation background in the experimental hall where the off-detector readout would be installed?

■ : answered by yesterday's presentations and discussions