# AMchip06 status

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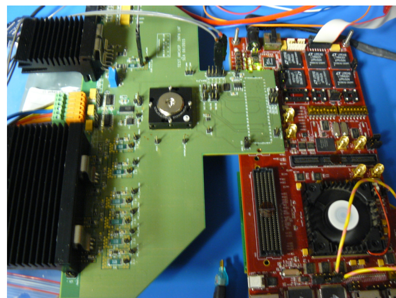
AM06-1552
PGT864.00
TSS

Test benches at LPNHE,
INFN Milano
and soon INFN Frascati

# AMchip06 Tests

- Internal fast self-test of the pattern bank
  - 50 chip tested
  - 8 chip with local defects (few localized patterns out of 128k not working)
  - 0 chip with severe defects (i.e. short circuit, non working IOs)
- "Run" mode testing
  - Power supply stability issues on the testbench
  - Zero errors run with 1.15 V, but not at target 1 V
  - Tests ongoing!



# Internal self-test

1. Program the bank with data `1<<((i+j+k)%18)` where i is a loop index, j is the pattern index and k bus index every 64 pattern location (i.e. pattern0 = pattern64 = pattern128 = ...,pattern1 = pattern64 = pattern127 = ..., ...)
2. Set the chip to threshold 1
3. Send data `1<<m` on all buses, where m is a loop index
4. Send init and wait for all matched patterns to go through the output
5. Increase m and go to step 2 until m = 18
6. Increase i and go to step 1 until i = 18
7. Check the CRC32 value of the stream of data that went through the output

# Internal self-test

- The internal self-test is able to detect single-bit defects
  - If a bit doesn't match when stimulated or always match it will alter the patter sequence in output
  - CRC32 will not match the pre-computed one
- This test is programmable: we can test any range of patterns in the bank multiple of 64 (i.e. the whole chip, patterns 64 to 1024, ...)
- Testing the whole chip is < 1 sec

# "Run" mode test

1. Generate a bank with random data and load into the chip
2. Generate random hit data (current FW limits to 32k hits per bus)
3. Given a fixed event length divisor of 16k (hits are always paired) compute the expected list of patterns per event given a certain threshold
   - There is the possibility to take into account OPCODE threshold lowering. Not used in current tests.
4. Load the predicted pattern list to the FPGA
5. Start looping events at full speed
6. The FPGA compares the output of the AM06 with the predicted list
7. After a certain time we stop and check for errors, then repeat from step 2
8. After a certain number of iteration we go to step 1 to change bank

# "Run" mode test

- It is a parametric test. Typical parameters used in our tests are 50x50 loops, threshold 7 / 512 hits per event when testing the whole bank, threshold 0 / 4096 hits per event when testing the first 2k
- It is a tough test for the power supply: each time the hits stream starts the VDDCore current goes from few hundreds of mA to few Amps!
- We are not able to run at 1 V with the current test bench board (caps not fast enough, not close enough)
- Tests are ongoing but at 1.15 V avg (during the test cycle the voltage goes $\pm$150 mV) I currently have 3/4 tested chips with 50x50 threshold 0 / 4k hits "run" mode test with 0 counted errors
- We noticed that if the voltage is too high (> 1.32 V) there are errors too

# Conclusions

- As of now we didn't find any serious bug in AMchip06 design
- Yield is very good!
- Power consumption and the induced voltage drop is a source of lots of troubles that somehow limits our ability to test the chip
  - We can't test the chip at low voltages (1 V and below) with tough data
- We have a voltage range around 1.15 V where everything is working very well
- These issues are mitigated on the boards (caps very close to the BGA, no socket, no elastomer "mat", BGA is soldered)
  - Preliminary tests on the LAMB shows the voltage to be within $\pm 50$ mV
- Tests and testbench board patching are ongoing!

# Conclusions II

- The AMchip06 "slow corner" meets its goal within the design voltage range (1-1.2 V)
- Needs to understand better the operational margin
- Looking forward to check "fast corner" devices