PRM for AM06

Daniel Magalotti

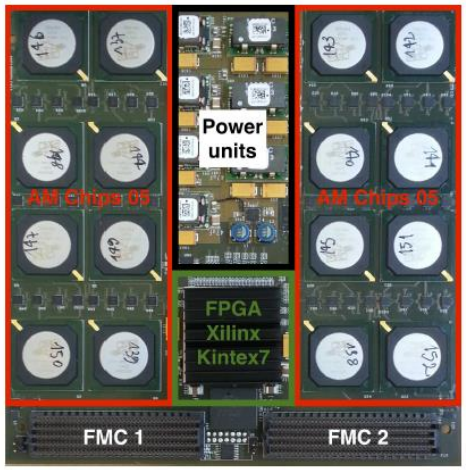
Collaboration between: KIT, INFN Pisa and INFN Perugia

Outline

- Overview of the PRM for AM05
- Comparison between PRM05 and PRM06
- Introduction of the PRM for the AM06
  - Top level schematic
  - Data logic distribution
  - Power consumption
  - Monitoring tools

PRM for AM05

Layout of the PRM for AM05



The PRM05 consist of:

- N°16 AM05 chips
- N°1 Kintex7 FPGA
- N°1 DDR2 RAM
- All the power generated onboard

The total logic resources are:

Logic blocks	Number of resources
AM Patterns	64 kpatterns
External Memory	18 Mbit
Logic Cells	356 k
Block RAM	25 Mb
DSP Slices	1444
Transceivers	24 @ 8 Gbps
I/O Pins	300

PRM for AM05

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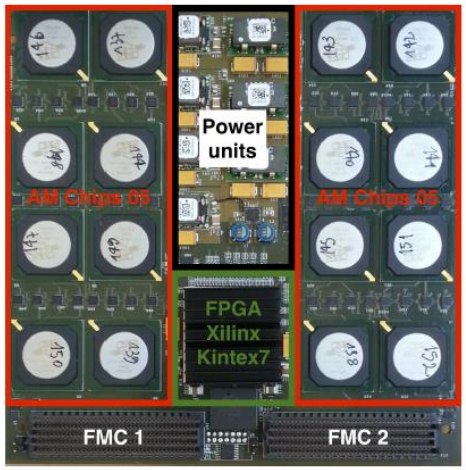

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The PRM05 is tested and firmware integration is ongoing

Moving to AM06

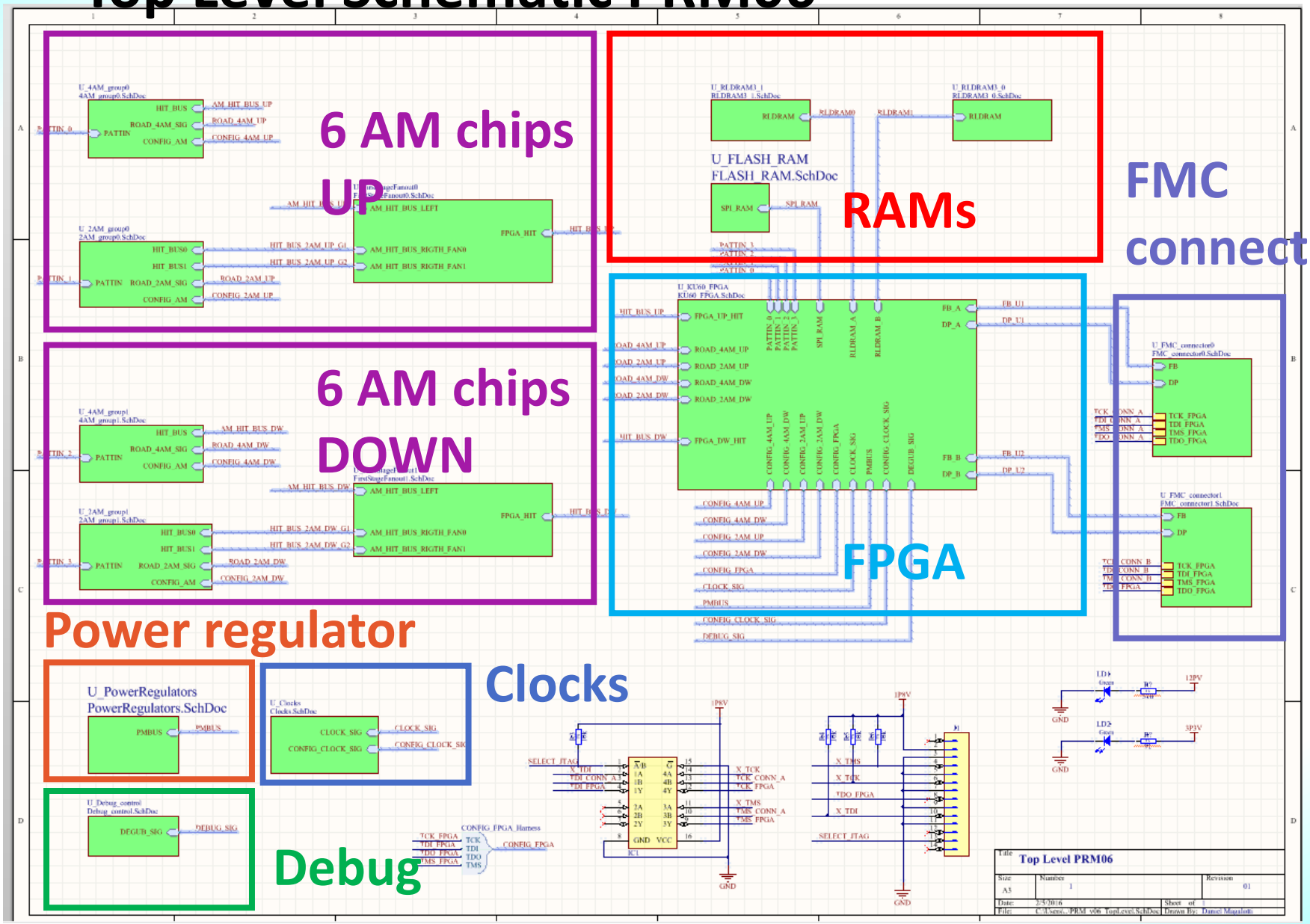
The PRM design has been changed to be interfaced with the AM06. The PRM06 consists of:

- **N°12** AM06 chips (limitated to the power consumption of the 1V)
- N°1 Kintex7 **Ultrascale** FPGA
- **N°2 RLDRAM 3 / SPI FLASH (**for fast AM pattern loading)
- **Monitoring tools**
- All the power generated onboard

A comparison between the two mezzanine:

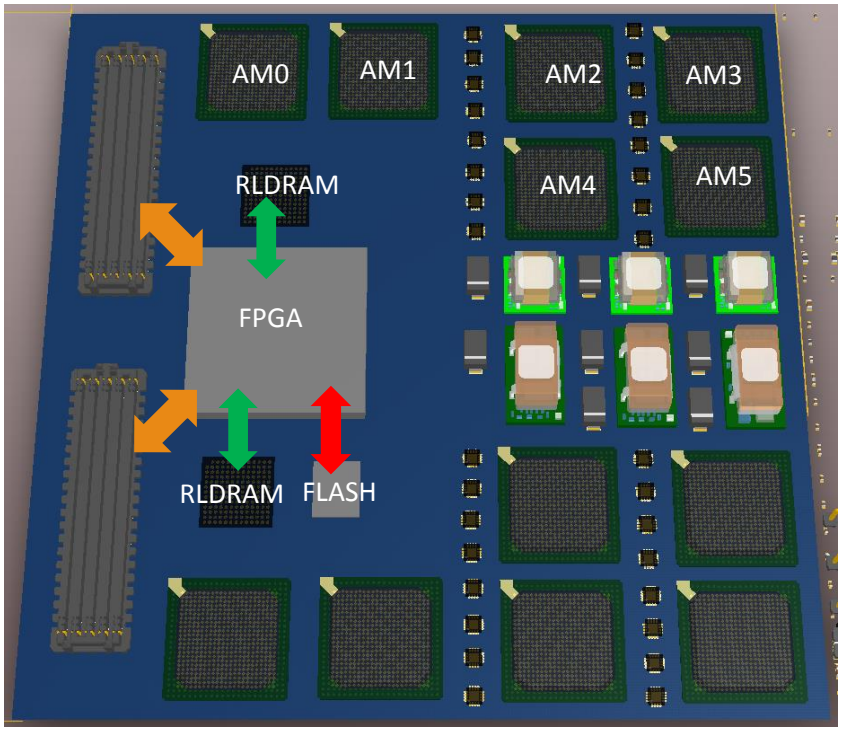
Logic blocks	Number of resources (PRM05)	Number of resources (PRM06)
AM Patterns	64 kpatterns	1,5 Mpatterns
External Memory	18 Mbit	1,1 Gbit
Logic Cells	356 k	726 k
Block RAM	25 Mb	38 Mb
DSP Slices	1444	2760
Transceivers	24 @ 8 Gbps	28 @ 10.3 Gbps
I/O Pins	300	104, 416

Top Level Schematic PRM06



First draft of the layout

- A first draft of the PRM06 layout



- Data to/from the FMC connectors
  - 8 MGT links @ 10.3 Gbps (80 Gbps)
  - 68 LVDS links @ 625 Mbps (42 Gbps)
- Dedicated buses for each RLDRAM3
- External SPI for store the AM patterns

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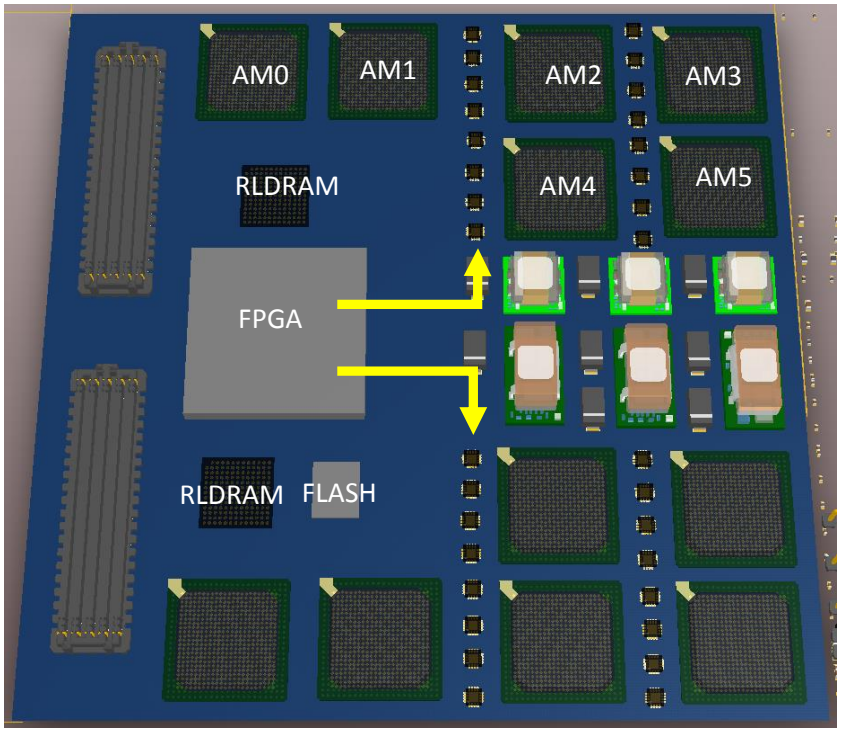
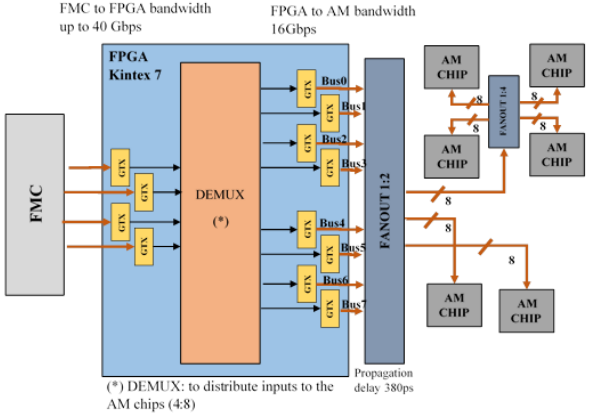


Input data flow (HIT + SSID)



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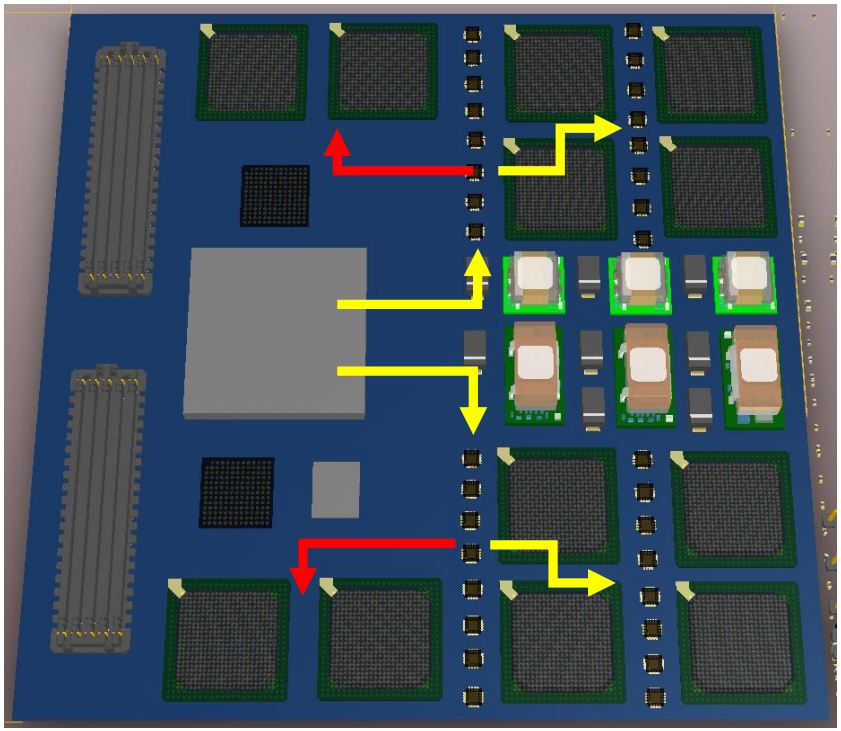

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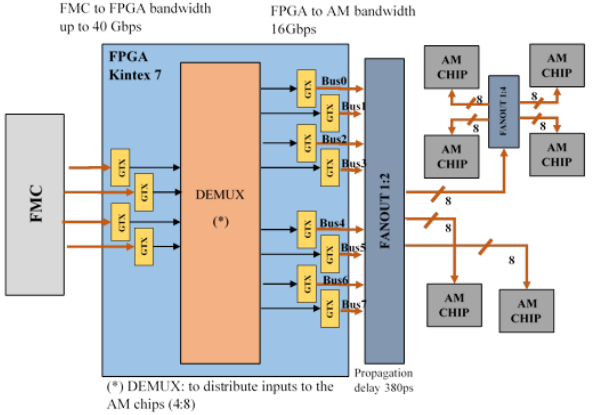

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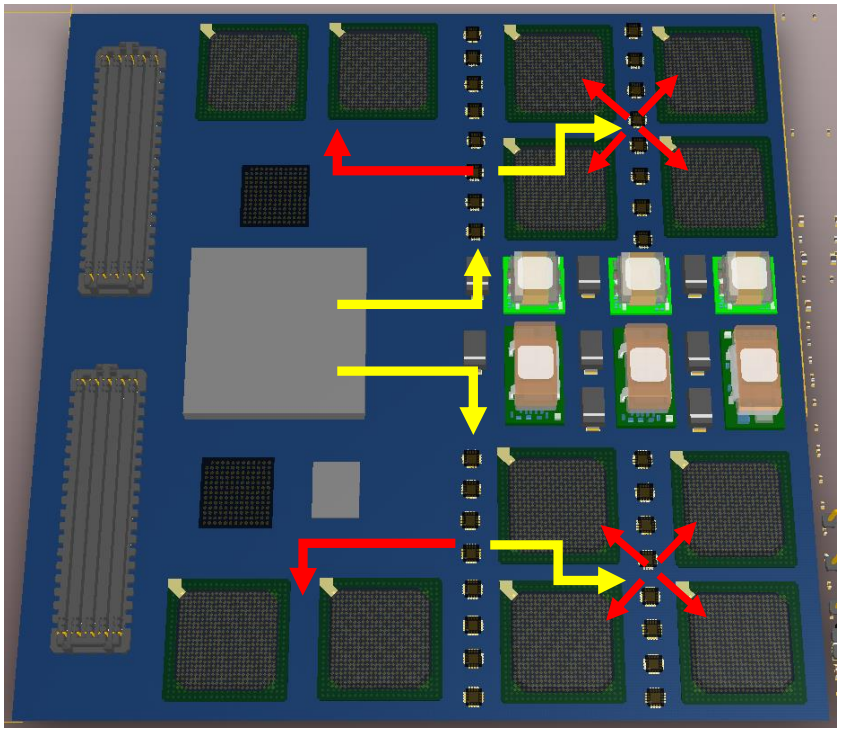

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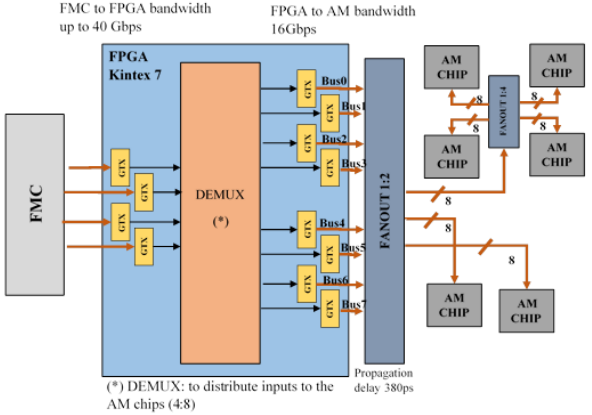

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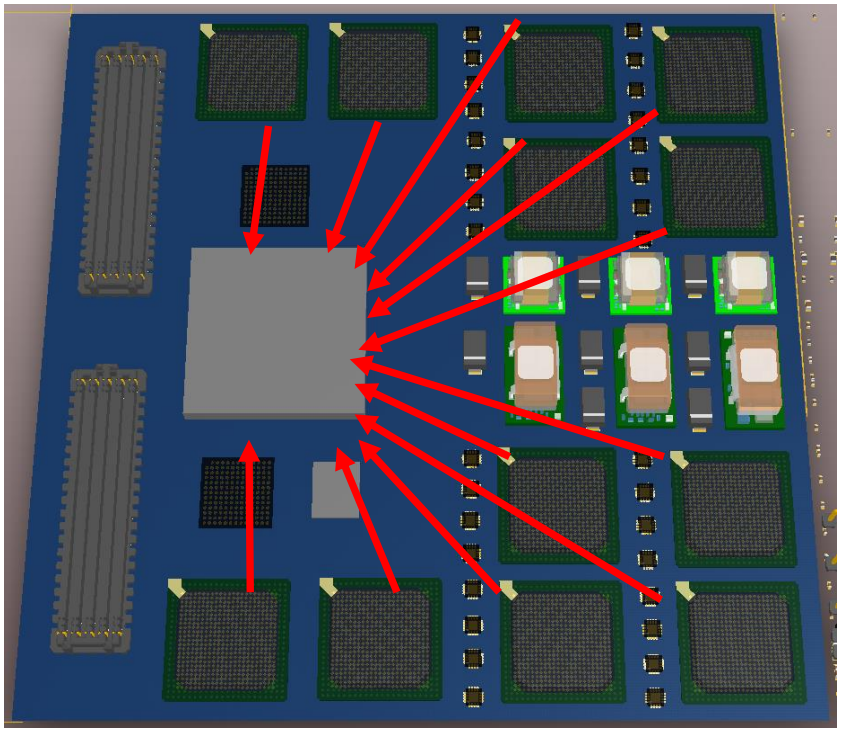
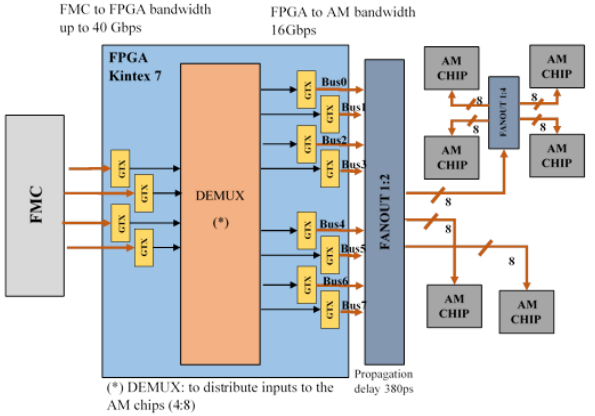
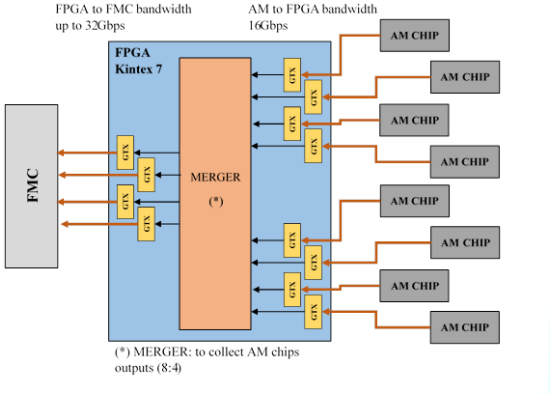


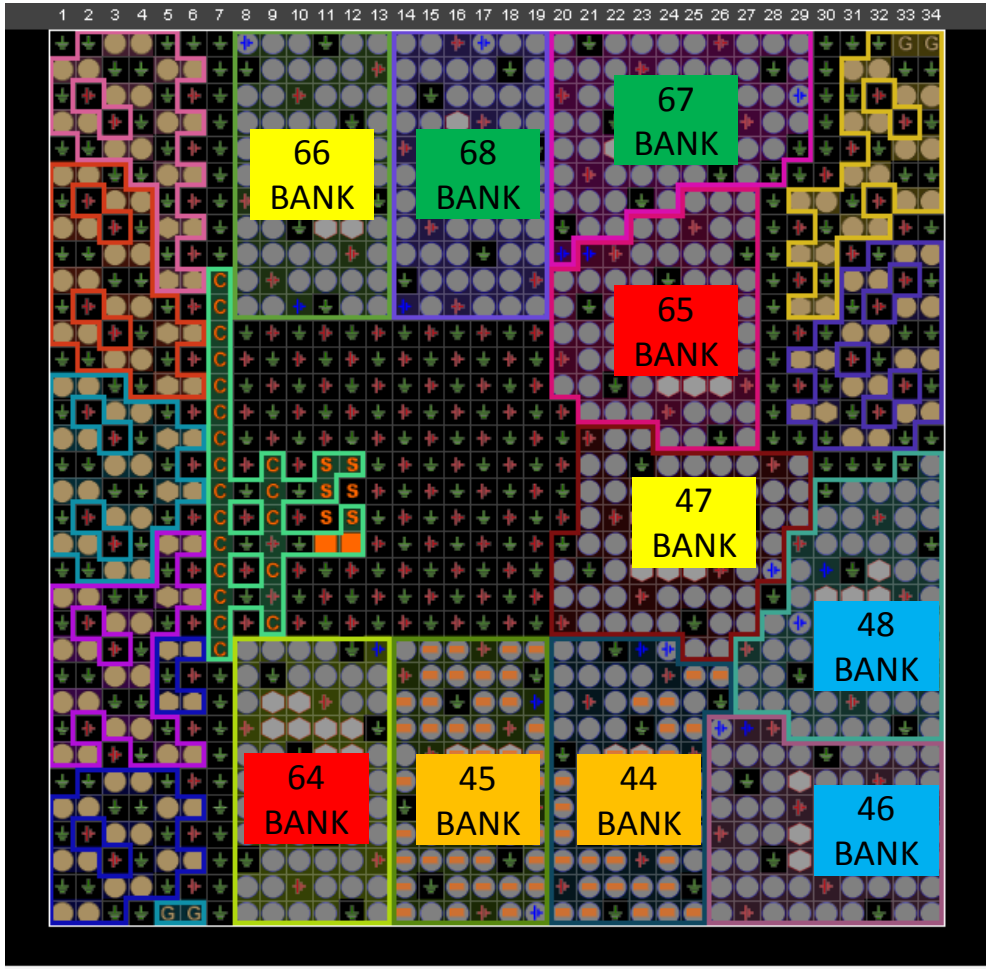
Input data flow (HIT + SSID)



Output data flow (ROAD + TRACKS)



FPGA banks pin mapping



47 BANK
66 BANK

1.8V (FMC connector)

68 BANK
67 BANK

1.2V (RLDRAM 3)

64 BANK
65 BANK

2.5V (AM and AUX)

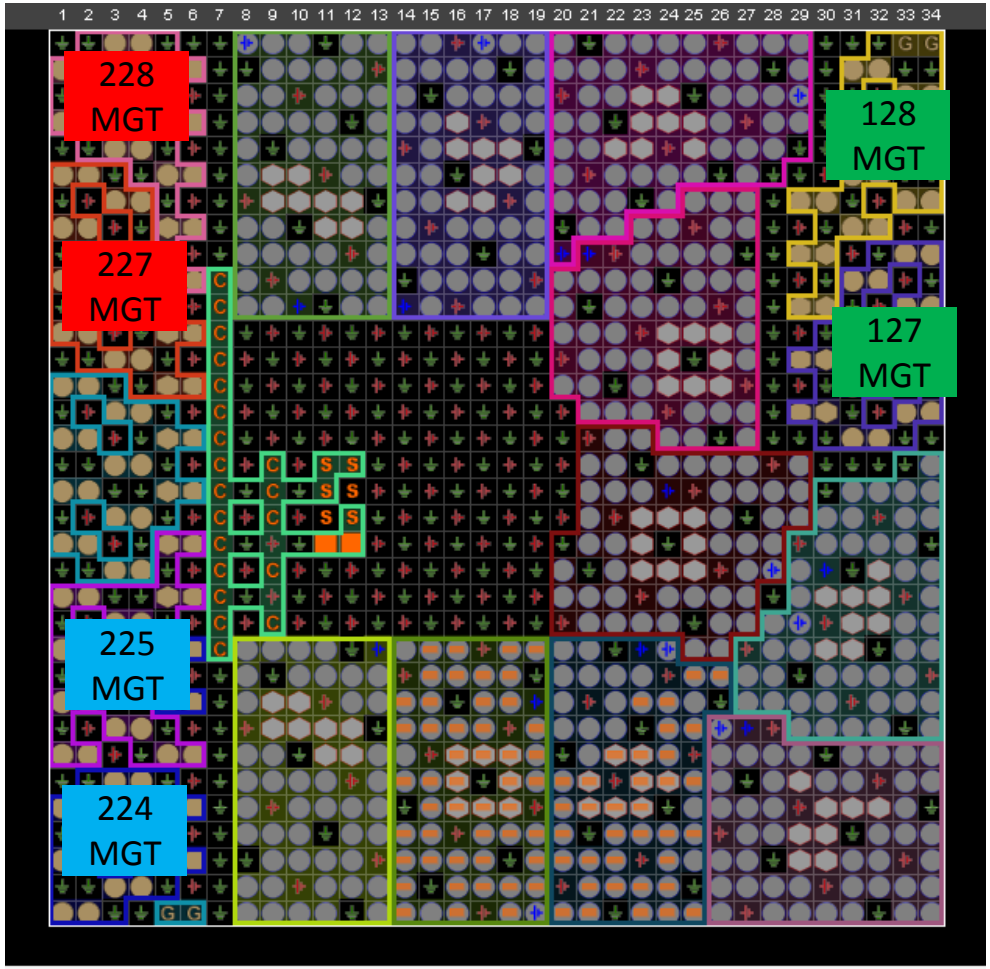
45 BANK
44 BANK

1.2V (RLDRAM 3)

48 BANK
46 BANK

1.8V (FMC connector)

FPGA banks pin mapping



228 MGT
227 MGT

2 Gbps (AM chip up)

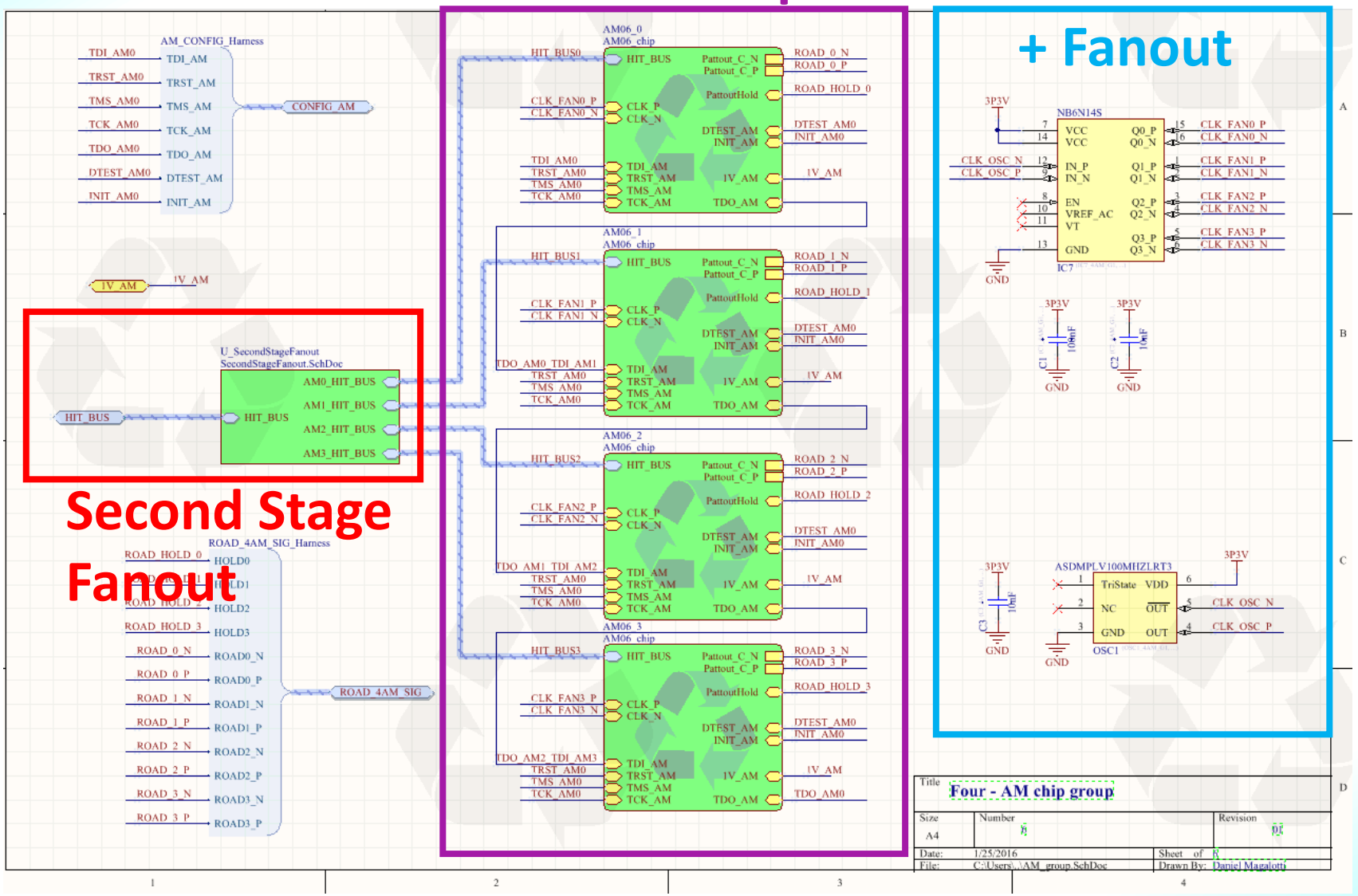
127 MGT
128 MGT

10.3 Gbps (FMC connector)

224 MGT
225 MGT

2 Gbps (AM chip down)

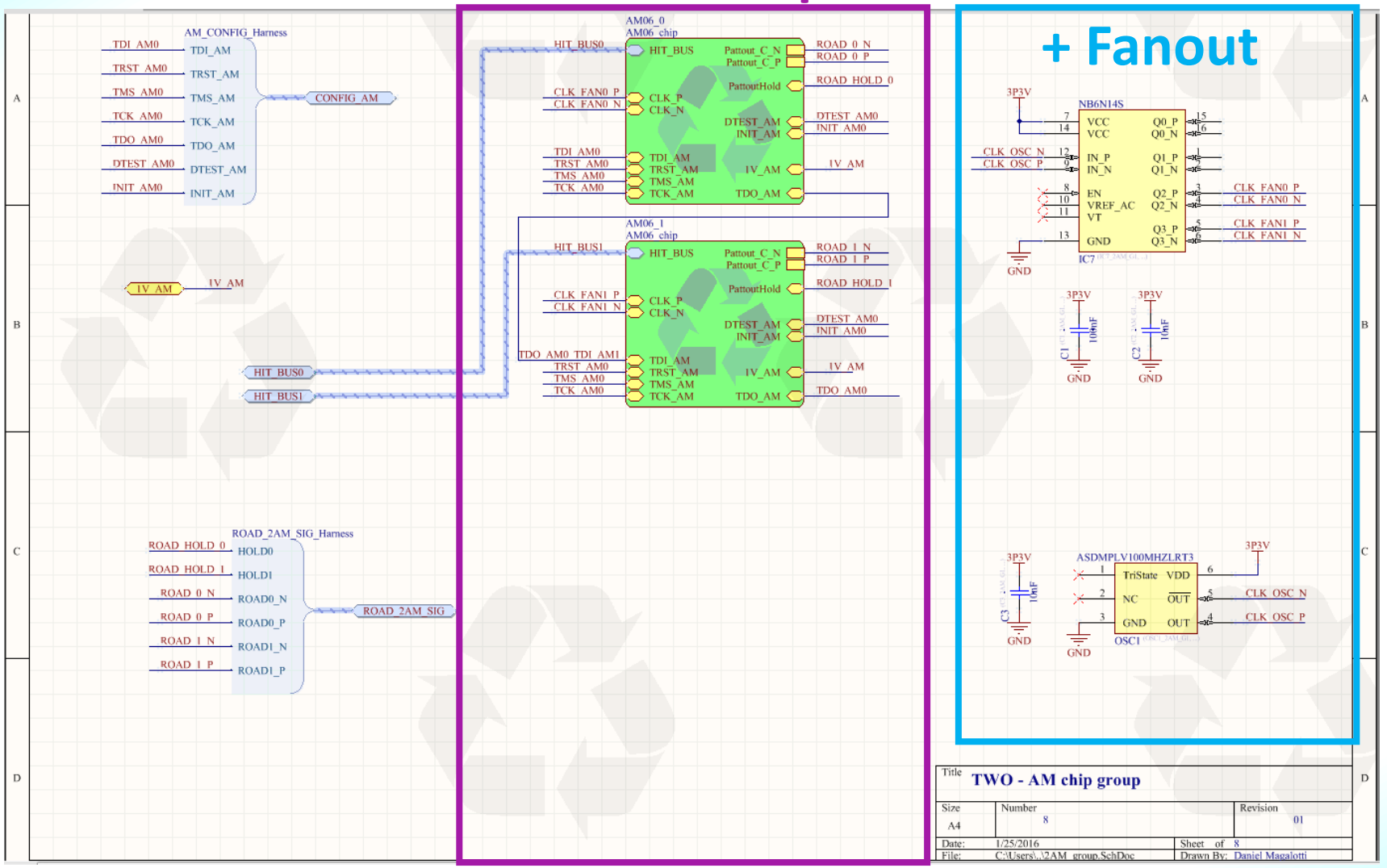
Four AM chip group



Two AM chip group

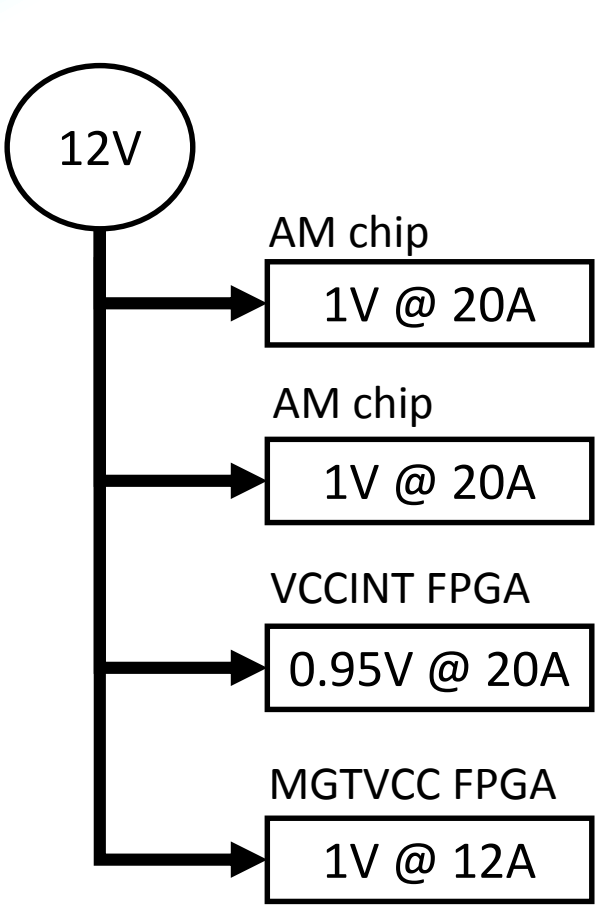
4 AM chips

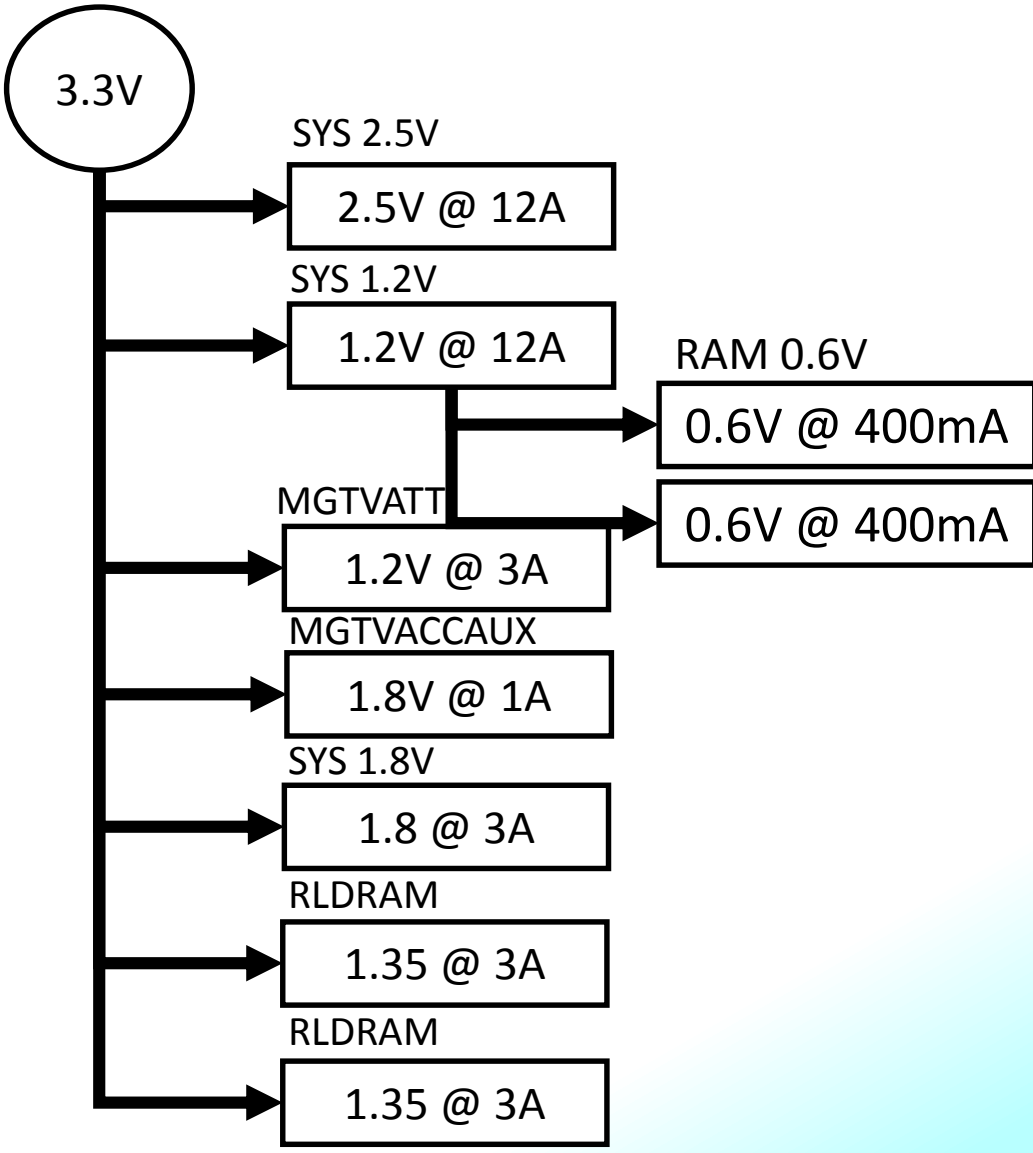
Oscillator + Fanout



Power distribution

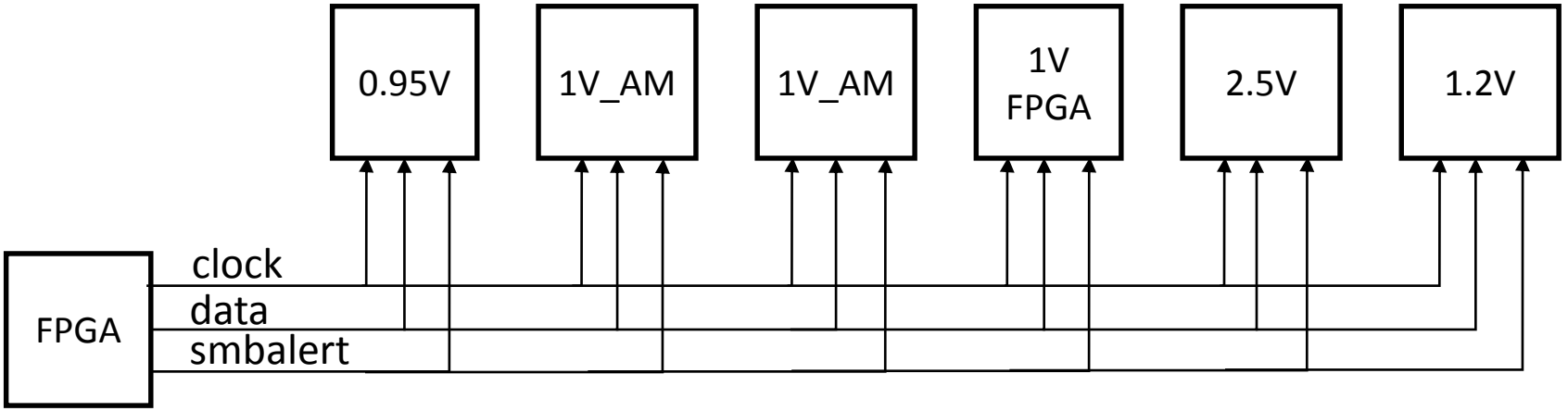
- The network tree of the power distribution





Monitoring tools: PMBUS

- A common PMBUS is distributed to all the power regulator
  - Each line has a pull-up resistor of 4.7kΩ to 2.5V

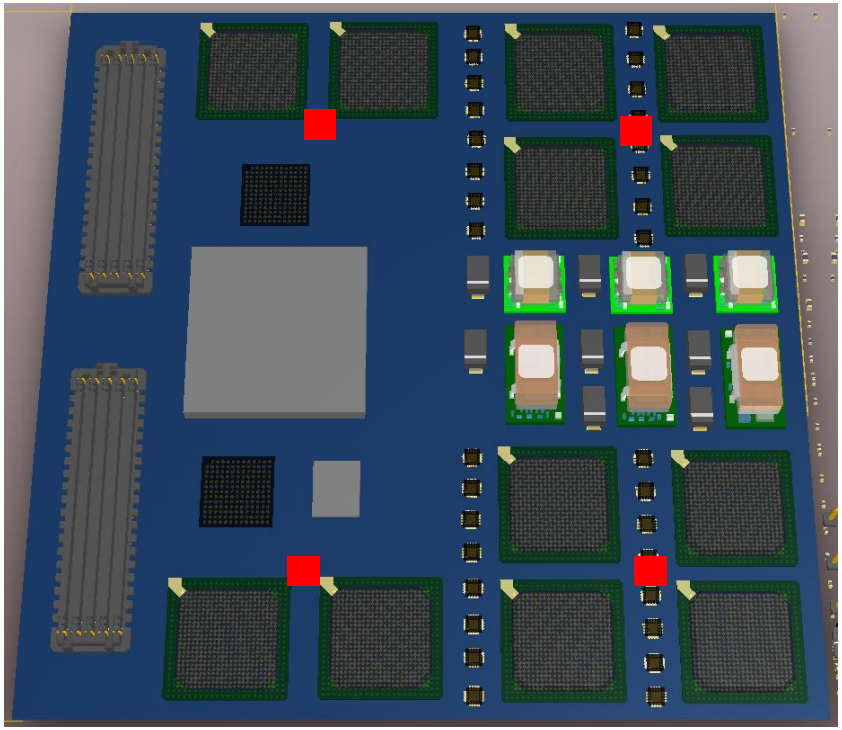


- Address table for the power regulators

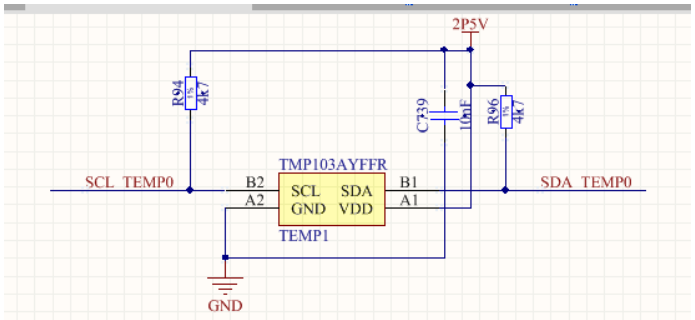
Power Regulator	Addr0	Addr1	Final Address
0.95V	15.4kΩ	10kΩ	1
1V AM0	23.7kΩ	10kΩ	2
1V AM1	36.5kΩ	10kΩ	3
1.2V	54.9kΩ	10kΩ	4
2.5V	84.5kΩ	10kΩ	5
1V FPGA	130kΩ	10kΩ	6

Monitoring tools: Temperature sensors

- Four temperature sensors are used near each group of the AM chip to measure the board temperature. The temperature is read back from the FPGA by using the I^2C protocol



Sensor temperature



The RED box can indicated the position of the four temperature sensors

Monitoring tools: signals

- The I^2C signal for the clock component are controlled by the FPGA
- Two LED are used for the 3.3V and the 12V
- One LED for the DONE signal of the FPGA.
- The I^2C signal from the FMC are connected to the FPGA
- One Spare connector with 10 pins (even more depending on the available space)