Barrel KLM Readout

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Agenda

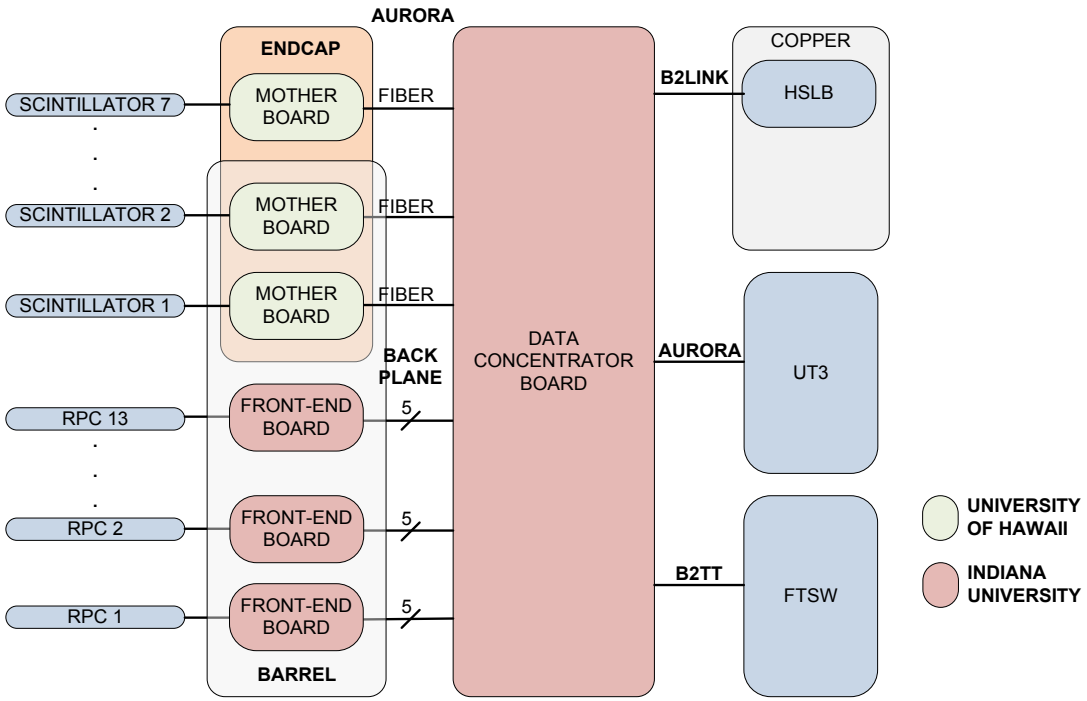
1. System Overview
2. RPC Front-End Board Test
3. Current Status
4. Discussion

SYSTEM OVERVIEW

KLM System

- 13 RPC Front-End boards connect to a Data Concentrator in the barrel
- 2 Scintillator Motherboards connect to a Data Concentrator in the barrel
- 7 Scintillator Motherboards connect to a Data Concentrator in the end-cap

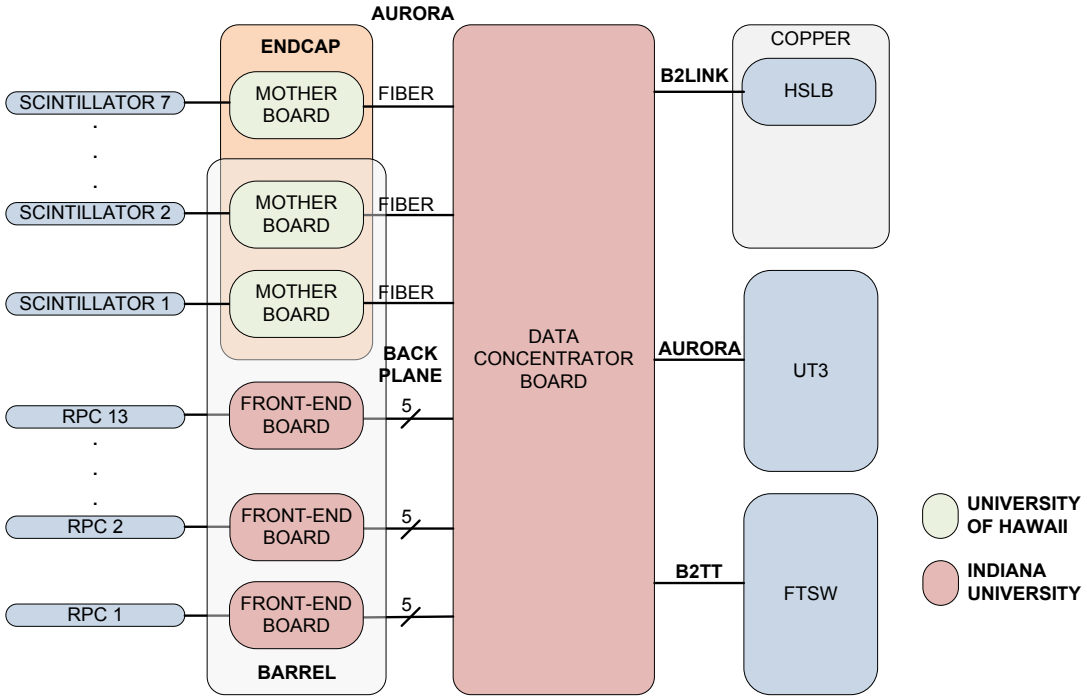
- The Data Concentrator connects to the detector interface (HSLB, UT3, FTSW)
- Indiana University designed the RPC Front-End and Data Concentrator
- University of Hawaii designed the scintillator Motherboard.



KLM System

- Four data paths (types): trigger data, DAQ data, run control data, status data
- Trigger data flows to the UT3 board in a low latency path
- The DAQ data is stored until it is stale or a trigger decision is made
- Valid DAQ data is packaged as an event then sent to the COPPER upon a trigger
- All data flows through the Data Concentrator to its destination
- The FTSW distributes the clock and trigger/timing information

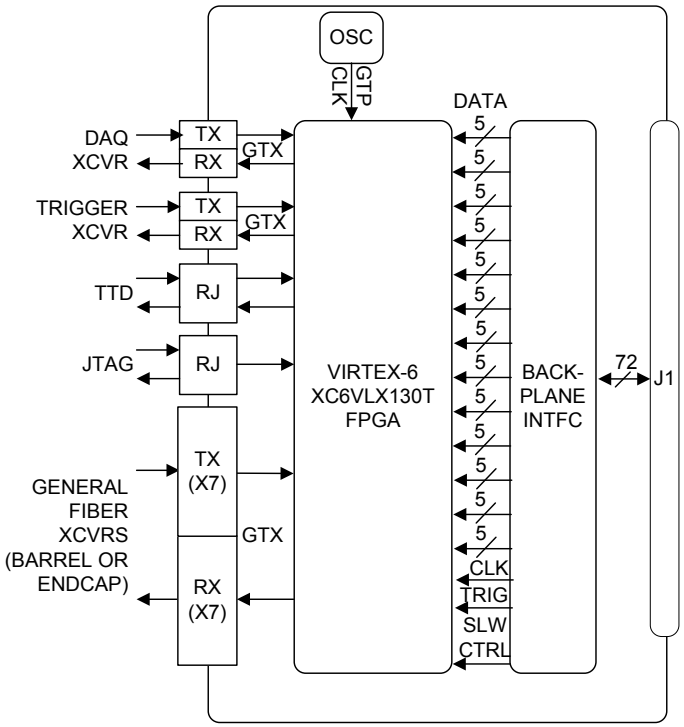
- Status/control data flows to/from copper
- The RPC Front-End - Data Concentrator interface is custom protocol over VME backplane
- All other interfaces to Data Concentrator are over fiber
- Scintillator Motherboard and UT3 interface are Xilinx Aurora
- The COPPER interface is custom Belle2Link

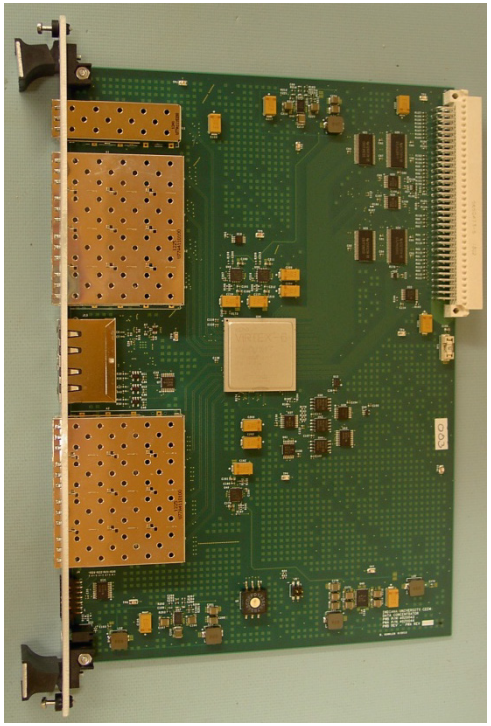


Data Concentrator Board

- One timing and trigger distribution (TTD) interface – RJ45 clock/trigger and RJ45 JTAG
- 9 SFP Transceivers: DAQ, trigger, and seven scintillator layers – 2 barrel or 7 endcap
- One Virtex-6 FPGA for data processing – trigger time ordering, scintillator coincidence, and event builder
- Onboard clock for test without FTSW

- RPC Front-End FPGA configuration interface over backplane
- RPC run control over backplane
- RPC status over backplane

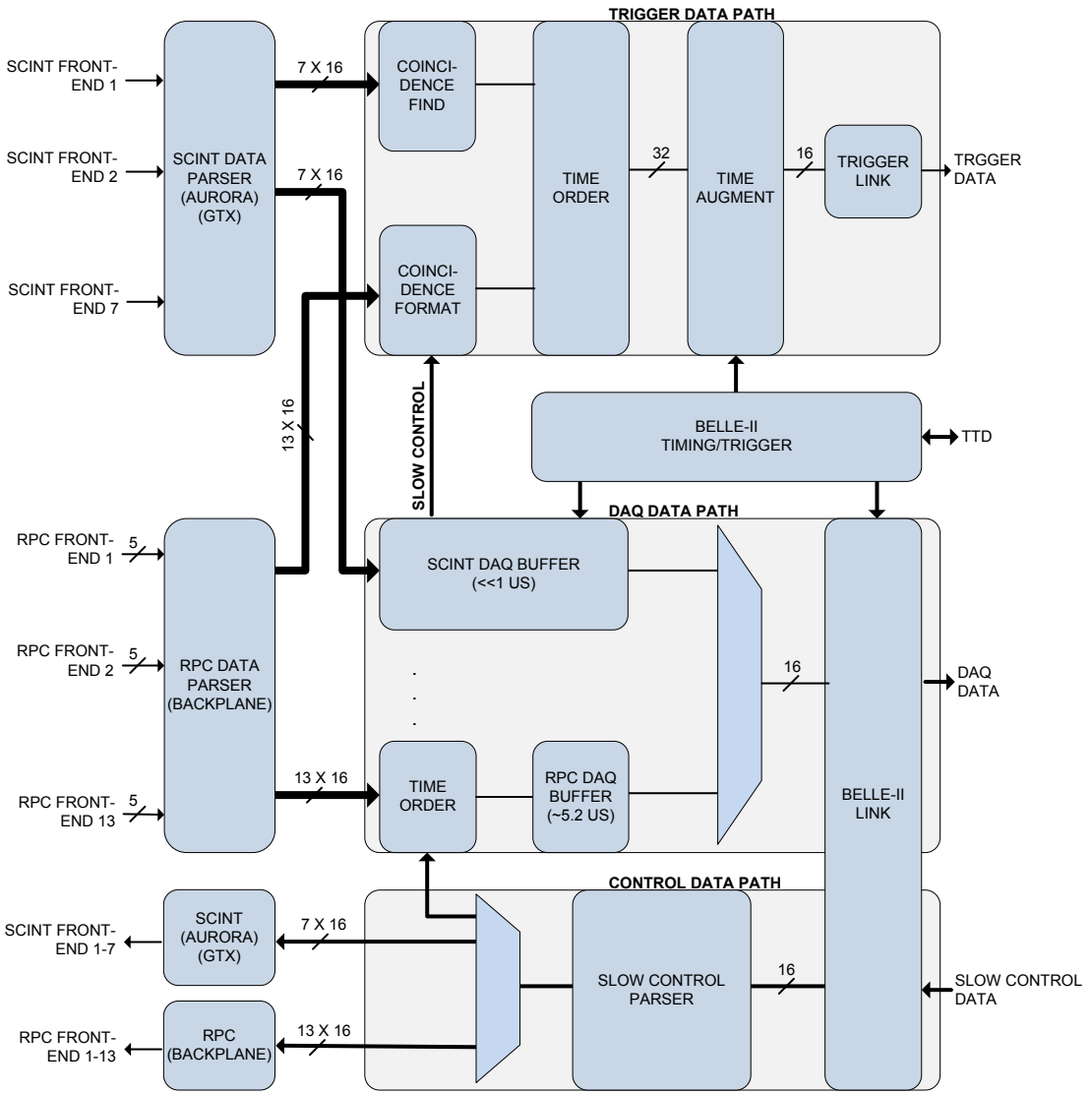




Data Concentrator Functions

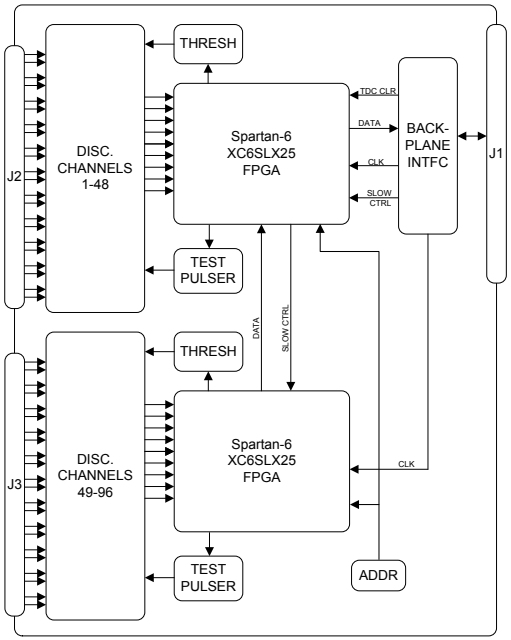
- Interfaces to 13 RPC Front-End boards
- Interfaces to 7 Scintillator Motherboards
- Interfaces to the detector infrastructure (TTD, UT3, COPPER)
- Performs 4 major functions:

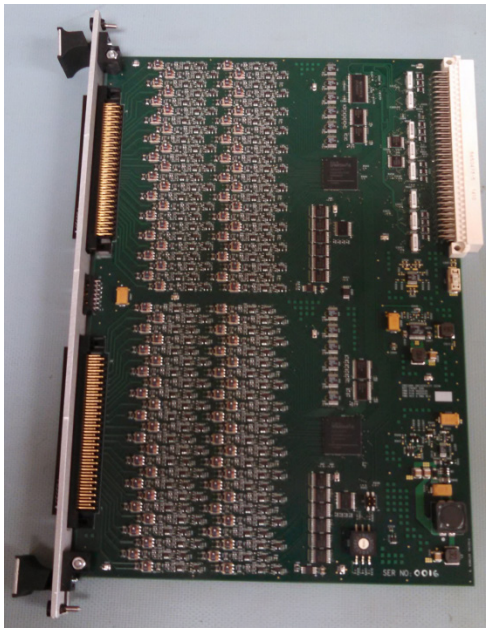
1. Trigger pre-processing
2. DAQ data management
3. Slow control distribution
4. Status collection



RPC Front-End Board

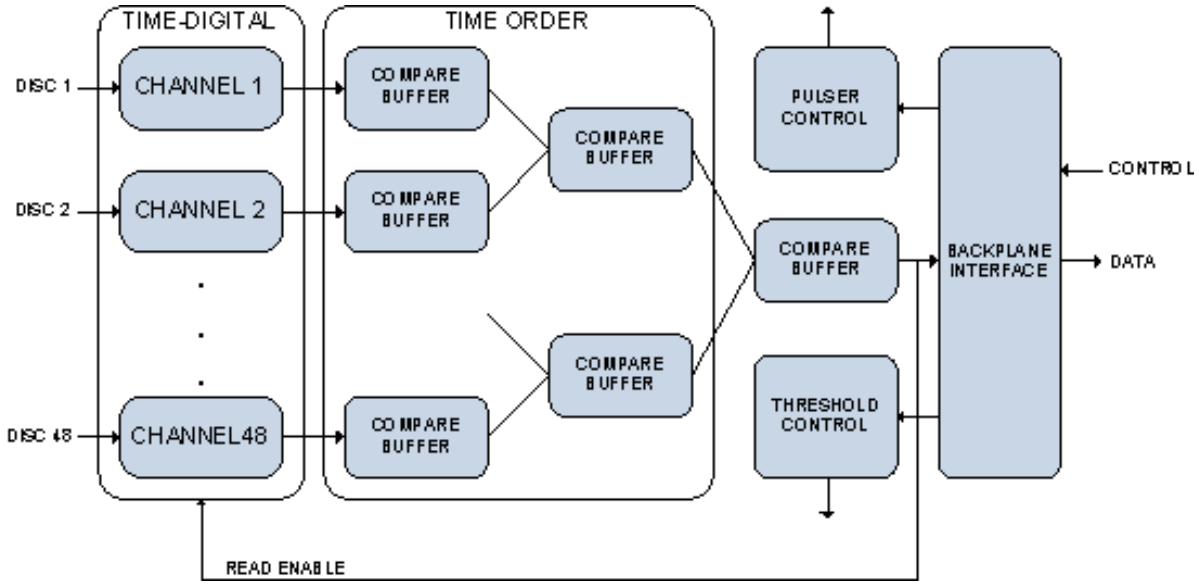
- Contains 96 line receivers and discriminator channels, 48 per front-panel connector
- Channels 1-48 (top) connect to negative RPC pulses while channels 49-96 (bottom) connect to positive RPC pulses
- Discriminator threshold controlled by DAC
- Analog test pulser provides independent built in test of each channel
- Two FPGAs for discriminator control and TDC generation
- FPGAs Configured over backplane using SERA/A08/A09
- Threshold and pulser operated with run control from COPPER
- Discriminator only generates rising edge for FPGA TDC generator





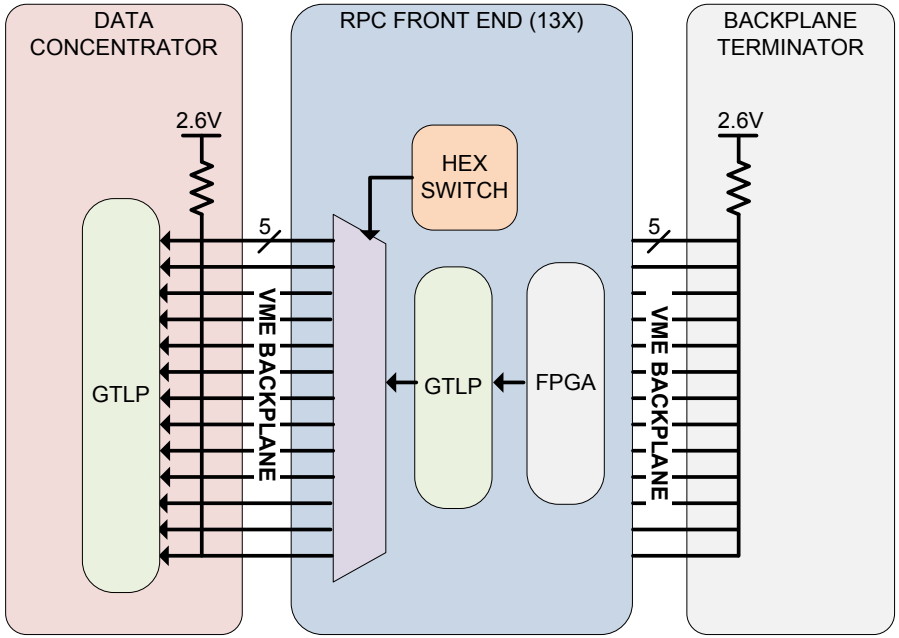
RPC Front-End Functions

- Creates fine time (TDC) with a resolution of 3.94 ns (2x system clock)
- Time orders TDC values to simplify event building on Data Concentrator board
- Transmits TDC values to Data Concentrator board using custom backplane protocol
- Receives run-control parameters from backplane using FPGA fabric UART



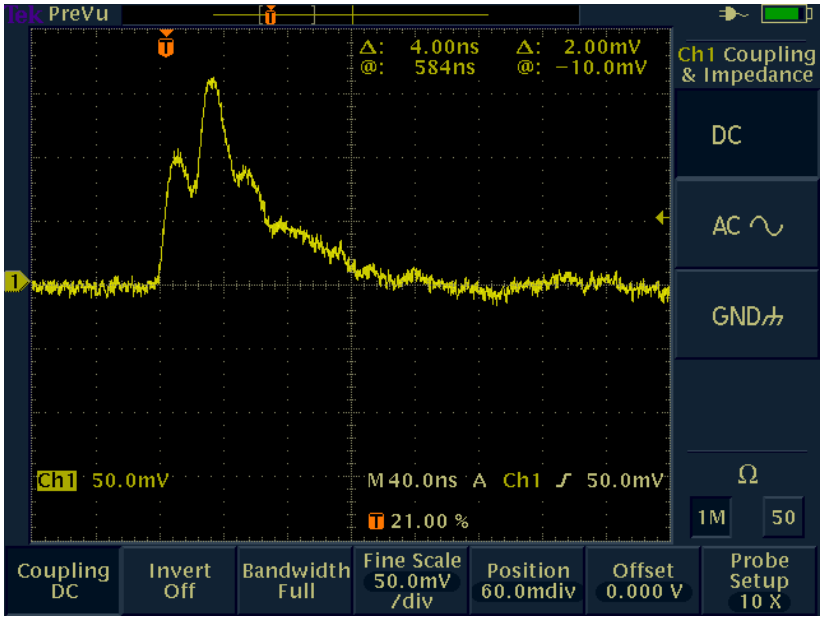
Custom Backplane

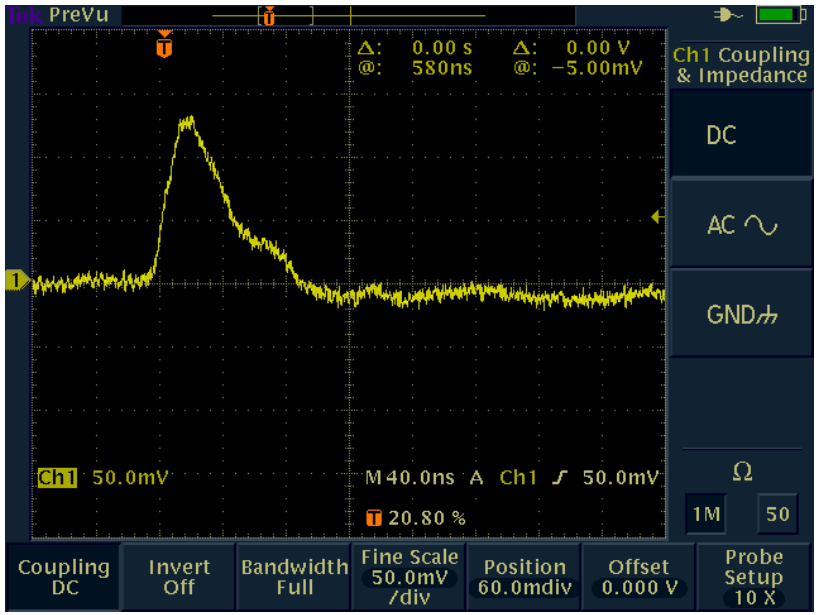
- Signal levels are GTLP
- Backplane termination voltage is lowered to 2.6V for GTLP
- TDC data transmitted over dedicated 5-bit slices
- 5-bit slice driven by single buffer and 1-13 de-muxed to desired slot/position that corresponds to layer
- Position selected by hex rotary switch on RPC Front-End



RPC Signals

- Z-axis (negative) left, Phi-axis (positive) right, from muon, measured on RPC front-end after termination – hence the same polarity
- Large amplitude, ~125 mV





RPC FRONT-END BOARD TEST

RPC Front-End Board Test Procedure

- Power
  - Verify that each power supply operates at required voltage
- RPC interface
  - Verify that each discriminator channel generates edge for TDC
  - Verify that each channels (DAC) threshold operates
  - Verify that each test pulser channel operates
- Custom backplane interface
  - Transmit test pattern
  - Cycle through every backplane position
  - Verify that every bit transitions
- FPGA configuration interface
  - Verify that all signals transition

Complicated Test Fixture

- External pulser with variable amplitude connects to Z and Phi connectors to pulse every channel while data is analyzed with COPPER readout
- Threshold and built-in pulser are manipulated with and data is analyzed with COPPER readout
- Configure FPGAs with Data Concentrator

- Requires: Custom pulser, PocketDAQ, Data Concentrator, Backplane Terminator Board, production firmware, test software, VME chassis

Simple Test Fixture

- Use ChipScope VIO to assert built-in test pulser channel, monitor associated channel with ChipScope ILA
- Use ChipScope VIO to program threshold with low threshold, monitor associated channels with ChipScope ILA
- Configure FPGA with Data Concentrator

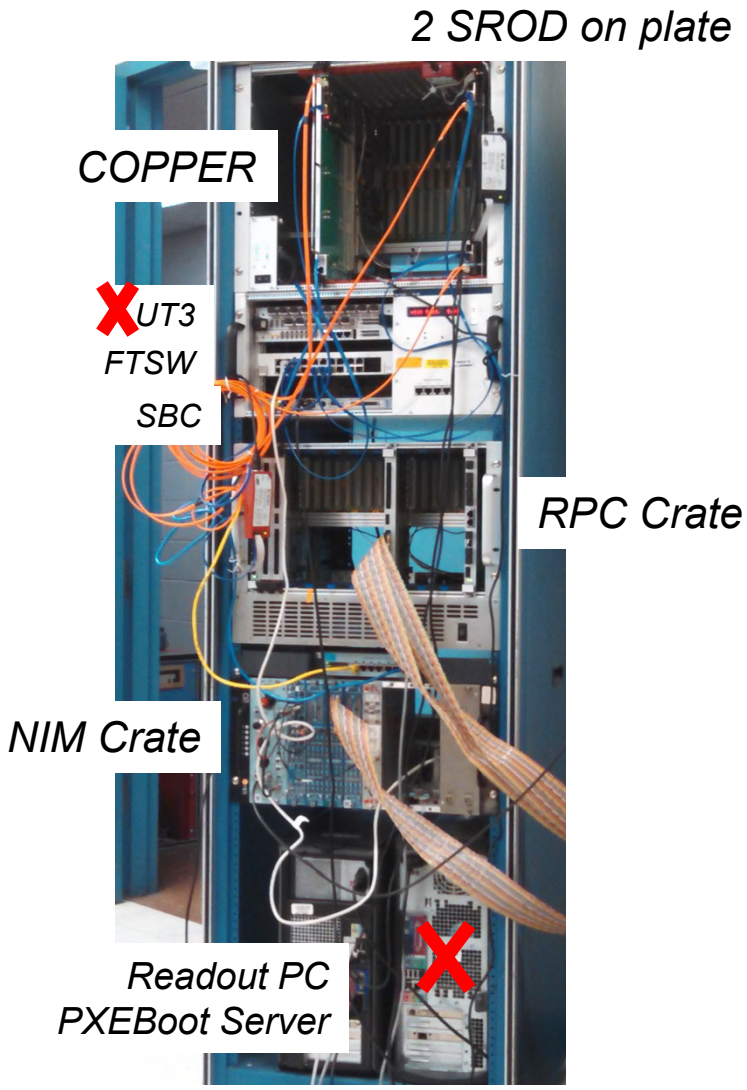
- Requires: Data Concentrator (any rev.), custom firmware, VME chassis

General Test Fixture Comments

- Test firmware exists, but probably not for casual user
- Production firmware will likely make testing overly complicated (scintillator electronics and triggers will be required)
- Simple test board could replace Data Concentrator
- Ethernet on Data Concentrator could replace COPPER readout/run control
- Using only the built-in test pulser does not test connector to analog channel connection - could be tested by inspection
- The RPC signals appear to be very large so a complicated external pulser may not be required

Indiana University PocketDAQ

- FTSW distributes clock and trigger – either from internal or external source
- Single board computer (SBC) controls FTSW
- COPPER provides run control data
- UT3 to be used in the coming weeks
- Two Data Concentrators – 1 read-out and one terminator



STATUS

KLM Read-Out Status

- Data Concentrator
  - 38 bare boards were manufactured Jan. 2015
  - 5 bare boards were assembled in Jan. 2015
  - Remaining 33 will be assembled in Jan. 2016
- RPC Front End
  - 240 bare boards manufactured in Jan. 2015
  - 15 bare boards assembled in Jan 2015
  - 225 boards still need assembly
- Firmware
  - Production: maintenance and bug fixes as required
  - Test: develop new or modify existing as desired
- Software
  - All test software to be developed

Integration Status

- PocketDAQ setups exist at Indiana University and the University of Hawaii
- A complete KLM sector is installed at KEK and muon tracks have been captured and analyzed
- All hardware interfaces have been tested locally or within the sector test stand or both
- There are firmware bugs being fixed and improvements being made

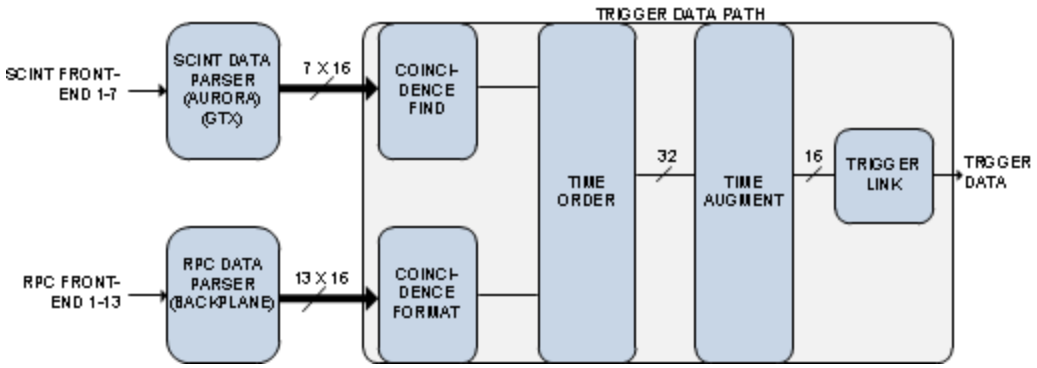
DISCUSSION

BACKUP

Data Concentrator - Trigger Data Path

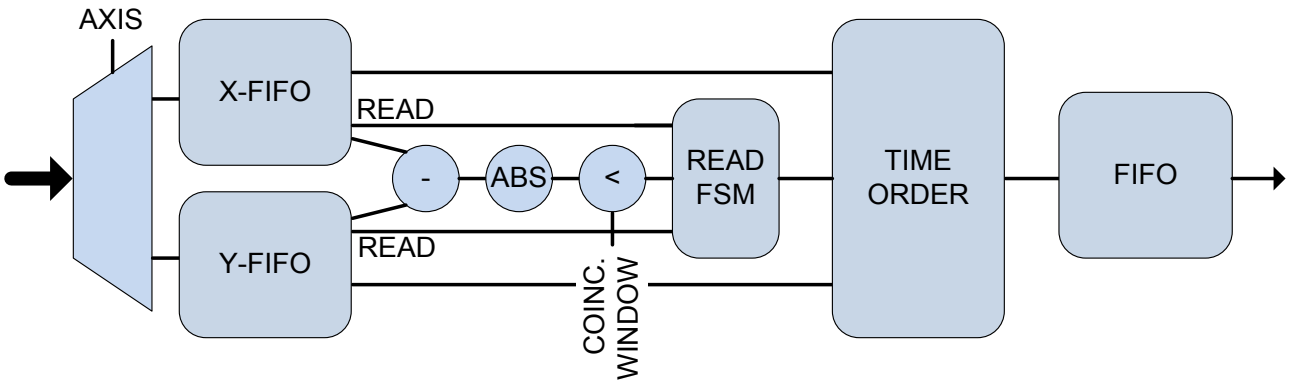
- Parses from Scintillator Aurora interface and RPC backplane to create unified trigger data format.
- Finds coincident hits on orthogonal Scintillator fibers.
- Formats RPC data to mirror Scintillator coincidence finder output (no coincidence finder on RPC data because always coincident).
- Time orders remaining trigger data – this process also combines data into a single 16-bit trigger data lane.*

*Requires hardware to convert four un-channel bonded Aurora cores into to a single UT3 quad SPF connection.



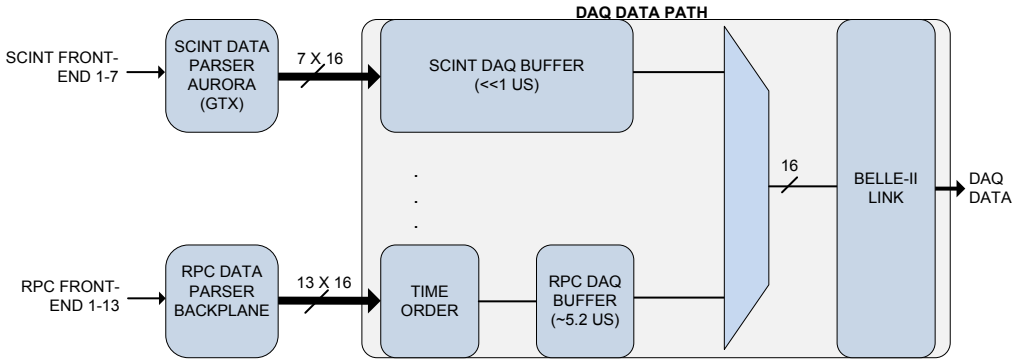
Data Concentrator - Coincidence Finder

1. Separate channels into respective axis.
2. Test for coincidence.
3. Write both samples to a FIFO if coincident.
4. Read earliest sample if no coincidence.
5. Test for coincidence (repeat)



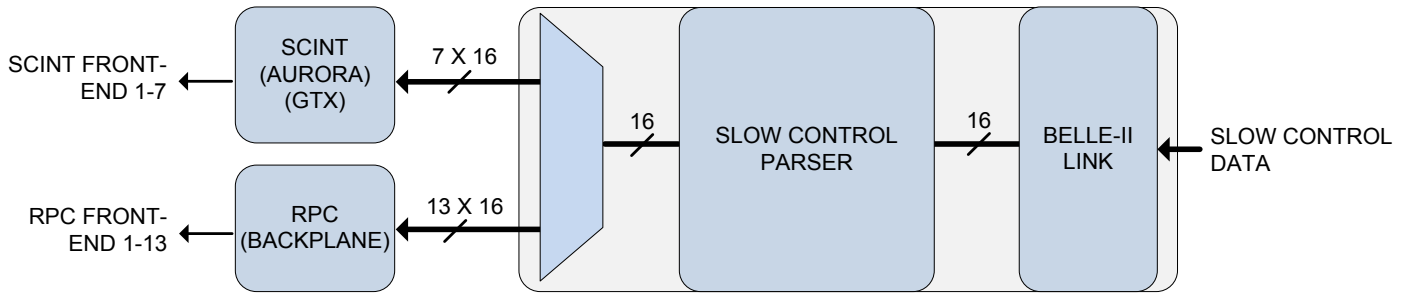
Data Concentrator - DAQ Data Path

- Parses scintillator and RPC data to creates smaller packets comprised of a single sample (e.g. channel and time word).
- Buffers ~5.2 μs of data while waiting for trigger.
- Buffers scintillator samples for lane combination.
- Time orders RPC samples so stale data can easily be removed from buffer.
- Combines scintillator samples and RPC samples into single B2link data stream.
- Time stamps are augmented by B2TT/B2Link.



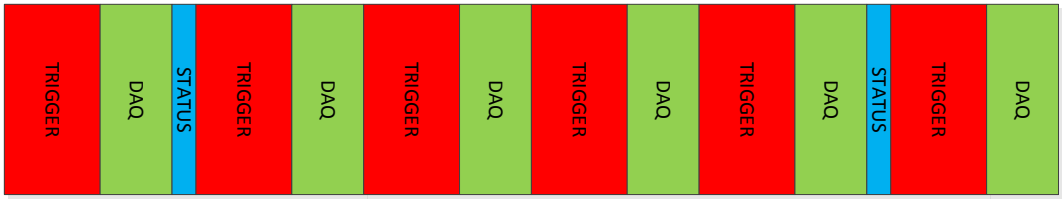
Data Concentrator - Slow Control Path

- Routes slow control data to Data Concentrator, RPC Front-End, Scintillator Motherboard.
- Some Data Concentrator parameters are controlled by B2Link register interface (not shown).
- All scintillator and RPC parameters are sent using B2Link serial file interface (because there are thousands)
- Routes data based on byte offset in serial file (packet).



Scint. Motherboard – Data Concentrator Interface

- Seven lanes of scintillator trigger data, DAQ data, and status data flow through a single Data Concentrator.
- Need a protocol for data transmission:
  - Each data type will have a time slot (as in communications standards).
  - Trigger data will have the largest time slot at >95% to limit delay.
  - DAQ data will use most of the remaining time.
  - A status packet can be sent infrequently – maybe every 2048 trigger packets.
- Implemented with Aurora core framing interface:
  - The SOF signal is asserted at the beginning of a slot.
  - The EOF signal is asserted at the end of a time slot
  - Pauses are used within a time slot if no data is present.
- Deterministic interface that maintains trigger priority, easy to implement, and easy to troubleshoot.



Scintillator Slow Control

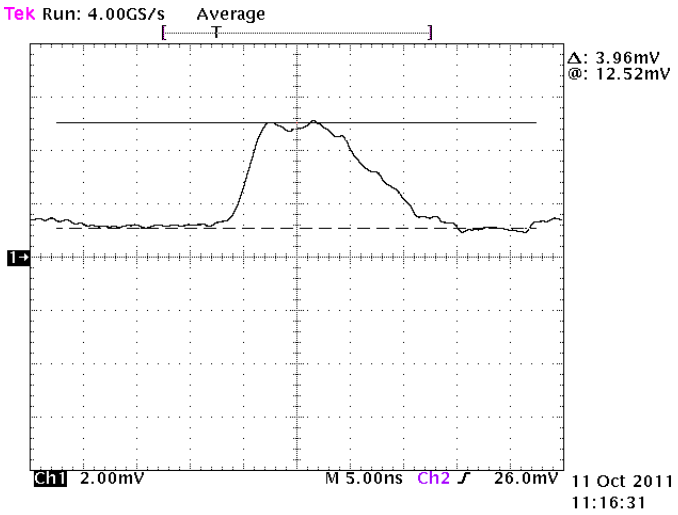
- The scintillator electronics require configuration values that are expected to be transmitted over each Belle2link
- Number of bKLM parameters if passed through Concentrator:
  - 300 MPPC channel bias voltage settings
  - 600 ASIC trigger threshold and DAC values
- Number of eKLM parameters if passed through Concentrator:
  - 1050 MPPC channel bias voltage settings
  - 2100 ASIC trigger threshold and DAC values

RPC Slow Control

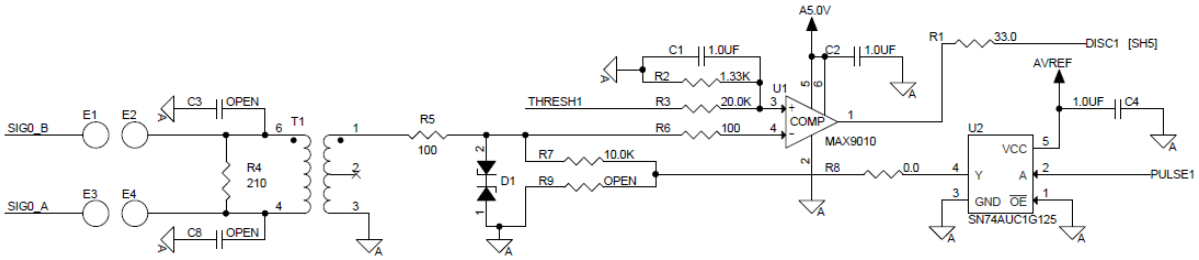
- The RPC Front-End board requires configuration values and (optionally) built-in-test control that is expected to be transmitted over each Belle2link:
  - Threshold value - 1248 values/Concentrator, 8-bits per value
  - Test pulser - 1248 built-in-test values/Concentrator, 1-bit per value
  - Test pulser control – some number of bits to turn test pulser on/off

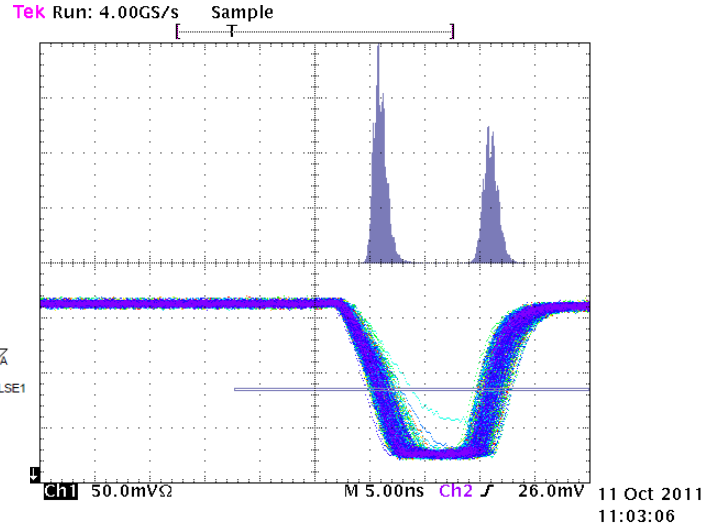
RPC Receiver/Discriminator

- Prototype TDC board discriminator circuit shown below
- Prototype circuit generated from lab tests that generated scope captures on right



Input (P6247 probe, averaged)





Output @ threshold = 3.3 mV

Custom Backplane Circuit

- All FEE boards feed data to one concentrator board
- We require to do this transfer with **minimal latency**
  - Use a simple, synchronous protocol
  - Don't share any resources
  - → *Thirteen independent point-to-point links is best*
- *But we should re-use old backplane (VME-J1)!*
  - → *Dedicate* 5 VME lines (selected by slot ID) for each FEE to communicate to concentrator, and run them as fast as possible
    - → GTL allows for proper termination and can run at over 100 MHz (total 775 MB/s to concentrator board)
    - → Use diodes to isolate non-driving boards
    - Also: use NMOS mux to control the diodes & to lower costs (fewer GTL devices required)
  - Concentrator board drives local clock to backplane, all boards (including concentrator) receive clock from backplane
  - FEE boards skew their received clocks according to slot ID in order to deskew data received at concentrator board