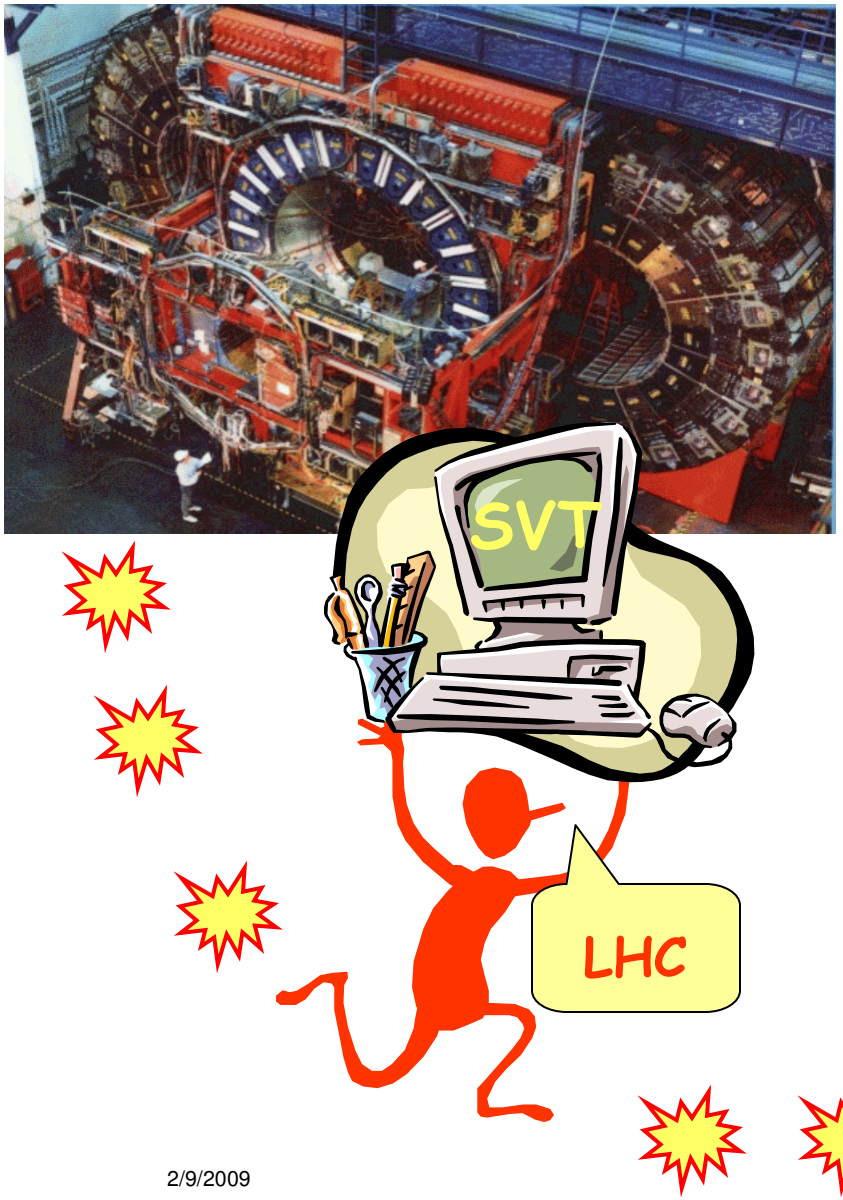
Fast Tracker (FTK) at Atlas

FTK

- The architecture (now) and how it is connected to the DAQ
- The R&D proposal to write a TDR: schedule, costs, institutions
- Physics case
- FTKSIM package for FTK simulation
- Conclusions

Paola Giannetti
Istituto Nazionale di Fisica Nucleare
Pisa

FTK idea:
Let's exploit the CDF effort also for LHC!



If we do a big effort (CDF), let's use it as much as possible!

FTK for LHC L2 @GR V 1999-2001→Upgrade @CDF 2003-08

IEEE Trans. Nucl. Sci. 48, 575 (2001)

IEEE Trans. Nucl. Sci. 48, 595 (2001)
IEEE Trans. Nucl. Sci. 48, 1313 (2001)
IEEE Trans. Nucl. Sci. 51, 391 (2004)
IEEE Trans. Nucl. Sci. 55, 145 (2008)

Let's use it also @ L1

"The CDF Associative Memory for a Level-1 Tracking System at CMS", Real-Time Conference, 2007 15th IEEE-NPSS, Fermilab, Page(s):1 - 4

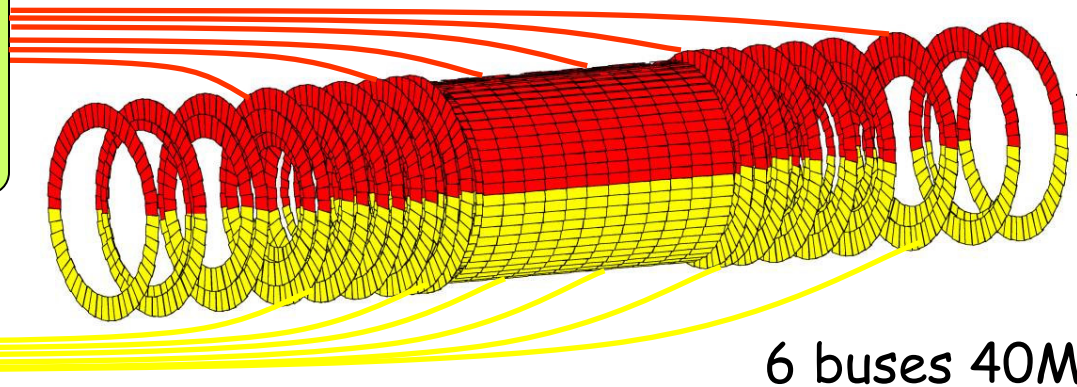
The Associative Memory for the Self-Triggered SLIM5 Silicon Telescope, IEEE 2008

FTK for L2→increase # sectors with instant luminosity increase

1/2 φ AM

1/2 φ AM

ATLAS Pixels + SCT



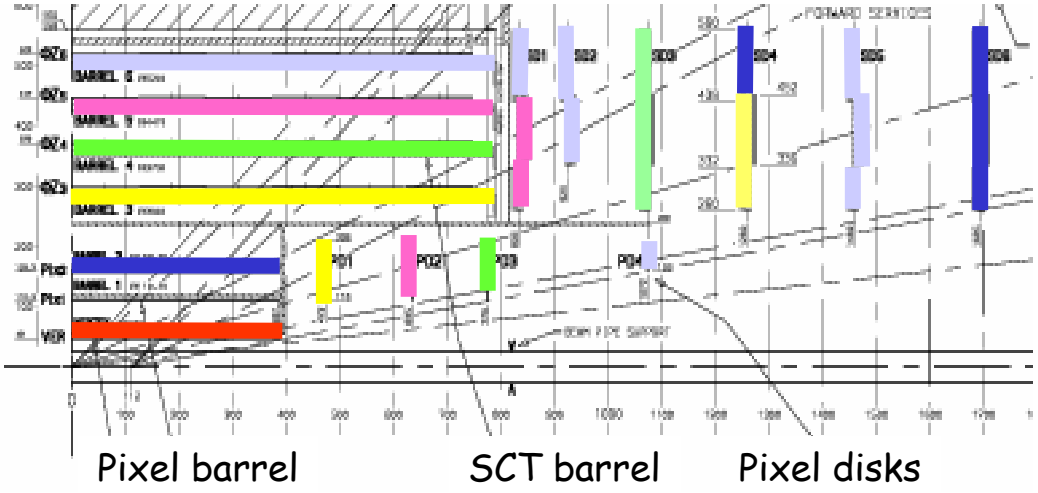
Divide into φ sectors

Allow a small overlap for full efficiency

6 buses 40MHz/bus

6 or 12 Logical Layers: full η coverage

~70MHz cluster/layer
(Low Luminosity, 50KHz ev.)



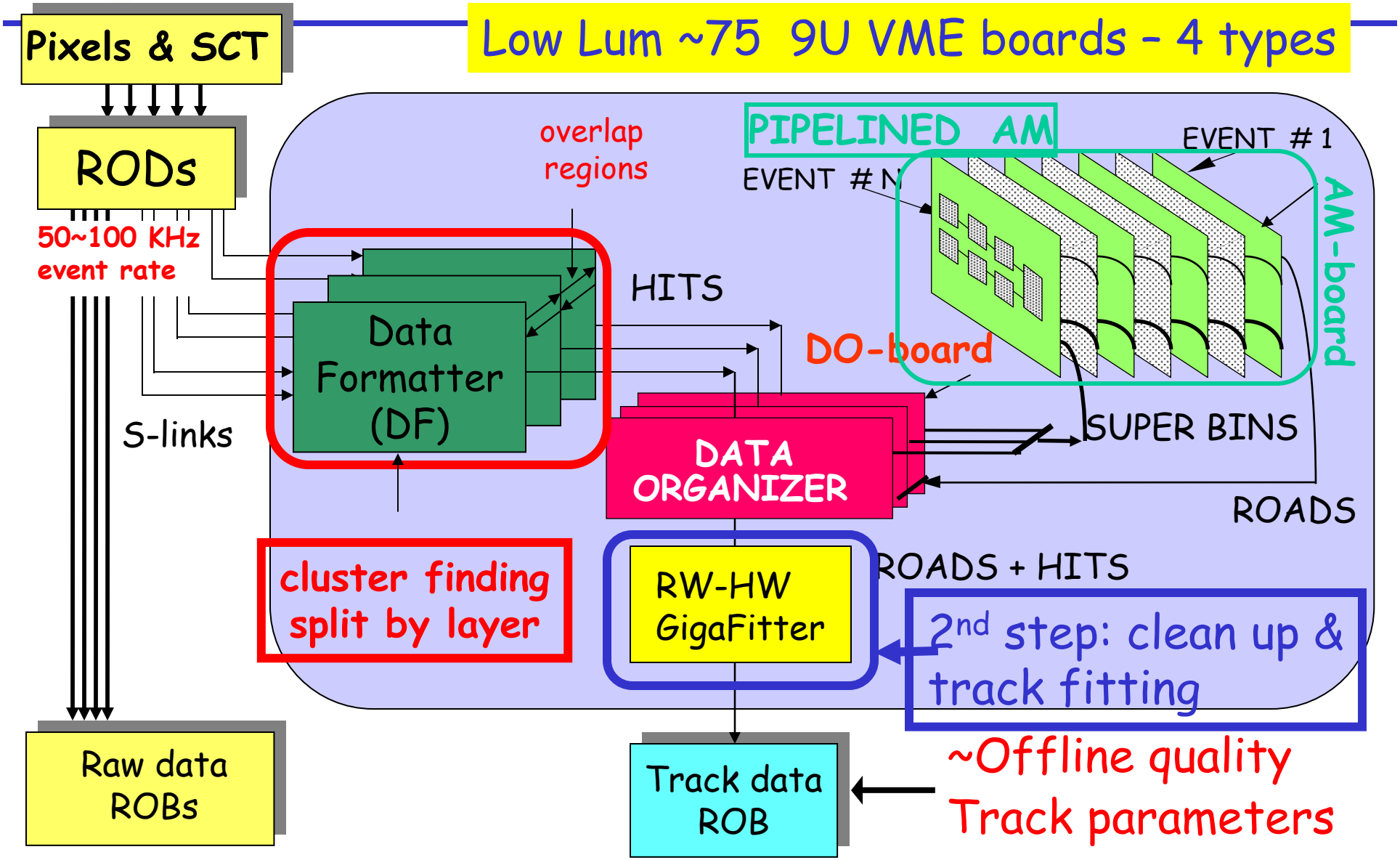
Pixel barrel SCT barrel Pixel disks

2 φ sectors for 10**33

8 φ sectors for 10**34

Inside Fast-Track

Low Lum ~75 9U VME boards - 4 types



Inside Fast-Track

Low Lum ~75 9U VME boards - 4 types

Pixels & SCT

RODs

50~100 KHz event rate

S-links

Module data

FPGA

overlap regions

PIPELIN

EVENT # N

HITS

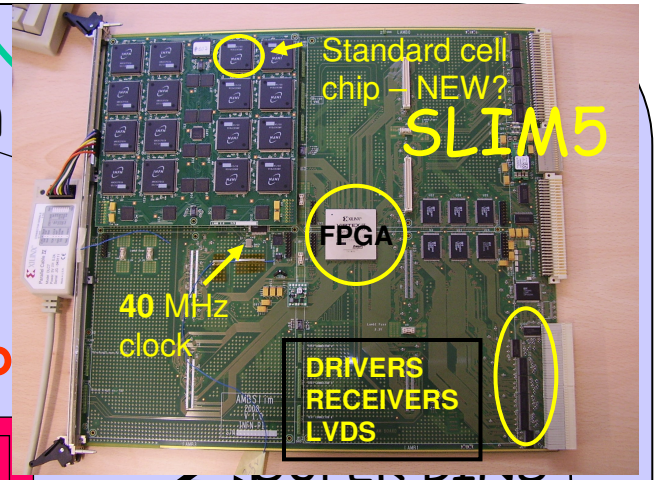
DO-b

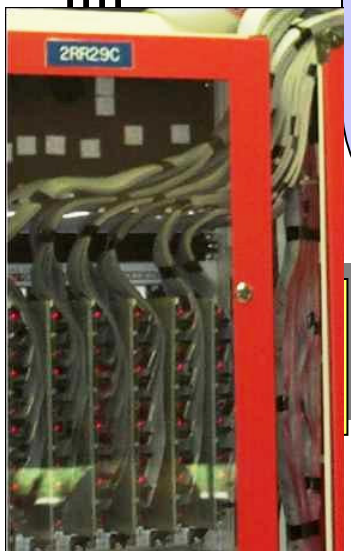
DATA ORGANIZER

ROADS

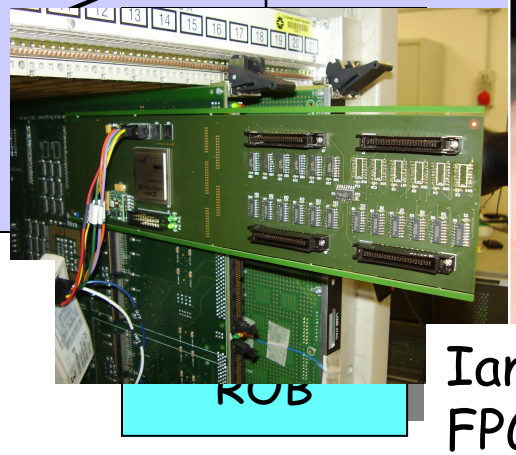
Eta direction -->

cluster finding split by layer

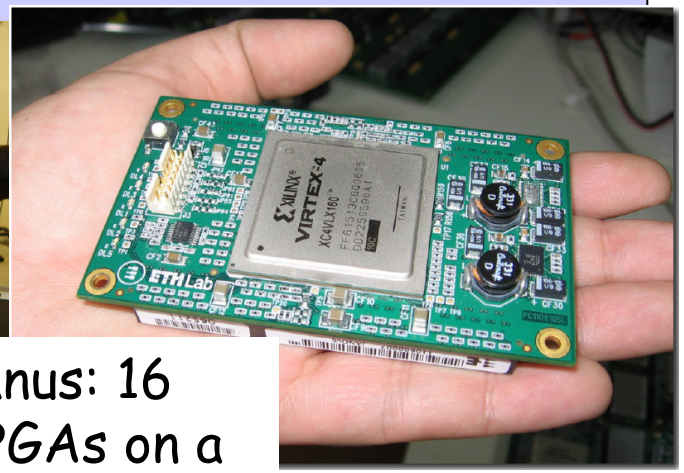




GigaFitter
now 3 FPGA
squeezing
~16 boards in 1



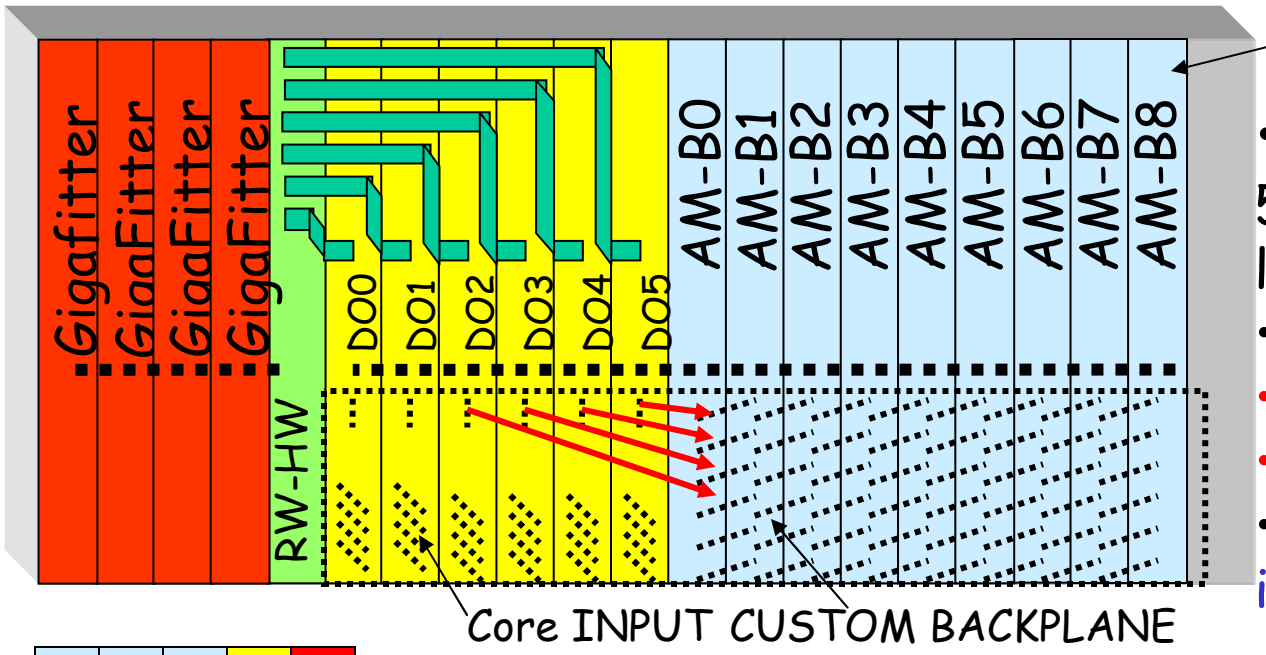
ROB



Ianus: 16
FPGAs on a
single board

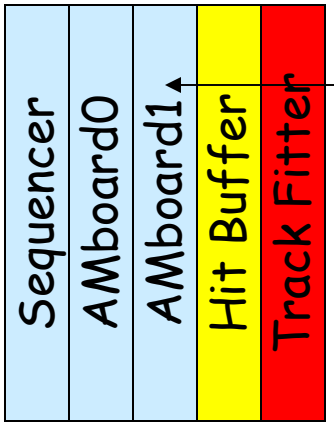
FTK sector Size

O(50 10^6) patterns

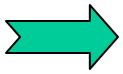


128 AMChips/board
40 kpat/chip

- ~offline quality tracking 50 KHz event (Low luminosity)
- **2 crates @low lum**
- **8-12 crates @high lum**
- **SLHC? Simul.**
- Data Formatter not included



64 AMChips/board
5 kpat/chip



O(512 10^3) patterns

To compare: here it is the SVT processor for one sector (12 sectors in SVT)

AM chips from 1992 to 2005

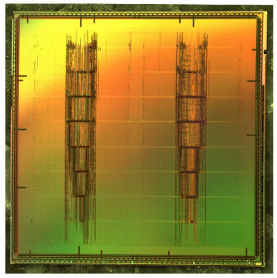
- (90's) **Full custom VLSI chip -** 0.7μm (INFN-Pisa)
- **128 patterns/chip, 6x12bit words each**

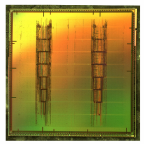
F. Morsani et al., "The AMchip: a Full-custom MOS VLSI Associative memory for Pattern Recognition", IEEE Trans. on Nucl. Sci., vol. 39, pp. 795-797, **(1992).**

On the opposite side: **FPGA** for the same AMchip

0,45 μm (INFN-Pisa)

P. Giannetti et al. "A Programmable Associative Memory for Track Finding", Nucl. Intsr. and Meth., vol. A413/2-3, pp.367-373, **(1998).**





NEXT: NEW VERSION For both L1 & L2

In the middle: **Standard Cell 0.18** μm (INFN-Pisa-Ferrara)→ 5000 pattern/chip AMchip

L. Sartori, A. Annovi et al., "A VLSI Processor for Fast Track Finding Based on Content Addressable Memories", **IEEE Transactions on Nuclear Science,** Volume 53, Issue 4, Part 2, Aug. **2006** Page(s):2428 - 2433

FTK R&D PROPOSAL: Who & schedule & costs FTK

University of Chicago

E. Brubaker, M. Dunford, A. Kapliy, Y.K. Kim, M. Shochet, K. Yorita

Laboratori Nazionali di Frascati

A. Annovi, M. Berretta, P.Laurelli

Harward University

M. Franklin, J. Guimaraes da Costa, C. Mills, M. Morii, J. Oliver

University of Illinois

C. Ciobanu, T. Liss, M. Neubauer

Dipartimento di Fisica e Istituto Nazionale Fisica Nucleare Pisa

V. Cavasinni, F. Crescioli, M. Dell'Orso, T. Del Prete, A. Dotti, P. Giannetti, G. Punzi, C. Roda, F. Sarri, I. Vivarelli, G. Volpi

Istituto Nazionale Fisica Nucleare Roma

M. Rescigno

New Institutions.: Argonne Lab USA (Jinlong Zhang)- Waseda Japan (Kohei Yorita)

- R&D Proposal to work on TDR: presented in July 07. Decision March 08
- 1 year to produce the TDR (2009)
- 3 years to build the system (2010-2012)
- first data taking with baseline LHC (10^34 cm^-2 s^-1)
- upgrade for SLHC with possible extension @ level 1

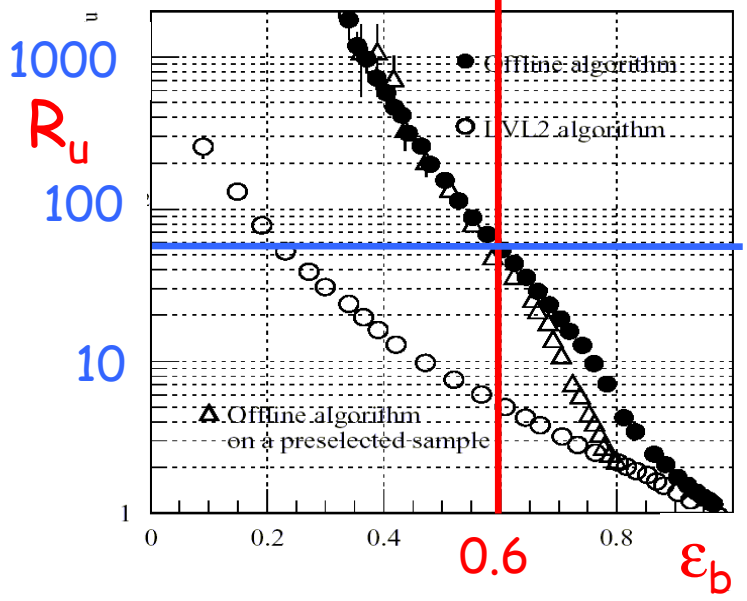
2M±2M$
Usa: 2M$?
Italy: x00 k€ ?
Japan: ?

Offline-quality b-tagging for events rich in b-quarks

Z0 ⟶ bb Calibration sample

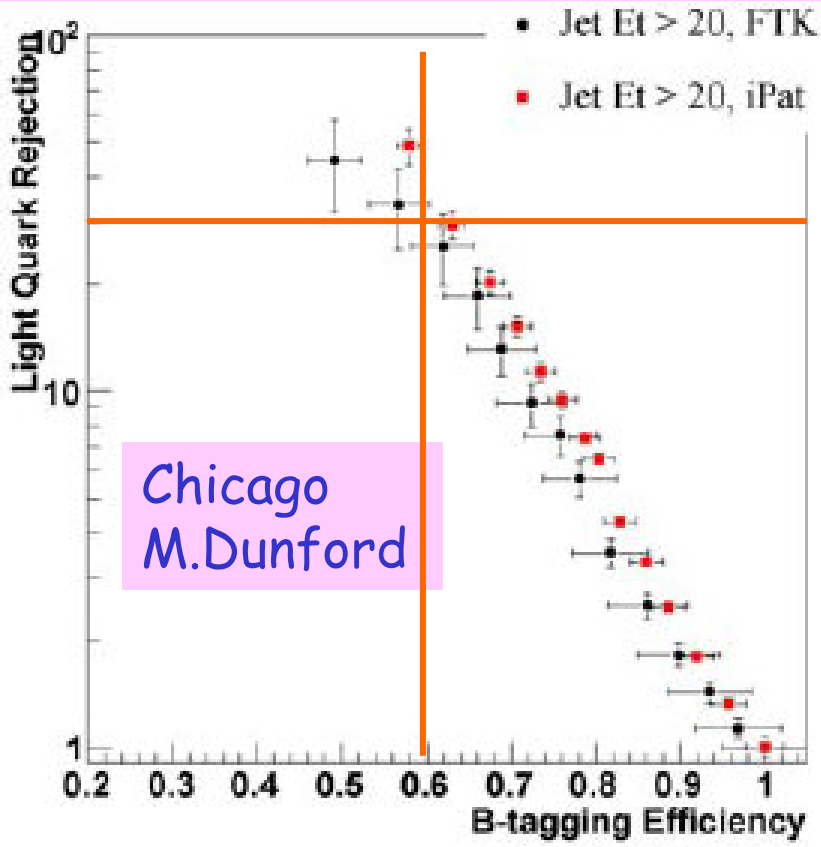
bbH/A ⟶ bbbb
tt ⟶ qqqq-bb
ttH ⟶ qqqq-bbbb
H/A ⟶ tt ⟶ qqqq-bb
H ⟶ hh ⟶ bbbb
H^{+-} ⟶ tb ⟶ qqbb

ATL-DAQ-2000-033



ATLAS TDR-016

FTKsim (G.Volpi, F.Crescioli). |η|<1



Chicago
M.Dunford

Athena WH events - No pileup

Physics case for b-tagged samples (No-pile-up): some examples

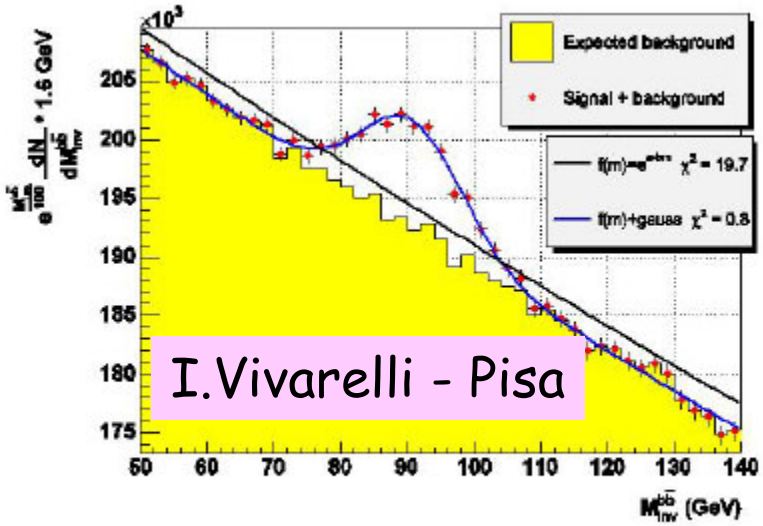
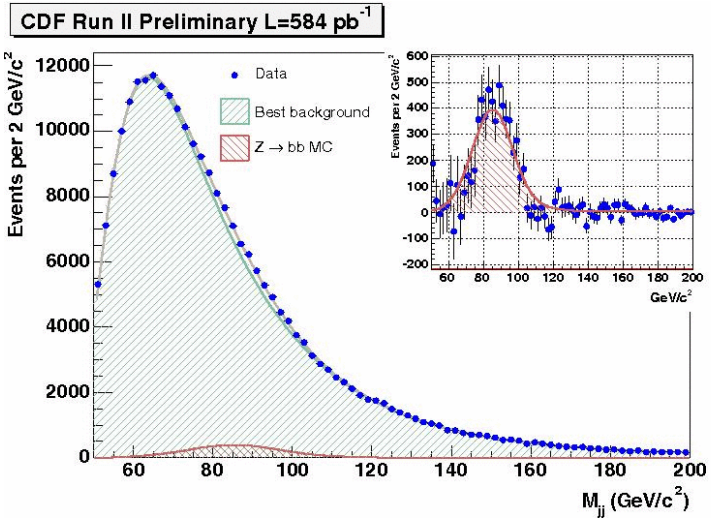
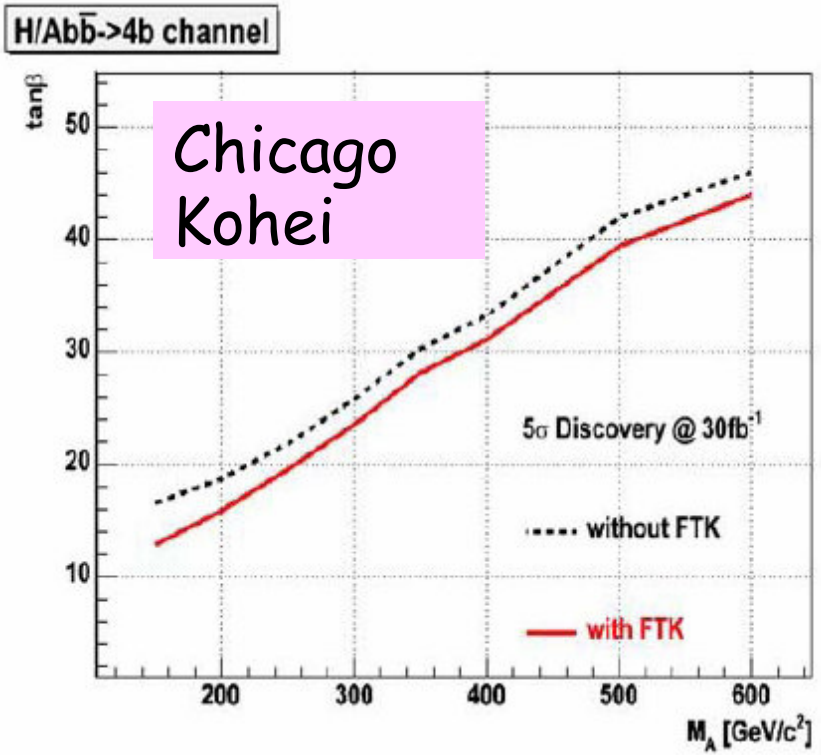
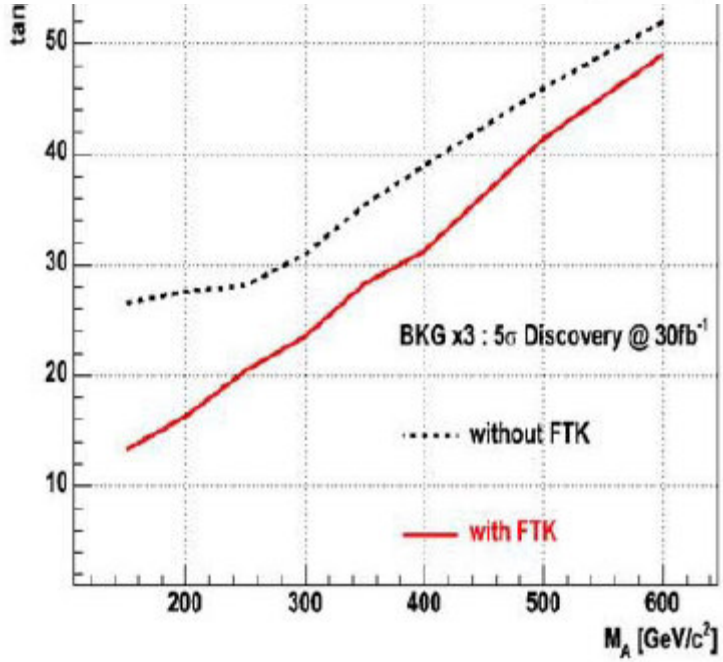


Figure 6: The $Z \rightarrow b\bar{b}$ signal after 30 fb^{-1}.

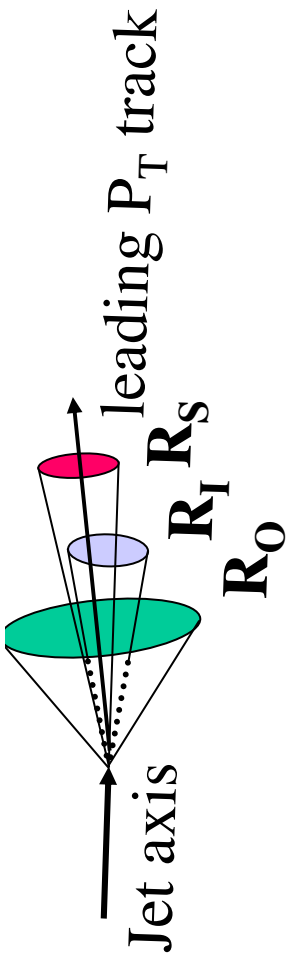


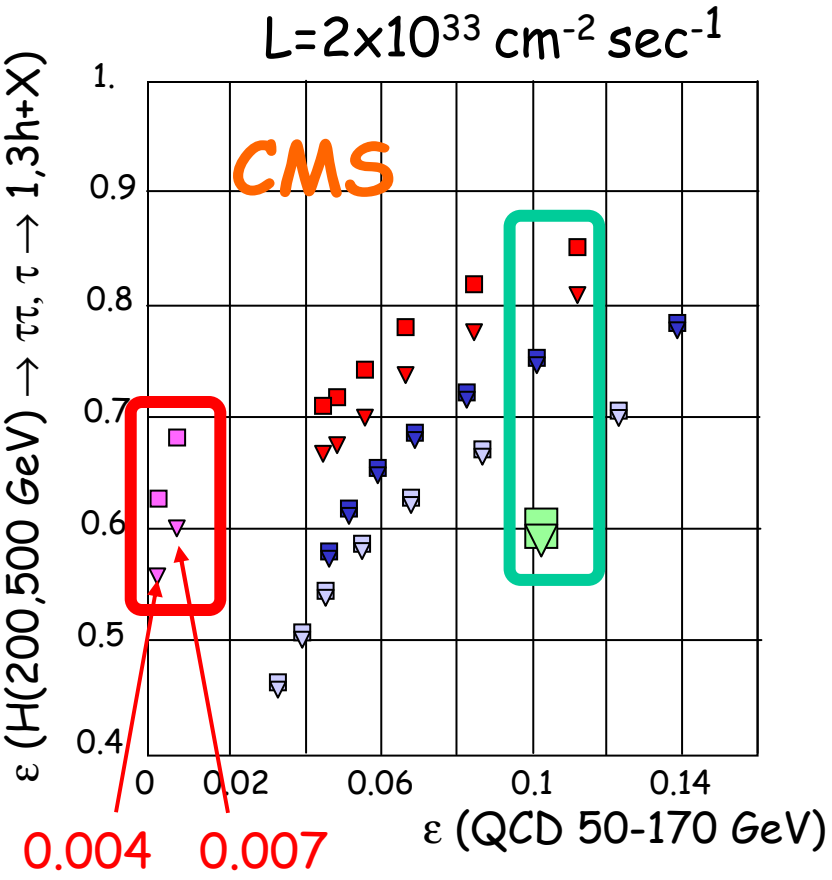




HLT τ selection @ CMS
H(200,500 GeV) → ττ, τ → 1,3h± + X

FTK





M. Neubauer -Illinois

- □ m_H=500
- ▽ m_H=200

□ ▽ Staged-Pix tau on first calo jet

■ ▼ Pix tau on first calo jet

■ ▼ TRK tau on first calo jets

■ ▼ TRK tau on both calo jets

■ ▽ Calo tau on first jet

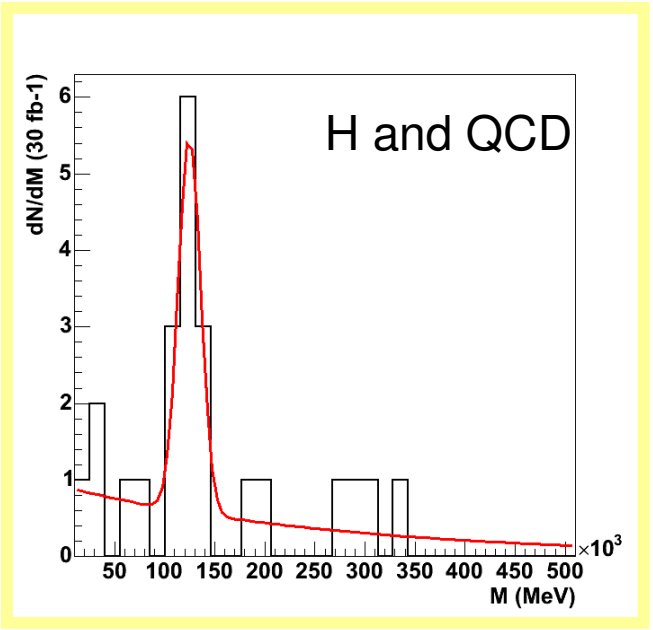
CMS TDR 6, Dec. 2002.

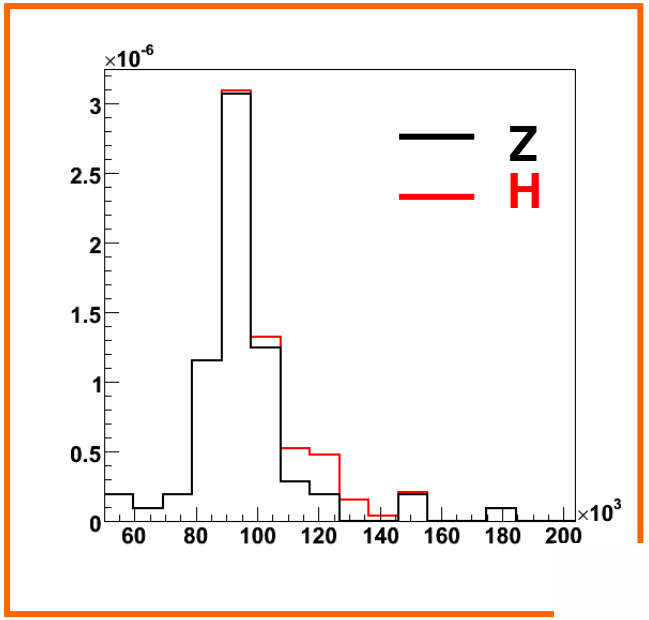
Efficiency & jet rejection could be enhanced by using tracks before calorimeters.

Physics case for τ-tagged samples: one example is VBF $Hqq \rightarrow \tau_h\tau_h qq$

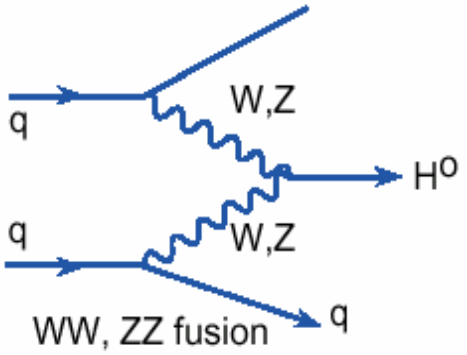
FTK

ATLFAST (9.0.4) 6 signal events and 4 bg events in 30 fb^{-1} (bg : Z+jets,ttbar,QCD dijets) with baseline trigger menu tau35i+XE45 foreseen for a luminosity of 2*10^33 $cm^{-2}s^{-1}$





F. Sarri e V. Cavasinni - Pisa



B_S -> μ μ (x3 using soft second μ)

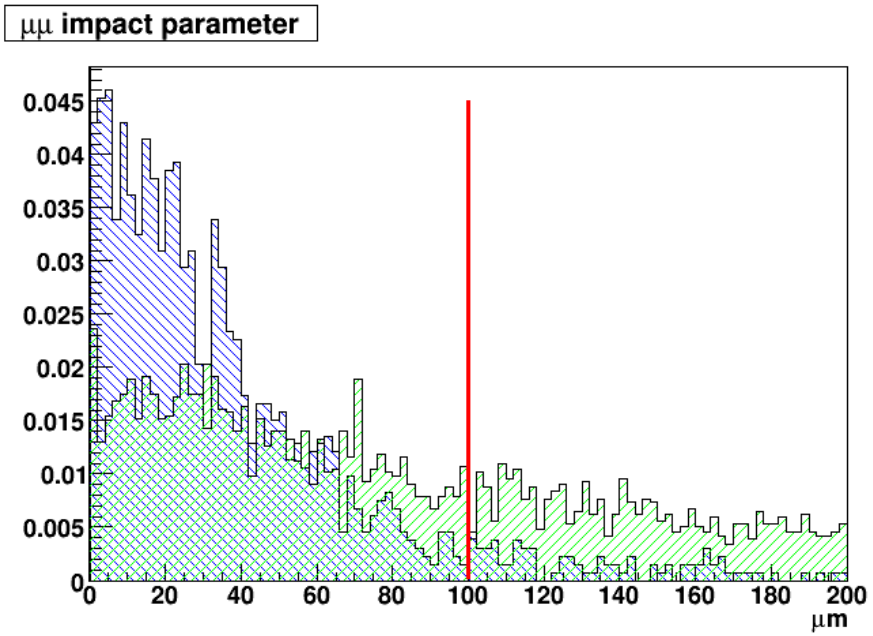
Pisa
Crescioli
e Volpi

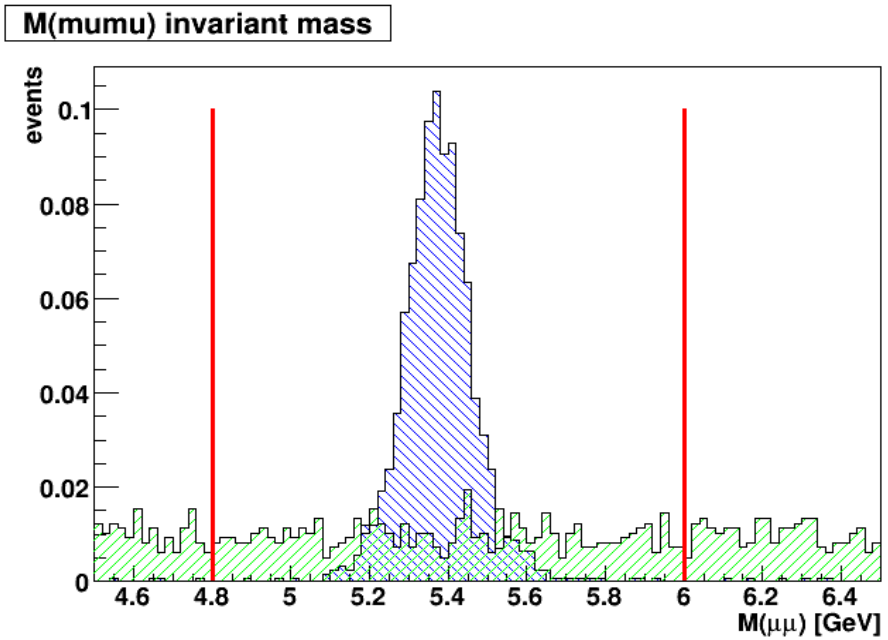
FTK

IEEE Trans. Nucl. Sci. 55, 145 (2008)
poi BS -> μ μ K*

Atlas: Level 1: 2MU6, Level 2: refine muons with tracks
Level 3: reconstruct & refine Bs

Atlas+FTK: Level 1: 1MU6, Level 2: refine muons with tracks
+ reconstruct & refine Bs Level 3….





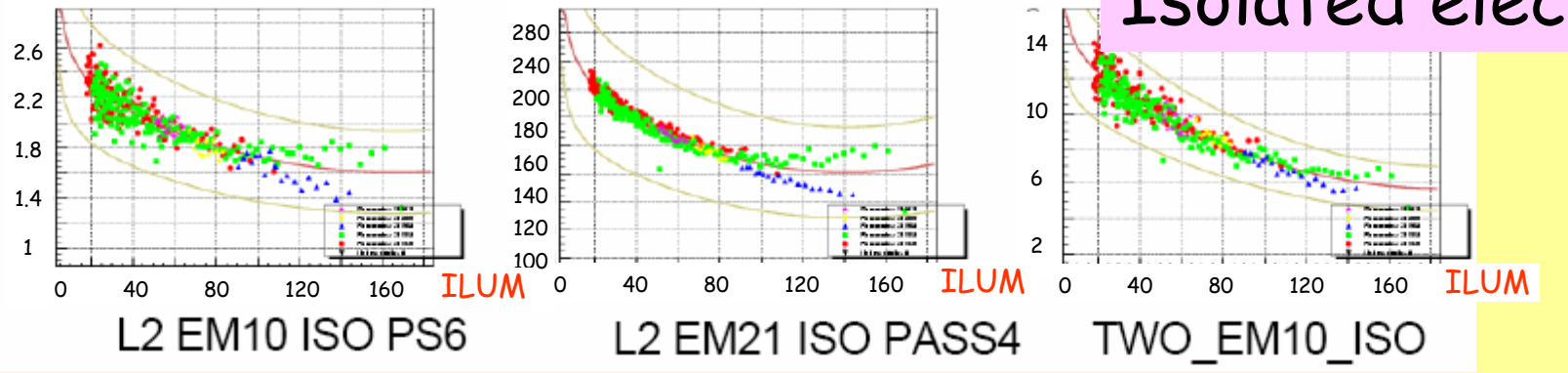
Athena + FTKsim

CDF Level-2

Isolated electrons

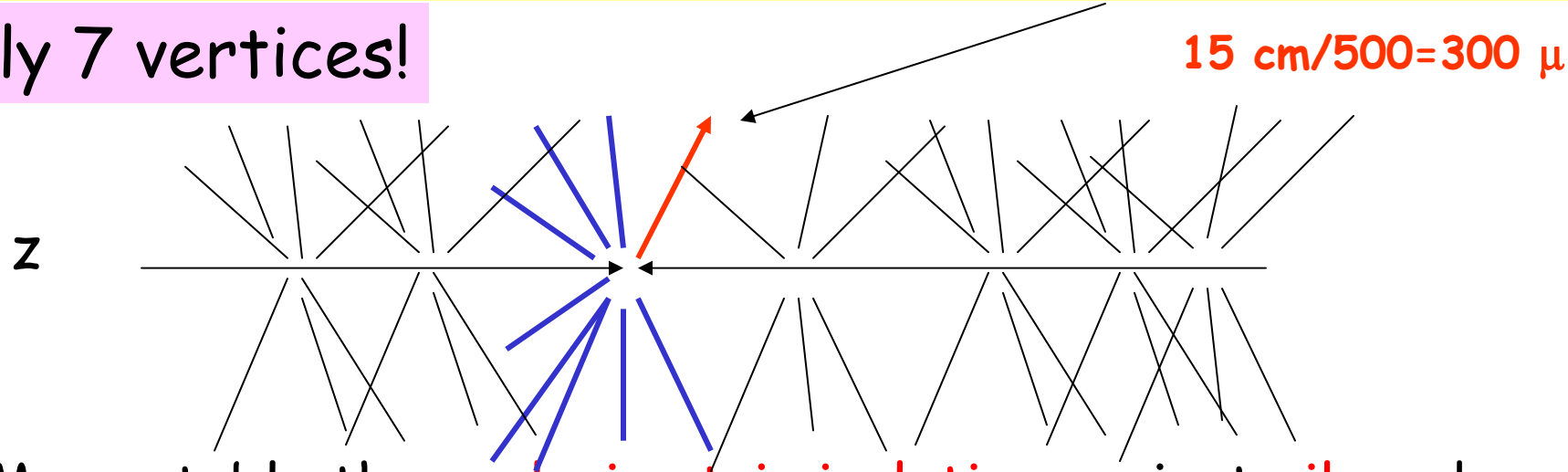
Xsection (nb)

- Rates tend to decrease with higher luminosity
  - Unique in the CDF LVL2 world?



Lepton identification: primary vertices fast identification
→ Isolation with tracks of Pt>Th and from right vertex

Only 7 vertices!

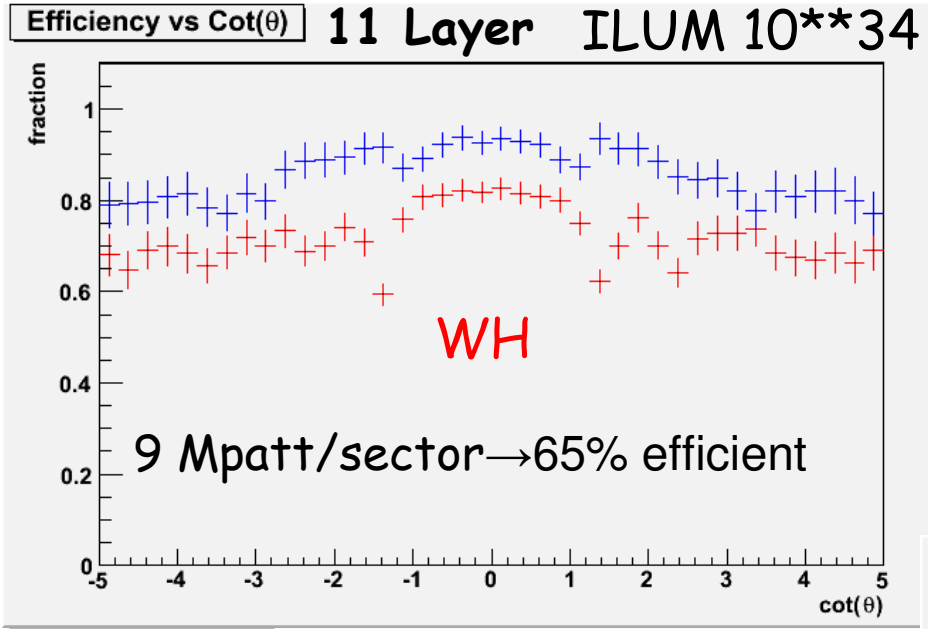


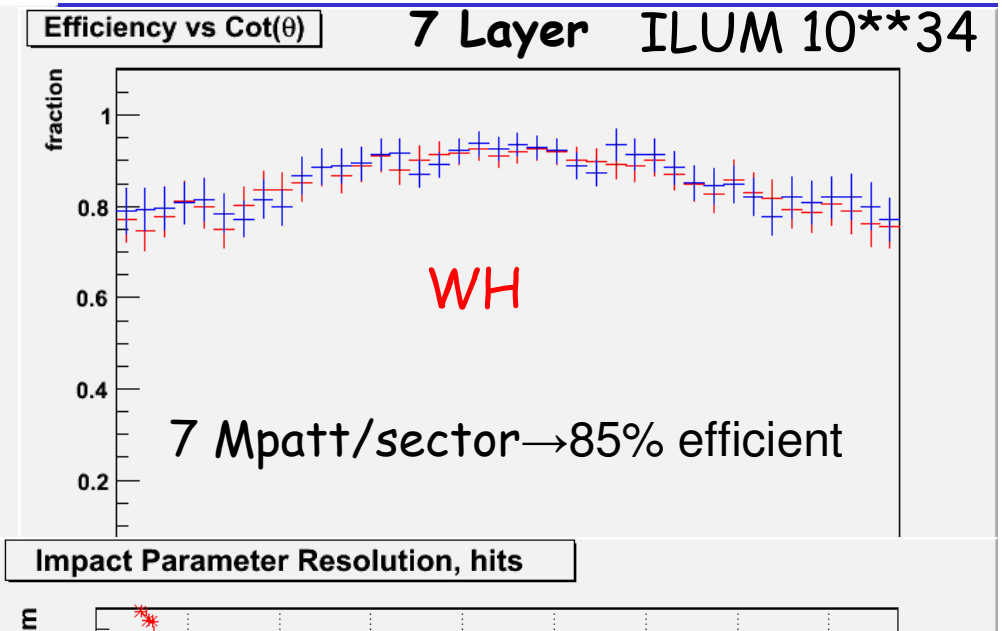
More stable than calorimetric isolation against pile-up!

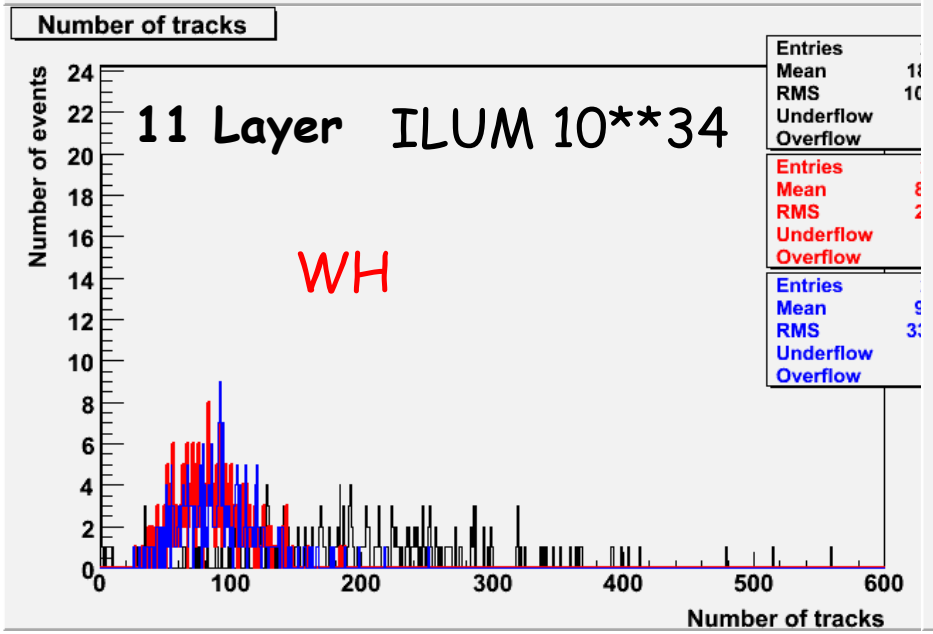
Lower Lepton thresholds! M. Dunford (Chicago)- Jinlong Zhang (ANL)

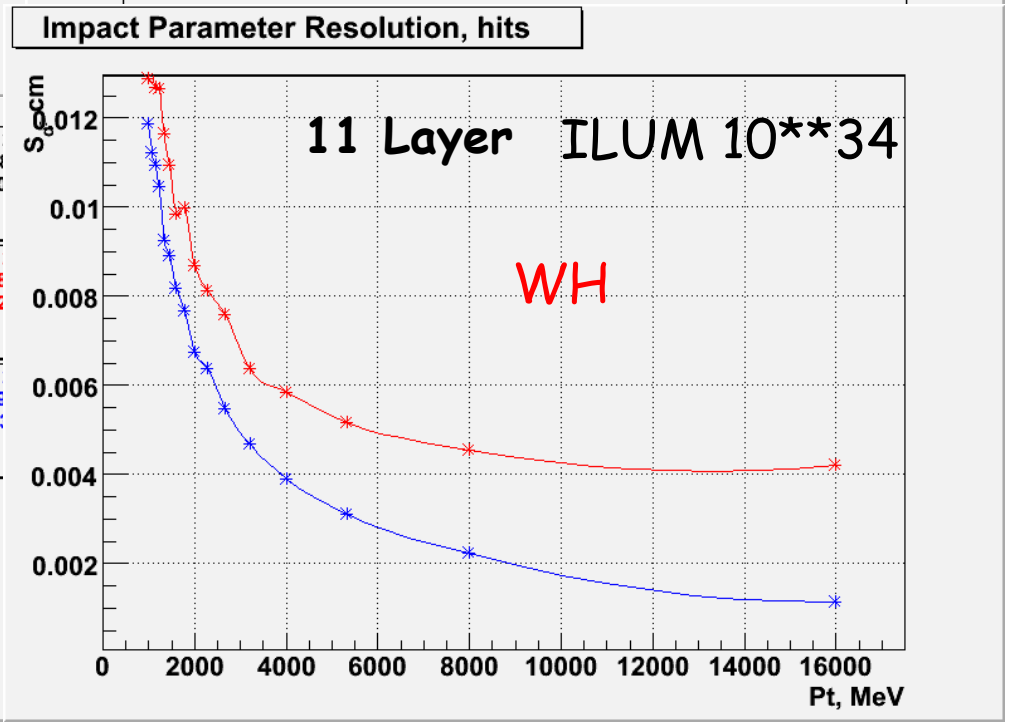
Performances Compare FTK (red) with Ipatrec (blue)

FTKSIM









CONCLUSIONS

- FTKsim is almost complete, but still un-friendly. Monitoring plots have been added. Insertion into Athena still in progress

- Timing study and hardware architecture choice: in progress this is the most complex part at the moment.

- Tau-jet and b-jet tagging performances at 10 **34 near to be ready

- Firmware/hardware development in progress: minimum needed for a reliable timing evaluation.

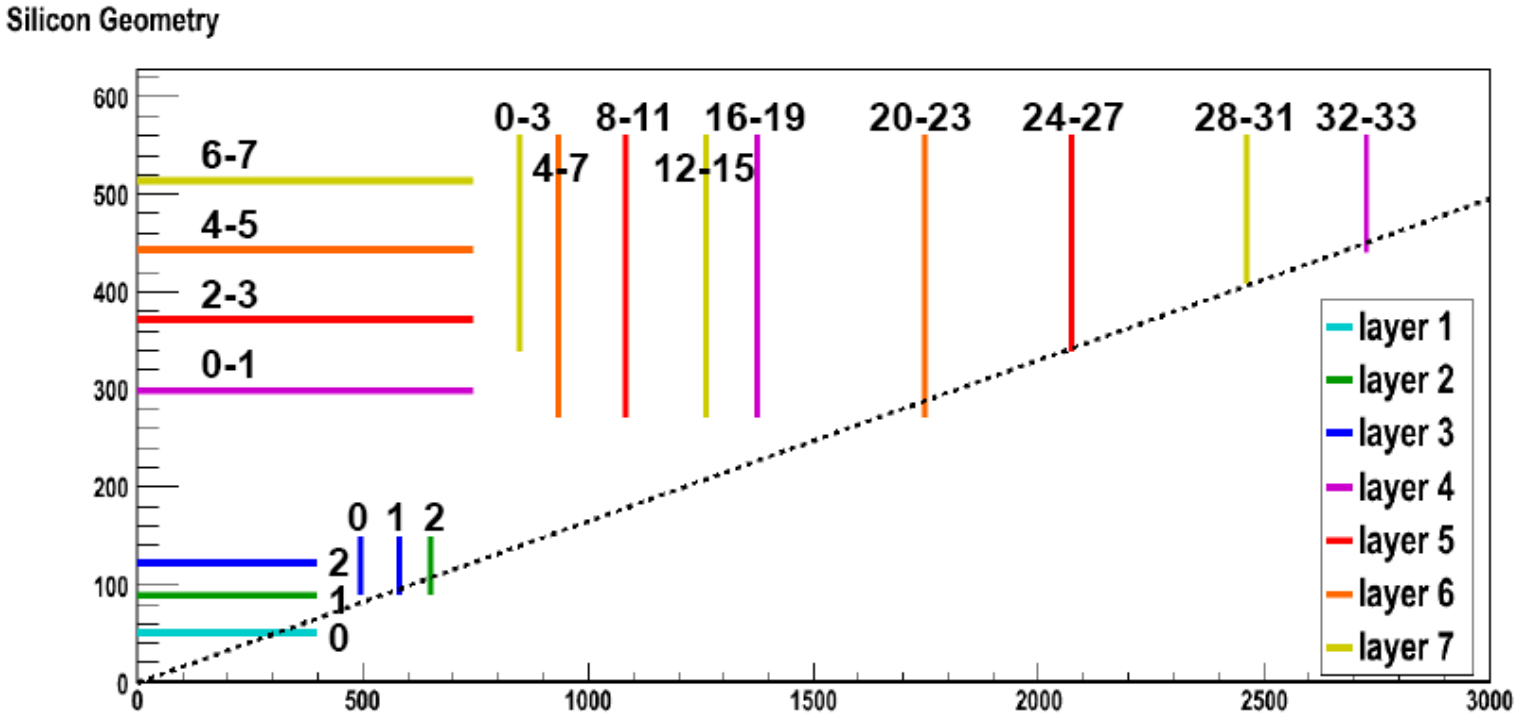
BACKUP SLIDES

FTK R&D PROPOSAL STATUS

✓ **Complete the FTK simulator:**

- use raw silicon hits as input instead of space points A. Kapliy, K. Yorita Chicago – Done.
- rapidity coverage extension from $|\eta| < 1$ to $|\eta| < 2.5$. C. Mills Harvard – Done
- very fast program for track road generation for FTKSim. F. Crescioli, G. Punzi Pisa – Done
- porting FTKSim into ATHENA A. Cerri (CERN)& M. Dunford (Chicago) strongly involved into commissioning & Run – Partially Done G.Volpi going ahead low priority

- Layer -to- logical layer conversion



✓Study FTK performance as a function of instantaneous luminosity (A.Kaplin-Chicago, A. McCarn-Illinois) :

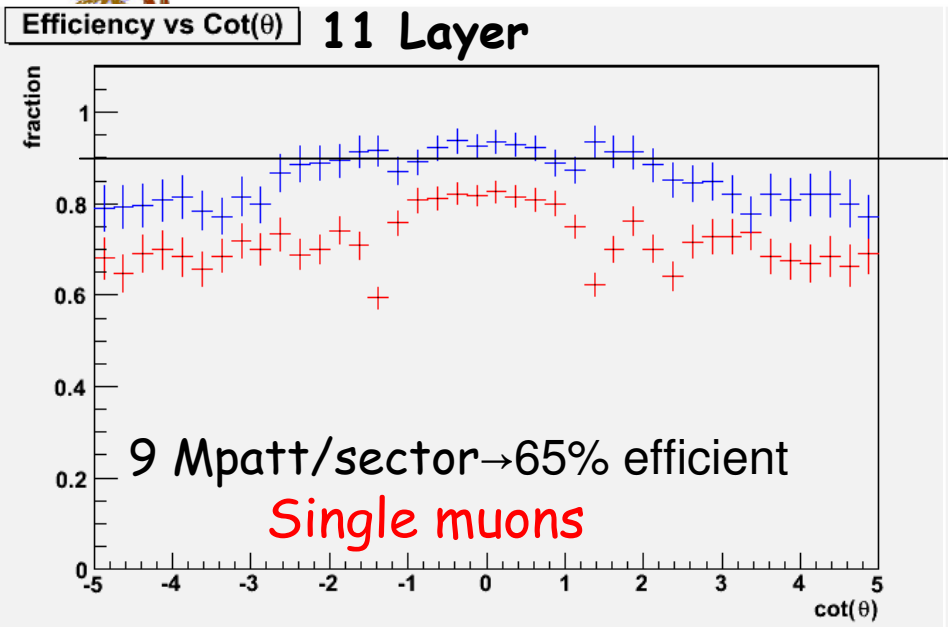
✓ **Determine the optimal size of the AM system**: G. Volpi, G. Punzi, M. Dell'Orso work in progress to handle overlap regions → specific tools to clean-up the bank relative to overlap regions

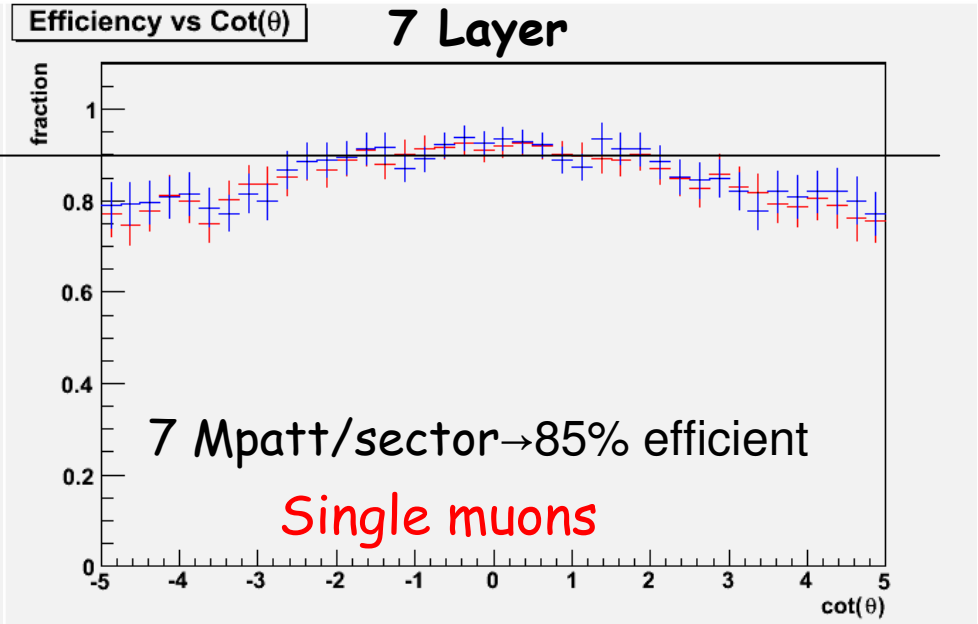
✓ **Produce specifications for each board**: DF (strips & pixels), DO, AM, TF: in progress

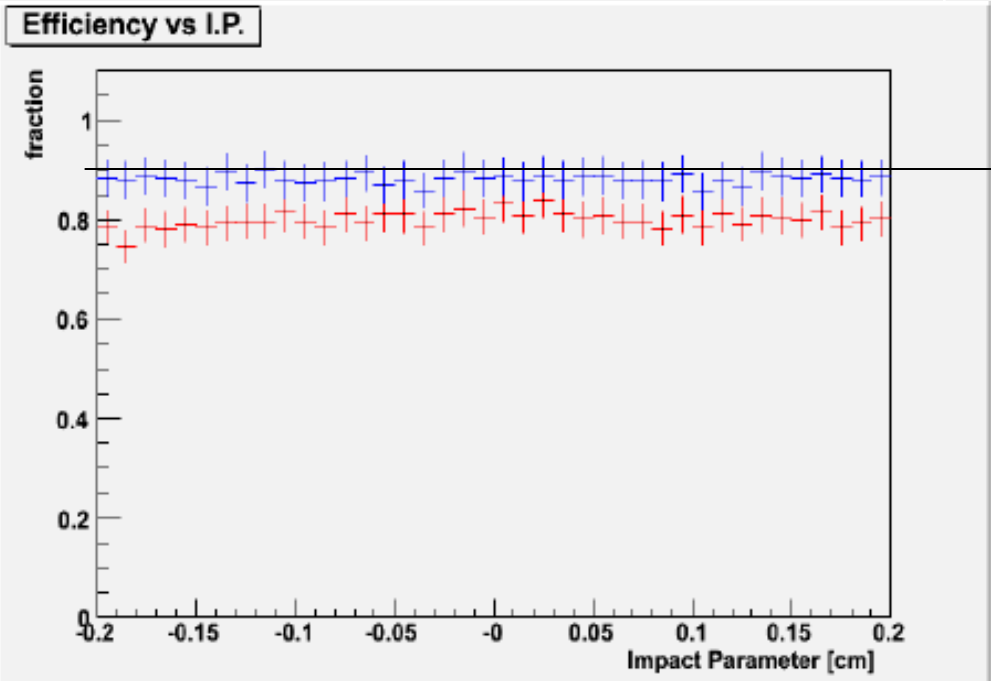
- ❑ DF: pixel 2D cluster finding, A. Annovi (Frascati); DF Mother board + Slinks etc (Argonne National Laboratory)
- ❑ AM: new prototype M.Piendibene, F.Crescioli, P.Giannetti (Pisa) – design new small chip in 2009 L.Sartori (Pisa).
- ❑ Track Fitter: from the CDF GigaFitter to a new powerful system for LHC (Pisa – Chicago)
- ❑ Data Organizer: waiting for AM & TF decisions (M. Neubauer ILL)
- ❑ Global FTK Timing studies: work in progress, K. Yorita (left Chicago, moved to Waseda-Japan)
- ❑ level-2 timing - same samples: in progress (M. Neubauer ILL)
- ❑ connection to ROS-L2 CPUs (Waseda-Japan)

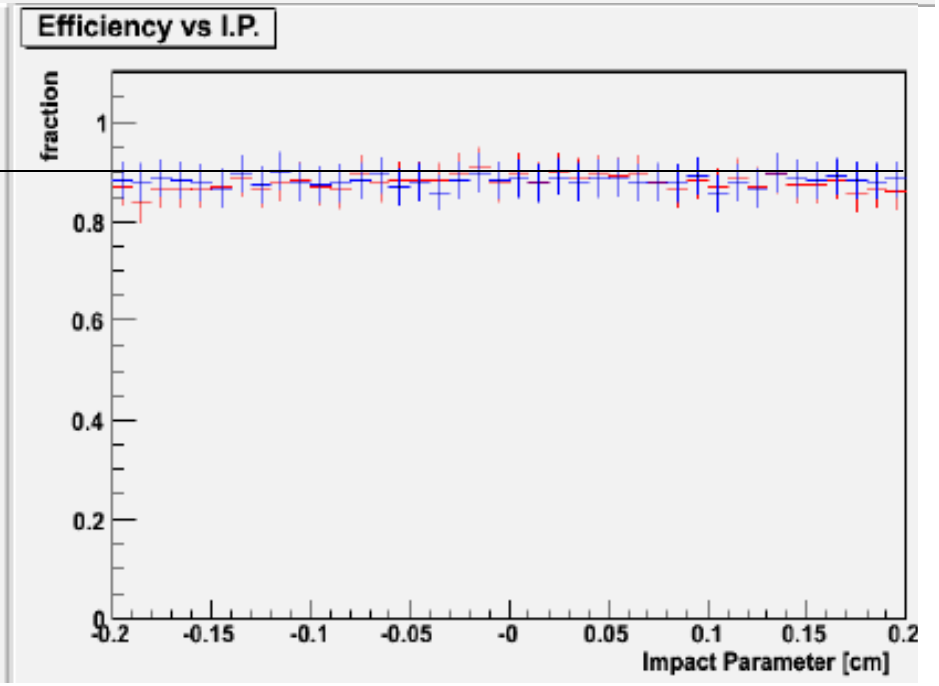
✓ **Specify the needed firmware**: in progress

Performances (A. Kapliy): FTK (red) with Ipatrec (blue)



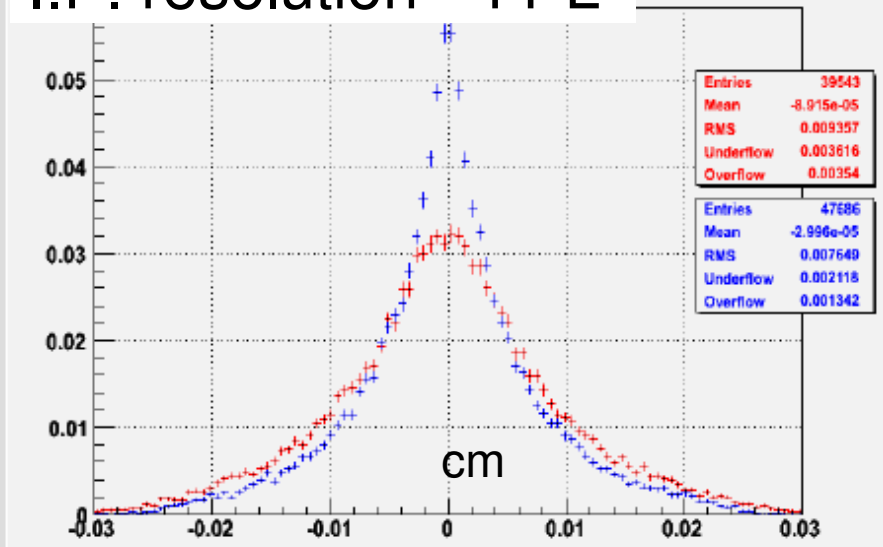




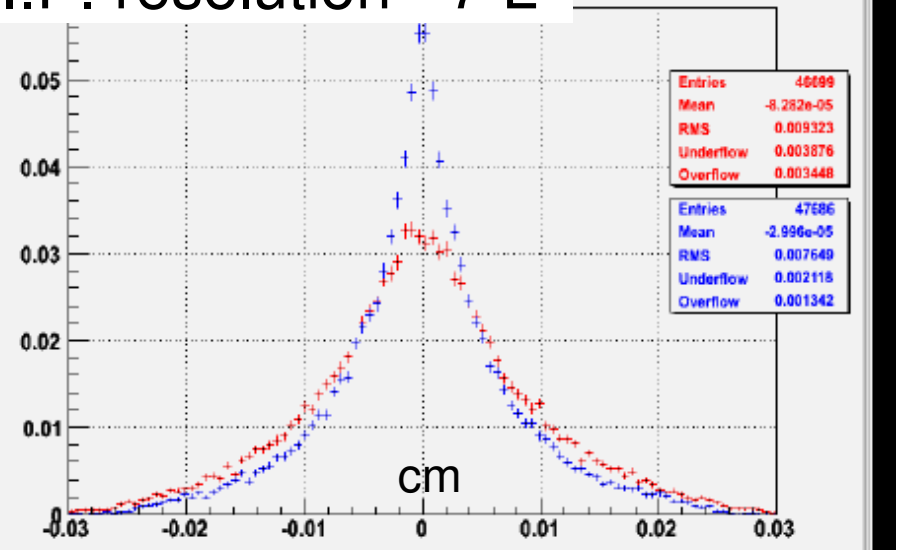


Performances (A. Kapliy): : FTK (red) with Ipatrec (blue)

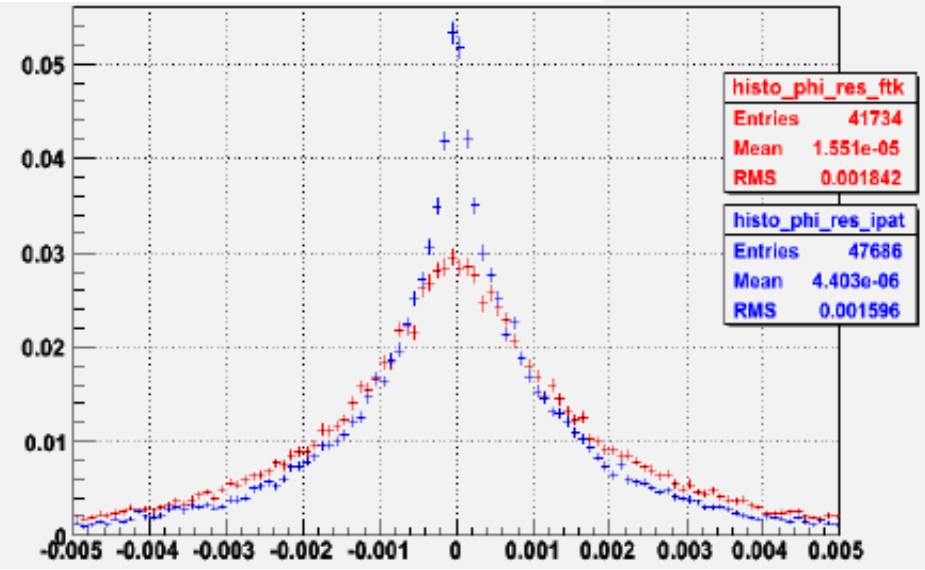
I.P. resolution - 11 L



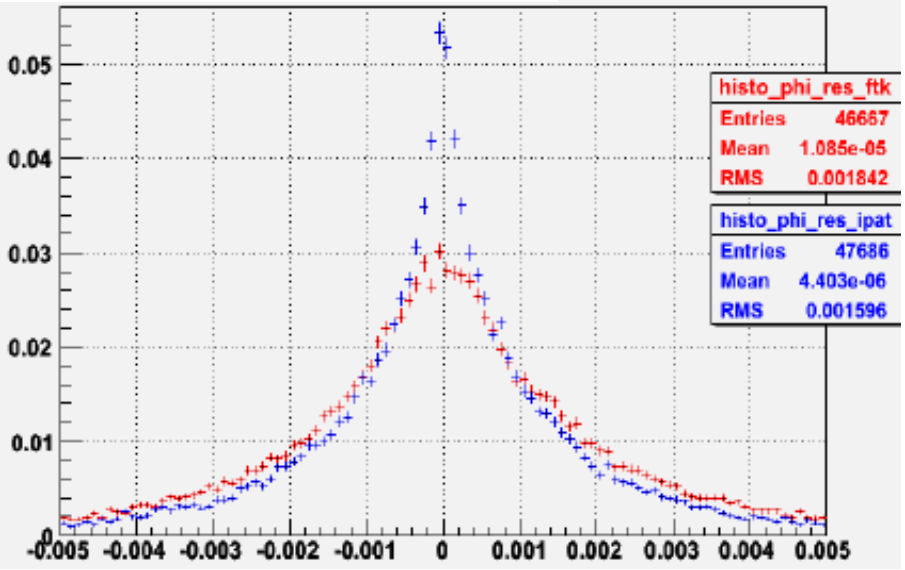
I.P. resolution - 7 L



Phi resolution - 11 L

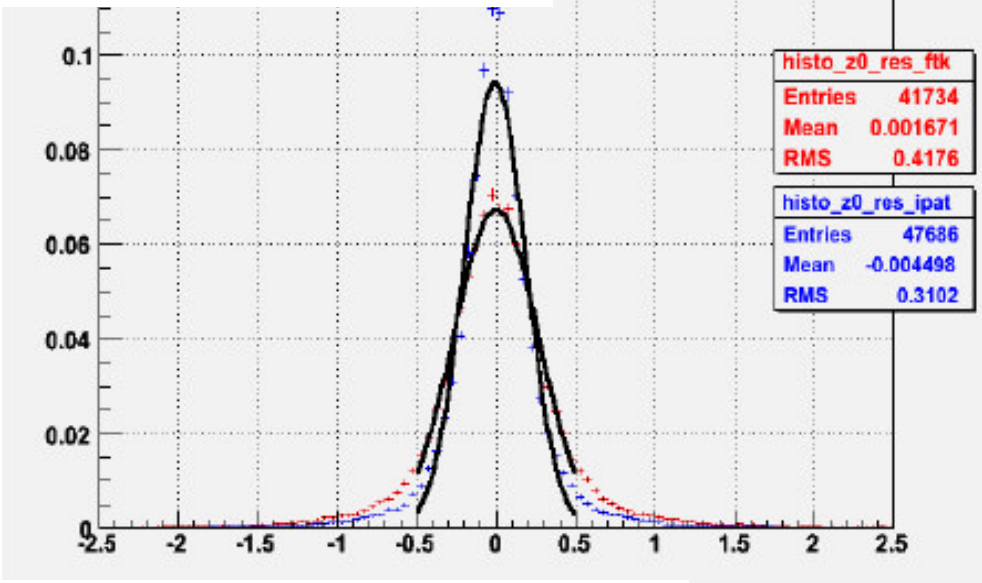


Phi resolution - 7 L

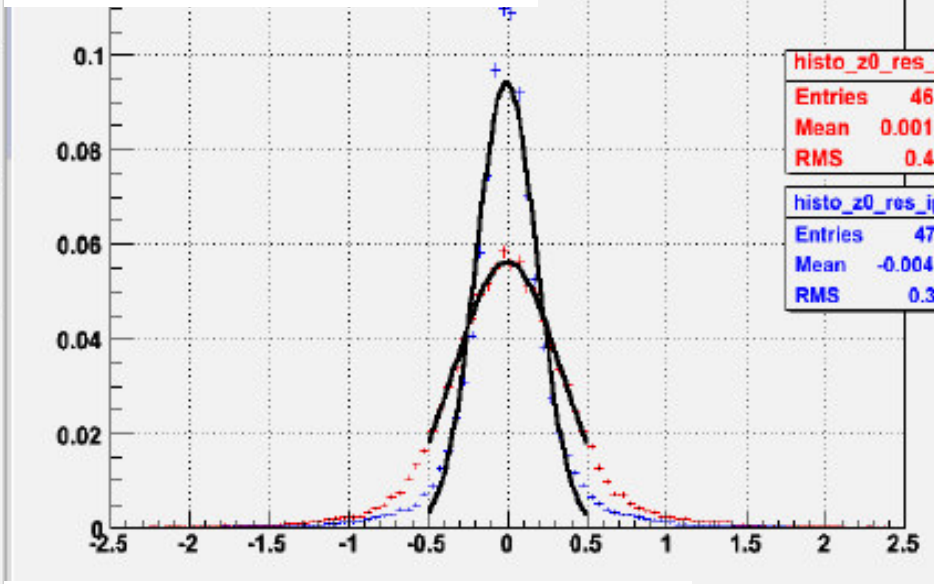


Performances (A. Kapliy): : FTK (red) with Ipatrec (blue)

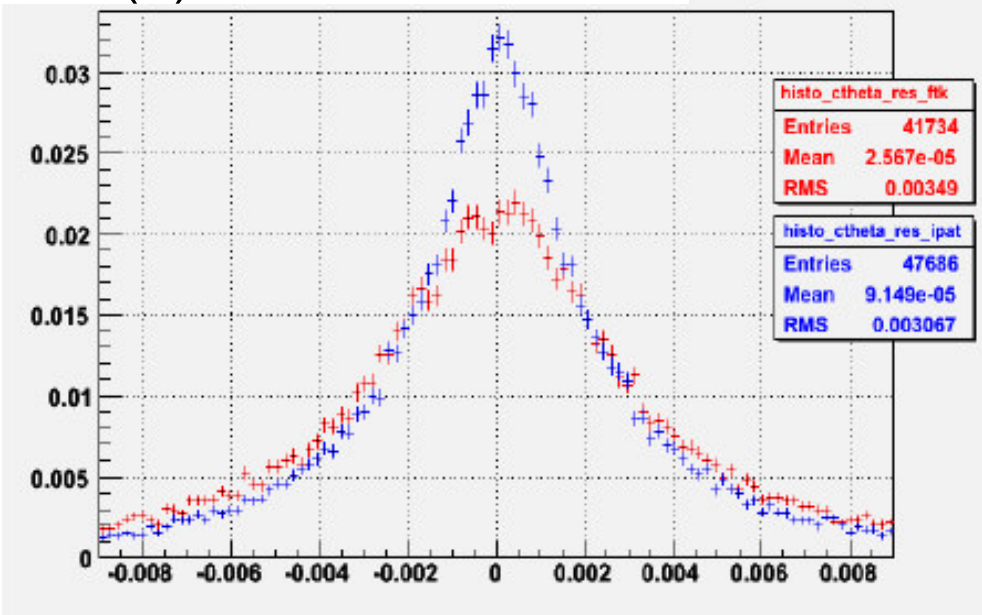
Z resolution - 11 L



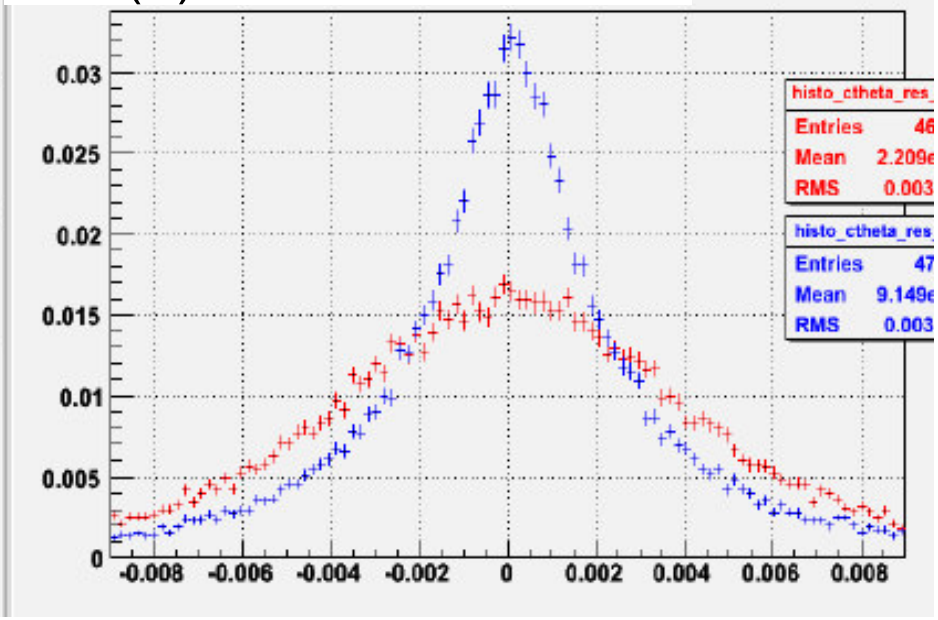
Z resolution - 7 L



Cot(θ) resolution - 11 L

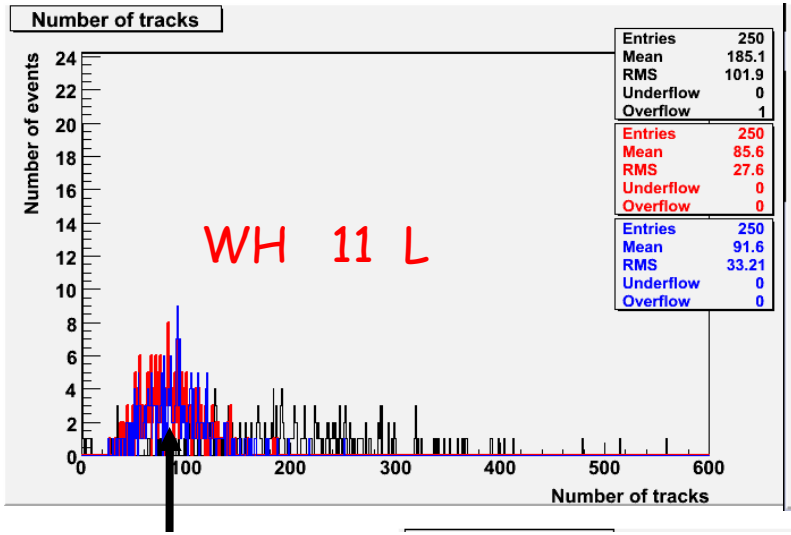


Cot(θ) resolution - 7 L

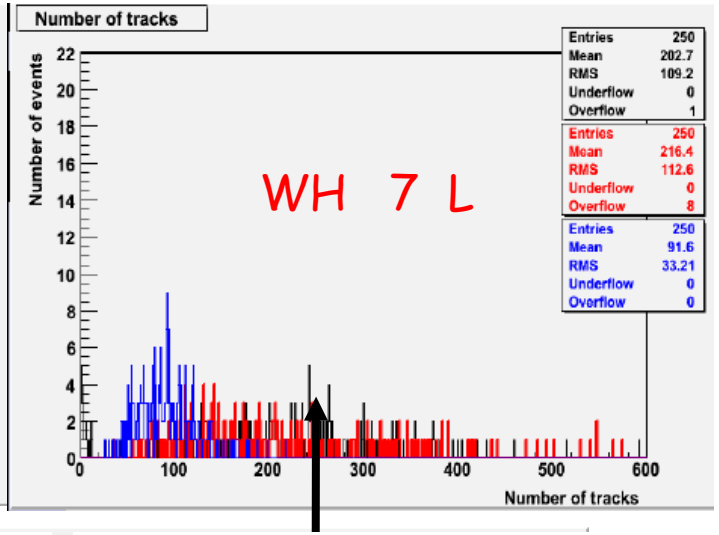


Performances (A. Kapliy): : FTK (red) with Ipatrec (blue)
WHbb @ 10^34 (11L & 7 L): fakes?

Number of tracks/event

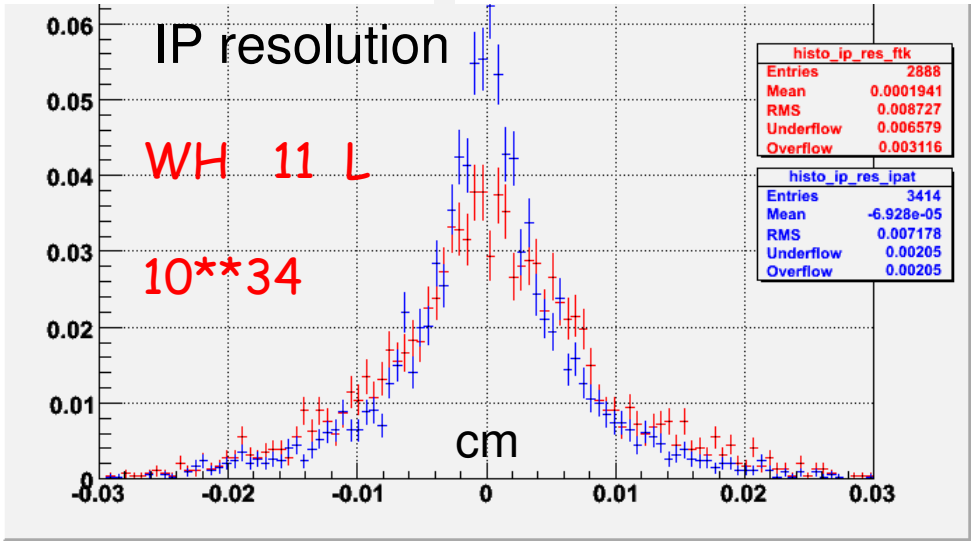


Number of tracks/event



FTK has same behaviour as **IPATREC**

FTK has much more fakes than **IPATREC**



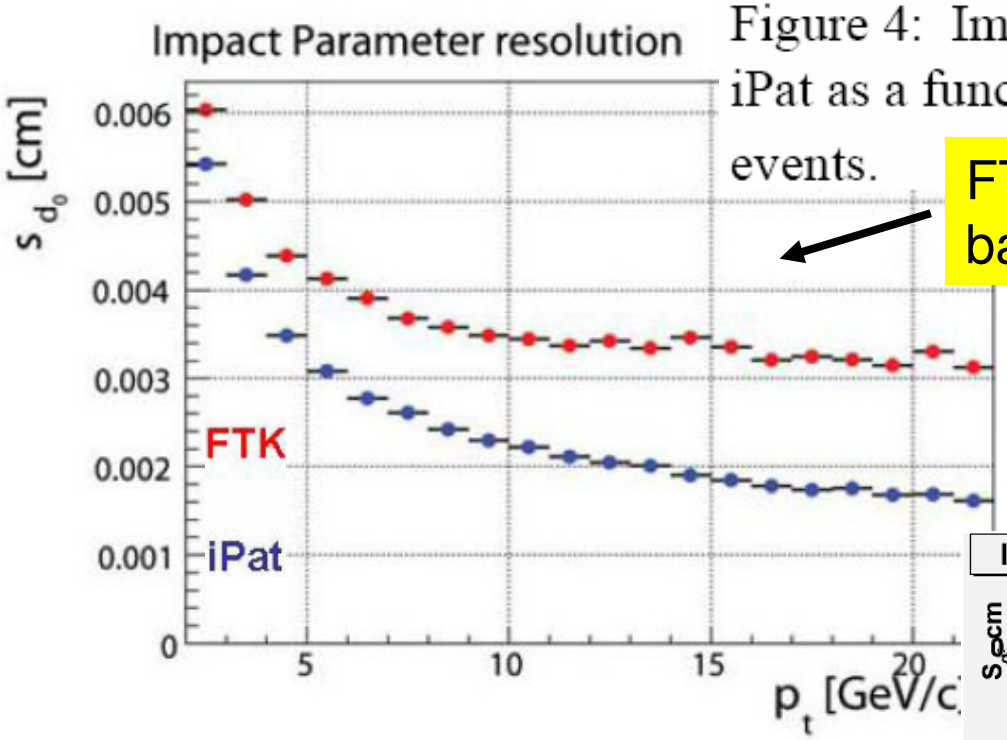
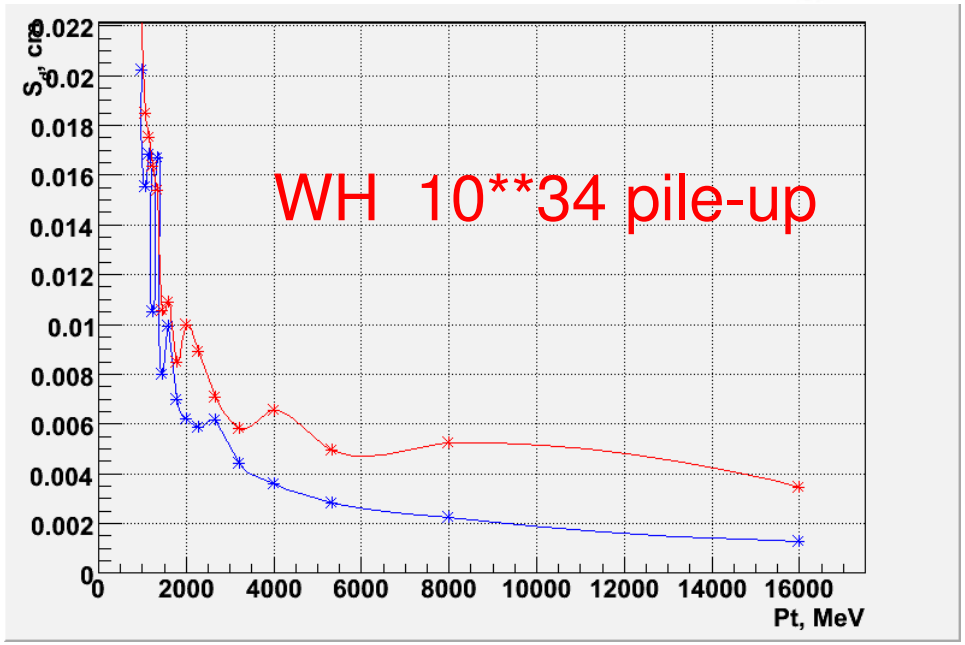
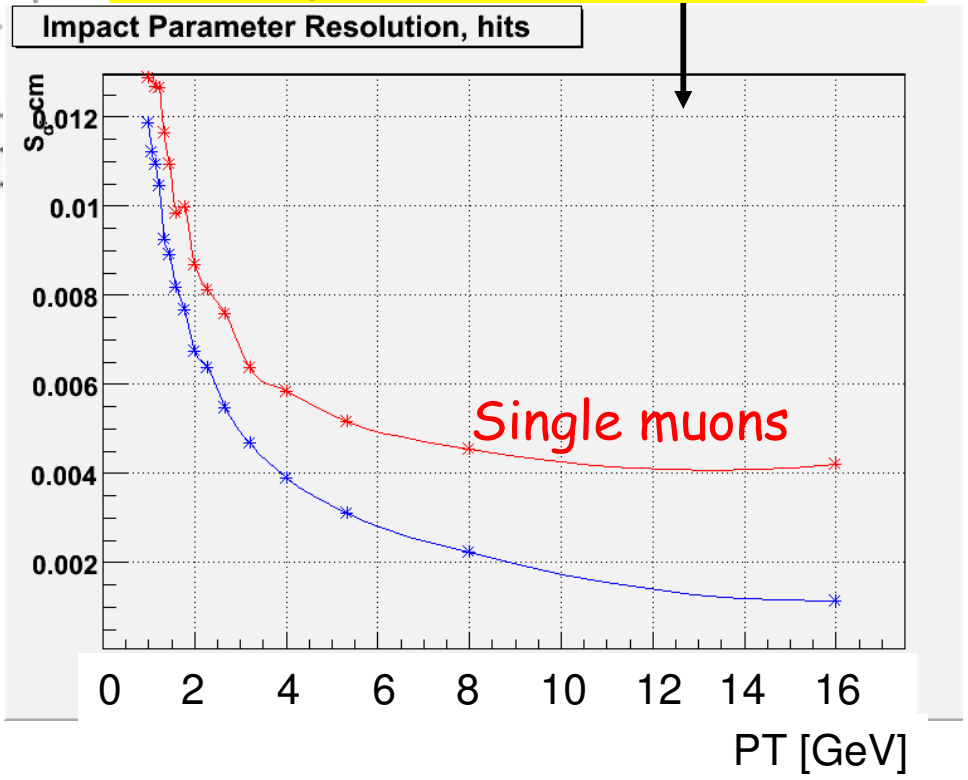


Figure 4: Impact-parameter resolution for FTK and iPat as a function of track P_T for muons in $B \to \mu\mu$ events.

FTK proposal: no pile-up
barrel only – space points

November 2008: nopile-up
– full η coverage raw hits

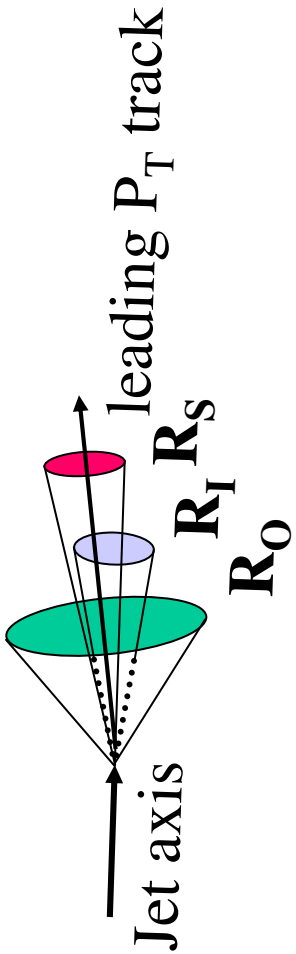


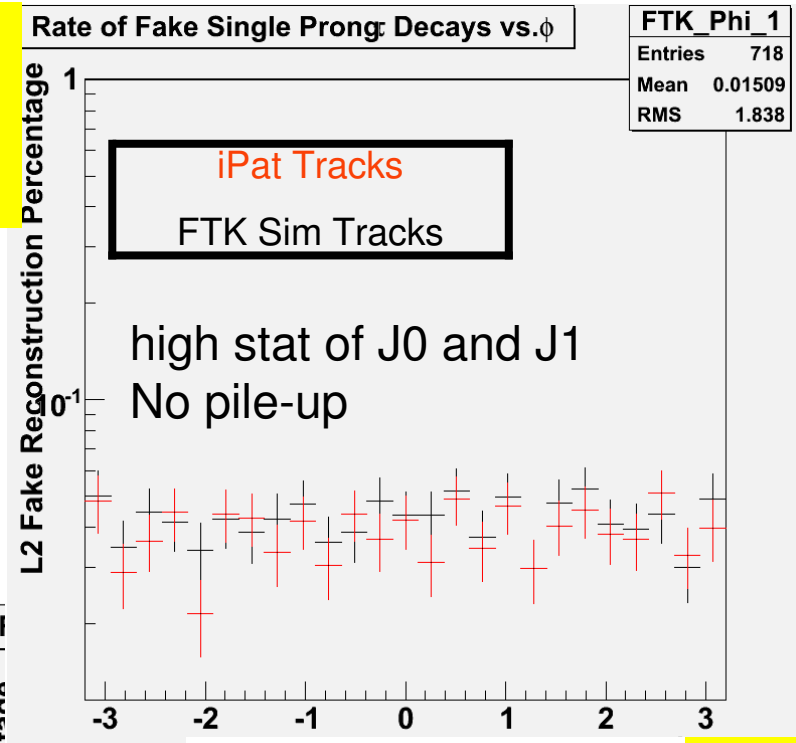


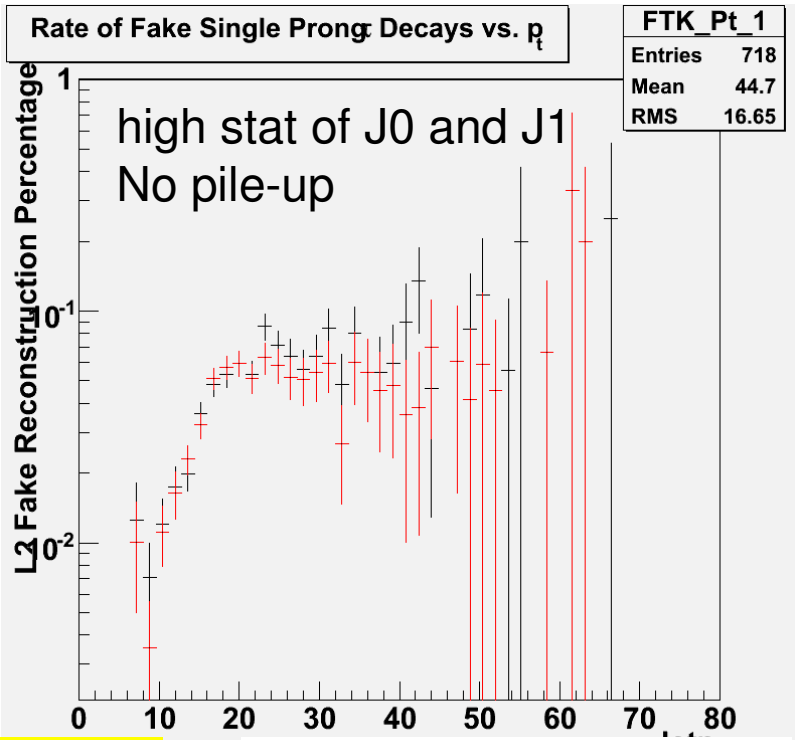
Tau Fakes

A. McCarn

Single Prong (1,0)



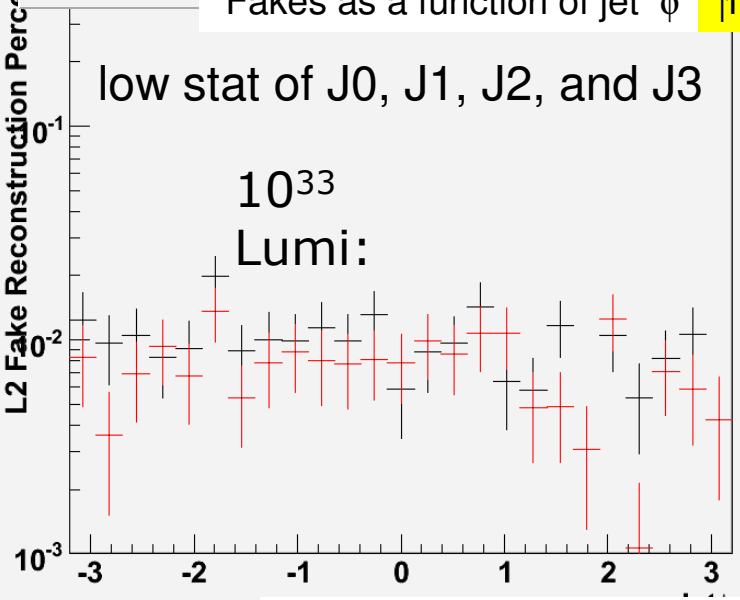


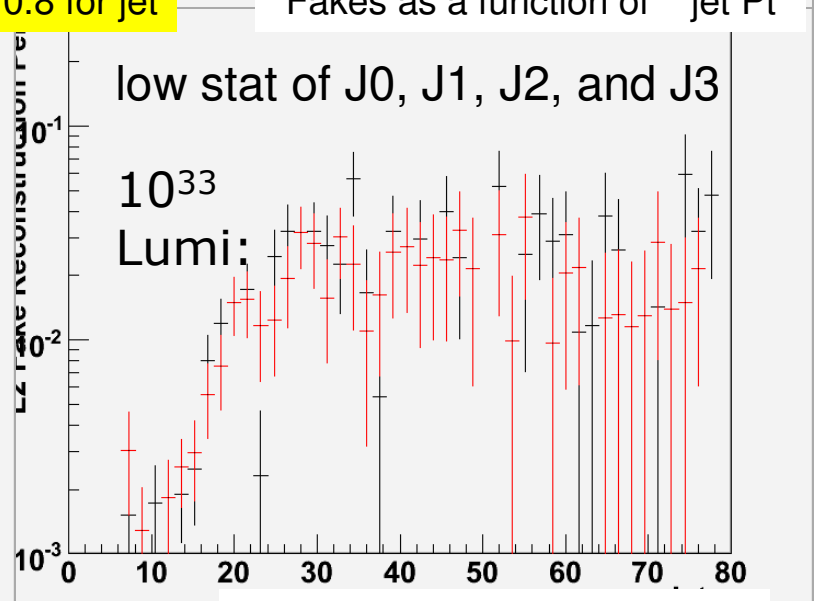


Fakes as a function of jet ϕ

$|\eta| < 0.8$ for jet

Fakes as a function of jet Pt



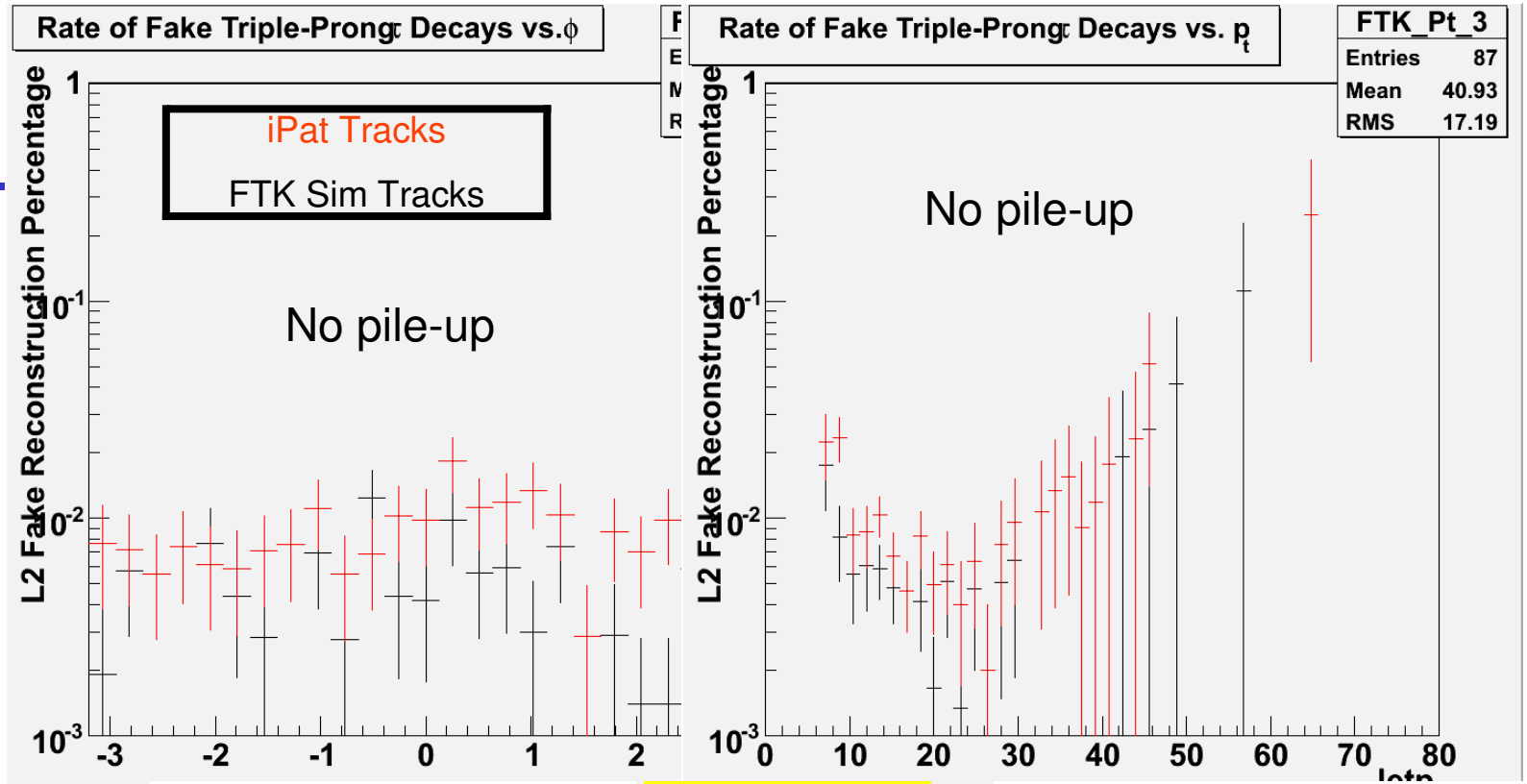


Fakes as a function of jet ϕ

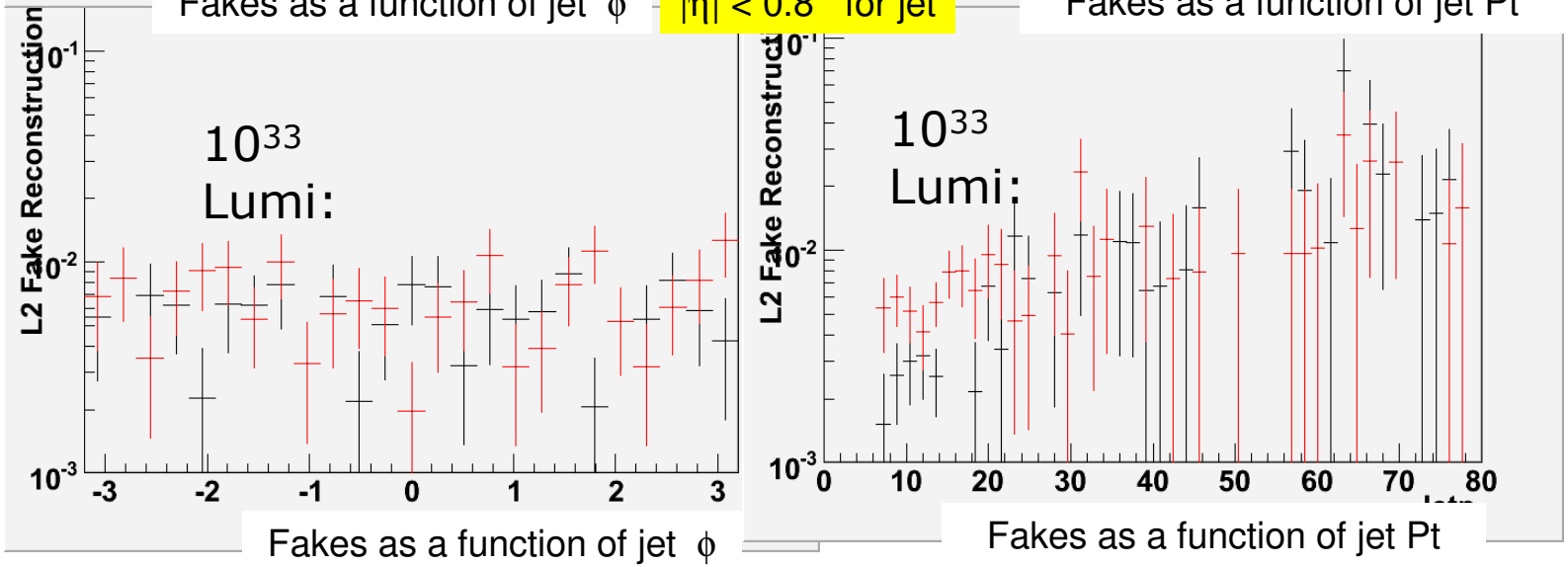
Fakes as a function of jet Pt

Triple Prong (3,0)

FTK similar to IPATREC

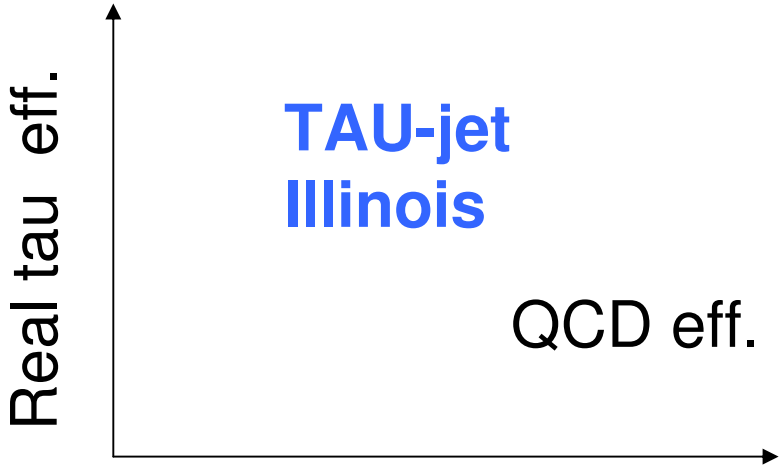


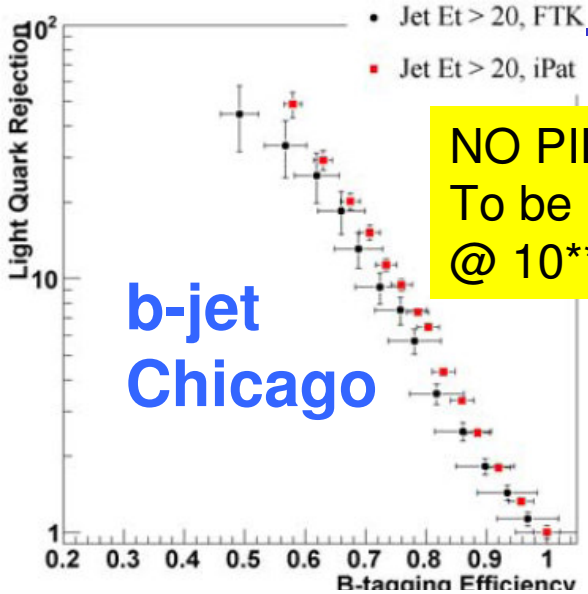
Fakes as a function of jet ϕ | $|\eta| < 0.8$ for jet | Fakes as a function of jet Pt



Fakes as a function of jet ϕ | Fakes as a function of jet Pt

Next step: produce these plots for taus and bs at 10**34





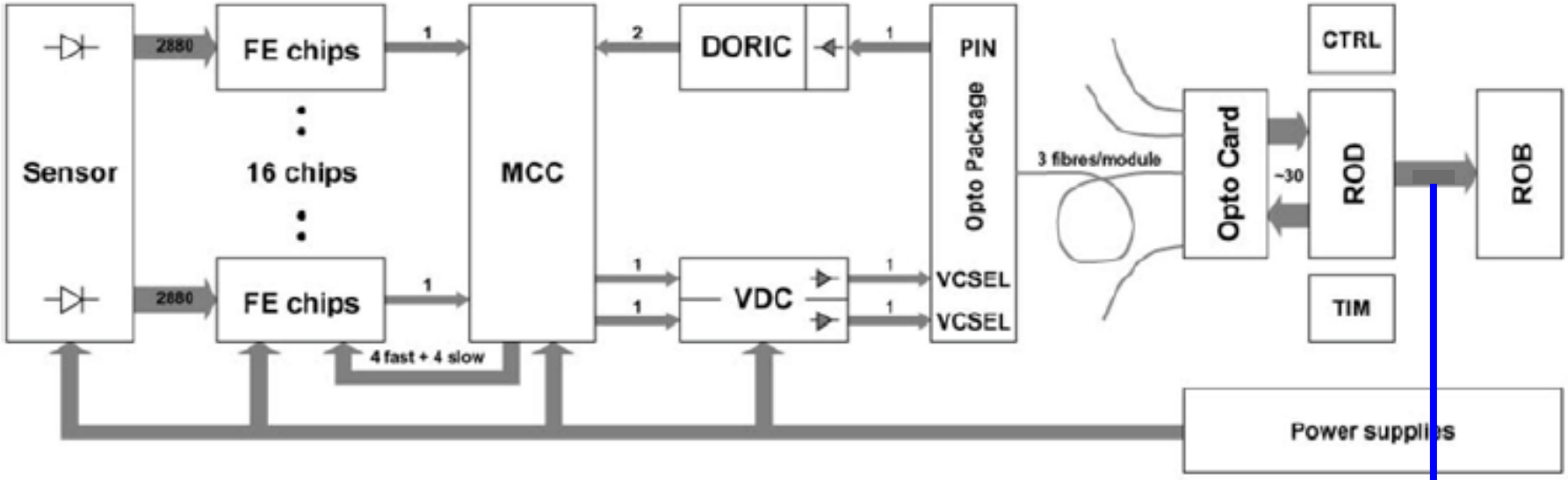
NO PILE-UP
To be repeated
@ 10**34

Figure 5: Light-quark rejection vs. *b*-tag efficiency for FTK and iPat from the standard WH samples.

Next step: apply the plots to physics case

Z→bb, Hbb, Hidden Valley, qqH →qqττ,
+ B → K*μμ + track-based lepton isolation

Data Flow

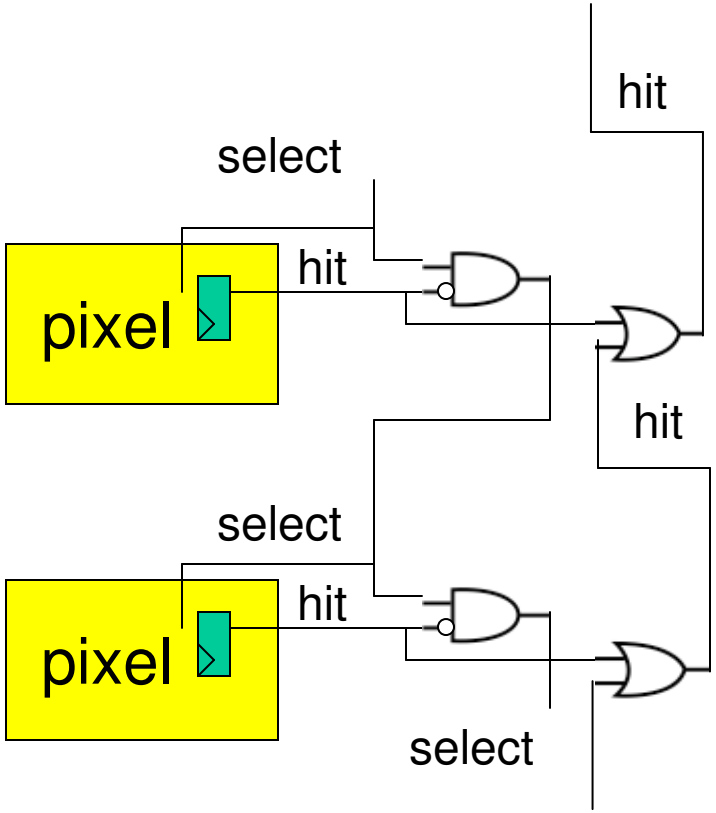


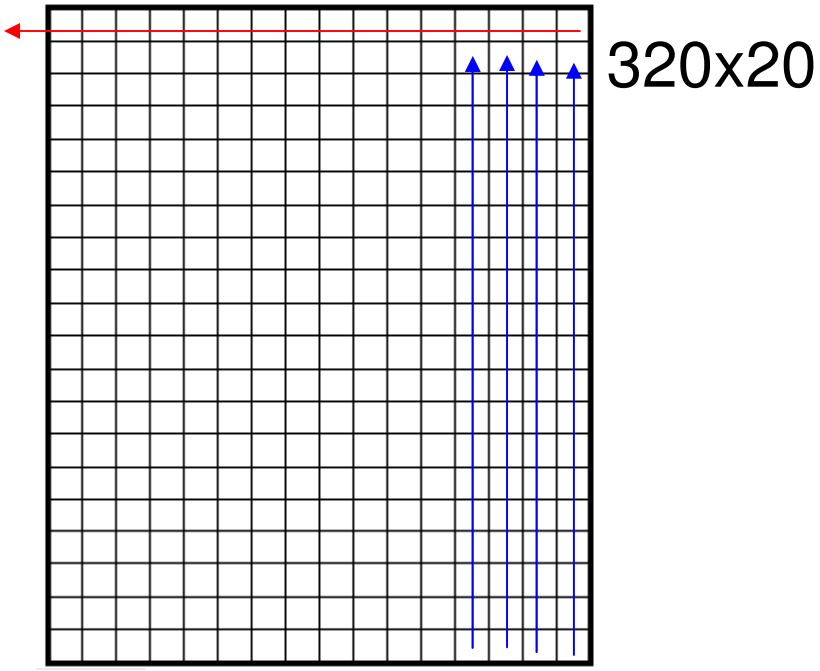
Total 120 S-links
15 S-links/region

Clustering board

Several modules merged by 1 ROD
16 FE chips merged by 1 module
Design clustering for 1 module
Modules processed sequentially
Total hit rate < 40MHz
Events @ 100kHz --->
less than 400 average hits/ROD

Readout logic

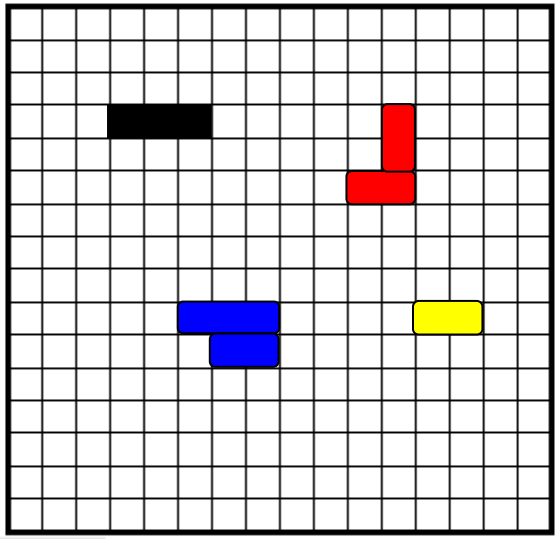




- X 320 pixels in a column

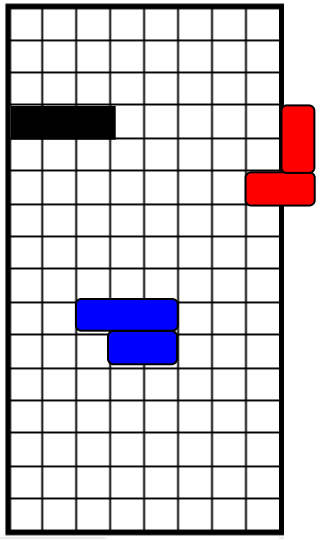
How does it work?

Module data



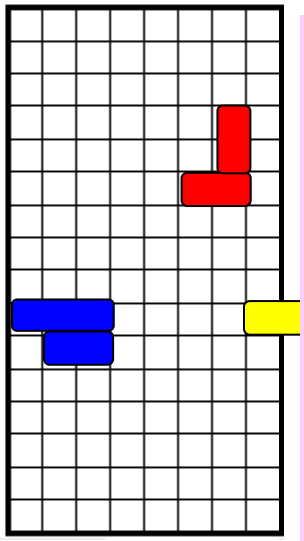
Eta direction -->

Fill 328x8 slice like this



Read 1st cluster

Fill 328x8 slice like this



Read 2nd cluster

And so on

328x8 18ns
14% area
~55MHz
2 clk/hit->hit rate 27MHz

In 1 FPGA
Can fit 3 (328x8) grids
<50% area
hit processing at ~80MHz rate
This means 2 S-link for FPGA
Total 15 Slink/sector

Shift of hits comes for free! Just use the slice as a circular buffer in the eta direction. Then hits are shifted by redefining first column.

An initial Timing Model for the FTK Core
Data Driven system, pipeline simulation, event sync