INSIDE Meeting

Report on the group activities on the

HW PET detector Back End Electronics

20 January 2016

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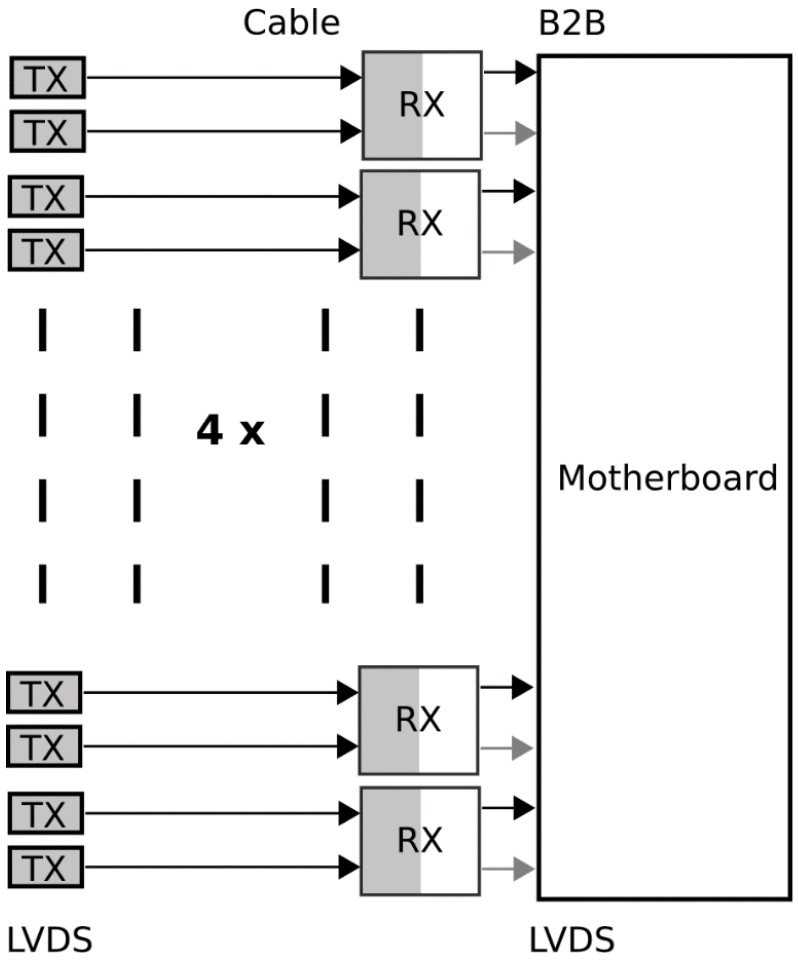
The INSIDE PET Back End Electronics

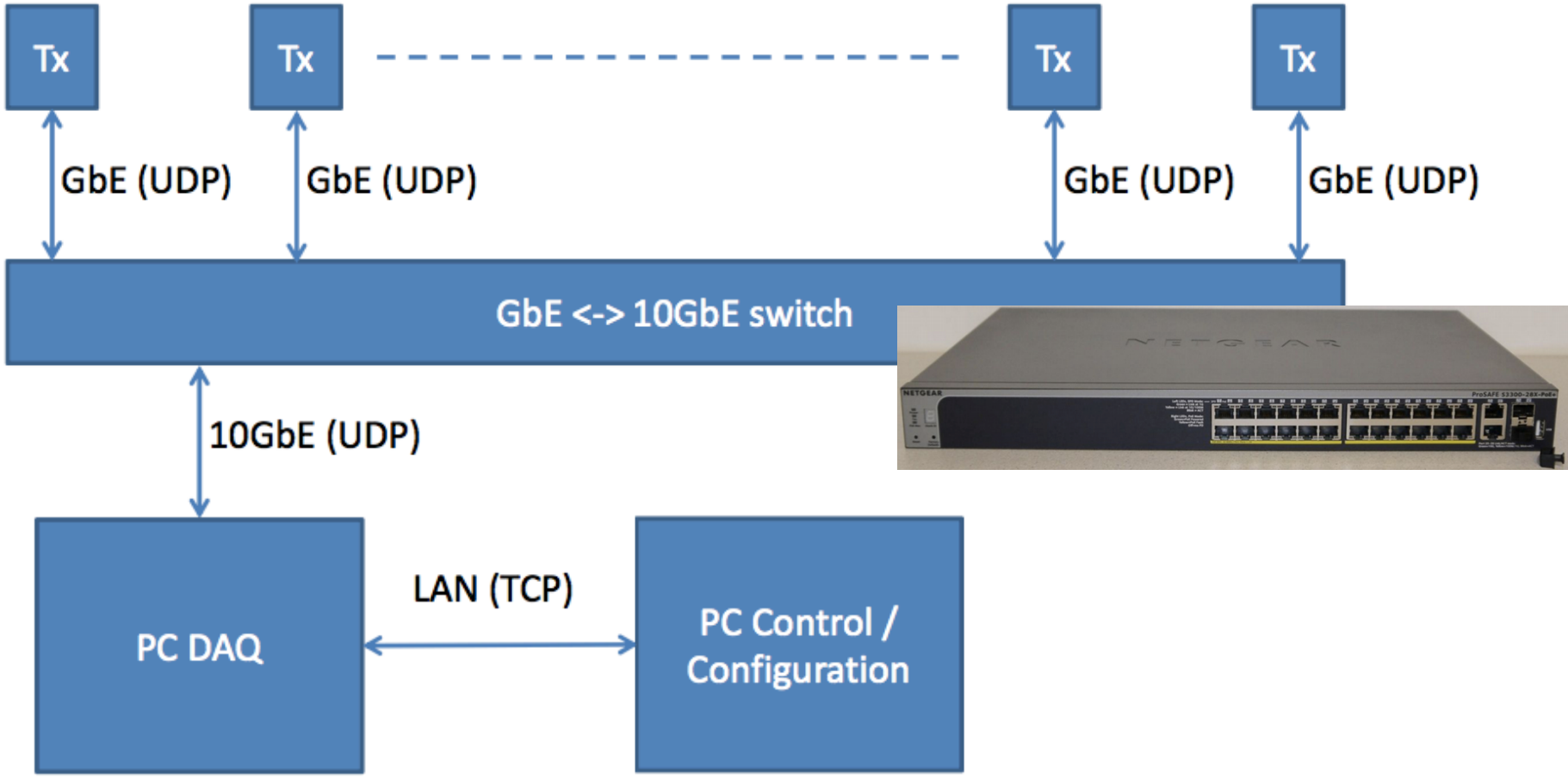
- Initial architecture
  - Provide a full in-beam PET system able to sustain annihilation and prompt photon rates during the beam irradiation
  - 30 kHZ/cm^2 maximum sustainable single rate
  - 16 independent modules
- Main changes
  - The TX-RX interconnection has changed (now they use Ethernet connections)
  - The TX boards are now calibrated by a separate unit



ASICs calibration

- The TX boards need calibration data from the user through the Ethernet interface
- This is being done by a preliminary LabView script originally developed by Richard Wheadon and extended by Matteo Morrocchi
- The translation to SW/FW on the motherboard required further planning to be completed
- Agreed strategy: develop an alternate calibration software and use it to test if calibration through the motherboard is needed at all and, in any case, to plan for the final calibration subsystem
- Two alternate methods have been carried out

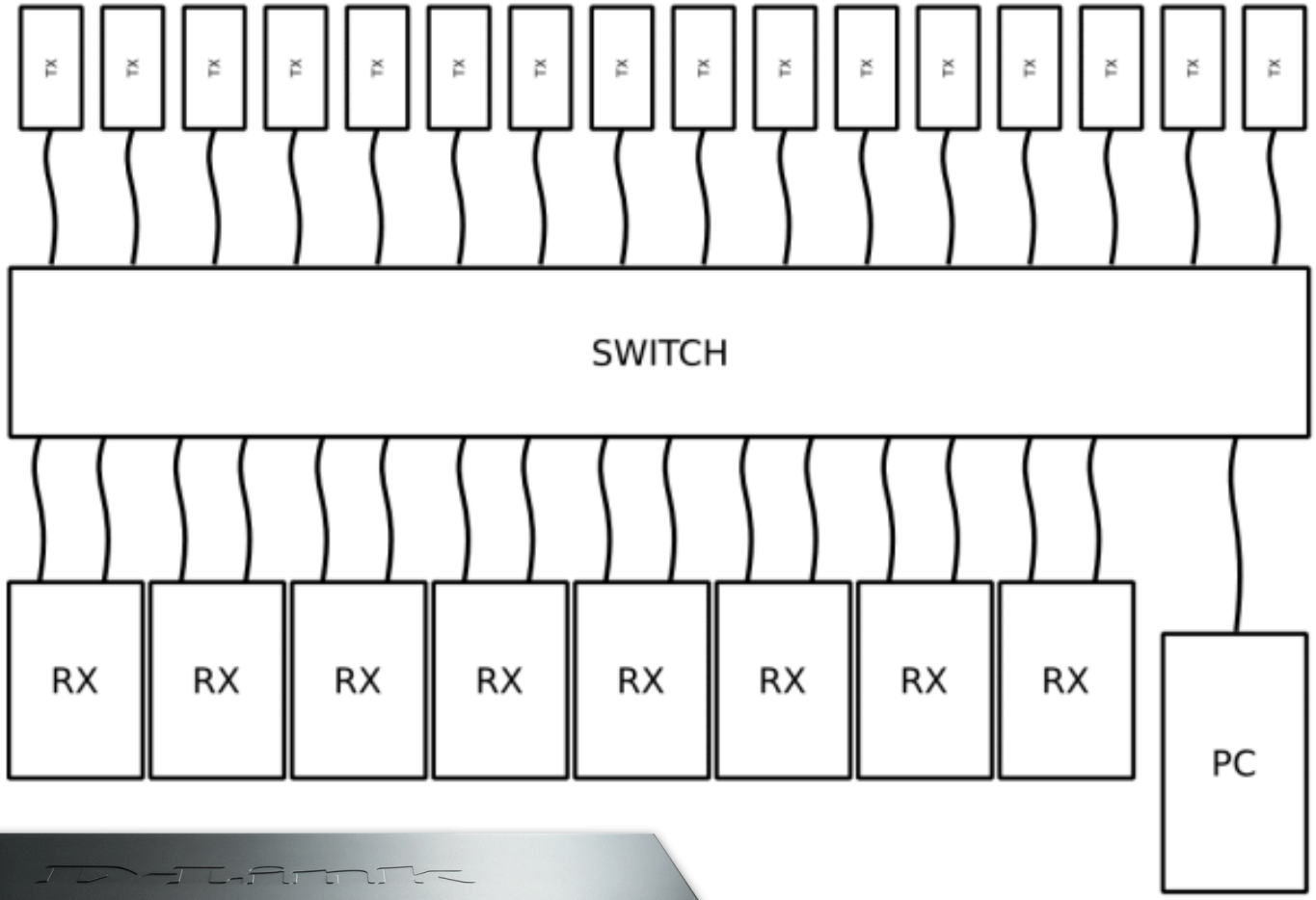
System configuration for SW-calibration: alternative 1



System configuration for SW-calibration: alternative 1

- Advantages
  - no custom FW development
  - full-SW based system
  - relatively cheap
  - part of the development is done already
- Disadvantages
  - the DAQ workstation might not be fast enough to process events at the expected count rates
  - SW development might not take less than the MB-based solution

System configuration for SW-calibration: alternative 2

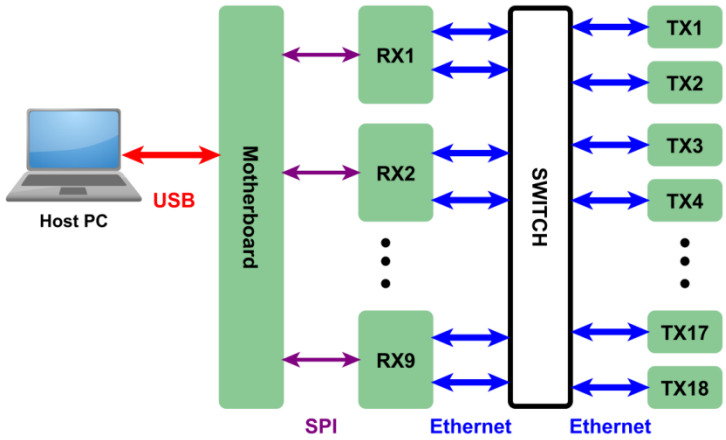


Ethernet cable

System configuration for SW-calibration: alternative 2

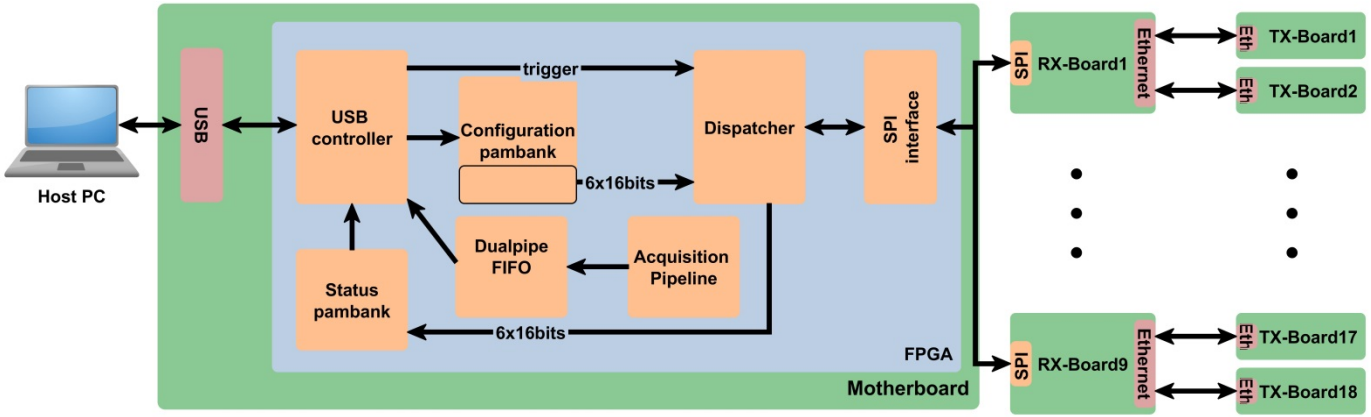
- Advantages
  - highest performance
- Disadvantages
  - ~~relies on contractors deadlines~~ (4 months delay for RX boards)
  - relies on prompt and successful FW/SW development

Slow control and plans for the ASIC Configuration

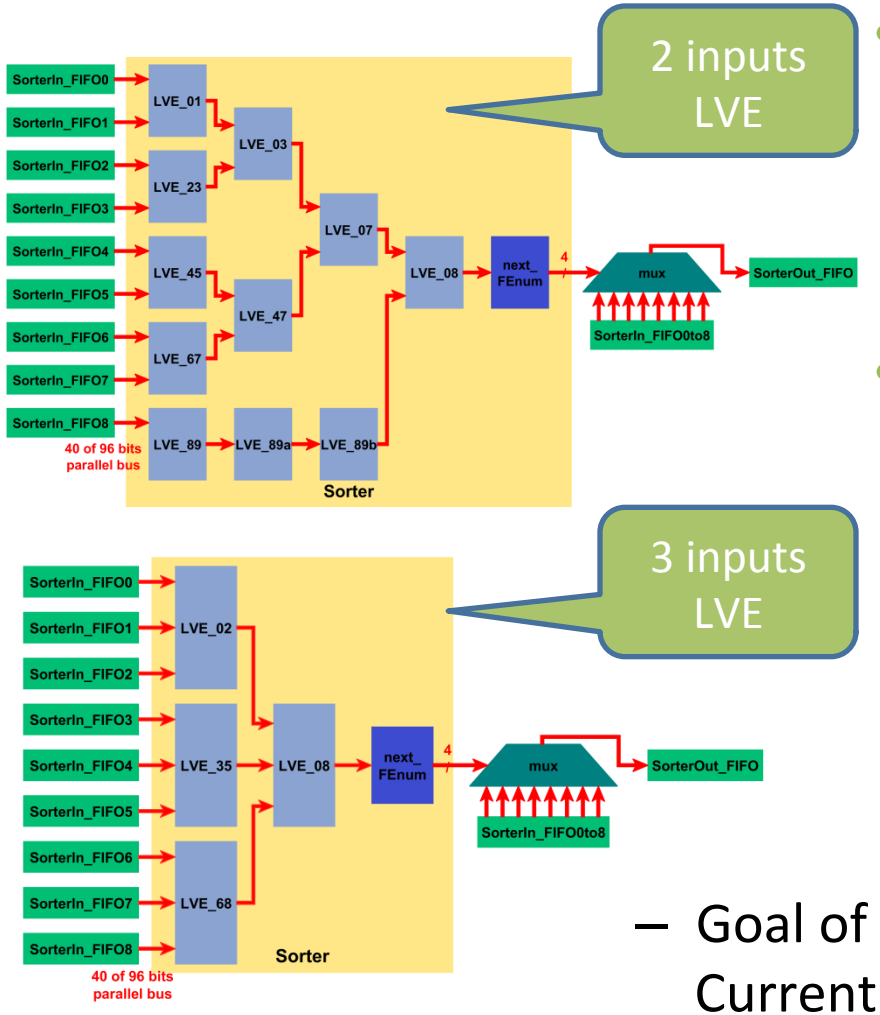


- Communication paths:
  - Host PC → MB:
    - USB
  - MB → RX-Boards:
    - SPI
  - RX → TX-Boards:
    - Ethernet

Words of the communication protocol		
Bit	15 to 8	7 to 0
W0	RX_ID	TX_ID
W1-4	DATA	
W5	T_ID	



Coincidence Sorter Architecture

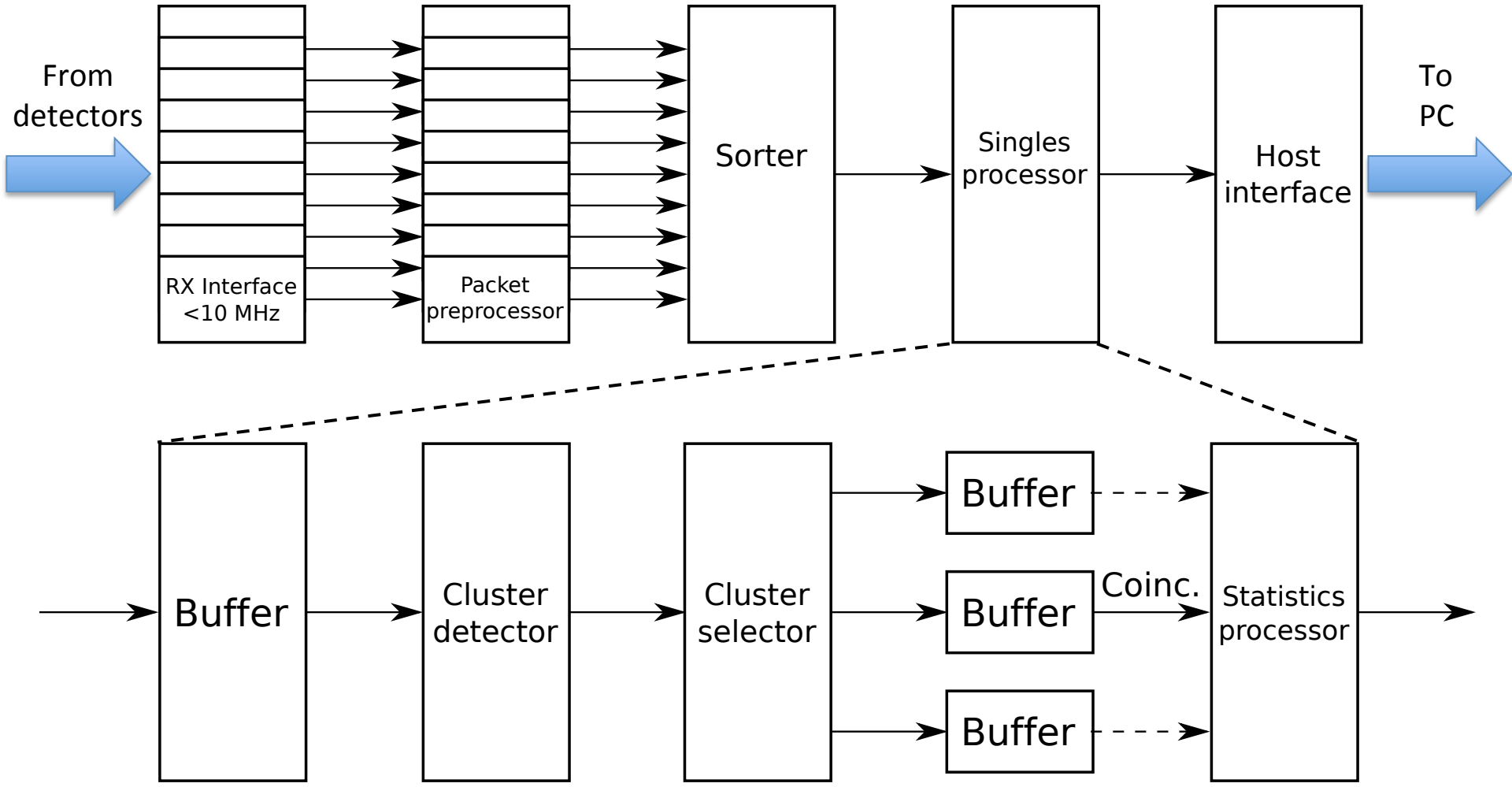


- LVE: acts like a comparator
  - Compares timestamps
  - Outputs the earliest timestamp
  - Outputs 5 additional bits
- next_FEnum stage
  - Outputs the 4 bits
  - Restarts the process
  - Multiplexer
    - Recovers the data packet from the input FIFO

– Goal of 20MHz minimum throughput rate → Current specs:

- 28MHz for the sorter with 2-inputs LVE
- 40MHz for the sorter with 3-inputs LVE

Coincidence streaming architecture



RX HW development status in the last meeting (06/2015)

- Functional design ✔
- Schematic design ✔
- Mechanical design ✔
- PCB design ✔
- Construction and assembly ✖

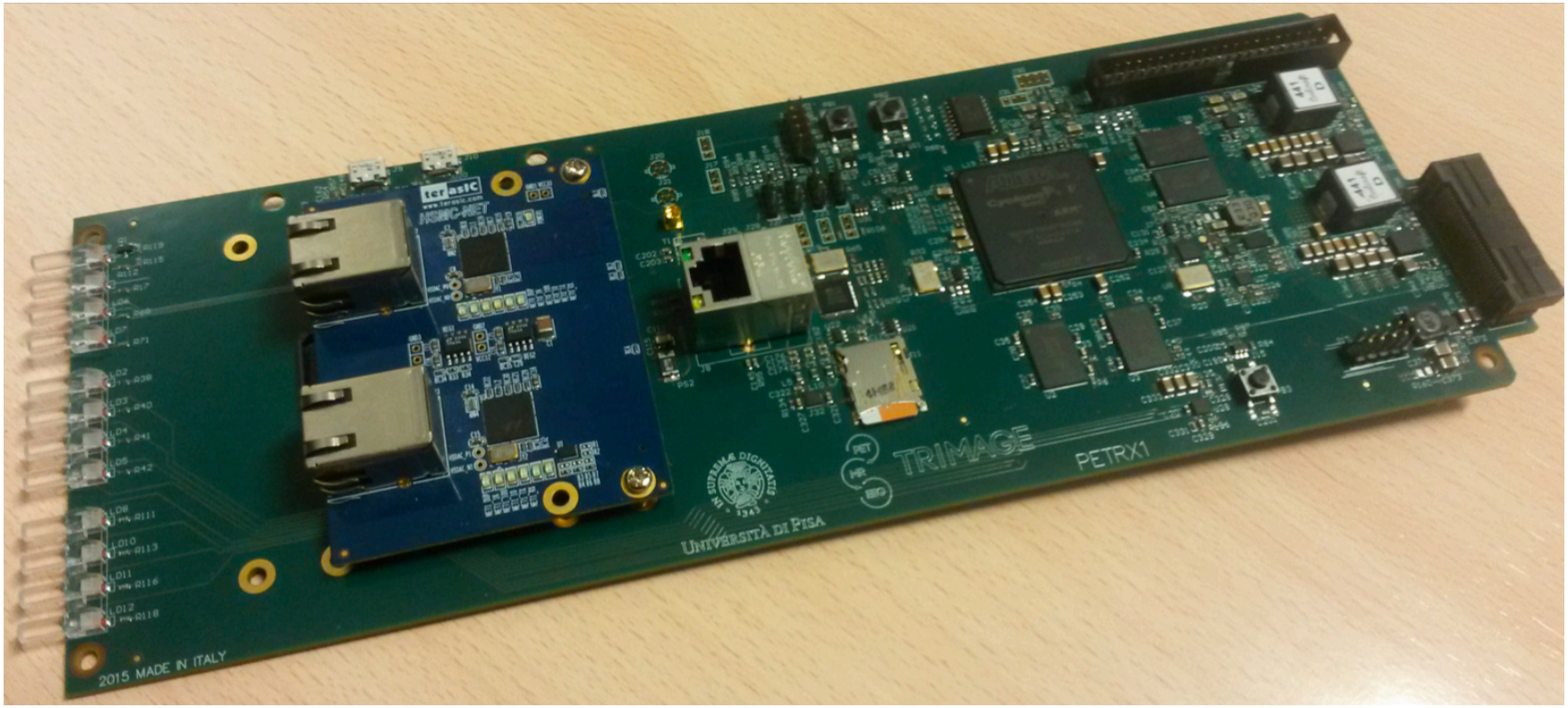
- Expected delivery 9/2015

RX HW development status as of today

- Functional design ✔
- Schematic design ✔
- Mechanical design ✔
- PCB design ✔
- Construction and assembly ✔
- Initial testing (Power-up, JTAG chain) ✔

Most recent results are marked in blue

The first prototype of RX board



Next work

- SoCKit board -> RX Board
  - Test constraining of ethernet connections
  - Update ethernet firmware
  - Run through all the XJTAG tests
- Motherboard
  - **Develop RX/MB interface**
  - Test coincidence sorting
  - Test coincidence streaming through USB