Dose Profiler electronics status

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Pisa, INSIDE meeting

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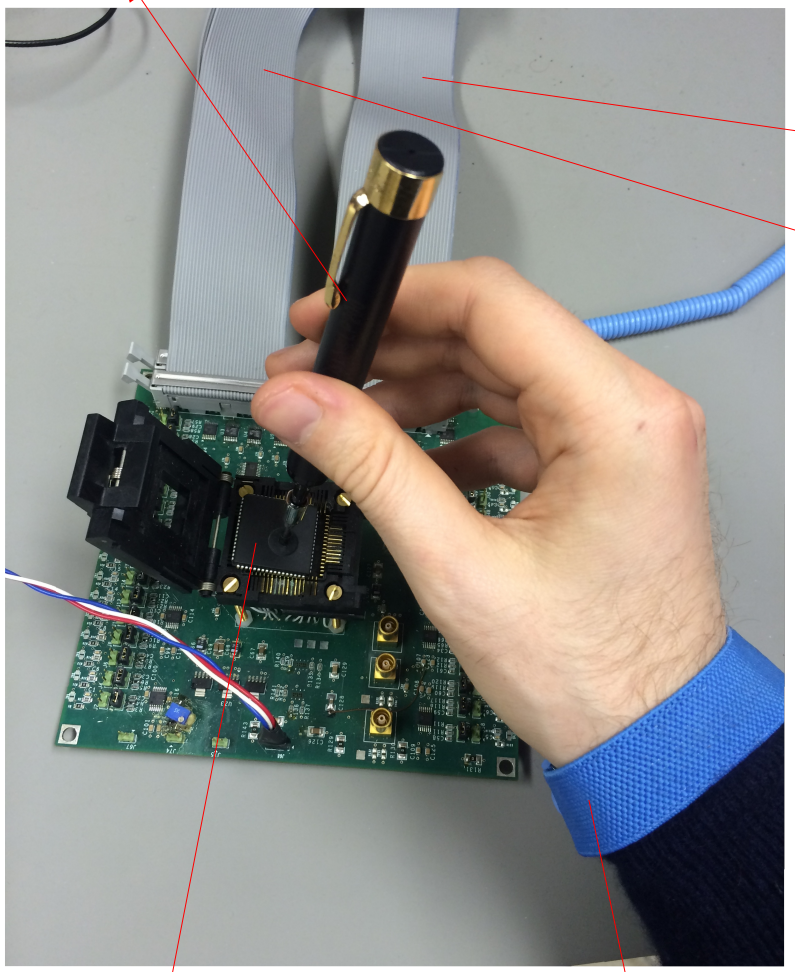
Outline

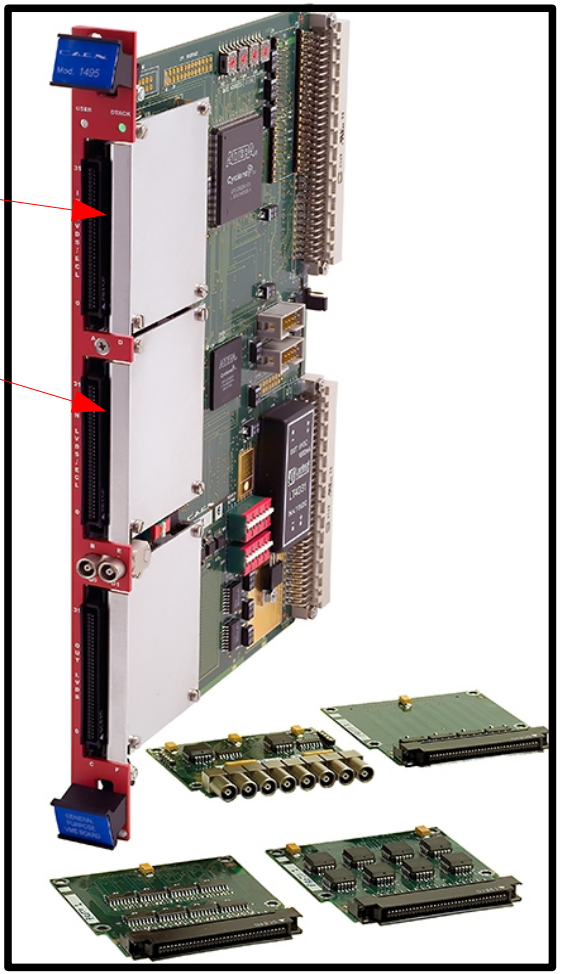
- BASIC32 test completed!!!
- Summary of test procedure and results
- What are next step for the read-out system development

Test Setup

Vacuum pick-up system



Plugged to V1495



BASIC32_ADC

Antistatic wrist strap

CAEN V1495: includes an FPGA that provides ASIC Configuration and DAQ

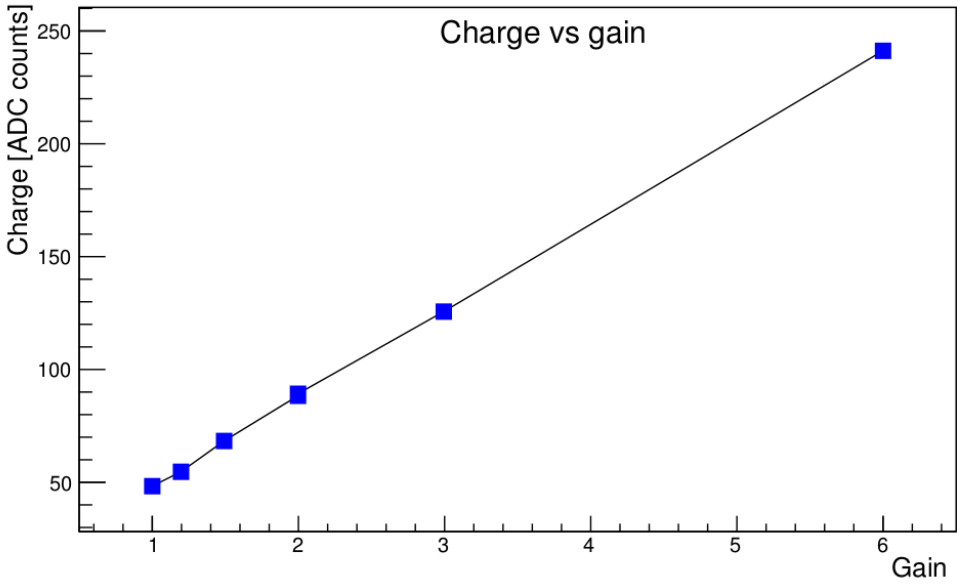
Test procedure

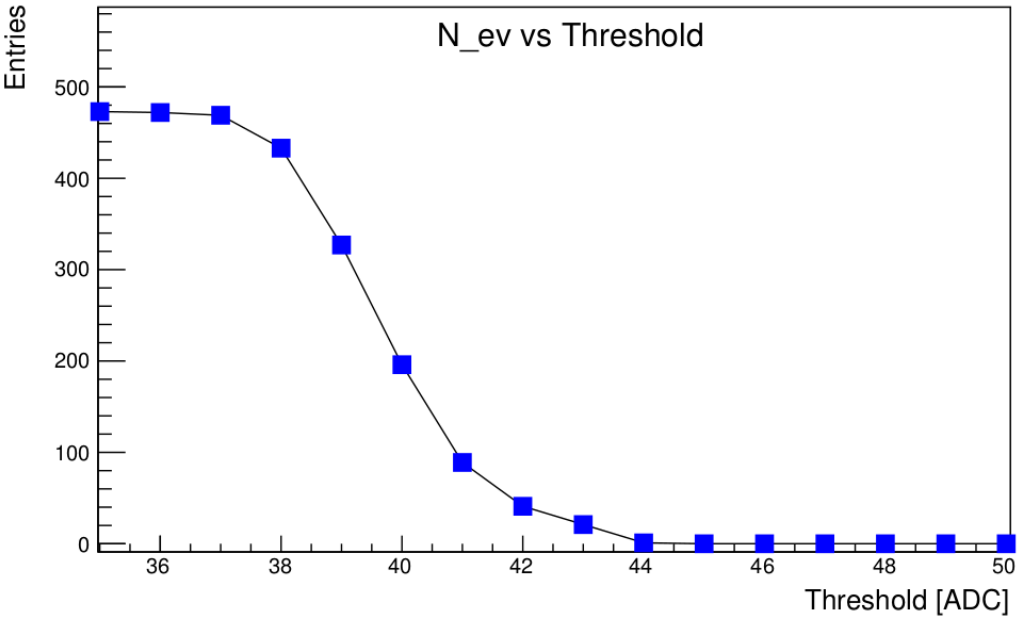
Goal: check the functionality of BASIC32_ADC

- Write and read configuration
- Pedestal acquisition: external trigger mode check
- Voltage offset DAC: we change bit of configuration, measuring the corresponding voltage at the input channels with an external ADC
- Gain: we inject a fixed charge signal through a capacitance on the board, measuring charge vs gain
- Threshold DAC: we inject a fixed charge signal through a capacitance on the board, measuring the rate vs threshold
- Read-out time window
- Clock max frequency

150 BASIC32_ADC tested

Results





- 6 BASIC show problems on voltage offset
- 3 BASIC shows problems on gain configuration
- 1 BASIC shows problems on read-out
- 1 BASIC show problems on setting configuration
- 150 BASIC can be used with clock up to 10 MHz

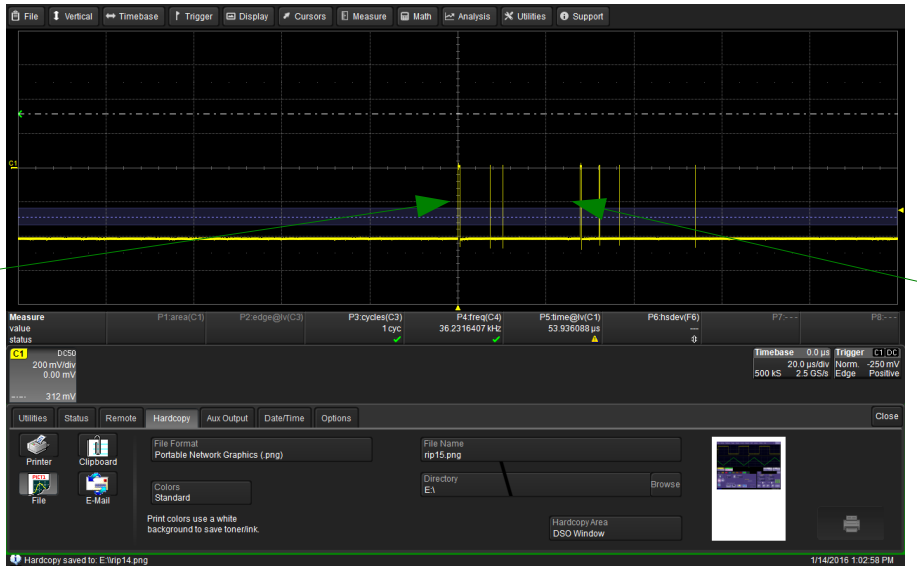
9 BASIC32_ADC have been excluded from the front-end electronics of the tracker

BASIC with only offset malfunctioning can be still used for calorimeter

108 BASIC32_ADC have been delivered to realize 16+2 front-end board for the tracker

Basic bad features: retriggering

Primary internal trigger pulse



"Afterpulses"

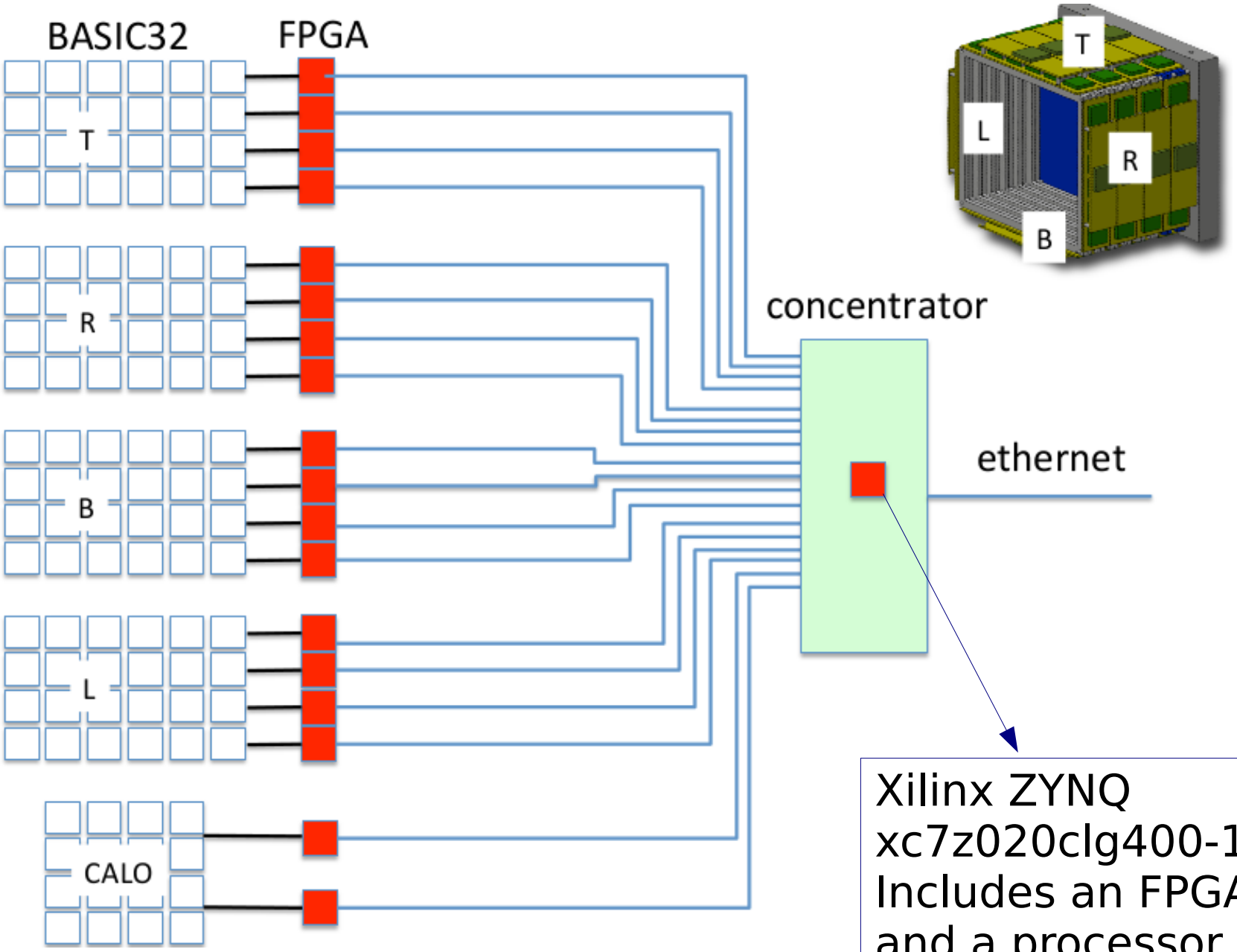
- All BASIC32_ADC affected
- Depends on set threshold and set damping time of CSA
- It probably derives from an undesired internal coupling between input channels and trigger signal

SOLUTION

- **Tracker**: max gain needed, plan coincidence reduce effect
- **Calorimeter**: high light yield, we can reduce gain

What happens now?

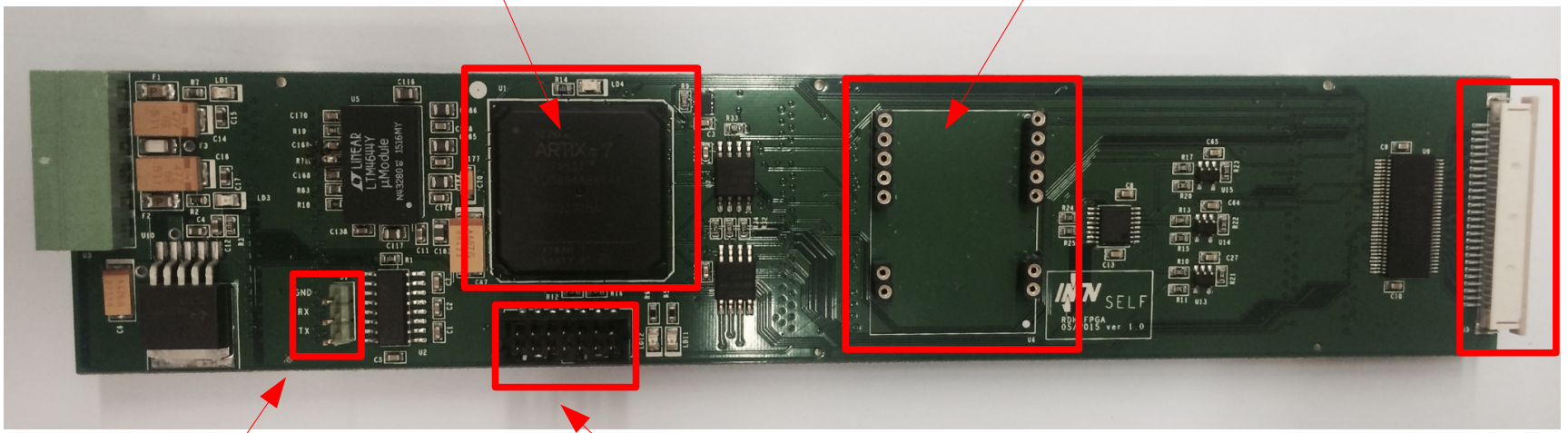
Read-out system development



FPGA board

FPGA Xilinx Artix-7
XC7A50T-1FGG484C

HV supply slot



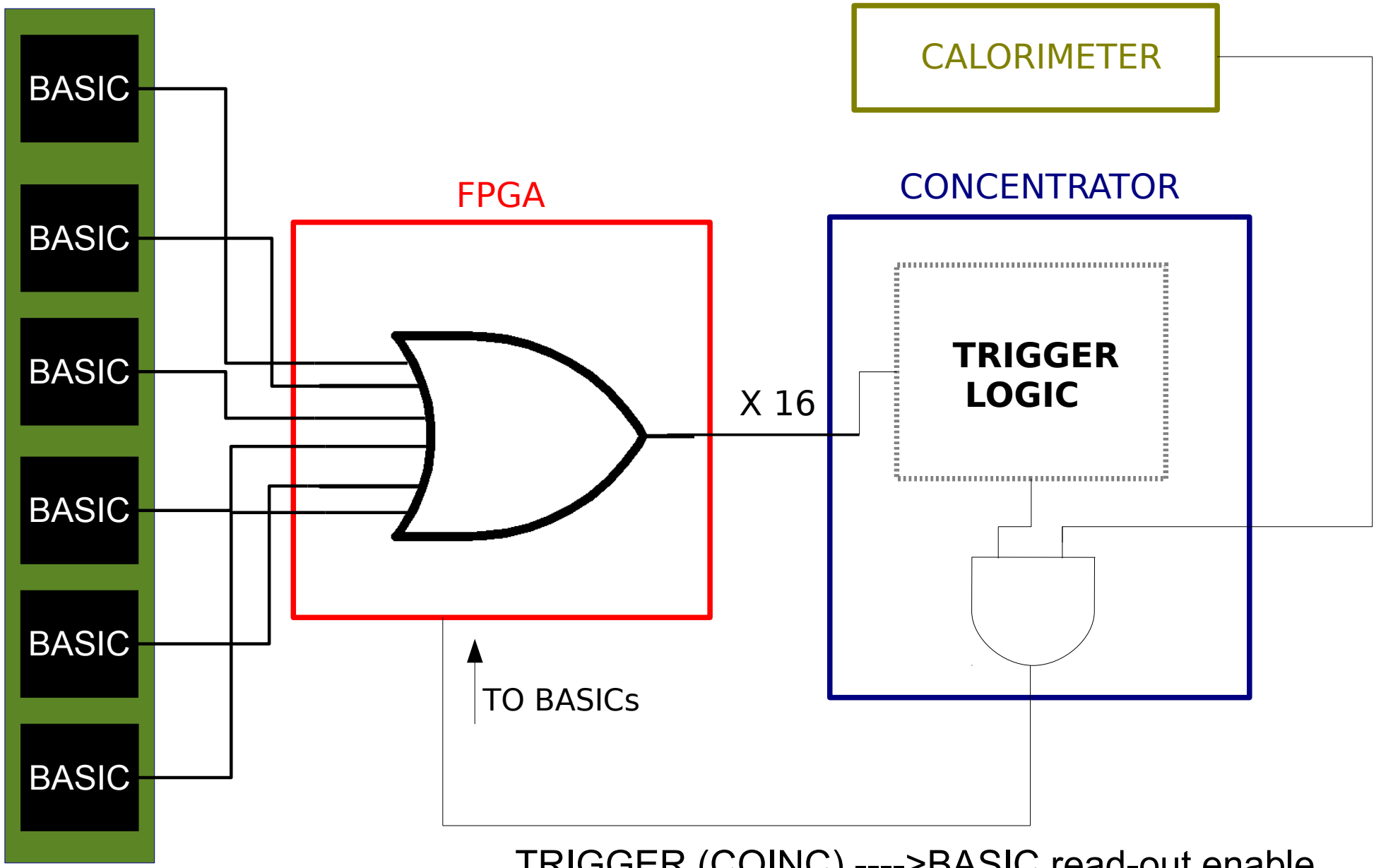
To
concentrator

SPI interface

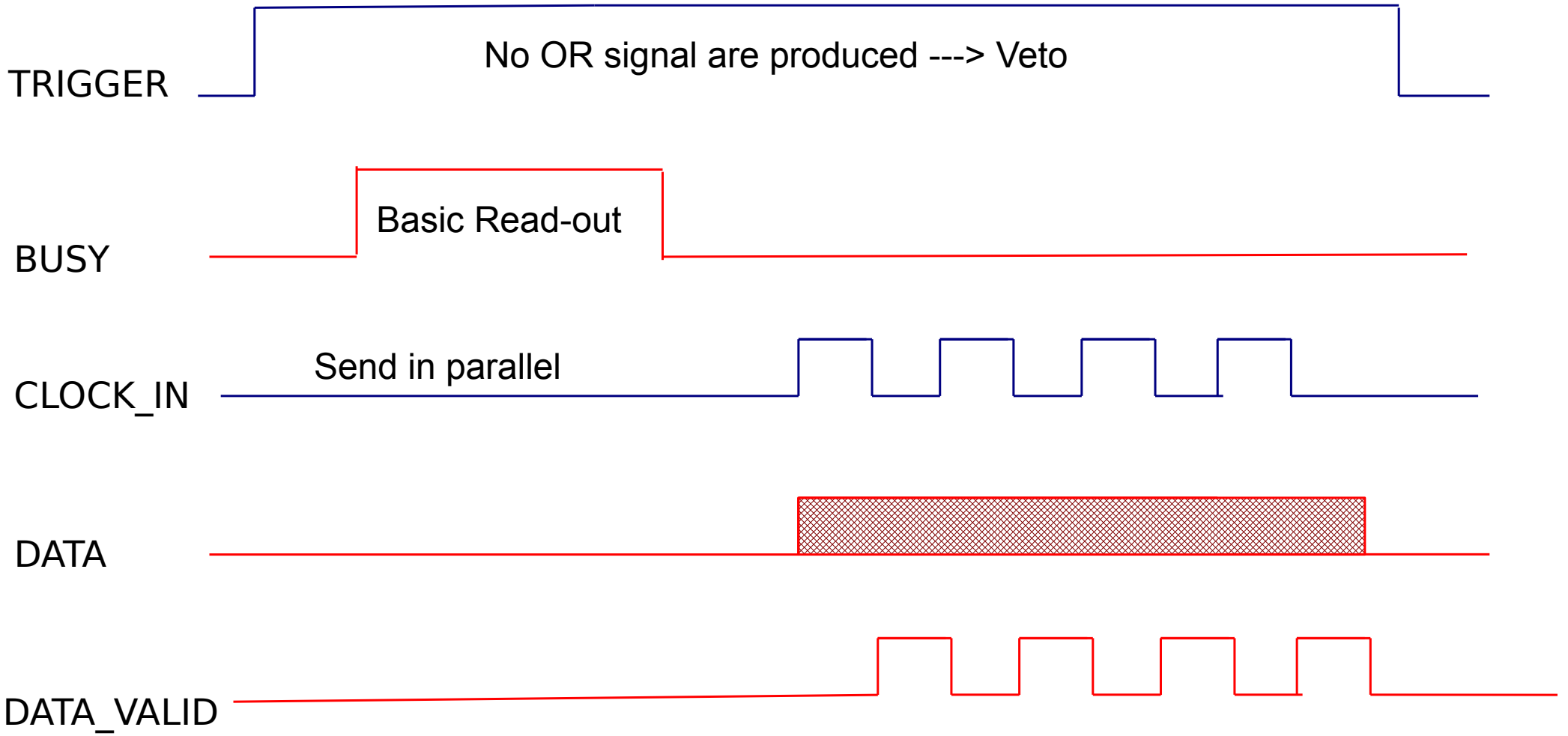
JTAG connector
(firmware)

Used for the test of the board with Raspberry Pi,
a dedicated interface board will be produced

Trigger scheme

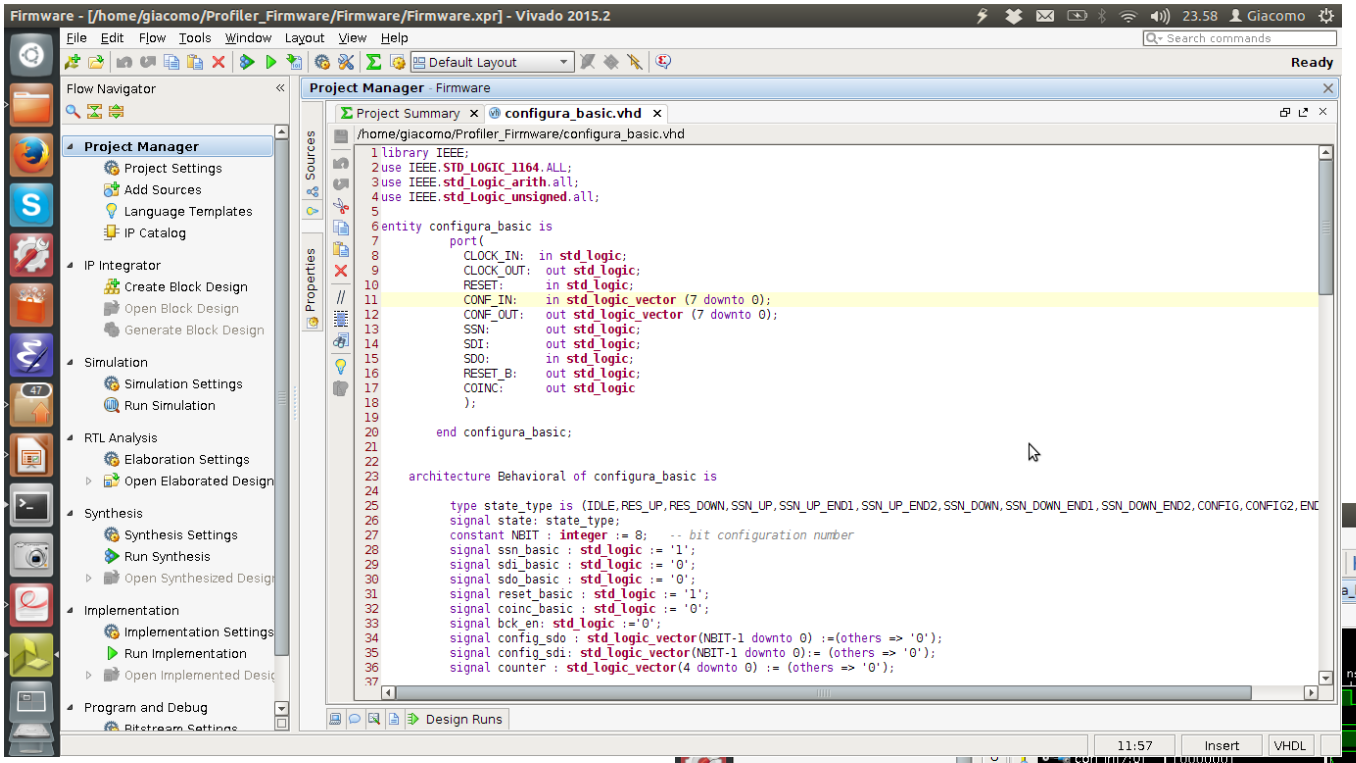


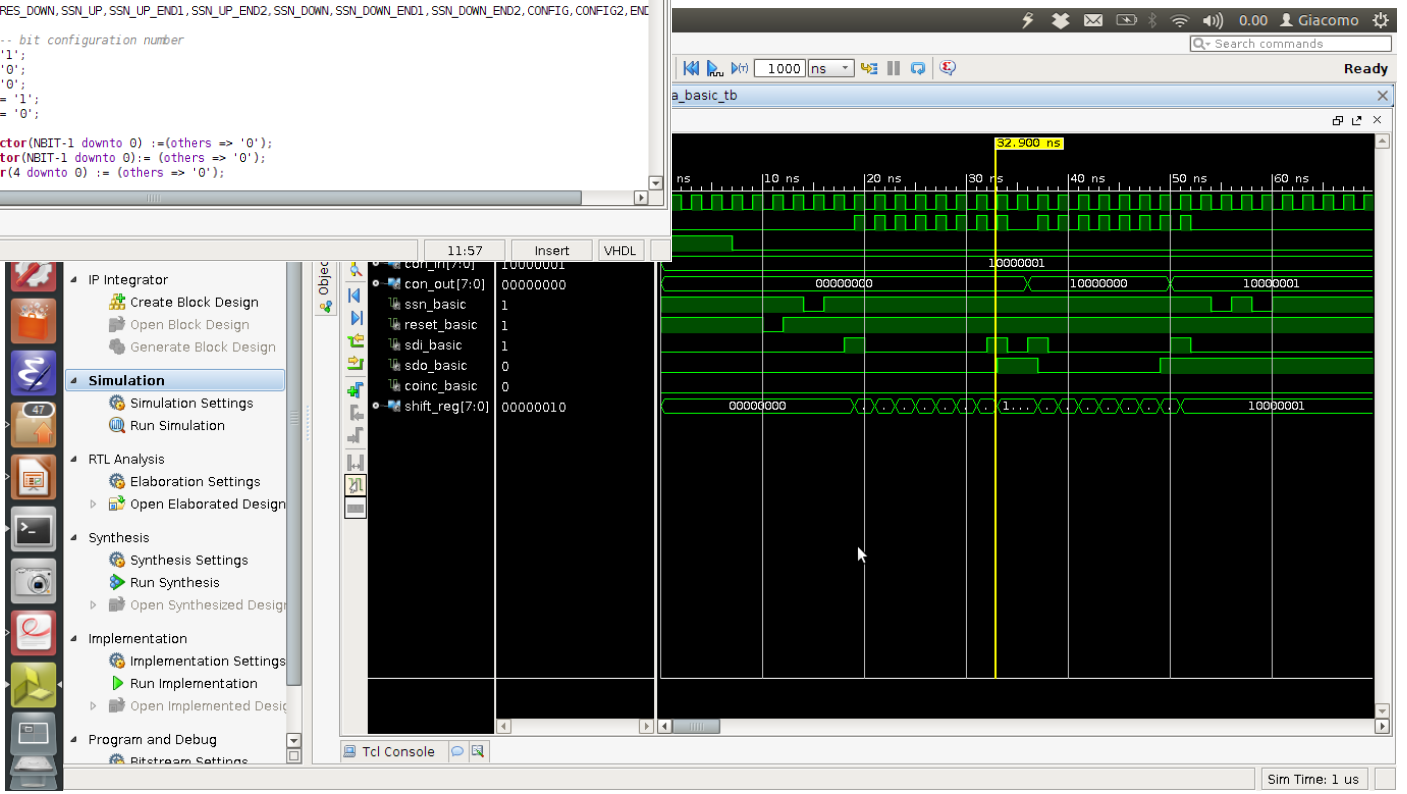
Read-out process



So my job in the next months will be...

... programming the firmware





Parts of the VHDL code used for BASIC test can be used

Thank you for the attention