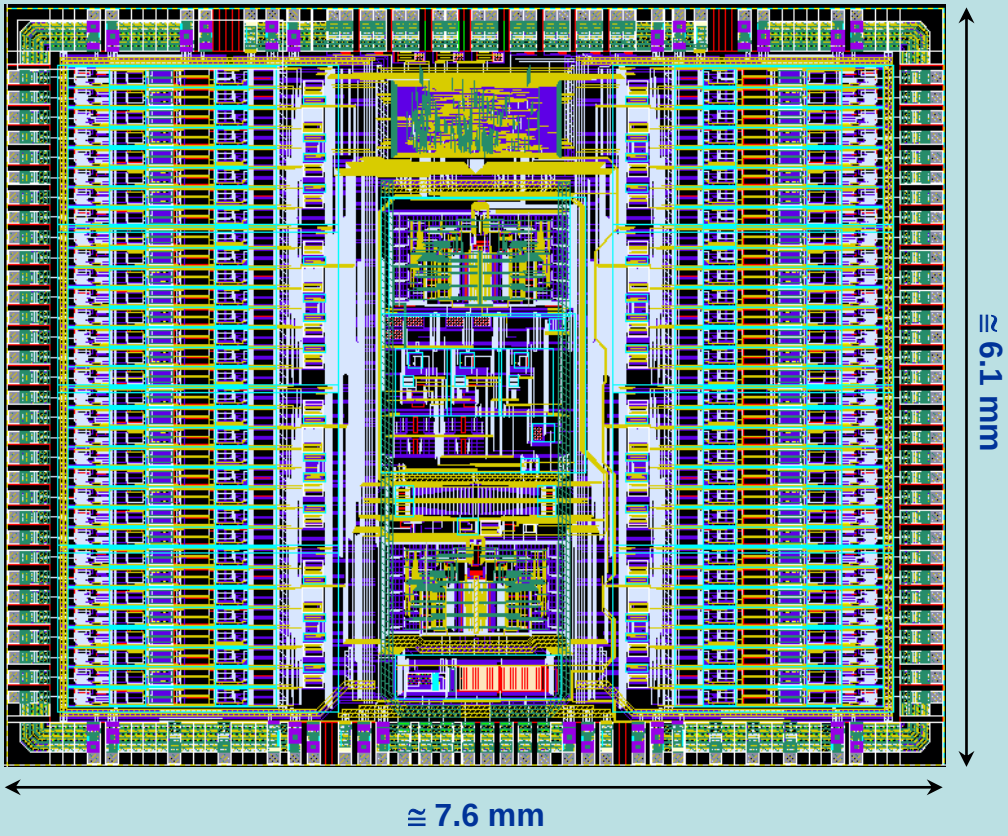
64-channel ASIC

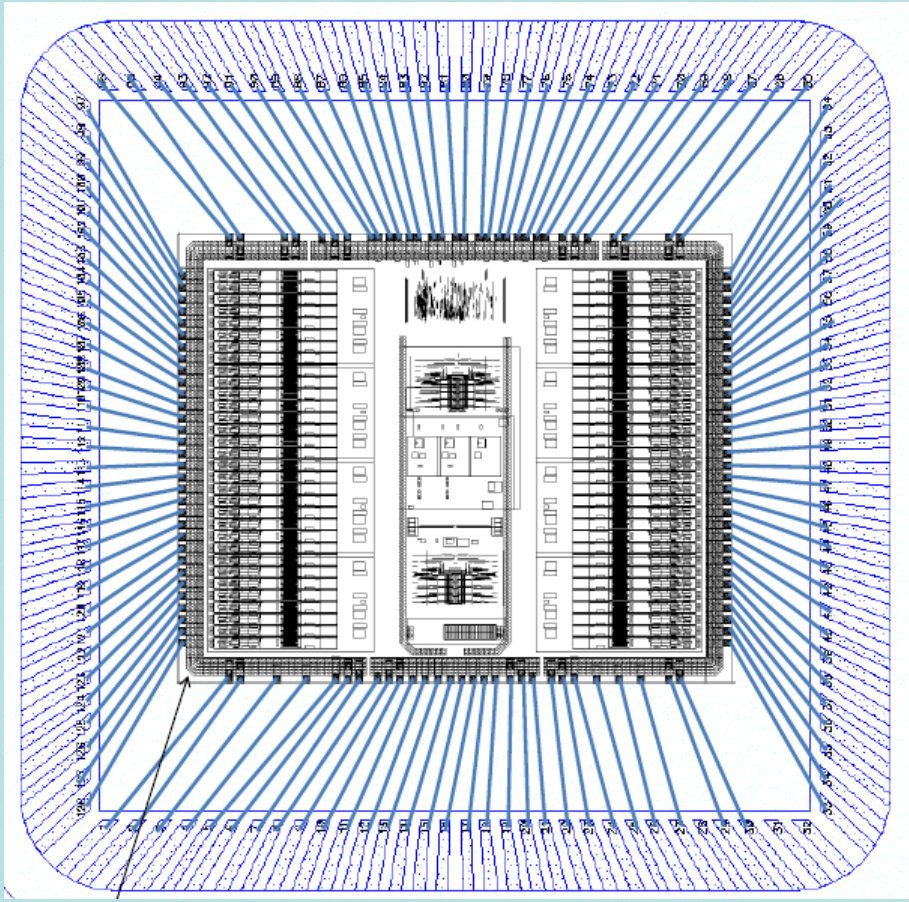
DEI - Politecnico di Bari and INFN - Sezione di Bari

- Final submission
- Main features of the ASIC prototype: short summary
- ASIC test schedule

Prototype submitted



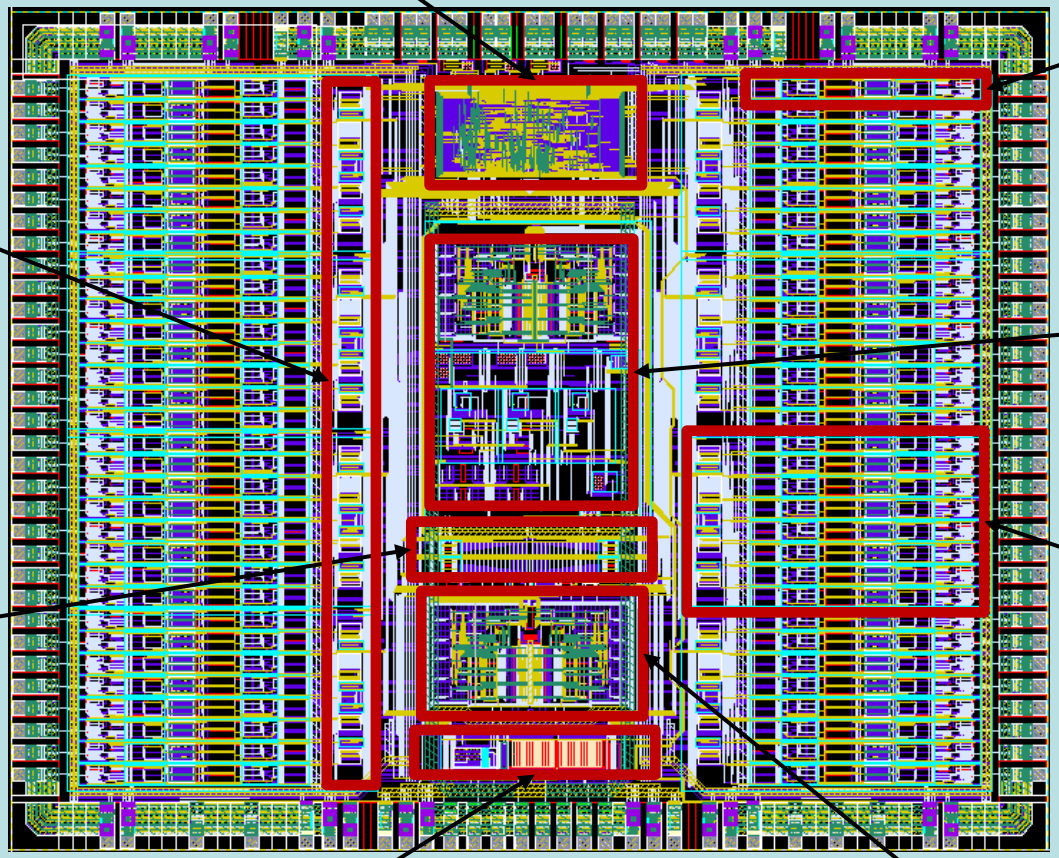
Layout of the ASIC



Bonding diagram

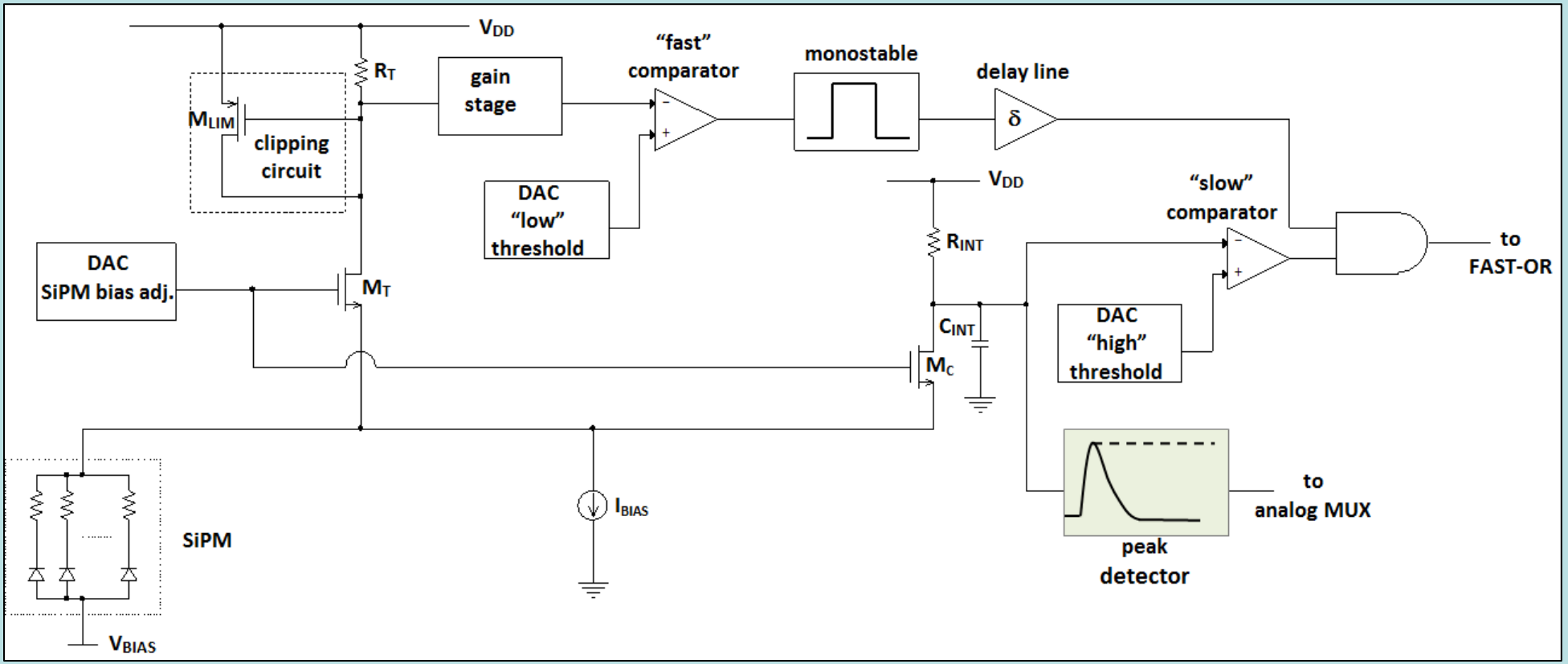
- ASIC submitted on July
- Package: CQFP 128 pin
- Delivered on November

Layout: main blocks



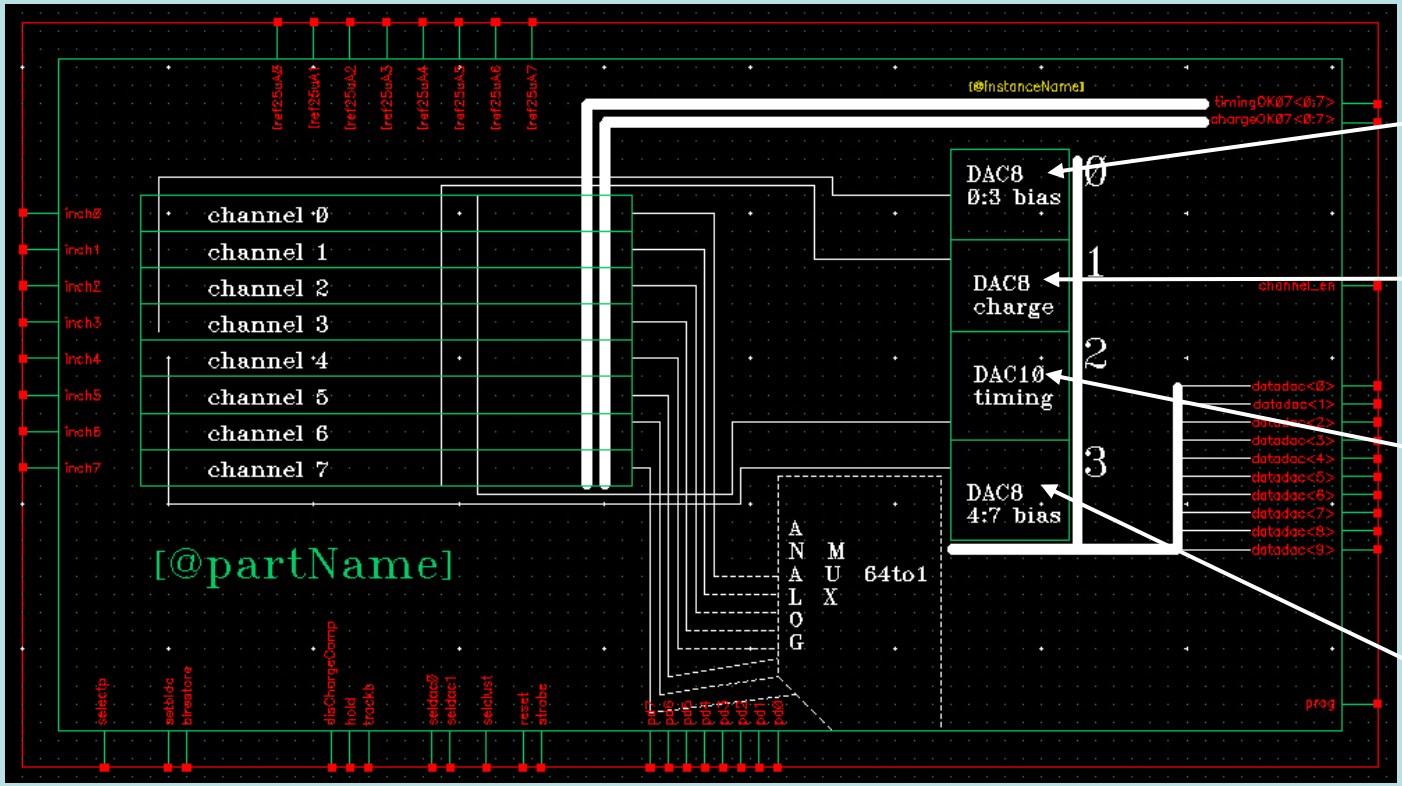
Analog channel: main features

- Dual common-gate input current buffer (“p-on-n” or “n-on-p” SiPMs)
- Dual signal path (“fast” for timing and “slow” for energy measurements): two matched common gates in parallel, to limit power consumption
- “Classic” fine tuning of the SiPM bias
- Signal validation: threshold on the integrated signal



Configuration: analog channels

- Configuration: standard SPI interface
- Configuration registers organized in 8-bit units (15 units), individually addressable in read and write mode
- 16 chips can share the same SPI clock and input data (hardware identifier)
- The 64 analog channels are organized in 8 clusters, each containing 8 channels



8-bit ADC: input bias for channels 0:3

8-bit ADC: charge threshold

10-bit ADC: fast comparator threshold

8-bit ADC: input bias for channels 4:7

8-channel cluster contains local configuration registers for the DACs

Further configurable features

- Internal reference generation: only an external resistor needed (for the 10-bit ADC bias current), four bits for fine adjustment
- Two reference currents monitored via dedicated pads
- Enable signal for the reference generator
- Enable (power-down) signal at clusters level
- P-on-n or n-on-p SiPMs
- Programmable gain amplifier placed between analog multiplexer output and ADC input: both DC level and gain are adjustable, to fit the input dynamic range of the ADC for both p and n type SiPMs
- 'Backup' 8-bit ADC selectable
- Test mode for the 10-bit ADC, with dedicated analog input
- Different RESET options:

  - Digital part: only digital macro, no configuration
    both digital macro and configuration (reset to default)
  - Analog channel: a fast baseline restorer can be enabled

- Power-on-reset
- Selectable duration of the time windows used in different possible read-out modes
- Possible masking of the trigger signals generated by the channel

Read-out modes

a) Internal trigger
- Read-out procedure started by the activation of the Fast-OR of the 64 trigger signals from the channels
- PD in peak detection mode (after time window for charge integration)
- Multiplexing and A/D conversion of the PD outputs, in sparse or serial mode
- Output data stream (total no. of hit channels, channel addresses and levels, first channel hit)
- Reset of the digital macro

b) External trigger
- Same read-out procedure, but started by the activation of the external trigger signal, regardless of internal triggers

c) "Coincidence" mode
- Read-out procedure started by internal or external trigger
- In case an external trigger is detected first, the read-out starts after a time window, as in b)
- In case an internal trigger is detected first, a time window is opened: if an external trigger arrives within this time window, then the read-out starts as in b), otherwise the system is reset

Test of the ASIC

- Test system based on a custom board, hosting the ASIC and ancillary electronics, and on an FPGA development board
- Custom board designed and submitted to the manufacturer, but not yet delivered
- Firmware under development (master thesis student)
- First tests will start as soon as the test board is available