

INSIDE in-beam PET Software & Simulation

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INSIDE meeting, Pisa, January 20th 2016

INSIDE in-beam PET 10vs10 modules was built!



JANUARY 2016

Torino Group's SW Tasks



Data AcQuisition (DAQ) Decided in the meeting in June 2015

- Acquisition of in-spill and inter-spill - Online analysis - Sending data to monitoring SW (singles & coincidences)



Online Monitoring - GUI

Available 1vs1 version, raw data

Update to 10vs10 and data format
 Calibration functionalities
 Online monitoring on true coincidence data



Simulation Distal fall off validated

-Coincidence rate validation





Data AcQuisition (DAQ)

ACQUISITION OF IN-SPILL AND INTER-SPILL DATA

- To reduce the transmitted event rate → The energy window filter and the time delay calibration have been implemented in the TX boards firmware and the decoded data format has been optimized.
- ② To design and implement a task-dedicated SW → Multi-threading and scalable approach, C/BOOST based.
- ③ To increase ethernet bandwidth, computational power and RAM memory → Use a server with 3 Gigabit NIC, 128 GB RAM, 16 cores (32 with HyperThreading).

ONLINE ANALYSIS

- 1 Only coincidences time-tagged are saved by the DAQ SW.
- ② Report on the DAQ SW performance.

SENDING DATA TO MONITORING SW VIA UDP PROTOCOL

- 1 To send singles to verify system performance and separate in-spill/inter-spill data.
- ② To send time-tagged true coincidences to obtain in-spill/inter-spill images and monitor the system performance in coincidence

UDP header

```
header[0] = 0 \times DC;
header[1] = 0xBA + boardID;
header[2] = (packetNumber & 0xff000000) >> 24);
header[3] = (packetNumber & 0x00ff0000) >> 16);
header[4] = (packetNumber \& 0x0000ff00) >> 8);
header[5] = (packetNumber & 0x00000ff);
header[6] = ((eventBytes & 0xff00) >> 8);
header[7] = ((eventBytes \& 0x00ff);
Data is formatted in groups of 3 bytes.
First byte is always
Bit 7 downto 4: Not used
Bit 3 downto 1: Chip
Bit 0: Frame start
The remaining two bytes can be:
Frame start [case (bits 19 downto 16)]
case "0000": frame ID(11 downto 0)
case "0001": frame ID(23 downto 12)
case "0010": "0000" & frame ID(31 downto 24)
```

Event

```
case "0011": TOT(5 downto 0) & channel(6 downto 0)
case "0100": Tcoarse (6 downto 0) & TOT (10 downto 6)
case "0101": Etime > Ttime & Tfine(7 downto 0) &
     Tcoarse(9 downto 7)
```

Frame end

case "0110": frame ID(4 downto 0) & num events(6 downto 0) case "0111": frame ID(16 downto 5) case "1000": frame ID(28 downto 17)

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First decoded data format

	First format
UDP header	8 bytes
Frame start	9 bytes
Event	9 bytes
Frame end	9 bytes



UDP header

```
header[0] = 0xBA + boardID;
header[1] = 0xDC;
header[2] = ((eventBytes & 0x00ff);
header[3] = ((eventBytes & 0xff00) >> 8);
header[4] = (packetNumber & 0x00000ff);
header[5] = (packetNumber & 0x000ff00) >> 8);
header[6] = (packetNumber & 0x00ff0000) >> 16);
header[7] = (packetNumber & 0xff00000) >> 24);
```

Frame start

Byte0(7 downto 6) <= "00" Byte0(5 downto 0) <= "000000" Byte1(7) <= '0' Byte1(6 downto 2) <= boardID Byte1(1 downto 0) <= chipID Byte2(7 downto 0) <= FrameID(7 downto 0) Byte3(7 downto 0) <= FrameID(15 downto 8) Byte4(7 downto 0) <= FrameID(23 downto 16) Byte5(7 downto 0) <= FrameID(31 downto 24)</pre>

Event

```
Byte0(7) <= '1'
Byte0(6 downto 5) <= "00"
Byte0(4 downto 3) <= TAC
Byte0(2 downto 0) <= TOT(10 downto 8)
Byte1(7 downto 0) <= TOT(7 downto 0)
Byte2(7 downto 6) <= chip
Byte2(5 downto 0) <= channel
Byte3(7 downto 6) <= Tfine(1 downto 0)
Byte3(5) <= Etime > Ttime
Byte3(4 downto 0) <= board
Byte4(7 downto 6) <= Tfine(7 downto 2)
Byte5(7 downto 0) <= Tcoarse(9 downto 2)</pre>
```

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New decoded data format

The new decoded data format was designed to: 1) Reduce the overhead.

2) Give the necessary information to sort and find coincidences as fast as possible

	First format	New format
Frame start	9 bytes	6 bytes
Event	9 bytes	6 bytes
Frame end	(9 bytes)	(6 bytes)
Bandwidth 10 evts x frame x TX	1.86Gbit/s	1.24Gbit/s
	Raw format	New format
Bandwidth 10vs10 background	208 Mbit/s	112 Mbit/s



System configuration, Data Acquisition and monitoring set up



Switch: 24-port Gigabit + 8 port Gigabit Control PC (desktop) DAQ Server: 32 cores HT, 128 GB RAM Monitoring PC: 4 cores, 6 Gb RAM (desktop)





Data AcQuisition (DAQ)

The energy window filter and the delay time calibration has been implemented in the TX board firmware. A new decoded data format was designed to reduce data overhead and speed up the coincidence finding. A multi-threading DAQ software was designed and implemented to satisfy project requirements and it has been already tested with dummy events (partial geometry) and background signal.

NEXT STEPS

 FDG sources available from the IRCC (Candiolo, TO) to forward test the DAQ performance and to calibrate the INSIDE in-beam PET system
 Test DAQ performance at very high rate with dummy events





Online Monitoring - GUI

UPDATE SW TO 10VS10 GEOMETRY AND TO DECODED DATA FORMAT

- 1 To check acquisition parameters and analyse singles.
- ② To analyse true coincidences.

AUTOMATIC CALIBRATIONS

- ① To calibrate via software T fine, TAC by TAC, raw data format.
- ② To select energy window, channel by channel, raw data format.
- ③ To calibrate time delay, channel by channel, raw data format.

ONLINE MONITORING ON TRUE COINCIDENCE DATA

① To divide true coincidences by using single event rate distribution

② To evaluate system performance in coincidence (e.g. CTR)





2) Acquisition



Raw data format	Settings/Monitoring Check acquisition Results In-beam PET images SETTINGS	Monitored quantities	
	time [ns] (min-max): 0 🚽 4.73e11 🚽	Check acquisition (chip by chip)	
	energy (min-max-nbins): 0 🚽 5e-07 🖨 500 🜩	Frame multiplicity	
	Event selection	(channel by channel)	
	TOT window: 0 🚽 5e-07 🚔	Inspill/Interspill Tcoarse Inspill/Interspill Ecoarse	
	coincidence time window [ns]: 2.0 🚖	Inspill/Interspill Tfine	
	energy window (number of STD): 1.0 🚔	Inspill/Interspill Eline Inspill/Interspill Tcoarse in coincidence	
	Calibration	Inspill/Interspill Tfine in coincidence	
	Select calibration path	(TAC by TAC)	
	Calculate SoC-EoC Window	EoC-SoC T EoC-SoC E	
	Calculate Energy Window		
	Calculate Time delay calibration		
	<u>S</u> ave histograms	(general)	
	MONITORING	Single distribution Single event rate	
Port: 10020 🚖		Coincidence event rate	
	Port True Coincidences: 10030 🖨	Inspill/Interspill Coincidence Time Resolution (CTR)	
		Coincidence map on head	
		(channel by channel)	
	OFFLINE ANALYSIS	TOT (not calibrated)	
		Inspill/Interspill TOT	
		TOT in coincidence Inspill/Interspill TOT in coincidence	
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Online Monitoring - GUI

The monitoring software was updated to the 10vs10 geometry and to new decoded data format.

An automatic calibration procedure was implemented to obtain fully calibrated decoded data from the final system configuration.

NEXT STEPS

To test the GUI performance with the FDG source.
 To calibrate the INSIDE in-beam PET system.

Inside

Simulation

COINCIDENCE RATE VALIDATION

- ① To check Lutetium Fine Silicate (LFS) formula.
- ② Results for F18-FDG and 1vs1 INSIDE geometry (data acquired at the CNAO in May 2015)



F18-FDG measurement validation – Candiolo 2015

Problems: >Vial characteristics >LFS atomic composition











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>LFS atomic composition: photoelectric effect evaluation (FLUKA)

	LSO	LFS
ρ (g cm**-3)	7.4	7.35
Attenuation length (cm)	1.15	1.15
LUTETIUM	2.0	4.0
OXYGEN	5.0	3.0
SILICON	1.0	0.2







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Simulation

Both the profile distal fall-off in the final in-beam PET image and the coincidence event rate have been validated.

NEXT STEPS

① Next beam test simulations.

② Simulation of carbon beams.



Torino Group's SW Tasks

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Data AcQuisition (DAQ)

- ✓ Decoded data format
 ✓ Multi-threading DAQ software
 ✓ Online data analysis
- ✓ Monitoring via UDP protocol



Online Monitoring - GUI

✓ Updated GUI sw (10vs10)
 ✓ Improved automatic calibrations
 ✓ Online monitoring on singles
 ✓ Online monitoring on true coincidence data



Simulation

✓ Coincidence rate validation

