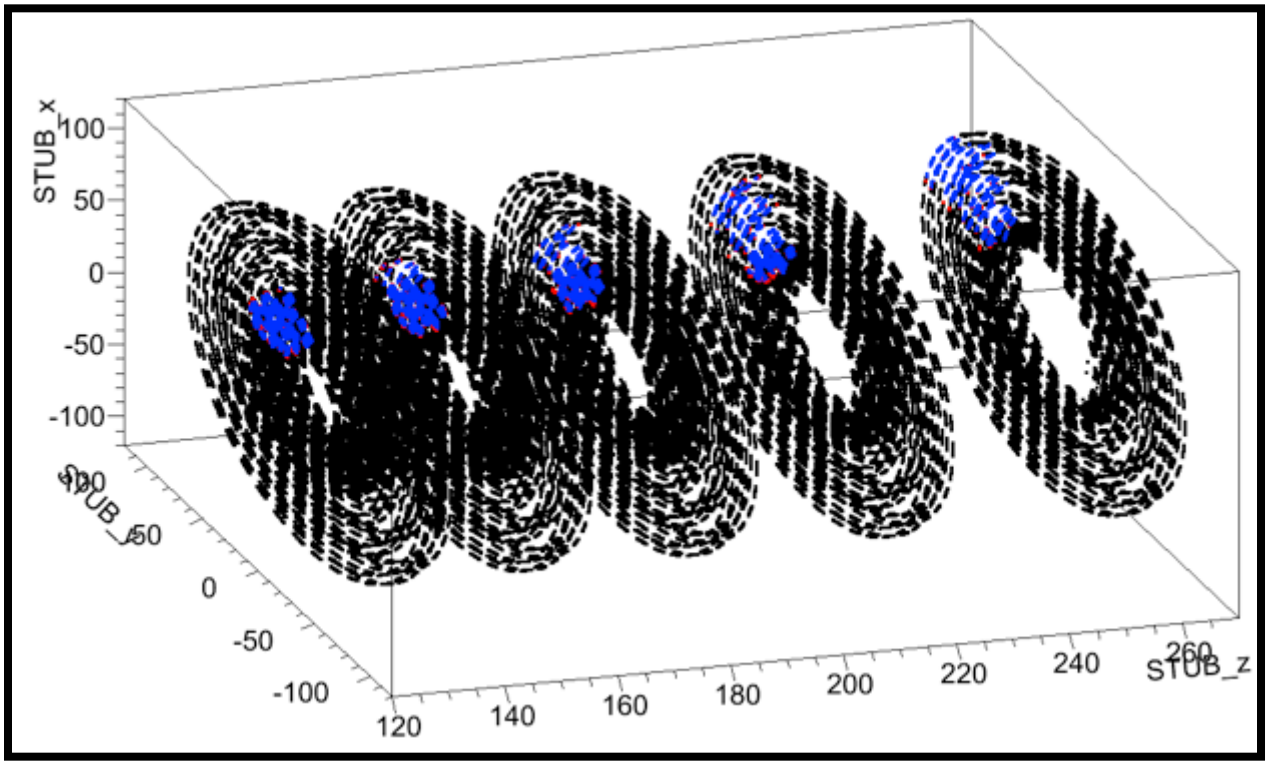
AM07b primilinary



Pre-requisites
Architecture
Conclusion and plan

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→ **AM07b**

The AM07b chip will be about 1000 pins.
The chip doesn't include high speed serial links for input/output data bus;
In this version data bus will be parallel :

- 8 Inputs data bus (36 bits width)
- 2 Outputs data bus (14 bits width)
- The maximum data rate for these bus is 200MHz

These specifications raise several questions :

- Can a FPGA drive simultaneous 288 ttl outputs at 200MHz ?
- If so, which one ?
- If not, which architecture can we implement to solve this issue ?

→ **FPGA choice**

The SSO (Simultaneous Switching Output) based on SSN (Simultaneous Switching Noise) is the parameter to calculate the number of output of FPGA bank which can switch in the same time.
In fact it is :

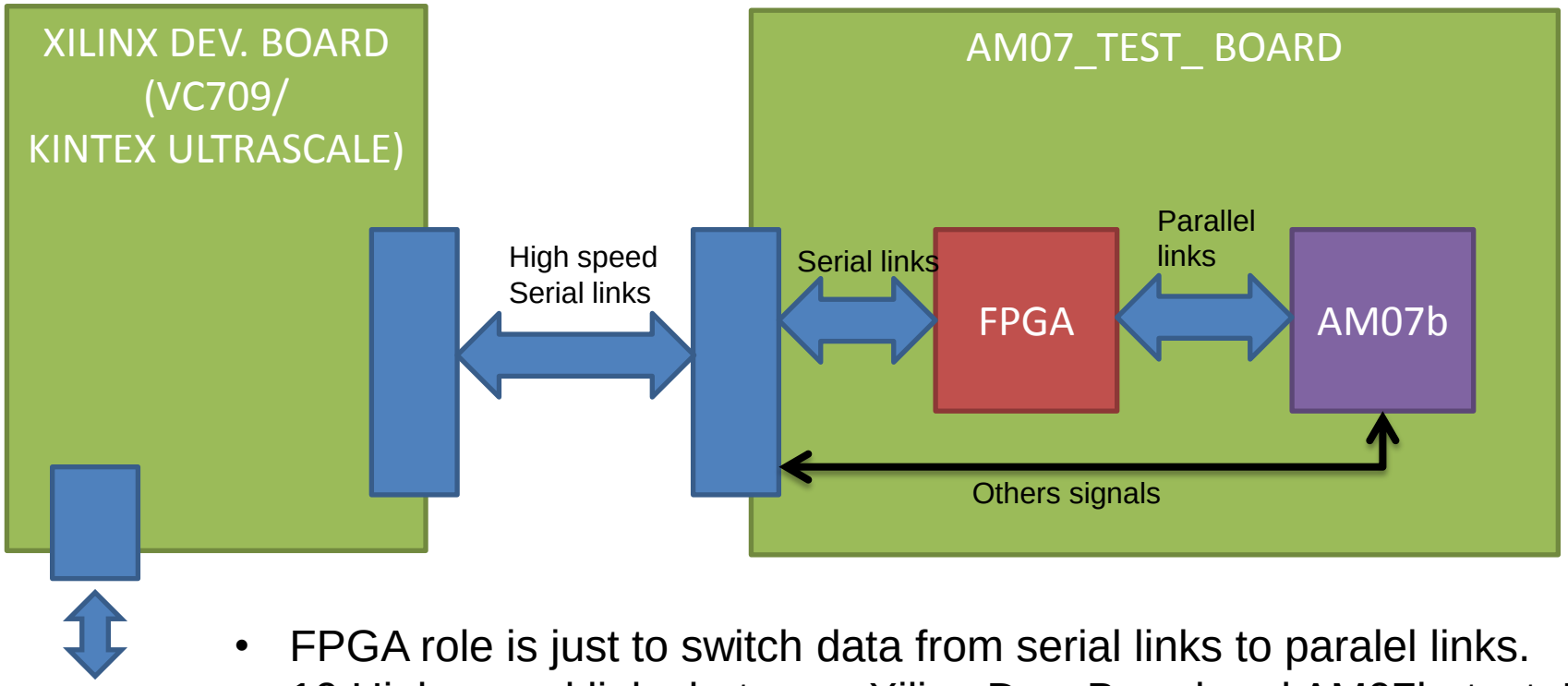
- What is the noise marge per output ?
- What is the crosstalk per output ?

In 7 series component datasheets, the SSO information is not available anymore.
To estimate the noise marge and crosstalk, a design implementation is necessary in vivado tool;

Nevertheless it exists several large FPGA with a lot of IO pins with which we can investigate:

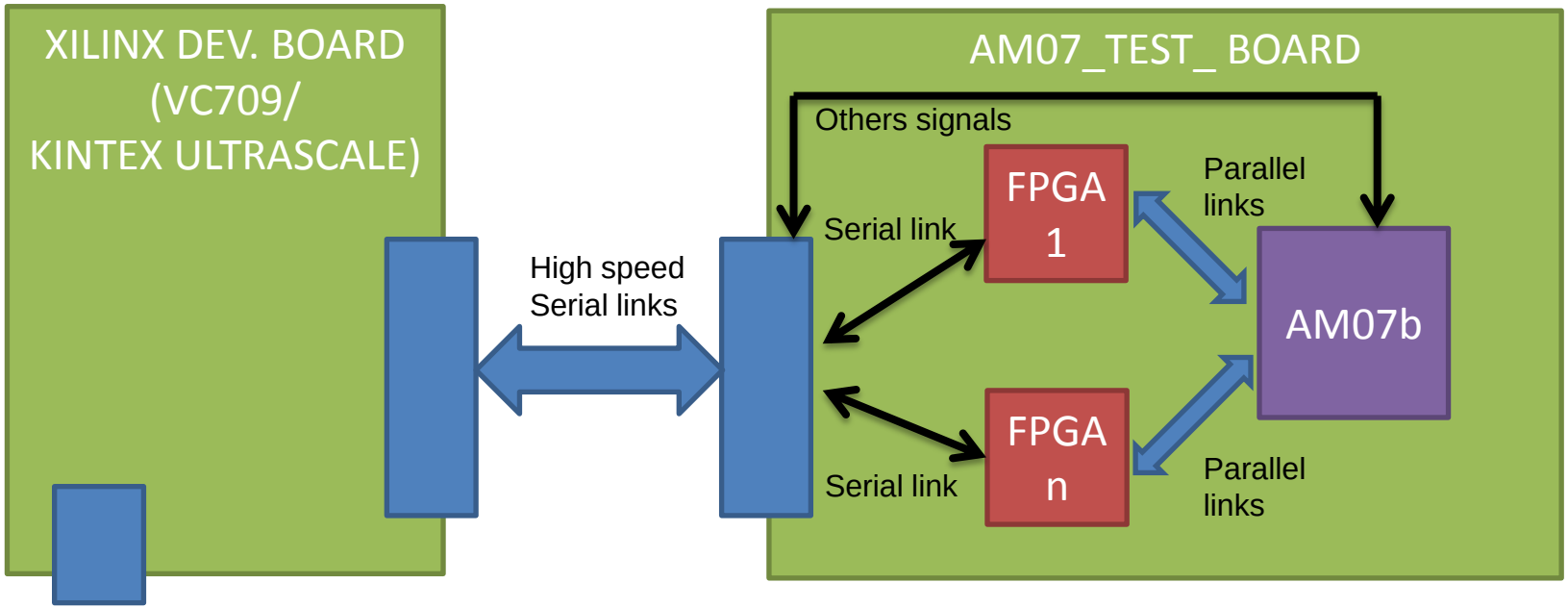
- XC7K325T (kintex 7) up to 500 IOs / 16 GTX (2000€)
- XC7V585T (virtex 7) up to 600 IOS / 32 GTX (3200€)

→ Architecture based on one FPGA



- FPGA role is just to switch data from serial links to paralel links.
- 10 High speed links between Xilinx Dev. Board and AM07b_test_Board up to 10Gb/s per links
- JTAG and others signals are drived by dev. board

→ **Architecture based on multiple FPGA**



- Multiple FPGA reduce the SSO issue.
- FPGAs role is to switch data from serial links to paralel links.
- 10 High speed links between Xilinx Dev. Board and AM07b_test_Board up to 10Gb/s per links
- JTAG and others signals are drived by dev. board

➢ FPGAs will be less larger and cheaper (ex: kintex7 XC7K160T / 300 IOs / 8GTX / 520€)

Before hardware design, to solve the SSO/SSN issue, several « tracks » must be studied or done:

- Can we reduce the number of single ended inputs in AM07b ? (with suppression of the 18bits complement data bus)
- We do the firmware before hardware to estimate the SSO/SSN and that will dertermine if several FPGA will be needed and how many.

After this work, It is necessary to write out specifications about AM07b test board :

- Comsuption
- Size
- Monitoring
- Budjet
- Schedule